EXPANDAMEM OWNERS MANUAL

PUBLISHED BY:

COMPU/THINK
965 West Maude Avenue
Sunnyvale, CA 94086
(408) 245-4033

JULY 1979

TABLE OF CONTENTS

Chapter 1 – INSTALLATION INSTRUCTIONS FOR THE EXPANDAMEM

1.1 GENERAL ***Power Off***

Before opening your PET for installation, tip it up so you can see the outside bottom of the case, and tighten the two screws on the bottom at the right rear and middle. They should be firmly secured, so that the brackets referred to in the next section can be properly screwed down.

Open the hinged top of your PET and prop open with the stay.

Place your Expandamem on a flat surface at the right of your PET.

1.2 MOUNTING THE BRACKETS

Inside your PET, unscrew the screws from the extreme right rear and right middle of the PET main board. Mount the two C-shaped brackets in the screw holes, using the two self-tapping screws supplied with the mounting kit. (The captive nuts on these brackets should be upward, to attach to the Expandamem.) The mounting bracket with the short foot attaches at the back of the board, the bracket with the long foot attaches in the middle of the board. Make sure that the foot of the rear bracket is clear of any conductors on the main board, and that both brackets are secured firmly, *feet forward*, so that they will not twist.

The four remaining metal screws insert at the four corners of the Expandamem board as follows. With the two screws nearest the capacitor-heat sink edge, attach spacer legs, *nylon insulating insert downward* to rest on the PET main board. These function as free-standing support, and rest against the PET board when installation is complete.

1.3 POWER SUPPLY LEAD

Unplug the power cable which is connected to the front left of the PET main board. This is a 5 conductor cable with color code Brown Red Black Red Brown.

Place the female 5 pin socket of the Expandamem power cord, 3 wire cable toward the rear, onto the male connector on the PET main board. Be careful to line up the connector so that all five pins mate, as there is no key to prevent incorrect insertion. Then reconnect the 5 conductor power cable from the PET transformer to the 5 pin male connector on the Expandamem power cable.

Bend the short piece of 5 wire cable so that it is out of the way of the cassette rear bracket of the PET. It may be necessary to loosen the cassette rear bracket and move it a little to get adequate clearance.

Connect the 3 pin female connector to the 3 pin male connector on the Expandamem board in the area of the vertically mounted capacitors. Push down firmly.

***Be sure to line up all the pins of the connectors!

1.4 EXPANSION CABLE CONNECTION TO EXPANDAMEM

Place the 50 pin female connector (if not connected before shipment) onto the male pins on the Expandamem board with the Brown wire edge of the connector toward the RAM array, the Black wire edge toward the daughter board sockets. The 50 wire cable will be bent over the top of the connector as it passes over the edge of the board.

1.5 DAUGHTER BOARD(s)

Push the daughter board(s) into any of the four slots, with components facing the RAM array.

1.6 MOUNTING THE EXPANDAMEM INSIDE THE PET

Position the Expandamem inside the PET at the right rear, cable connector toward the right side. Line board up with the two open mounting holes over the C-shaped mounting brackets previously mounted and attach with remaining two screws.

The service loop of the power cable may now be neatly coiled and stored away behind the large tubular capacitor near the power transformer.

The dual 40 pin edge board connector is pushed firmly onto the expansion connector, with the cable running upward.

1.7 TESTING THE EXPANDAMEM

Turn on power to your PET and check that the number of bytes free shown on the CRT matches the configuration of your memory board as shown in the Table 1.

Number of 4K Blocks of Contiguous Memory	Bytes Free on Power Up	Memory Configuration
2	7167	Standard 8K PET (w/o Expandamem)
3	11263	
4	15359*	
5	19455*	
6	23551*	16K Expandamem in 8K PET
7	27647*	
8	31743	24K* or 32K Expandamem in 8K PET

*Note that these figures are reduced by 4096 and 8192 bytes when a single or double density disk system respectively is installed with the appropriate header.

Table 1. Memory Byte Table

To test the memory, run the Diagnostic Test Tape according to the instructions for at least one full pass of the memory test program.

The hinged top of the PET may now be closed. Run the extended memory diagnostic program for several hours to give good confidence in the operation of the combination unit.

1.8 OUTSIDE OPERATION

If you wish to operate the Expandamem outside the PET, detach it and move it in normal position to the right side outside the PET. Notice that the cable necessarily makes a 180° twist as you do this.

1.9 CAUTION IN SHIPPING AFTER EXPANDAMEM INSTALLATION COMPLETED

When shipping the PET with Expandamem installed, mark for Vertical Shipment, THIS SIDE UP. As two of the four Expandamem "legs" are free standing, not attached, damage could result from upside-down shipment.

If vertical shipment is not possible, simply reverse your installation directions, remove the Expandamem, and ship separately.

1.10 RAM MEMORY

The RAM memory selects are jumpered to make the memory contiguous to the internal PET memory. Thus a 16K Expandamem in an 8K PET responds to SEL 2, 3, 4, 5. SEL 2, 3 is the edgemost row of memory chips. (The memory chips are the regular rectangular array at the front left of the Expandamem main board.) A 32K Expandamem responds to SEL 2, 3, 4, 5, 6, 7, 9, A.

The bit value of the memory chips within each row from left to right, looking from the front of the installed Expandamem, is 1, 2, 4, 8, 16, 32, 64, 128.

1.11 I/O EPROM BOARD

The EPROM area of the board is jumpered for two 2708 type EPROMs. In 16K and 24K units, these respond to A000-A3FF (left chip) and A400-A7FF (right chip). In the 32K unit these respond to B000-B3FF and B400-B7FF respectively.

In all units the I/O chip is addressed at BFC0 to BFCF (49088 to 49103 decimal).

The I/O Port pinouts are as follows:

PIN#	LEFT	RIGHT	PIN#	LEFT	RIGHT
1	CA1	CB1	8	PA4	PB4
2	CA2	CB2	9	PA5	PB5
3	PA0	PB0	10	PA6	PB6
4	PA1	PB1	11	PA7	PB7
5	PA2	PB2	12	(spare)	
6	PA3	PB3	13	(spare)	
7	GND	GND	14	+5	+5

Chapter 2 – THEORY OF OPERATION

2.1 MAIN BOARD

The Expandamem consists of a mother board containing a DC power supply that generates the necessary power for a dynamic RAM memory array (+12, +5, -5V) and also for the necessary support circuitry and buffers. Power is also available for expansion daughter boards. The main board contains the solid state memory array which can hold up to 32K bytes. The board has refresh control logic to give invisible refresh of the array. On-board buffers present one low power schottky load to the expansion port of the host computer. The main board also contains buffers and control circuitry to drive up to 4 daughter boards. There is also provision for generating the 4K block select from the 4 high order address lines of computers such as the KIM.

The ten 4K block selects which are available from the PET may be connected by header to any of the 4K blocks of memory or I/O on the Expandamem. Since the RAM array uses 8K chips, two 4K block selects are ORed together to select one row of RAM chips. The low order addresses (A-0 to A-12) are multiplexed together by the control circuitry to produce the six address lines that drive the memory array.

Refer to the Expandamem main board schematic for component designation in the following discussion.

RAM ARRAY DRIVERS

The RAM memory array is driven in parallel by the outputs from U1 and U4 together with the signals $\overline{CAS}$ and $\overline{WR}$. The individual rows of the RAM array are selected by the $\overline{RAS}$ signals coming from U9. These are decoded from the input select signals by U10 and U16. The control signal REFAD* enables all the $\overline{RAS}$ signals in parallel during refresh. For a fuller understanding of the operation of Multiplex Dynamic rams refer to the manufacturers' data sheets. U1, U4 multiplex the addresses for the column address strobe $\overline{CAS}$ while U2 and U5 multiplex the other signals for the row address strobe $\overline{RAS}$ by switching between inputs from addresses BA0 to BA6 and the outputs of the refresh counter (U3). The refresh circuitry is driven by the output of U7 which counts the incoming clock signals and generates a refresh request every 8 microseconds. The refresh occurs during the phase one part of the CPU clock and hence is transparent to operation of the CPU.

The timing of both the refresh and memory cycles is generated by U26, U25 and U20 and associated circuitry. U26 generates the timing for the $\overline{RAS}$ strobe and the resistor capacitor networks between U25 and U20 generate the signal timing for the CAS strobe, the multiplexer and the write pulse. The order of the signals is $\overline{RAS}$, $\overline{MPX}$, $\overline{CAS}$, $\overline{WEN}$. U21 pins 8, 9 and 11 stretch the CAS signal until the end of the phase 2 clock cycle which maintains the data output of the RAMS until the CPU chip has latched them.

MEMORY ADDRESS DECODING

The signals M0* to M7* at the input of U11 decode the memory space of the RAM array. U11, pin 6 (HEN) high enables the upper half (4K) of each memory row and when low enables the lower 4K.

WRITE PROTECT

The three sections of the U18 connected to the 22 pin header control the write protect feature. If either of the inputs to U18 (pins 2 and 12) are connected to one of the memory block selects while the incoming signal to pin 18 of the board is held low, then that 4K block of memory will be write protected (i.e., cannot be written into, only read).

ADDRESS/DATA BUFFER

The address and control lines are buffered by U6 and U8 while the data lines are buffered by U12, U13 and U14. U13 buffers the data out from the RAM array while U12 and U14 buffer the bi-directional data bus used as the input to the memory array and also as the input/output for the I/O cards in the PC card slots.

KIM ADAPTER

The locations U19 and U24 can be used for an optional KIM adapter. These are normally empty when the Expandamem is used with a PET. Also U28 provides partial decodes for using Apple II type boards in the PC card slots. This chip is also not supplied for use with the PET.

2.2 EPROM I/O BOARD

The EPROM I/O board combines a general purpose I/O chip (MPS 6522) and sockets for two EPROMs, together with decoding logic with flexible selection capabilities. The I/O chip is driven by the buffers on the main board and may be selected to be in a variety of different memory locations according to the requirements of the system. The two halves of the I/O chip are connected to two dip sockets through holes and conductors which are so arranged that additional I/O chips such as opto couplers or relay drivers may be easily connected in on a patch area at one side of the boards.

The EPROM area is also set up so that it can be flexibly configured in different memory addresses according to user requirements. Also, several different kinds of EPROMs using the same pin outs may also be utilized. However, the EPROMs used must be of the same type, i.e. two 2708s or two 2716s.

Refer to schematic Expandamem EPROM I/O board for component designations in the following discussion.

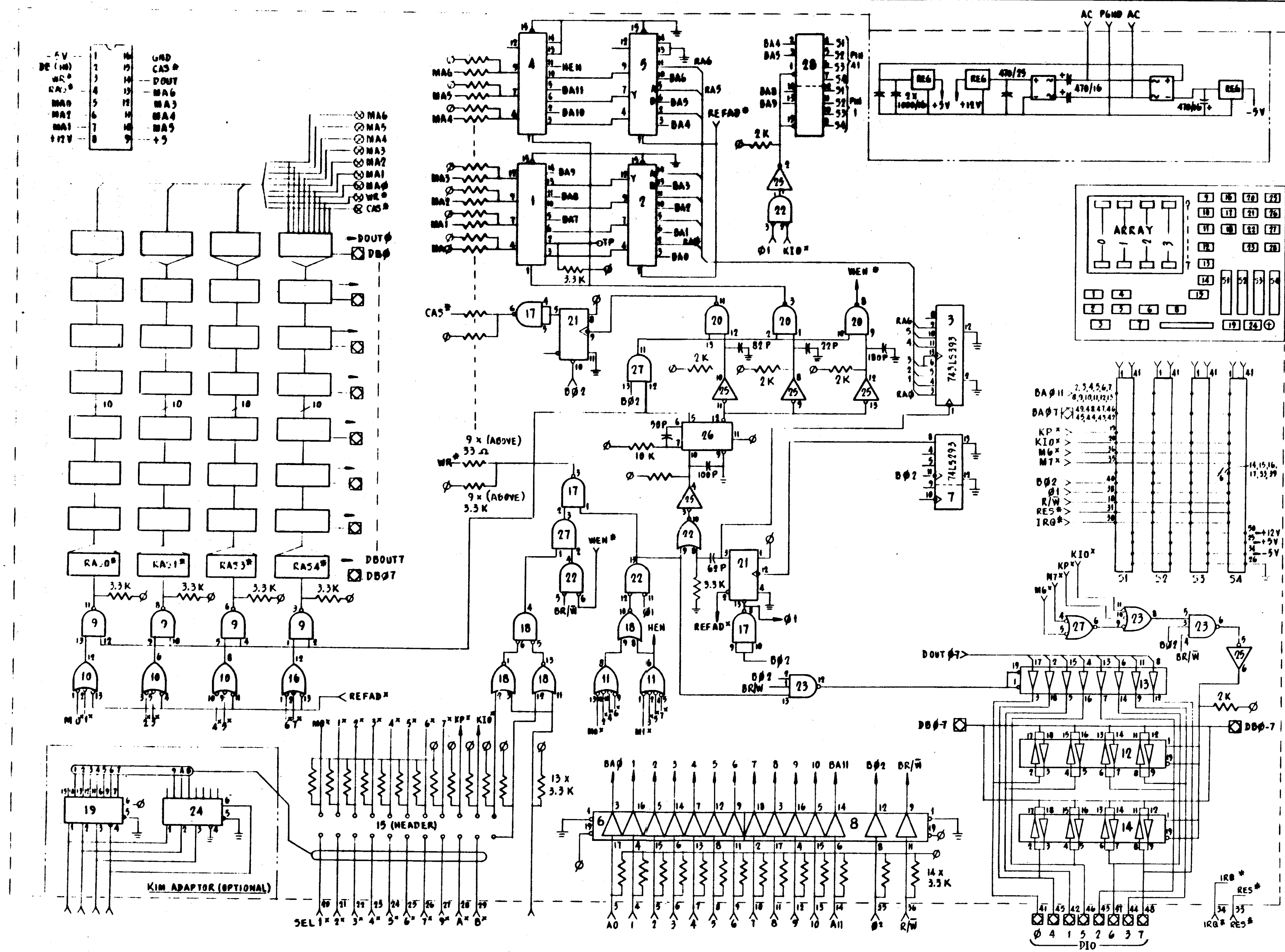
I/O CHIP DECODING

Z3 performs the main I/O functions for the board and provides two parallel I/O ports with handshake signals plus other internal registers. For further information regarding the operation of this chip refer to the manufacturers' data sheets for the 6522 VIA chip (the same device as the one used for the user port in the PET). This chip is positioned in the memory space by decoding address signals in Z4 and Z7. The chip is enabled when the selected output pin on Z4 goes low causing Z3-23 to go low while the output of Z7 (pin 8) also goes low corresponding to the selected address inputs to Z7 being high. The normal base address location for the I/O chip with Z3-23 connected to Z4 pin 12 is BFC0. If the link to pin 12 is removed and the link made to pin 11 this moves to BFD0.

EPROM ADDRESS SPACE DECODING

The EPROM is enabled by the signal on Z4 pin 1 (normally corresponding to KP) being low, while phase 1 (B phase 2 inverted) is low. In addition the position of the EPROM within the 4K block select connected to KP is selected by the inputs to pins 2 and 3 of Z4. Thus the signal at Z4 pins 4 to 7 correspond to 1K blocks within the 4K address space. By changing jumpers the EPROMs may be positioned either as the low 2K or as the high 2K in this 4K block. Also if it is desired to use 2K EPROMs such as 2716s by grounding pin 3 and taking BA11 to pin 2, the output of Z4 becomes 2K block select. BA10 should also be linked to the appropriate pin of the 2716.

Additionally by changing jumpers on the power inputs to Z1 and Z2, the power supply requirements of a wide range of ROMs and EPROMs may be accommodated. (Refer to the manufacturers' data sheets for the particular device you may want to use.)



REV	DESCRIPTION	DATE

DRN. BY	J. Attenborough	4/11/79
CKD. BY	R. Tobey	4/11/79
APP. BY	R. Tobey	4/11/79

COMPU/THINK
MENLO PARK, CA.

SCHEMATIC,
EXPANDAMEM MAIN BOARD

NEXT ASSY	USED ON

SIZE	DWG. NO.	REV
D		

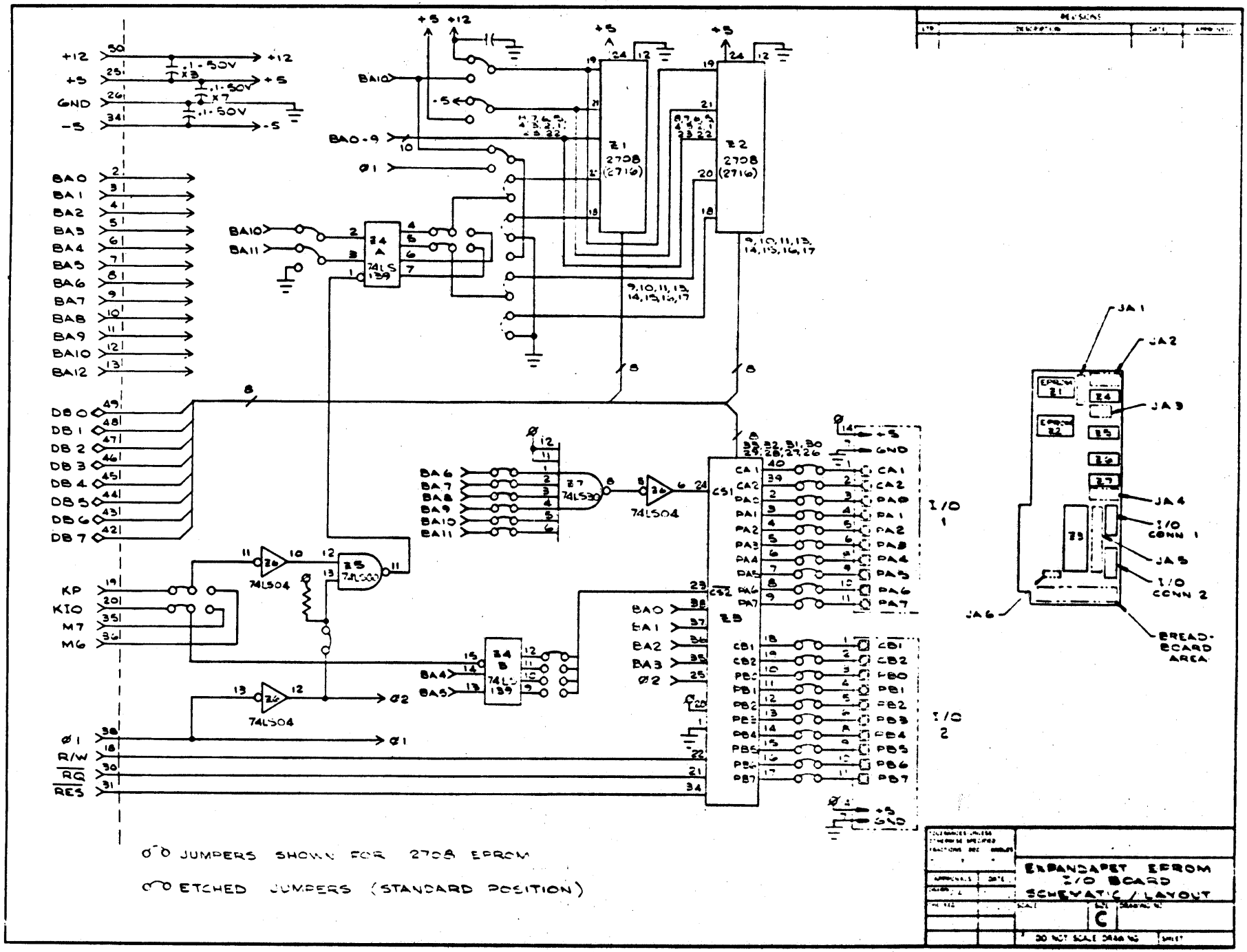


Fig. 2.2 — Expandamem I/O Board Schematic

Chapter 3 – CONFIGURING THE MEMORY SPACE

3.1 4K BLOCK SELECTS

The Expandamem can be very flexibly configured with any 4K block of the Expandamem lying in any 4K memory address space of the PET. This is done by suitable wiring on the 22 pin header. The incoming block select signals from the main board are on one side of the connector, and the 4K select lines for each area of memory of the PET are on the other side of the connector. Any 4K block can be joined to any 4K input depending on the way that the jumper wires are positioned. In addition there are 2 pins on the end of the 22 pin connector nearest the daughter board area, which are associated with the Write/Protect feature.

Normally, most of the RAM memory would be configured to be directly adjacent to the PET's own memory to give as large as possible a contiguous memory space. This memory space is found during the power up initialization routines of the PET and can be used by the BASIC routines automatically. Figures 3.1 to 3.8 show drawings of the select header wired for various memory configurations.

3.2 MEMORY ABOVE THE SCREEN

The area above the screen (blocks 9, A, B) may also be used for RAM for special machine code programs. They cannot be directly addressed by some of the BASIC routines, including the tape save routines but can of course be called by SYS commands. If desired to save and load code from this area, it must be first transferred to or from the basic area below the screen by a utility move program.

3.3 EPROM I/O SELECTS

Normally the EPROM and I/O blocks are also selected to respond in this area of the machine memory map. For example, block A is normally configured to be the EPROM block, and block B is configured as the I/O block.

Block selects A and B are connected to the daughter boards, and are the main select signals for this area of the Expandamem. In addition memory select signals 6 and 7 are also connected to the daughter boards and can be used to drive EPROM and I/O. Note that when these signals are used for I/O they must not be connected to the RAM chips. Also jumpers must be inserted on the main board area near the rearmost daughter board connector to enable the I/O EPROM data buffers during memory select 6 and 7.

3.4 CHANGING THE 8K PET TO 4K PET AND RECONFIGURING THE EXPANDAMEM

Sometimes it is useful to make an 8K PET work like a 4K PET (for example, if some of the PET memory chips have gone bad). This is done by cutting the link to the left of the 74154 on the PET main logic board – that is, the single 24 pin IC mounted at 90° to and just behind the rows of ROM and RAM near the front of the PET.

To reconfigure the Expandamem for contiguous memory to the 4K PET, change the links on the 22 pin header to match Figure 3.3.

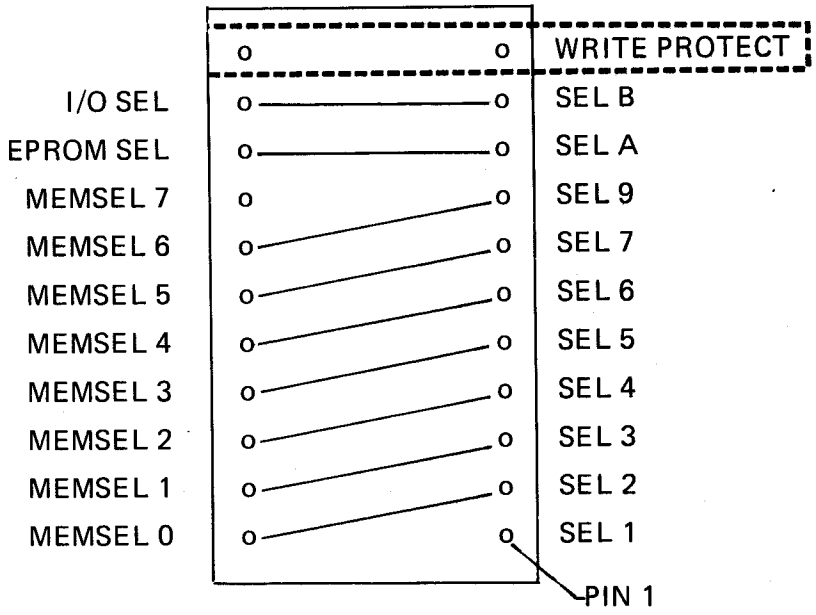


Figure 3.1

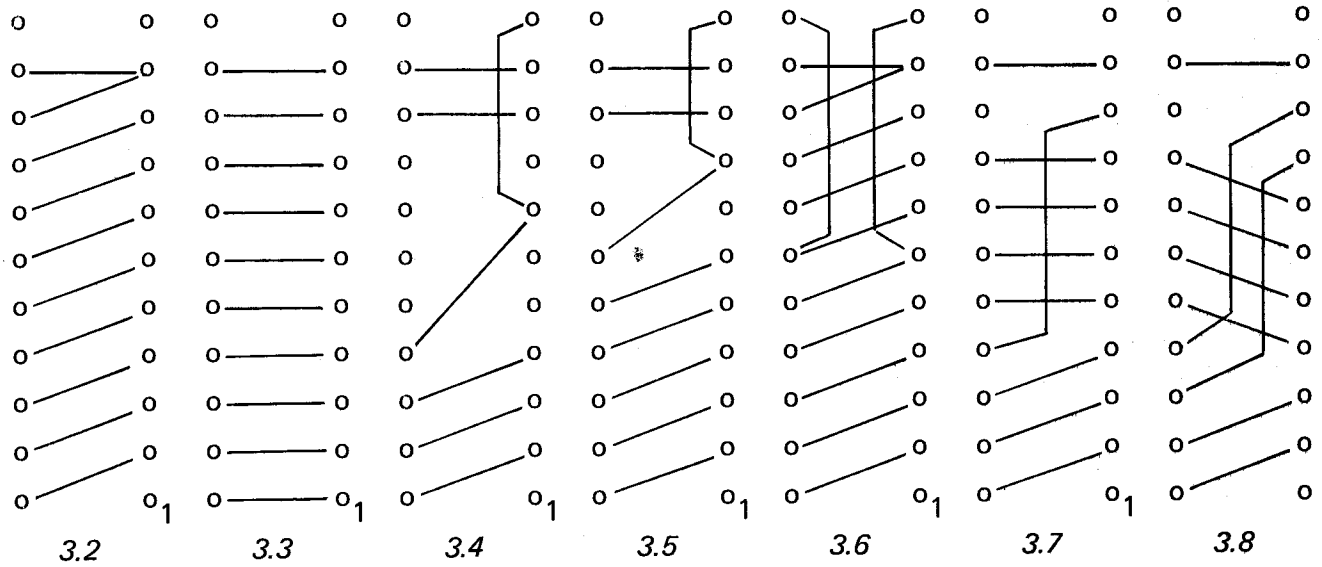


FIGURE NUMBERS

3.1 STANDARD 16K OR 24K IN 8K PET.

3.2 STANDARD 32K IN 8K PET.

3.3 STANDARD 16K, 24K OR 32K IN 4K PET.

3.4 16K EXPANDAMEM 12K CONTINUOUS TO 8K PET, 4K WITH WRITE PROTECT IN BLOCK 7.

3.5 24K EXPANDAMEM 20K CONTINUOUS TO 8K PET, 4K WITH WRITE PROTECT IN BLOCK 7.

3.6 32K EXPANDAMEM 8K WITH WRITE PROTECT IN BLOCKS 6 & 7.

3.7 DISK SYSTEM ALL MEMORY SIZES: SINGLE DENSITY

3.8 DISK SYSTEM ALL MEMORY SIZES: DOUBLE DENSITY

Chapter 4 – WRITE/PROTECT

A Write/Protect feature is built into the Expandamem that can be connected to any two 4K blocks of memory. The two pins at the end of the 22 pin block select header nearest the daughter boards enable this feature. They should be wired to whichever of the memory blocks it is desired to Write/Protect. The selected blocks are Write/Protected when the Write/Protect control signal is grounded by a switch. When the switch is open, the memory functions normally. This signal is the 14th pin from the front on the bottom row of the PET connector, or pin 18 on the Expandamem end of the main cable. Figures 3.4, 3.5, 3.6 are examples of write protected memory configurations.

Chapter 5 – MEMORY DIAGNOSTIC TEST

5.1 GENERAL

The Expandamem Memory Diagnostic Test Tape has a different test program on each side of the tape. Side A contains the EXPANDAPETEST 2.3, a 4K block memory test program. Side B contains EXPANDAMEMTST 3.1 which tests the memory in 256 byte pages. Both programs write changing pseudo-random test patterns into selected areas of memory and then after a delay period, check the memory for the same patterns. When the test program finds a bad bit, it stops and displays on the screen the block and page location of the bad bit. (Refer to Figure 5-1 for the physical memory chip locations corresponding to the blocks and pages of the memory in the standard configuration and the Diagnostic Test Error Message.) Also displayed by the program is the memory data and test data which show the malfunctioning chip. For example, if the difference between the memory data and the test data is 1, then the chip in the left hand row (value 1) is malfunctioning. If the difference between the memory data and the test data is 32, then the chip in the third row from the right (value 32) is bad. If the difference between the test and memory data is not one of the binary values 1, 2, 4, 8, 16, 32, 64, or 128, then a failure other than a memory chip failure is indicated.

NOTE: Different Memory Diagnostic programs must be used when the Diskmon Disk Operating System is in use. These are BLOCKTEST and PAGETEST on the utility disk. These correspond to and work similarly to EXPANDAPETEST 2.3 and 3.1 respectively.

5.2 RUNNING THE TEST TAPE WITH STANDARD EXPANDAMEM CONFIGURATIONS

5.2.1 EXPANDAPETEST 2.3 (or BLOCKTEST)

When running the 4K block test, EXPANDAPETEST 2.3, the first block of memory is designated as block 1. An 8K PET contains blocks 1 and 2, and blocks 3 and up are in the Expandamem. A 4K PET contains block 1, and the Expandamem contains blocks 2 and up. Thus to test the Expandamem memory with this program in an 8K PET with a 16K Expandamem, proceed as follows:

Run the program, and then enter 3 for "FROM BLOCK" and 6 for "TO BLOCK." Next, the program will request the number of passes required, and if zero is entered here the program will run continuously until stopped. Finally the program will ask for a delay which is normally set to zero. If refresh problems are suspected, a delay can be entered. A hundred seconds delay will check any problems in this area.

During normal operation of the program, it prints out a pass number from 0 to 255. In addition, it also prints out the elapsed time from the turn-on of the PET, so that you can leave the program running, and know how long the memory test has run without error.

5.2.2 EXPANDAMEMTST 3.1 (or PAGETEST)

This program is essentially similar to the first program but tests the memory in 256 byte pages. The bottom of the PET memory is considered to be page zero, and hence an Expandamem in an 8K PET starts at page 32. Thus when running the program the "FROM PAGE" should be 32, and the "TO PAGE" should be 95 for a 16K Expandamem and 127 for a 24K or 32K Expandamem.

5.2.3 Testing Memory Above the Screen

The memory area above the screen must be tested as a separate operation. When using EXPANDAPETEST 2.3, the memory is normally blocks 10 and 11. Using EXPANDAMEMTST 3.1, the memory runs from page 144 to page 175.

5.3 USING THE DIAGNOSTIC TAPE FOR TESTING THE PET MEMORY

The EXPANDAPETEST 2.3 block memory test can test the top 4K block in an 8K PET by entering 2 for the "FROM BLOCK." EXPANDAMEMTST 3.1 can test all of the top 4K and some of the bottom 4K of the 8K PET by entering 12 for the "FROM PAGE."

DIAGNOSTIC TEST ERROR MESSAGE:

ERROR IN BLOCK	B	
(Page P)		AT LINE L
TEST DATA	X	MEMORY Y
NEXT LOCATION	?	

In the above message,
- B = Block containing bad bit
- P = Page containing bad bit
- L = Line within page containing bad bit
- X = Data written to memory
- Y = Data retrieved from memory

NOTE: X-Y or Y-X gives value of bad bit, thus indicating position in row of defective chip.

Box signifies Reverse Video Display

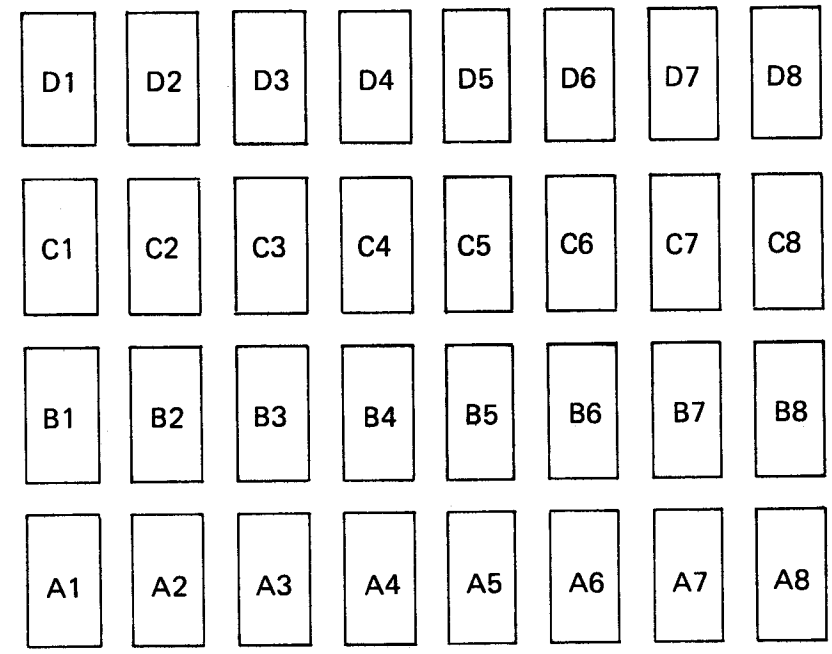
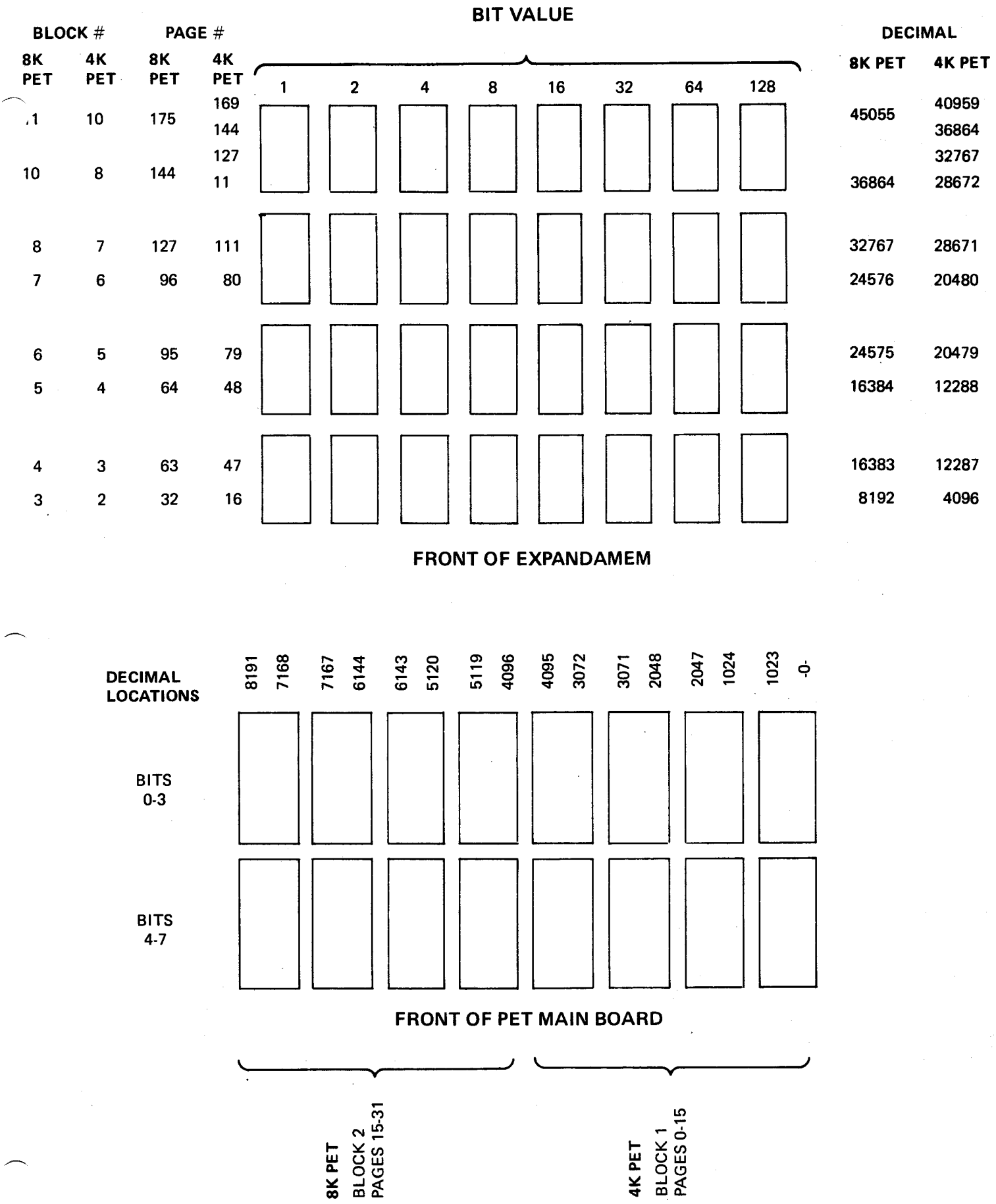


Fig. 5.1 – Memory Chip Layout


BIT VALUE
BLOCK #
8K PET
4K PET
PAGE #
8K PET
4K PET
1
2
4
8
16
32
64
128
DECIMAL
8K PET
4K PET
1
10
175
169
144
45055
40959
36864
10
8
144
127
11
36864
32767
28672
8
7
127
111
32767
28671
7
6
96
80
24576
20480
6
5
95
79
24575
20479
5
4
64
48
16384
12288
4
3
63
47
16383
12287
3
2
32
16
8192
4096
FRONT OF EXPANDAMEM
DECIMAL LOCATIONS
8191
7168
7167
6144
6143
5120
5119
4096
4095
3072
3071
2048
2047
1024
1023
-0-
BITS 0-3
BITS 4-7
FRONT OF PET MAIN BOARD
8K PET
BLOCK 2
PAGES 15-31
4K PET
BLOCK 1
PAGES 0-15

PET (4 or 8K)			BITS 0	1	2	3	4	5	6	7	
Blocks	Decimal	Pages	(1)	(2)	(4)	(8)	(16)	(32)	(64)	(128)	
1	0-1023	0- 3	I1 →				J1 →				4K PET ↓
	1024-2047	4- 7	I2 →				J2 →				
	2048-3071	8-11	I3 →				J3 →				
	3072-4095	12-15	I4 →				J4 →				
2	4096-5119	16-19	I5 →				J5 →				8K PET ↓
	5120-6143	20-23	I6 →				J6 →				
	6144-7167	24-27	I7 →				J7 →				
	7168-8191	28-31	I8 →				J8 →				

EXPANDAMEM & 8K PET		EXPANDAMEM & 4K PET		EXPANDAMEM & DISK, 8K PET			EXPANDAMEM & DISK, 4K PET			BITS 0	1	2	3	4	5	6	7
BLOCKS*	PAGES	BLOCKS*	PAGES	BLOCKS*	PAGES		BLOCKS*	PAGES		(1)	(2)	(4)	(8)	(16)	(32)	(64)	(128)
3	32-47	2	16-31	3	32-47		2	16-31									
4	48-63	3	32-47	4	48-63		3	32-47		A1	A2	A3	A4	A5	A6	A7	A8
5	64-79	4	48-63	5	64-79	144-159	4	48-63	144-159	B1	B2	B3	B4	B5	B6	B7	B8
6	80-95	5	64-79	11	160-175	160-175	11	160-175	160-175	C1	C2	C3	C4	C5	C6	C7	C8
7	96-111	6	80-95	6	80-95	64-79	5	64-79	48-63	D1	D2	D3	D4	D5	D6	D7	D8
8	112-127	7	96-111	7	96-111	80-95	6	80-95	64-79								
10	144-159	8	112-127	8	112-127	96-111	7	96-111	80-95								
11	160-175	10	144-159	10	144-159	112-127	8	112-127	96-111								
					Single Density	Double Density		Single Density	Double Density								

TO TRANSLATE BLOCKS FOR PEEK AND POKE DECIMAL LOCATIONS:

DECIMAL START ADDRESS OF BLOCK B = (B-1)*4096

DECIMAL END ADDRESS OF BLOCK B = (B*4096) -1

Fig. 5.2 — Location Reference Table for Memory Chip Layout

6.1 GENERAL

The I/O circuitry uses the MCS-6522 integrated circuit. For a full discussion of the complete capability of this chip, see the manufacturer's data sheet and application notes. The output side of the chip is divided into two ports, port A and port B. The port A signals are on I/O connector number 1, and the port B signals are on I/O connector number 2. (See 6.2 below for pin connections.)

6.2 CONNECTOR PIN-OUTS

The EPROM area of the board is jumpered for two 2708 type EPROMs. In 16K and 24K units, these respond to A000-A3FF (left chip) and A400-A7FF (right chip). In the 32K unit these respond to B000-B3FF and B400-B7FF respectively.

In all units the I/O chip is addressed at BFC0 to BFCF (49088 to 49103 decimal).

The I/O Port pinouts are as follows:

PIN#	LEFT	RIGHT	PIN#	LEFT	RIGHT
1	CA1	CB1	8	PA4	PB4
2	CA2	CB2	9	PA5	PB5
3	PA0	PB0	10	PA6	PB6
4	PA1	PB1	11	PA7	PB7
5	PA2	PB2	12	(spare)	
6	PA3	PB3	13	(spare)	
7	GND	GND	14	+5	+5

6.3 INTERFACE SUGGESTIONS

The breadboard area of the EPROM I/O Board (see Layout) may be used to build special interface requirements such as opto couplers, relay drivers, etc.

The interface drivers may be installed between the Z3 and the output connectors by cutting the appropriate etch link in the jumper area JA5 and wiring to the extra circuitry built up on the breadboard area.

Suitable drivers for relays up to 24V or for the emitters of optocouplers are 8 pin minidip peripheral driver ICs such as the 75451.

6.4 JUMPER CONFIGURATIONS AND HOW TO CHANGE THEM

Refer to the EPROM I/O Board schematic layout for the position of the jumper areas, and to the schematic together with manufacturers' data sheets to understand how to reconfigure the board for various chips.

The standard board configuration is set up by an etched pattern on the board. However, in certain jumper areas the etch may be broken with a sharp knife, and jumpers soldered onto the board allow positioning of the various elements of the EPROM I/O board in different portions of the computer memory. For example, if it is desired to address several EPROM I/O boards, it will be necessary to configure the boards to respond to different addresses.

The I/O chip on board number 1 should be left in the standard position, responding at BFC0-BFCF while the linkage would be changed on a second I/O board to allow the I/O chip to respond at BFD0 through BFDF. This would be done simply by cutting the etch in jumper area JA2 and soldering an alternative link.

6.5 DESCRIPTION OF JUMPER AREAS

JA1 selects between 2708 type chips and 2716 type chips. The standard configuration is for two 2708 chips. In addition, there are jumpers for the power supply to allow the use of single power supply type EPROMs. Also for 2716 EPROMs, the jumpers in JA3 must be moved to the upper address positions (Z4-6,7).

JA2 jumper area allows a choice of 4 memory addresses for the I/O chip on the I/O board.

Link to Z4-12	Base Address BFC0
Link to Z4-11	Base Address BFD0
Link to Z4-10	Base Address BFE0
Link to Z4-9	Base Address BFF0

JA3 allows selection when using 2708 1K EPROMs for positioning EPROMS IN ANY of the four 1K segments of the 4K block select assigned to a PROM. Standard position in the lower two 1K sub-blocks.

JA4 decodes the address lines BA6-11 for the I/O chip and enables the chip when these lines are high. Other decoding is possible by utilizing some of the spare inverters in Z6 in series with certain of the address lines.

JA5 jumper area is for use in conjunction with the breadboard on the bottom of the board to install special I/O driver or receiver circuitry in series with the signals from the I/O chip. For example, if it is desired to put a relay driver on the output of PA-9, then the link in series with pin 3 I/O connector #1 is broken, and wires taken over to the breadboard area to insert a relay driver chip such as a 75451 in series with the output from the chip.

JA6 normally connects the PROM select line through to the PROM decoding, and the I/O select line from the header on the main Expandamem board through to the I/O decoding. Alternatively, the PROM and I/O may be selected by M7 or M6 block selects from the Expandamem header by changing the links in this area. Also, in case of a 32K Expandamem in an 8K PET which has only one 4K block select left outside a RAM memory, both the PROM and I/O chip can be selected by the same 4K block select by changing the links in the JA6 area.

Chapter 7 – KIM ADAPTOR FOR THE EXPANDAMEM

7.1 SYMMETRICAL CLOCK MOD FOR KIM 1

In order for correct operation of the Expandamem, the KIM must be modified to produce a square and symmetrical phase 2 clock signal (see figure 7.1). This allows correct operation of the invisible refresh of the Expandamem which occurs during the phase 2 off-cycle that is normally used by the CPU to decode and execute the current instruction.

7.2 KIM ADAPTOR THEORY OF OPERATION

The KIM adaptor consists of the necessary cabling to match the pinouts of the Expandamem and KIM expansion socket, plus a 4 to 16 line decoder which produces the 4K block select signals used by the Expandamem from four high-order addresses of the KIM (A12 through A15). In addition, a signal is generated to enable the KIM onboard address decoder during block selects corresponding to the first 8K and the last 4K of memory addresses. The other thirteen 4K block selects are available for the Expandamem.

7.3 MEMORY MAP

The memory map of a 16K Expandamem is wired to respond to addresses 2000 to 5FFF. The EPROM area responds to 6000 to 67FF and the I/O chip responds to 7FC0 to 7FCF. The main 4K block selects may be changed by changing the wires which go to the output side of the 22 pin dip header. The spare wires which are tied back correspond to the 4K block selects 8, 9, A and B.

7.4 WHEN EXPANDAMEM IS SET UP FOR THE KIM, TO CHANGE TO SET UP FOR THE PET

(1) Change the main 50 wire cable.

(2) Pull out the 22 pin header, tie back the wire and KIM header.

(3) Insert the 22 pin header with jumper wires, with empty *two* pins toward the daughter boards.

(4) Insert the 16 pin resistor pack in the empty 16 pin socket with the package oriented in the same way as the other ICs.

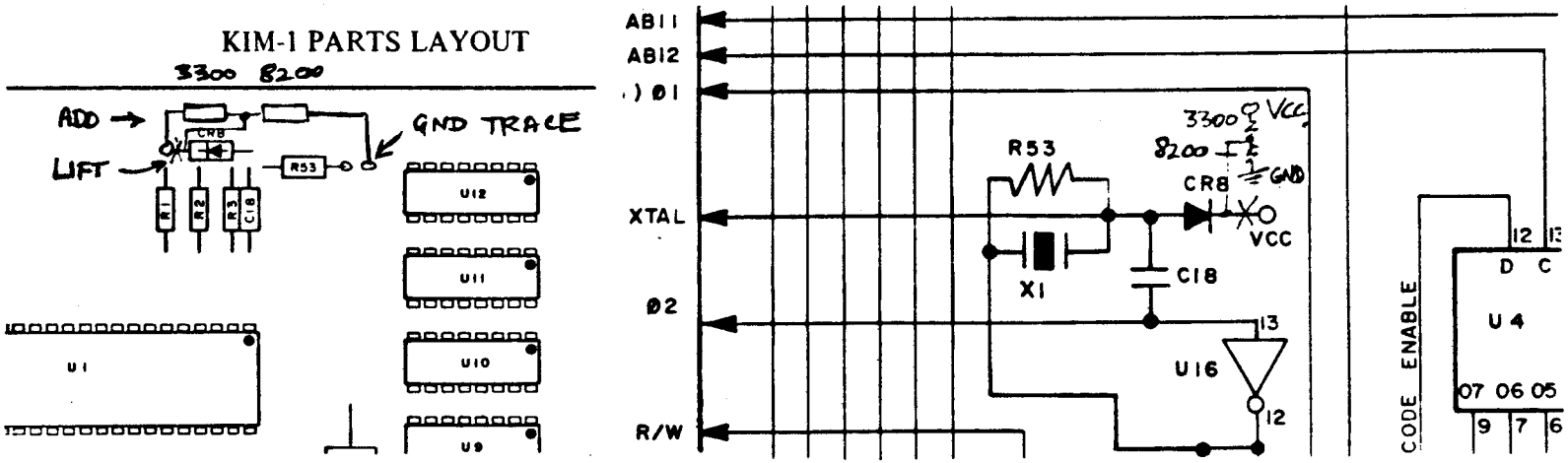


Fig. 7.1 – Kim Parts Layout