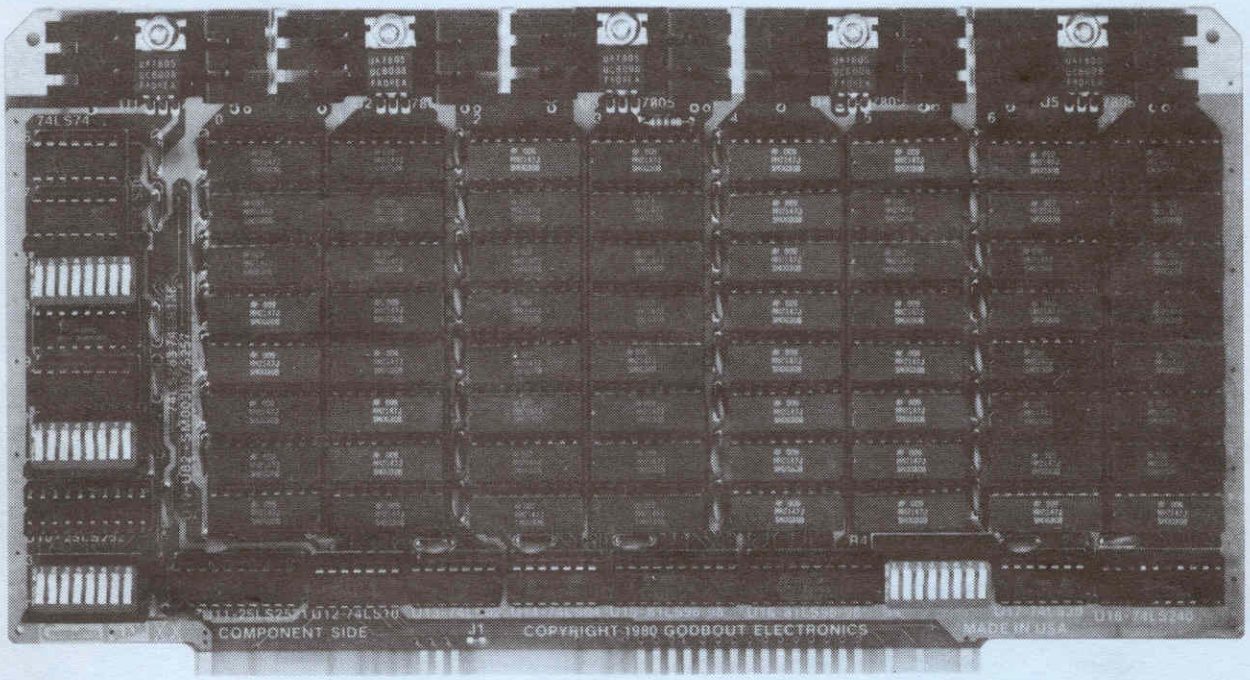
# RAM 20™

# USER MANUAL




## IEEE 696 / S-100

# 32K STATIC RAM

## Extended Addressing & Bank Select

164A

mac

CompuPro™ division GODBOUT ELECTRONICS

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## TECHNICAL OVERVIEW

The **RAM 20** is a high speed (10 MHz), low power (about 1.5 Amps on 8V), 32K byte static RAM board designed to conform to IEEE spec 696 for the S-100 bus. The **RAM 20** can be configured as a conventional Bank Select board (compatible with Cromemco and North Star Bank Select schemes), as an Extended Address board (compatible with the 8088 CPU or with CompuPro memory management hardware), or as a Global memory. The board is addressable as a single 32K block which may begin at any 4K address within a 64K page. Within the selected 64K page, the board addressing will, if necessary, 'wrap around' from the top of RAM to the bottom. Also within the 64K page, up to 8 4K 'windows', or unoccupied address spaces, may be created manually through an 8 paddle DIP switch provided for this purpose.

The **RAM 20** is shipped as a 16K, 24K, or 32K board. Partially populated boards may be upgraded simply by inserting additional 5257/2147 type RAM IC's into pre-installed DIP sockets (all boards come with all 64 RAM IC sockets wave soldered in place.) Extra heavy duty power traces, generous bypassing of supply lines, sockets for all integrated circuits, careful layout, innovative design conservatively implemented, premium parts, and a double sided, solder-masked printed circuit board with complete component legends make this a versatile, dependable, high performance memory board.

Since dense memory is among the most costly items in any S-100 installation, using the **RAM 20** as the heart of a system insures that the transition to faster CPU's and/or more sophisticated memory management software will be as easy and inexpensive as possible. Because of the board's extremely low power consumption, numerous **RAM 20's** can be combined without over heating the system or exceeding the capacity of the system power supply. And because the **RAM 20** uses static RAM memory, the user is assured of long, reliable operation and easy maintenance.

## RAM 20 SWITCH FUNCTIONS

Four 8 position DIP switches on the **RAM 20** are used to select most of the board options. The addressing mode (Global, Extended Address or Bank Select) is selected by a switch as well as by the inclusion or exclusion of certain integrated circuits in sockets U6, U10, and U11. Depending upon the addressing mode chosen, either none, one, or two of these sockets should be populated. These three sockets should NEVER all be populated at one time. See the section entitled **RAM 20 ADDRESSING MODES** for a complete discussion of the three addressing modes: Global, Extended Address and Bank Select.

## SWITCH 1 - 4K BLOCK ENABLE

Switch 1 is used to enable or disable the eight individual 4K blocks of RAM which comprise the **RAM 20.** Setting any paddle 'ON' enables its associated 4K block, while setting any paddle 'OFF' disables its associated block so that the address space that would otherwise have been occupied is freed for use by off-board memory devices. The relationship between paddle number and 4K row number is illustrated below. (The 4K row number is shown on the silk screened legend of the P.C. board beside the eight rightmost RAM IC's of each horizontal row.)

**SWITCH S-1**

| | PADDLE NUMBER | 4K RAM ROW NUMBER |
|---|---|---|
| | 1 | 0 |
| 'ON' enables 4K row | 2 | 1 |
| | 3 | 2 |
| | 4 | 3 |
| | 5 | 4 |
| 'OFF' disables | 6 | 5 |
| | 7 | 6 |
| | 8 | 7 |

EXAMPLE: for starting address of 8000H, paddle 7 'OFF' disables on-board RAM from E000H to EFFFH.

**SWITCH S-2 : LOWER 16 BIT ADDRESSING, PHANTOM, & MODE**

Switch S-2 is used to select the lower 16 bit 4K starting address of the **RAM 20**, the Addressing Mode (Global or Extended Address/Bank Select), and the board's response to PHANTOM (S-100 line 67). In Bank Select mode, S-2 also determines the **RAM 20** start-up status, i.e., enabled or disabled.

**SWITCH S-2 : LOWER 16 BIT STARTING ADDRESS PADDLES 1 - 4**

Switch S-2 paddles 1 to 4 are used to select the lower 16 bit address (or base address) of the **RAM 20.** Each of the four addressing paddles can be thought of as controlling one address bit (A12 - A15) in forming the 4K starting address of the board, so that switching a paddle 'ON' or 'OFF' causes its associated starting address bit to become a '1' or a '0' respectively. The user can then form a 4K starting address of the form N000H by using paddles 1 to 4 to write in binary the Hex digit 'N'. The following table illustrates these relationships:

**SWITCH S-2 ADDRESSING**

| Decimal Starting Location | Hex Starting Address | Switch S-2 Paddle Number 1 (4K) or (A12) | 2 (8K) (A13) | 3 (16K) (A14) | 4 (32K) (A15) |
|---|---|---|---|---|---|
| 0K | 0000H | OFF | OFF | OFF | OFF |
| 4K | 1000H | ON | OFF | OFF | OFF |
| 8K | 2000H | OFF | ON | OFF | OFF |
| 12K | 3000H | ON | ON | OFF | OFF |
| 16K | 4000H | OFF | OFF | ON | OFF |
| 20K | 5000H | ON | OFF | ON | OFF |
| 24K | 6000H | OFF | ON | ON | OFF |
| 28K | 7000H | ON | ON | ON | OFF |
| 32K | 8000H | OFF | OFF | OFF | ON |
| 36K | 9000H | ON | OFF | OFF | ON |
| 40K | A000H | OFF | ON | OFF | ON |
| 44K | B000H | ON | ON | OFF | ON |
| 48K | C000H | OFF | OFF | ON | ON |
| 52K | D000H | ON | OFF | ON | ON |
| 56K | E000H | OFF | ON | ON | ON |
| 60K | F000H | ON | ON | ON | ON |

For example, to address the board to begin at 8000H, Switch S-2 paddle 4 should be 'ON', and paddles 1 through 3 should be 'OFF'.

**MEMORY WRAP-AROUND**

If the **RAM 20** is addressed to begin at address 9000H or higher, so that some 4K rows are left over after reaching 64K, the board addressing will 'wrap around' and begin again a location 0000H until all eight 4K rows are assigned an address. Thus if the board were addressed to begin at address F000H, then memory space would be occupied from F000H to FFFFH and from 0000H to 6FFFH.

**CORRESPONDENCE BETWEEN ADDRESS, DATA & PHYSICAL RAM LOCATION**

The 5257/2147 type RAM IC used with the **RAM 20** is arranged as a 4K X 1 matrix. Therefore in any given 4K byte address block (comprised of eight RAM IC's in a single horizontal row), each chip controls one and only one data bit. The data bits controlled by each vertical column of RAM IC's is printed on the silk screened legend of the circuit board above the top left corner of the top RAM IC in each of the eight vertical columns. The data bits progress sequentially from data bit 0 to data bit 7 from left to right. Thus each RAM IC in the leftmost vertical column controls data bit 0 of its respective 4K horizontal row, while the rightmost chips control data bit 7.

The 4K address controlled by each horizontal row of RAM IC's is determined by the starting address selected for the board through Switch S-2. The first, topmost 4K row, legended on the right edge of the P.C. board as '0', ALWAYS controls the starting 4K block of the board as set by S-2. This is not necessarily the lowest 4K memory address, since the addressing will wrap around after F000H. Beginning at row 0, each 4K row proceeds sequentially from top to bottom. Thus, if the board is addressed to begin at 8000H, row 0 would control the 4K block from 8000H to 8FFFH, row 1 would control 9000H to 9FFFH, and so on to row 7, which would control F000H to FFFFH. If the board were addressed to begin at E000H (so that it would have to wrap around), row 0 would control E000H to EFFFH, row 1 F000H to FFFFH, row 2 0000H to 0FFFH, and so forth until row 7, which would control 5000H to 5FFFH.

**SWITCH S-2, PADDLE 5 : GLOBAL ENABLE**

Switch S-2 paddle 5 is used to set the addressing mode of the **RAM 20** to Global. If this switch is put in the 'ON' position, the **RAM 20** will become Global RAM-- i.e., it will occupy the same address space on ALL pages. In Global mode, sockets U6, U10 and U11 should be empty. If S-2 paddle 5 is set 'OFF', the **RAM 20** must be set up either as an Extended Address board or as a Bank Select board. See instructions under **SWITCH S-3** for setting up the **RAM 20** for Extended Addressing. For setting the board for Bank Selection, see **SWITCH S-2, PADDLES 7 & 8, SWITCH S-3,** and **SWITCH S-4.**

**SWITCH S-2, PADDLE 6 : PHANTOM ENABLE**

Switch S-2 paddle 6 allows the assertion of the PHANTOM line (S-100 line 67) to disable the **RAM 20.** When PHANTOM is asserted (low) and S-2 paddle 6 is set to 'ON', the on board RAM cannot be read or written. This applies to ALL addressing modes. Many S-100 Power-on-Jump circuits rely on the ability of system RAM to be disabled by the PHANTOM line, as do a

number of Interrupt Controller boards. Setting S-2 paddle 6 'OFF' will cause the **RAM 20** to disregard PHANTOM.

### SWITCH S-2, PADDLES 7 & 8 : BANK SELECT POWER-UP STATUS

Paddles 7 and 8 of Switch S-2 control the status of **RAM 20** RAM immediately after a reset. These paddles are of concern only when the board is operating in Bank Select mode. When in Bank Select mode (IC's U6 and U10 installed), these paddles must always be set opposite one another. Setting paddle 7 'ON' and paddle 8 'OFF' will cause the **RAM 20** bank to be initially enabled, without the need of outputting the proper data to its Bank Select I/O port. Setting paddle 7 'OFF' and paddle 8 'ON' will cause the board to be initially disabled. This allows a Bank Select system to power up with a full complement of memory without the need of first executing some Bank Selection code.

### ATTENTION USERS OF OLDER S-100 CPU'S

The **RAM 20** monitors two S-100 lines to determine whether a reset condition exists: pRESET* (line 75) and SLAVECLR* (line 54). The functions of these lines are fully described in IEEE spec 696. The assertion (a low level in both cases) of either or both of these lines will always disable the **RAM 20** for as long as the reset condition lasts and, in Bank Select mode, will cause the board to revert to its start-up status as set by paddles 7 and 8 of Switch S-2. CPU's which do not drive SLAVECLR* (line 54) and which are not running in a terminated bus risk sporadic deselection of the **RAM 20** due to possible noise on this unterminated line. Under these circumstances, it is recommended that pRESET* (line 75) and SLAVECLR* (line 54) be tied together somewhere in the system. A convenient place is on the solder side of the **RAM 20** board, by jumpering pins 1 and 2 of IC U12 (a 74LS10). This modification will not void the board warranty.

### SWITCH S-3 : EXTENDED ADDRESS OR BANK SELECT PORT ADDRESS

Switch S-3 is used to set either the Extended Address or the Bank Select port address of the **RAM 20**. In Global mode, this switch is ignored. The setting of this switch and the inclusion and exclusion of IC's U6, U10 and U11 for the three modes is described below:

### SWITCH S-3 GLOBAL MODE

1. Sockets U6, U10 and U11 SHOULD BE LEFT EMPTY.
2. Ignore SWITCH S-3.

### SWITCH S-3 EXTENDED ADDRESS MODE

1. Place a 25LS2521 in socket U11.
2. Sockets U6 and U10 SHOULD BE LEFT EMPTY.

| | PADDLE NUMBER | EXTENDED ADDRESS LINE |
|---|---|---|
| | 1 | A16 |
| 'ON' = '0' | 2 | A17 |
| | 3 | A18 |
| 'OFF' = '1' | 4 | A19 |
| | 5 | A20 |
| | 6 | A21 |
| | 7 | A22 |
| | 8 | A23 |

EXAMPLE: To set the **RAM 20** to reside in extended page 80XXXXH, paddle 8 of S-3 should be turned 'OFF', and paddles 1 - 7 should be turned 'ON'.

**SWITCH S-3 BANK SELECT MODE**

1. Place a 74LS74 in socket U6 and a 25LS2521 in socket U10.
2. Socket U11 SHOULD BE LEFT EMPTY.

| | PADDLE NUMBER | BANK ADDRESS BIT |
|---|---|---|
| | 1 | A0 |
| 'ON' = '1' | 2 | A1 |
| | 3 | A2 |
| 'OFF' = '0' | 4 | A3 |
| | 5 | A4 |
| | 6 | A5 |
| | 7 | A6 |
| | 8 | A7 |

EXAMPLE: To set the **RAM 20** to reside in Bank 40H, paddle 7 of S-3 should be turned 'ON', and paddles 1 - 6 as well as paddle 8 should be turned 'OFF'.

**SWITCH S-4 : BANK SELECT DATA BIT DECODE**

Switch S-2 is used to select the data bit that will enable the **RAM 20** when an output cycle addresses the Bank Select I/O port selected by Switch S-3. This switch may be ignored when operating the **RAM 20** in Global or Extended Address mode. The use of S-4 is described below:

**SWITCH S-4 SETTINGS**

1. For Bank Select Mode, Place a 74LS74 in socket U6 and a 25LS2521 in socket U10.
2. Socket U11 SHOULD BE LEFT EMPTY.
3. Ignore this switch in Global or Extended Address Modes.

| | PADDLE NUMBER | DATA BIT |
|---|---|---|
| | 1 | D0 |
| 'ON' = '1' | 2 | D1 |
| | 3 | D2 |
| 'OFF' = '0' | 4 | D3 |
| | 5 | D4 |
| | 6 | D5 |
| | 7 | D6 |
| | 8 | D7 |

EXAMPLE: To set the **RAM 20** to become selected when data bit 4 is output high to the I/O port selected by Switch S-3, set paddle 5 'ON', and paddles 1 - 4, and 6 - 8 'OFF'.

## RAM 20 ADDRESSING MODES

Three addressing modes are supported by the **RAM 20:**

1. Global
2. Extended Address
3. Bank Select

The **RAM 20** must be assigned one of these three modes. Within a given **RAM 20**, only one mode is possible (e.g., one cannot have half the board Global and the other half Bank Select), but it is possible to configure a SYSTEM with a combination of Global, Extended Address and Bank Select boards. These modes are selected both through special switch settings and through the use or disuse of three IC sockets, namely, U6, U10 and U11. In Global mode, none of these sockets should be filled; in Extended Address mode, only U11 should be filled; in Bank Select mode, U6 and U10 should be filled.

## DEFINITION OF A MEMORY PAGE

When this manual refers to a Page NN of memory, it means a 64K byte block beginning at NN0000H and ending at NNFFFFH. Since IEEE spec 696 defines 24 address lines, there are 256 possible pages on the S-100 Bus. Each page is uniquely identified by the 8 highest address lines (the 'Extended Address' lines), A16-A23. Thus, Page 0 (Base Page) extends from 000000H to 00FFFFH, Page 1 from 010000H to 01FFFFH, etc.

**GLOBAL MODE :** (U6, U10, and U11 empty) (Switch 2, Paddle 5 'ON')

Global memory is memory that occupies all pages. In Global Mode, the **RAM 20** will respond only to the lower 16 S-100 address lines (A0-A15), ignoring the upper 8 lines (A16-A23) and disregarding any I/O instructions. Global memory boards allow an area of memory that is common to all pages-- a necessity for standard Bank Select schemes. Global memory also limits the amount of non-global memory available in any page, since the lower 16 bits of Extended Address or Bank Select memory must not conflict with the system's global memory. Thus if a Global board is addressed from 0000H to 7FFFH (the first 32K), then the lower 16 bit addressing of any Extended Address or Bank Select board in the system must fall between 8000H and FFFFH, limiting each non-global board in this example to a maximum of 32K.

The maximum Global memory possible in a system is 64K.

**EXTENDED ADDRESS MODE :** (U11 filled, U7 and U10 empty) (Switch 2, paddle 5 'OFF')

Extended Address memory occupies a single page and no other. In Extended Address mode, the **RAM 20** will decode all 24 address lines in order to become selected. It will also ignore any I/O instruction. Although all 8 bit S-100 CPU boards will generate the lower 16 address bits (A0-A15), few besides COMPUPRO CPU's are capable of generating the

additional 8 address bits (A16-A23). In order to generate these 8 extra address bits in a system driven by an 8 bit CPU, some type of 'memory manager' device is required.

**Memory Managers** For our purposes, a memory manager is any device capable of driving address lines which the CPU cannot drive. COMPUPRO produces CPU boards with built-in memory management circuitry, and a stand-alone memory manager board is available as well. These can be made to generate address bits A16-A23 through the following software mechanism:

1. Assign the memory manager an I/O port number
2. Output the page number to the memory manager port

As an example, suppose that an Extended Address memory board is addressed to Page 5 (05XXXXH), and the memory manager is addressed to I/O port FDH. The following 8080 assembly code will qualify this board for selection:

```
MVI  A,5   ;page number into accumulator
OUT  0FDH  ;output to memory manager port
```

The above sequence would cause the memory manager to latch the contents of the accumulator (in this case a five) onto the Extended Address lines (A16-A23), and preserve these lines in this state until they are changed by a subsequent output to the memory manager port or by a system reset. Specifically, Extended Address lines A16 and A18 would be latched high, while the other six Extended Address lines would be latched low.

The above software mechanism is compatible with that used by conventional 'Bank Select' schemes. In fact, it would be impossible to tell from a software standpoint whether a 'Bank Select' system were implemented with Bank Select boards, Extended Address boards plus a memory manager, or a combination of both.

The maximum Extended Address memory available in a system is 256 times 64K, or 16 Megabytes.

**BANK SELECT MODE** : (U7 and U10 filled, U11 empty) (Switch 2, paddle 5 'OFF')

Bank Select memory uses I/O decoding to extend Page 0 (Base Page) so that Page 0 supports more than 64K bytes of memory. Bank Select memory ignores extended address lines A16-A23. In a conventional Bank Select scheme, a certain block of Page 0 memory is made Global (appears in all Banks), and every Bank Select board is addressed within the area of Page 0 NOT occupied by the Global memory. Usually all Bank Select boards are addressed to the same Page 0 space.

Though the software used to qualify a Bank Select board is the same as that used with a memory manager to qualify an Extended Address board, the memory board hardware requirements for these two modes differ radically. Each Bank Select board must have a built-in I/O port decoder so that the board can be assigned an I/O port number (usually the same for all Bank Select boards in a system). A Bank Select board must also have a data bit

decode circuit. These two circuits monitor all system I/O write instructions and will qualify the board for memory selection if and only if two conditions are true:

1. An output instruction is executed to the port address to which the Bank Select board is assigned.

2. The data byte being output contains at least one bit high which matches a bit set high in the Bank Select board's data bit decode circuit.

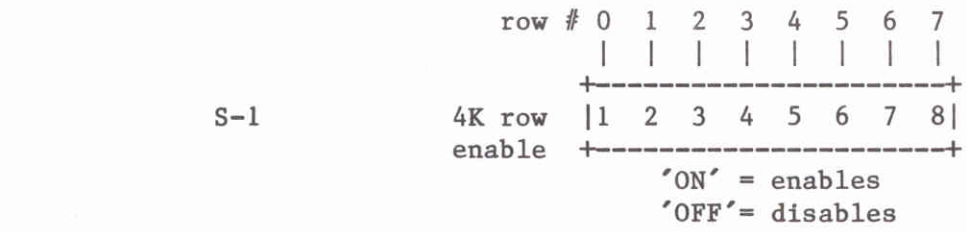
Thus when using the **RAM 20** in Bank Select mode, it is necessary to choose both an I/O port number for the board to monitor (selected through DIP switch S-3) and a data bit qualifier (selected through DIP switch S-4).

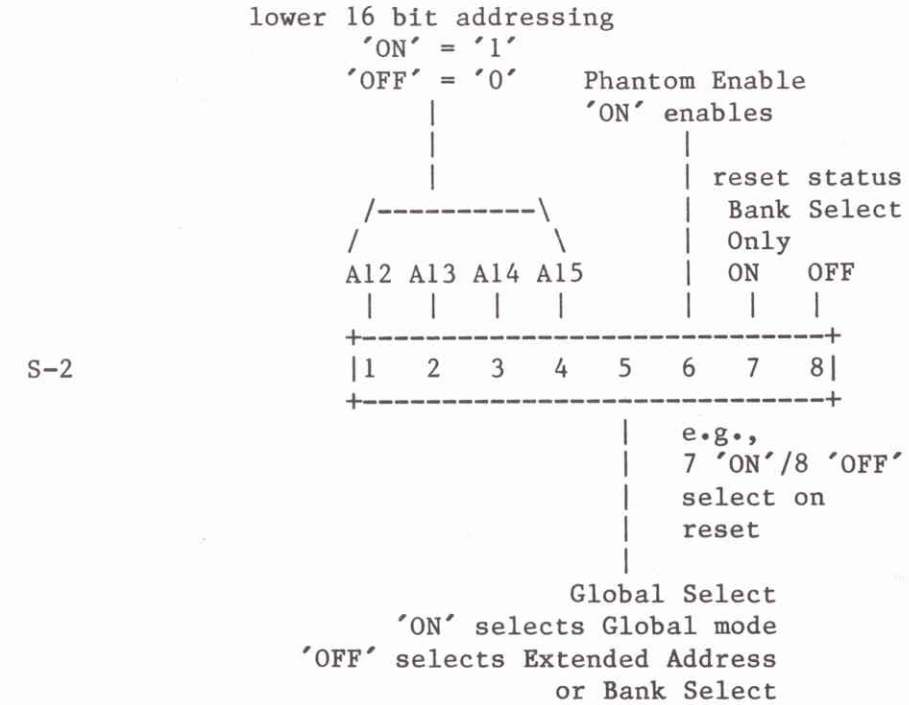
As an example of using Bank Selection, suppose that two boards are addressed at I/O port 40H and memory address 8000H, and that the first board is set to select when data bit 0 is high and the second when data bit 1 is high. The following 8080 program, when run out of Global memory below 8000H, would put the contents of Register B into address 8000H of the first board and the contents of Register C into address 8000H of the second board.

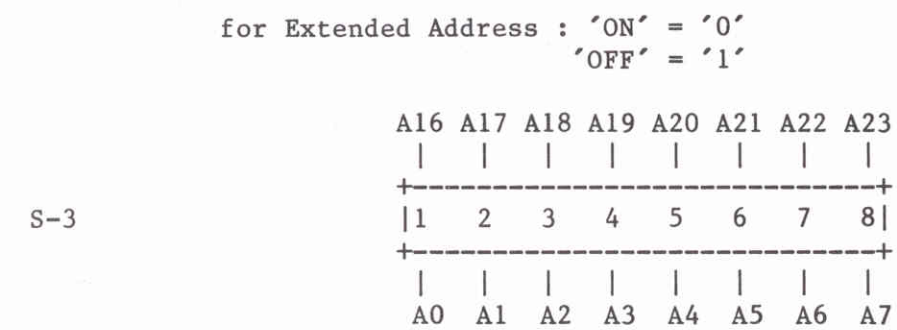
```
LXI   H,8000H   ;HL Reg points to address 8000H
MVI   A,1       ;Set data bit 0 high for Bank 1
OUT   40H       ;Qualify Bank 1 and kill other Banks
MOV   M,B       ;Contents of Reg B into Bank 1
INR   A         ;Set data bit 1 high for Bank 2
OUT   40H       ;Qualify Bank 2 and kill other Banks
MOV   M,C       ;Contents of Reg C into Bank 2
```

The maximum number of Banks (of some size less than 64K) possible in a system is 256 (I/O ports) X 8 (data bits)= 2048.

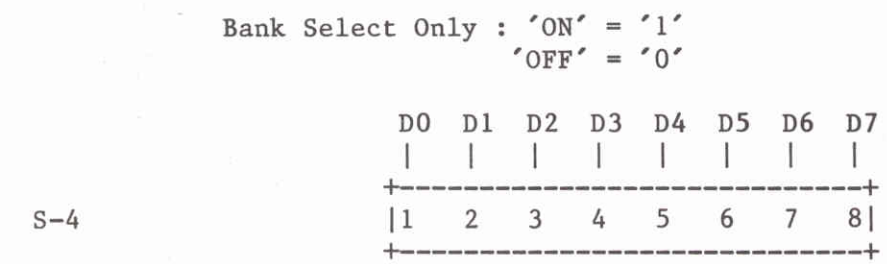
**SWITCH SETTINGS AT A GLANCE** (see Manual for Complete Description)

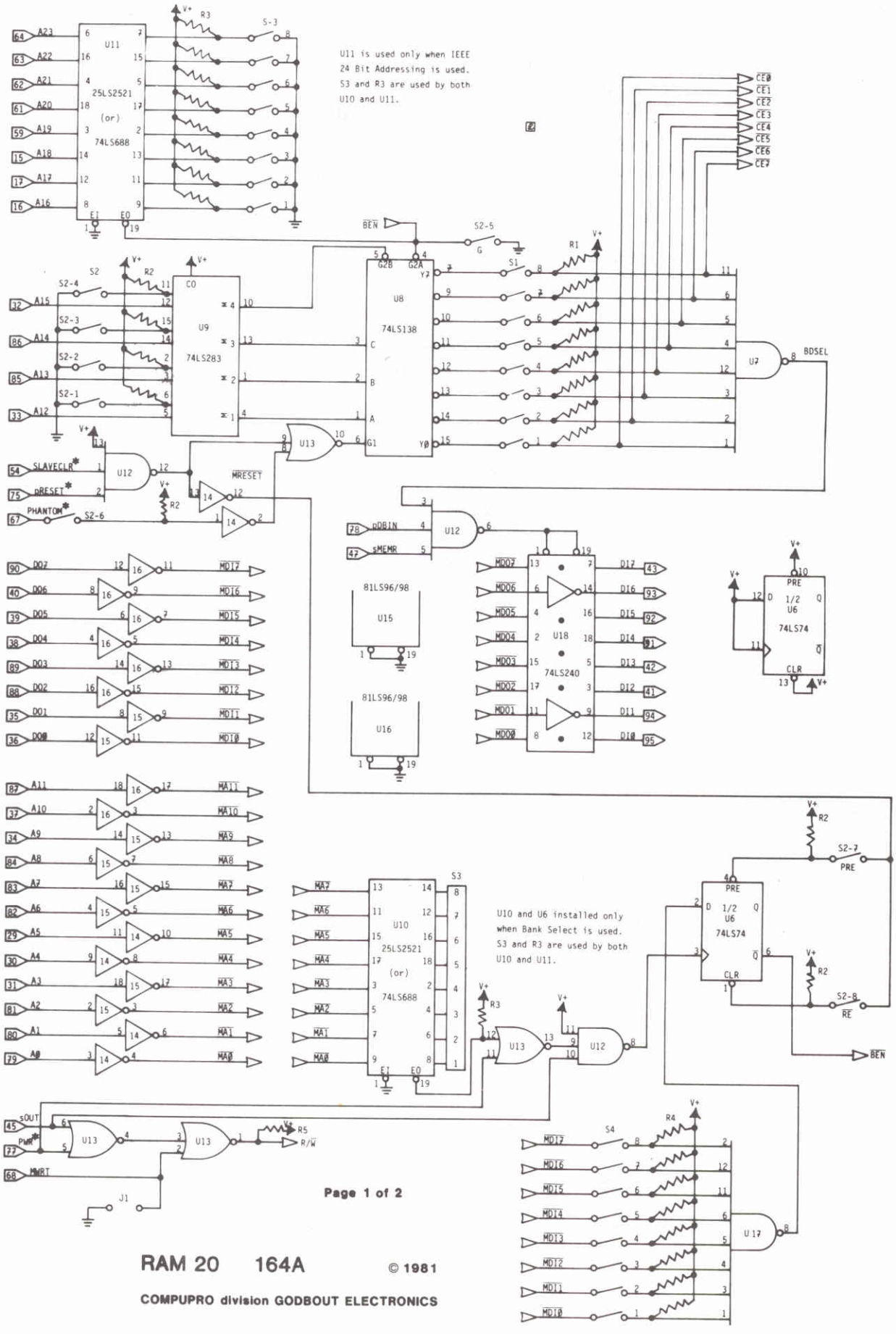





for Bank Select : 'ON' = '1'
'OFF' = '0'



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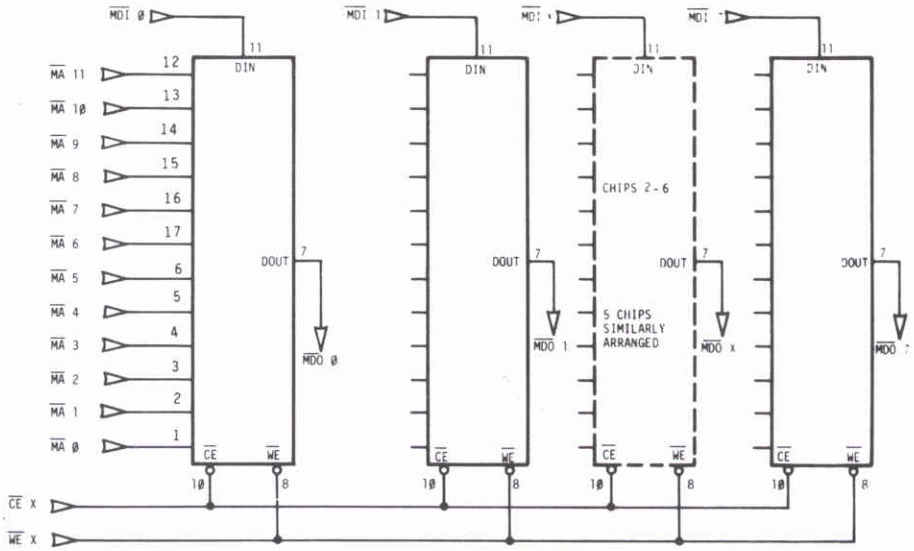


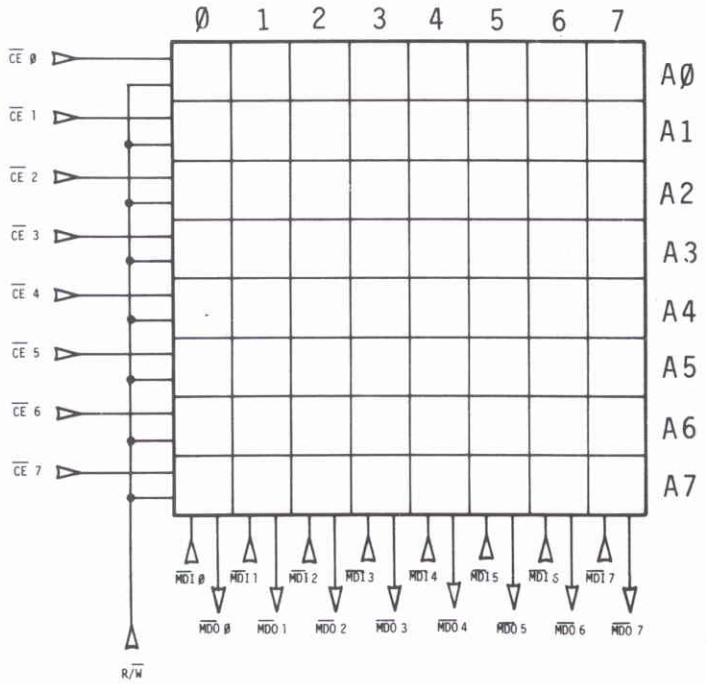




## RAM 20 164A



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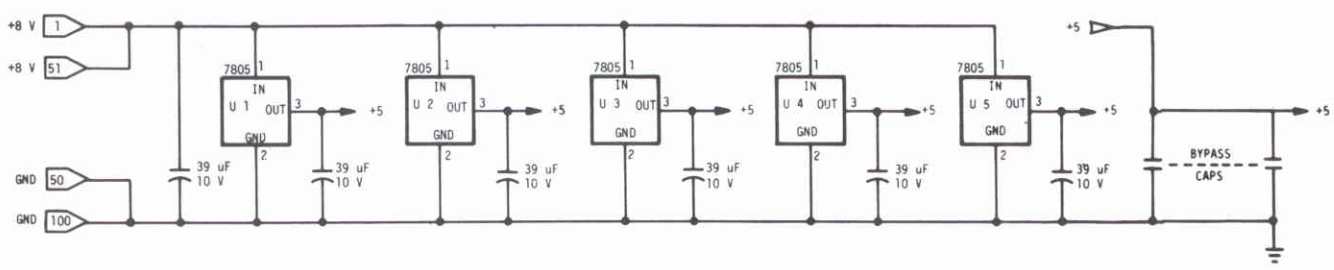


## PARTS LIST

INTEGRATED CIRCUITS (Note: the following parts may have letter suffixes and prefixes along with the key numbers given below.)

| | | | |
|---|---|---|---|
| (64) | MM5257N-3L | 4K x 1 static RAM | |
| (1) | 74LS02 | quad 2 input NOR | (U13) |
| (1) | 74LS04 | hex inverter | (U14) |
| (1) | 74LS10 | triple 3 input NAND | (U12) |
| (2) | 74LS30 | 8 input NAND | (U7, U17) |
| (1) | 74LS74 | dual "D" flip flop | (U6) |
| (1) | 74LS138 | decoder | (U8) |
| (1) | 74LS240 | octal bus driver | (U18) |
| (1) | 74LS283 | 4 bit adder | (U9) |
| (1) | 25LS2521 | octal comparator | (U11, or U10) |
| (2) | 81LS96/98 | octal inverter | (U15, U16) |
| (5) | 7805 | 5 volt regulator | (U1 - U5) |

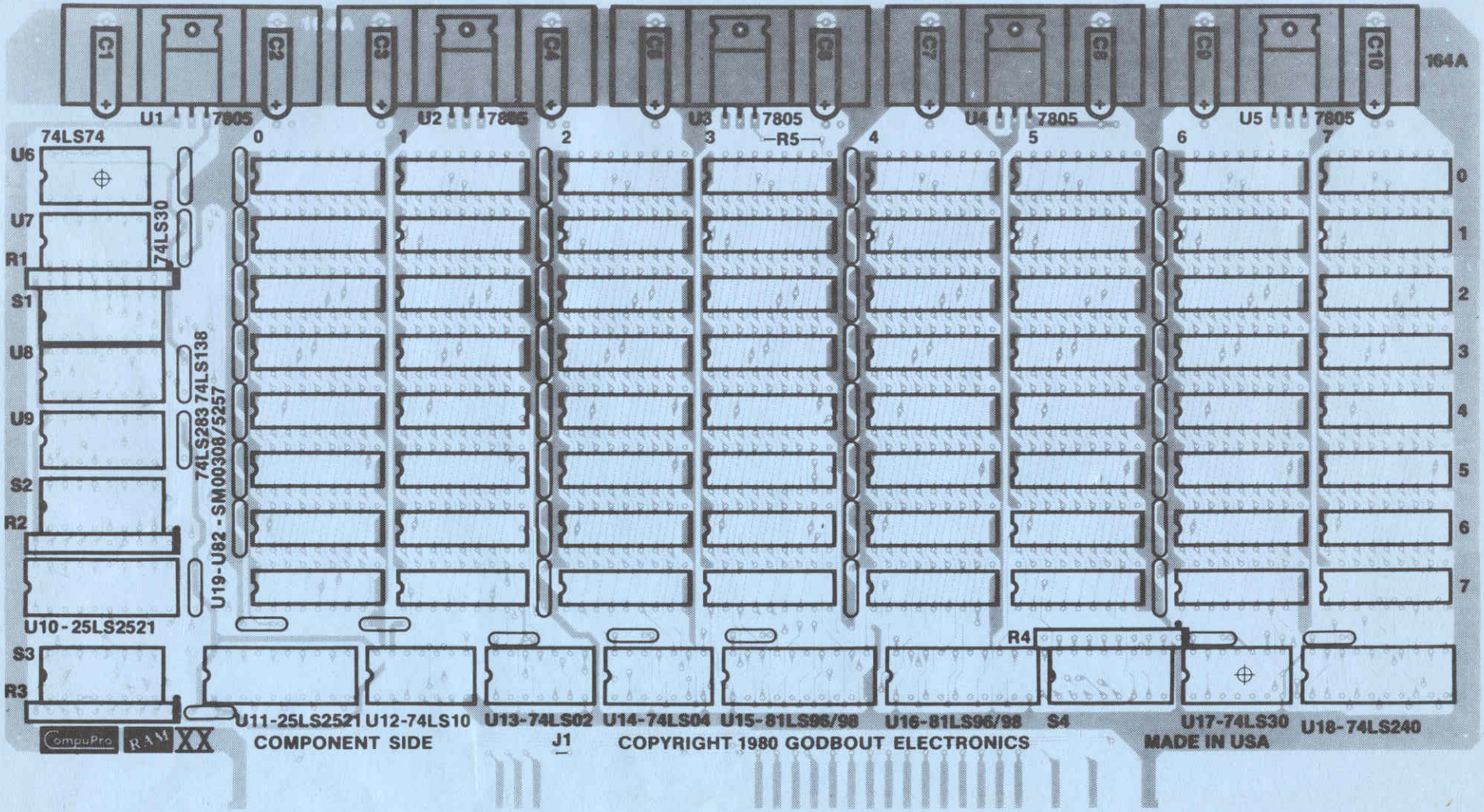
OTHER ELECTRICAL COMPONENTS

| | | |
|---|---|---|
| (4) | SIP resistor packs* | (R1 - R4) |
| (10) | 39 uf Tantalum capacitors | (C1 - C10) |
| (45) | Ceramic bypass capacitors* | |
| (1) | 2.7 ohm resistor 1/4 w | (R5) |

MECHANICAL COMPONENTS

| | | |
|---|---|---|
| (1) | Circuit board | |
| (77) | Low profile sockets* | |
| (4) | DIP switch, 8 position | (S1 - S4) |
| (5) | TO-220 heat sinks | |
| (5) | Sets 6-32 hardware | |
| (1) | User manual | |

* supplied already soldered to board




# COMPONENT LAYOUT

## CUSTOMER SERVICE INFORMATION

Our paramount concern is that you be satisfied with any Godbout CompuPro product. If this product fails to operate properly, it may be returned to us for service; see warranty information below.

If you need further information feel free to write us at:

**P.O. Box 2355, Oakland Airport, CA 94614.**

When writing, please be as specific as possible concerning the nature of your query. We maintain a 24 hour a day phone for taking orders, (415) 562-0636. If you have any problems or questions which cannot be handled by mail, this number can be used to connect you with our technical people ONLY during normal business hours (10am-5pm Pacific Time). We cannot return calls or accept collect calls.

## LIMITED WARRANTY INFORMATION

Godbout Electronics will repair or replace, at our option, any parts found to be defective in either materials or workmanship for a period of 1 year from date of invoice. Defective parts *MUST* be returned for replacement.

If a defective part causes a Godbout Electronics product to operate improperly during the 1 year warranty period, we will service it free (original owner only) if delivered and shipped at owner's expense to and from Godbout Electronics. If improper operation is due to an error or errors on the part of the purchaser, there may be a repair charge. Purchaser will be notified if this charge exceeds $50.00.

We are not responsible for damage caused by the use of solder intended for purposes other than electronic equipment construction, failure to follow printed instructions, misuse or abuse, unauthorized modifications, use of our products in applications other than those intended by Godbout Electronics, theft, fire, or accidents.

Return to purchaser of a fully functioning unit meeting all advertised specifications in effect as of date of purchase is considered to be complete fulfillment of all warranty obligations assumed by Godbout Electronics. This warranty covers only products marketed by Godbout Electronics and does not cover other equipment used in conjunction with said products. We are not responsible for incidental or consequential damages.

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