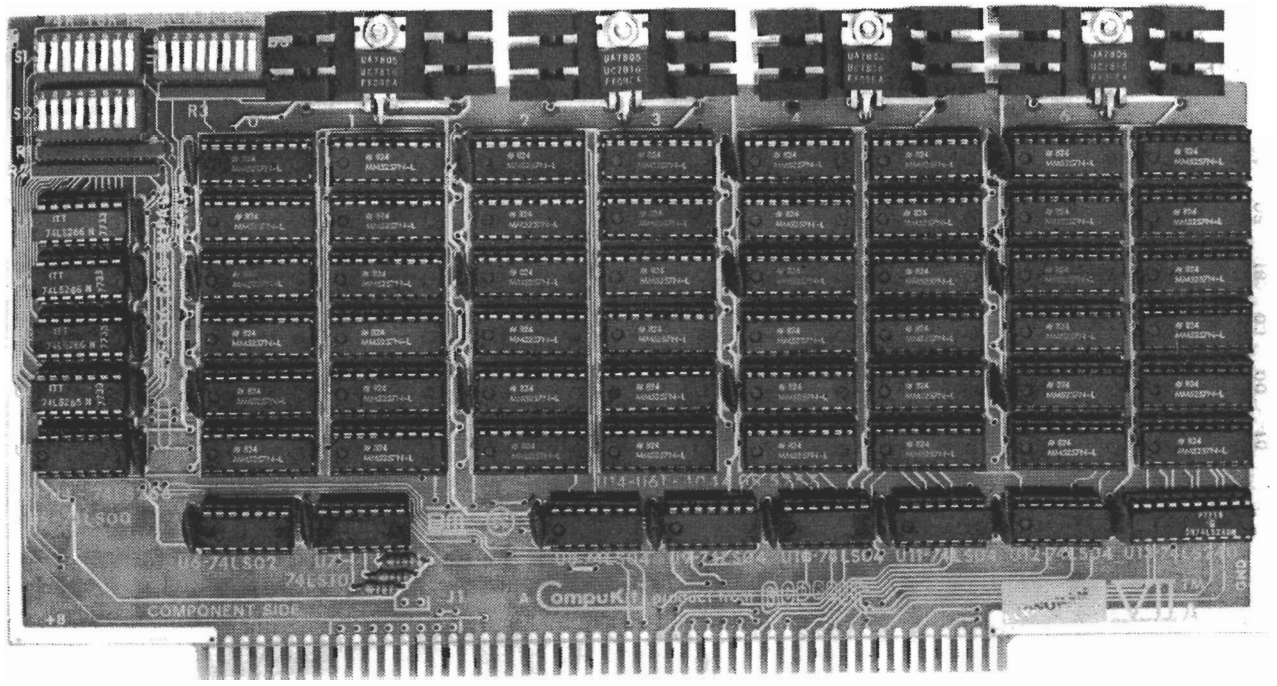
# ECONORAM VII A T.M.
# USER'S MANUAL




## 24K x 8 static memory · S-100
### using MM5257/TMS40L44 · 4MHz

122 mac

A CompuKit T.M. product from GODBOUT

Rev 3/79

## ABOUT ECONORAM VII

Congratulations on your decision to purchase ECONORAM VII, a 24K x 8 memory board designed specifically for electrical and mechanical compatibility with the S-100 buss standard. The S-100 buss currently is one of the most popular in the industry and by far the most prolific; we believe this board, with the rest of the S-100 portion of the ECONORAM family, is one of the best memory boards available for that buss.

We recommend that the parts in this kit be checked against the parts list for completeness and that these instructions be read through carefully before starting. Completion of the assembly should take from one to four hours, depending on previous assembly experience, and upon completion, you will discover -- as thousands of satisfied ECONORAM owners have discovered -- the pleasure of using a fine memory board that just works, and works, and works.

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing ECONORAM VII . . . welcome to the club.

## TECHNICAL OVERVIEW

This board incorporates proven static memory technology. There are currently two popular types of memory being used in products such as this: static and dynamic. Static memories are the overwhelming choice in applications where speed, complexity, ease of use, and reliability must all be considered. There is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far more reliable and easier to implement.

The individual memory ICs used on this board are grouped together to form four larger blocks of memory, two 4K X 8 and two 8K X 8. The 4K blocks may be addressed on any 4K boundary, and the 8K blocks on any 8K boundary by setting the starting locations with the on-board dip switch (no jumpers required). Additional features include write protect switches for each of the four blocks; a write strobe selection switch which allows use of memory in systems with or without a front panel (MWRITE strobe); allowance for use with or without the PHANTOM line; thorough capacitor bypassing of supply lines to suppress transients plus on-board regulation and heat-sinking for reliably cool operation. All this and sockets for all ICs go onto a double-sided, solder-masked printed circuit board with a complete component-layout legend.

# Parts List

Upon receipt of your kit, check your parts against the list below.

- ☐ (1) Econoram VIIA circuit board

**INTEGRATED CIRCUITS** (note: the following parts may have letter suffixes and prefixes along with the key numbers given below.)

- ☐ (48) MM5257N-3L or TMS 40L44 (U14 - U61)
- ☐ (1) 74LS00 nand gate (U5)
- ☐ (1) 74LS10 3-input nand gate (U7)
- ☐ (1) 74LS02 nor gate (U6)
- ☐ (5) 74LS04 hex inverters (U8 - U12)
- ☐ (1) 74LS240 TRI-STATE® inverters (U13)
- ☐ (4) 74LS266 ex-nor o.c. (U1 - U4)
- ☐ (4) 7805 positive 5V regulators (U62 - U65)

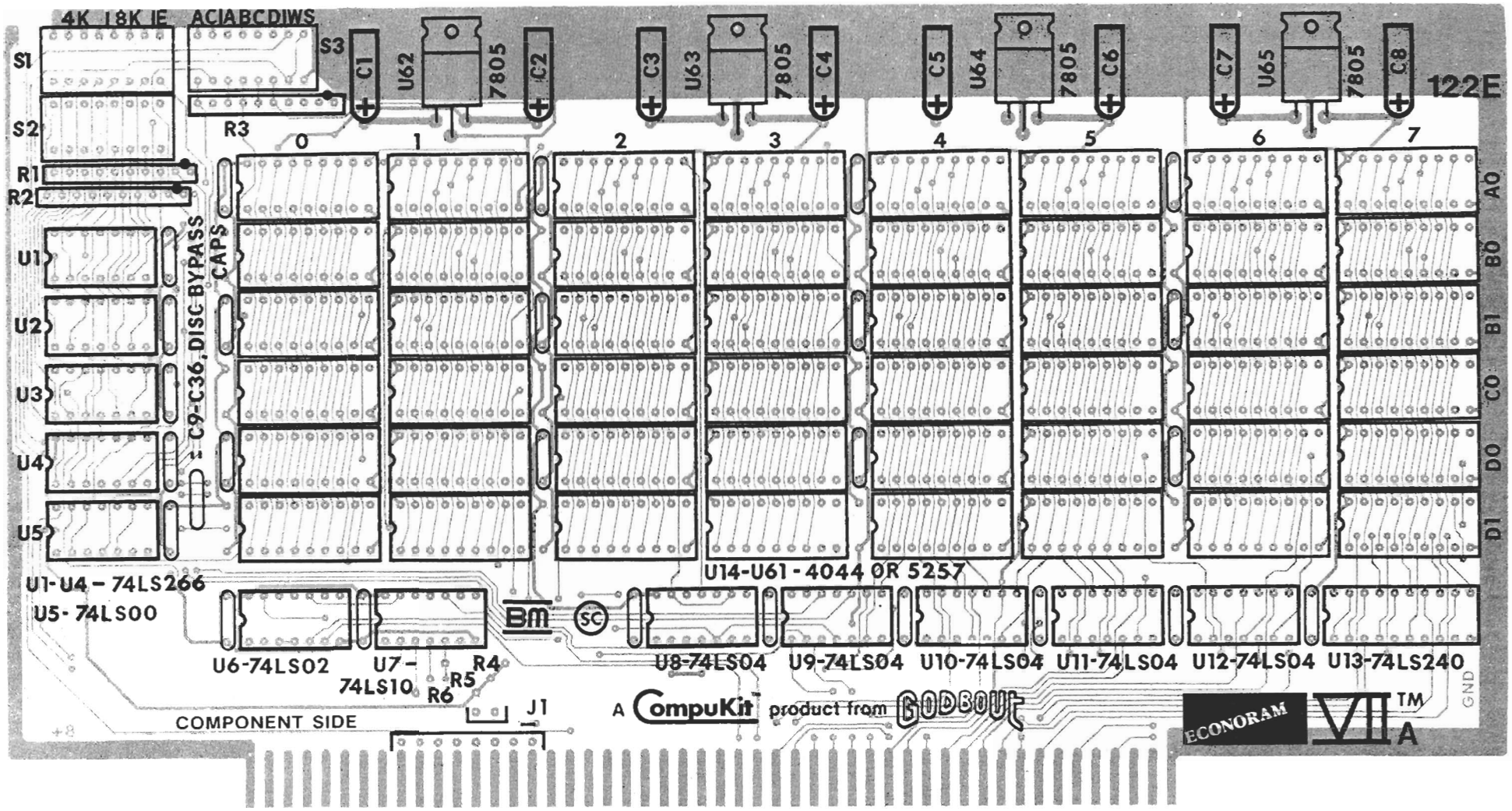
**OTHER ELECTRONIC COMPONENTS**

- ☐ (3) S.I.P. resistor packs (R1 - R3)*
- ☐ (3) 2.7K 1/4 watt resistors (red-violet-red; R4 - R6)
- ☐ (8) 39uF tantalum capacitors (C1 - C8)
- ☐ (25) ceramic disk bypass capacitors*

**MECHANICAL COMPONENTS**

- ☐ (61) low profile sockets*
- ☐ (3) dipswitch (S1 - S3)*
- ☐ (4) TO-220 heat sinks
- ☐ (4) 6-32 bolts
- ☐ (4) 6-32 lockwashers
- ☐ (4) 6-32 hex nuts
- ☐ (1) instruction booklet

*supplied already soldered to board.




# Component Layout

UP

## MEMORY ADDRESS CONFIGURATION

This board is configured as two 4K blocks addressable on 4K boundaries and two 8K blocks independently addressable on 8K boundaries. Switches S1 and S2 each select one 4K and one 8K block. (switch S1 : block A - 4K and block B - 8K, switch S2 : block C - 4K and block D - 8K) as follows:

| 4K | | 8K | |
|---|---|---|---|
| SWITCH POSITION | STARTING ADDRESS | SWITCH POSITION | STARTING ADDRESS |
| 1 2 3 4 | | 5 6 7 | |
| Ø Ø Ø Ø | ØØØØ | Ø Ø Ø | ØØØØ |
| Ø Ø Ø 1 | 1ØØØ | Ø Ø 1 | 2ØØØ |
| Ø Ø 1 Ø | 2ØØØ | Ø 1 Ø | 4ØØØ |
| Ø Ø 1 1 | 3ØØØ | Ø 1 1 | 6ØØØ |
| Ø 1 Ø Ø | 4ØØØ | 1 Ø Ø | 8ØØØ |
| Ø 1 Ø 1 | 5ØØØ | 1 Ø 1 | AØØØ |
| Ø 1 1 Ø | 6ØØØ | 1 1 Ø | CØØØ |
| Ø 1 1 1 | 7ØØØ | 1 1 1 | EØØØ |
| 1 Ø Ø Ø | 8ØØØ | | |
| 1 Ø Ø 1 | 9ØØØ | | |
| 1 Ø 1 Ø | AØØØ | | |
| 1 Ø 1 1 | BØØØ | | |
| 1 1 Ø Ø | CØØØ | Ø = OFF | |
| 1 1 Ø 1 | DØØØ | | |
| 1 1 1 Ø | EØØØ | 1 = ON | |
| 1 1 1 1 | FØØØ | | |

In addition, position 8 on each switch enables (OFF) or disables (ON) the associated 8K block. Positions 1 and 2 of switch S3 disable/enable the 4K blocks A and C respectively.

## MEMORY PROTECT SWITCHES

Switch S3 positions 3-6 are write enable switches. Conversely they may be used for manual write protection of the memory. Each position 3, 4, 5 and 6 is associated wih one memory block A, B, C and D respectively. Any combination of these four swtiches may be ON write enabling or OFF write protecting the particular block.

## WRITE STROBE SELECT SWITCHES

Switch S3 positions 7 and 8 select write strobe. S3-8 ON causes $\overline{\text{PWR}}$ to qualify the memory for write commands. S3-7 ON causes MWRITE to qualify the memory for write commands. In normal operations with systems which have front panels ie., Altair, Imsai etc., or others which generate $\overline{\text{MWRITE}}$ with or without front panels use MWRITE. All others use $\overline{\text{PWR}}$. Positions 7 and 8 both ON at the same time will ground MWRITE on the buss. This condition must be avoided if MWRITE is present.

## MEMORY TESTING

If the memory board seems to be working properly, the Memory Testing Routine (page 11) can be used to give the board a more thorough workout. It is rather slow; but will do the job well. It can be entered via editor/assembler or front panel switches.

The routine is set up to test 24K from 4000 hex up to AØØØ hex. This may be changed by entering a different starting address at "STRT" (3001 - 3002) and/or a different end address at "END" (3004 - high order byte only).

If the memory passes the test it starts over again. You may on the other hand, insert a jump instruction at "MARK" to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart.

If the memory fails the test, critical information is stored and the routine enters a software "HALT", that is a "jump to here' at "SHLT". Front panel lights, if any, will show this state. The user may then use the front panel or dump routines to display the following stored failure info:

| | | |
|---|---|---|
| 3069* | "FDE" | = D, E pair . . . D is the fill character and E is the test character |
| 306B* | "FHL" | = H, L pair . . . the failure address |
| 306D* | "FOUT" | = the data expected at this address |
| 306E* | "FIN" | = the data read from, the address |

* address from *Memory Testing Routine Listing.*

The user may replace the "jump" at "SHLT" with a jump to a display or notification routine.

The difference between "FOUT" and "FIN" should indicate which bit is failing, indicating which chip or area is causing the problem.

This test will find most of the harder to distinguish errors.

## PHANTOM LINE

In response to increasing numbers of users who have requested inclusion of "PHANTOM LINE", buss pin 67 which is often used for implementing power on jump features. This board is designed for use with active or inactive PHANTOM lines.

### *CAUTION*

Some manufacturers use PHANTOM line (buss pin 67) for a refresh signal. This will conflict with the PHANTOM feature, and cause boards with PHANTOM to fail. If your system has this conflict it must be resolved by either eliminating the refresh signal on the CPU board or disabling the PHANTOM feature on this and other boards.

The PHANTOM feature may be disabled by cutting the trace on the back of the PC board between pads for J1. It may be reactivated at any time simply by installing a jumper at J1 (see Figure 11).

If you want the PHANTOM feature, the conficting refresh signal may be eliminated (IF NOT USED ELSEWHERE IN THE SYSTEM) by cutting the trace connected to buss pin 67 on the CPU board. *BE SURE OF YOUR SYSTEM CONFIGURATION BEFORE CUTTING ANY TRACES.*

## MEMORY TESTING ROUTINE

```
0000 21 00 40          0010 STRT LXI  H,4000H
0003 3E A0             0020 END  MVI  A,0A0H
0005 32 6E 30          0030      STA  FIN
0008 3E 10             0040      MVI  A,10H
000A 84                0050      ADD  H
000B 4F                0060      MOV  C,A
000C 16 00             0070      MVI  D,0
000E 1E FF             0080      MVI  E,0FFH
0010 22 65 30          0090 DONE SHLD STAD
0013 AF                0100      XRA  A
0014 47                0110      MOV  B,A
0015 7B                0120 SCND MOV  A,E
0016 5A                0130      MOV  E,D
0017 57                0140      MOV  D,A
0018 79                0150      MOV  A,C
0019 2A 65 30          0160      LHLD STAD
001C 72                0170 FILL MOV  M,D
001D 23                0180      INX  H
001E BC                0190      CMP  H
001F C2 1C 30          0200      JNZ  FILL
0022 2A 65 30          0210      LHLD STAD
0025 73                0220 NEXT MOV  M,E
0026 7B                0230      MOV  A,E
0027 BE                0240      CMP  M
0028 C2 6F 30          0250      JNZ  FAIL
002B 79                0260      MOV  A,C
002C 23                0270      INX  H
002D 94                0280      SUB  H
002E C2 4D 30          0290      JNZ  NDON
0031 B8                0300      CMP  B
0032 44                0310      MOV  B,H
0033 CA 15 30          0320      JZ   SCND
0036 3A 66 30          0325      LDA  STAD+1
0039 00                0330 MARK NOP
003A 00                0331      NOP
003B 00                0332      NOP
003C 3A 6E 30          0340      LDA  FIN
003F B9                0350      CMP  C
0040 CA 00 30          0360      JZ   STRT
0043 79                0370      MOV  A,C
0044 67                0380      MOV  H,A
0045 2E 00             0390      MVI  L,0
0047 C6 10             0400      ADI  10H
0049 4F                0410      MOV  C,A
004A C3 10 30          0420      JMP   DONE
004D 22 67 30          0430 NDON SHLD NXAD
0050 7A                0440 LOPB MOV  A,D
0051 BE                0450 LOPA CMP  M
0052 C2 6F 30          0460      JNZ  FAIL
0055 2C                0470      INR  L
0056 C2 51 30          0480      JNZ  LOPA
0059 79                0490      MOV  A,C
005A 24                0500      INR  H
005B BC                0510      CMP  H
005C C2 50 30          0520      JNZ  LOPB
005F 2A 67 30          0530      LHLD NXAD
0062 C3 25 30          0540      JMP  NEXT
0065                   0550 STAD DS   2
0067                   0560 NXAD DS   2
0069                   0570 FDE  DS   2
006B                   0580 FHL  DS   2
006D                   0590 FOUT DS   1
006E                   0600 FIN  DS   1
006F 22 6B 30          0610 FAIL SHLD FHL
0072 32 6D 30          0620      STA  FOUT
0075 7E                0630      MOV  A,M
0076 32 6E 30          0640      STA  FIN
0079 EB                0650      XCHG
007A 22 69 30          0660      SHLD FDE
007D C3 7D 30          0670 SHLT JMP  SHLT
0080                   0680 *
```

## CIRCUIT DESCRIPTION

The heart of Econoram VII is the MM5257/TMS4044 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4K x 1" memory IC). Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts.

These ICs are arranged in rows that are 8 ICs wide. This way, each row can store 4K x 8 bits of information. Paralleling 6 of these rows together produces a total memory storage of 24K x 8 bits. (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array).

Now that we have this storage, there are still other aspects we must consider. First, we need to address a specific location in memory; and, we need to be able to *write* data into the memory, or *read* data from the memory.

The schematics on pages 8 and 9 show the address circuitry along with the other Econoram VII circuitry. Each memory IC requires 12 address bits (A0-A11) to access any one of the 4096 bits available in the IC. These address bits are generated by the CPU and are buffered by a number of inverters. After buffering, a particular address is presented to all IC address selection pins. However, we additionally need to select which particular row of ICs is to react to the given address. This requires 4 more address bits (A12-A15), which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array).

When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buss). Data to be read on to the data buss from memory passes through 8 TRI-STATE® inverting buss drivers; when data is not being read on to the buss, the outputs of these inverters are in a high-impedance or "disconnected" state.

An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines. If these transients work their way into the logic circuitry, problems can appear. To prevent such occurances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC.

This board is guaranteed to operate at 4MHz over the full temperature range (0° - 70° C ambient) and to draw less than 2500 mA (2.5 amps). Our typical measured currents were less than 1210 mA at cold start-up, rapidly decreasing to around 1600-1900 mA, depending on the surrounding temperature. We have heard similar reports from the people already using these boards.

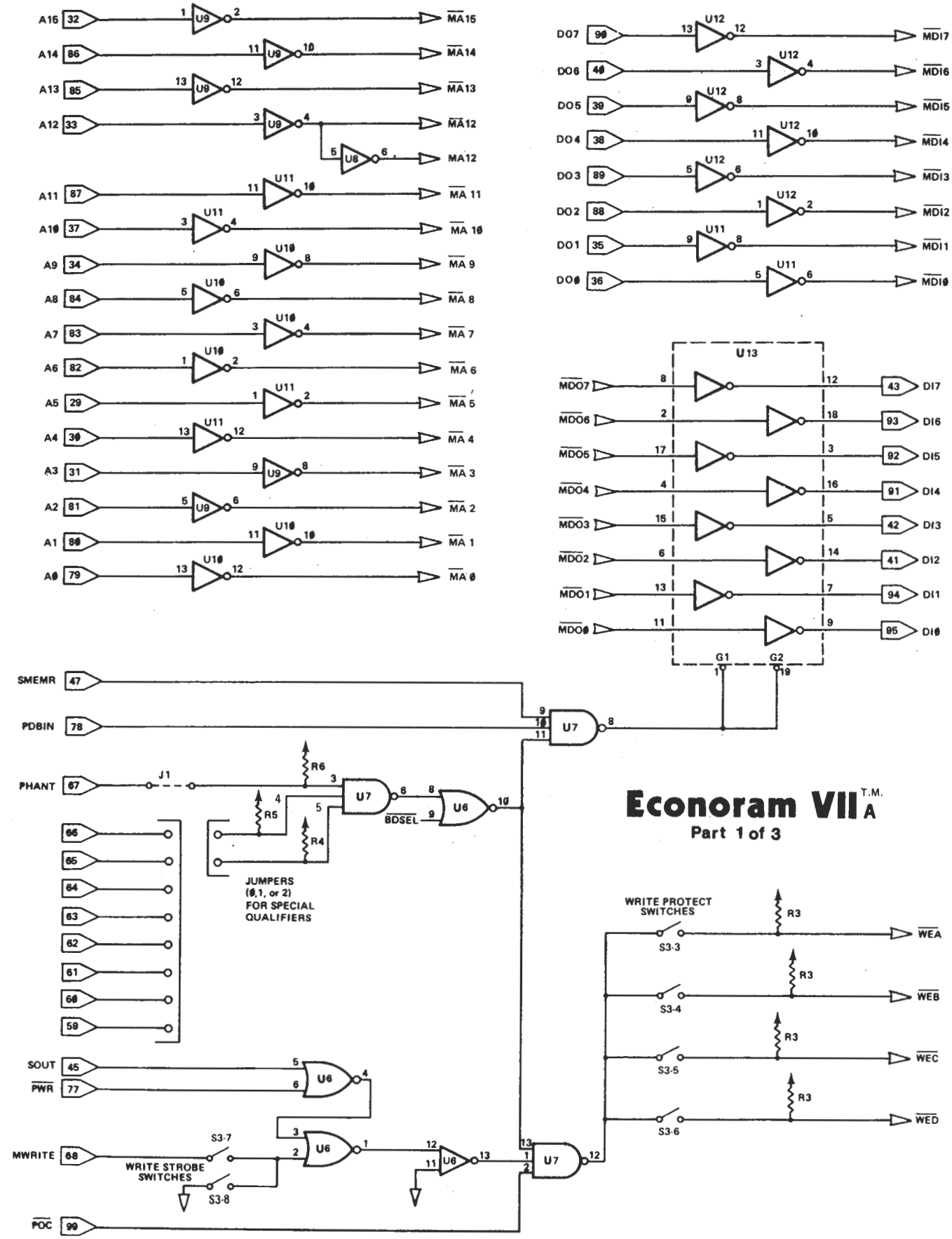
It is interesting to note that static RAM technology has progressed to the point that this high-performance static RAM board is comparable in cost and power consumption to dynamic memory boards.

## THANK YOU

This board is the result of much time, work and experience on the part of a number of people.

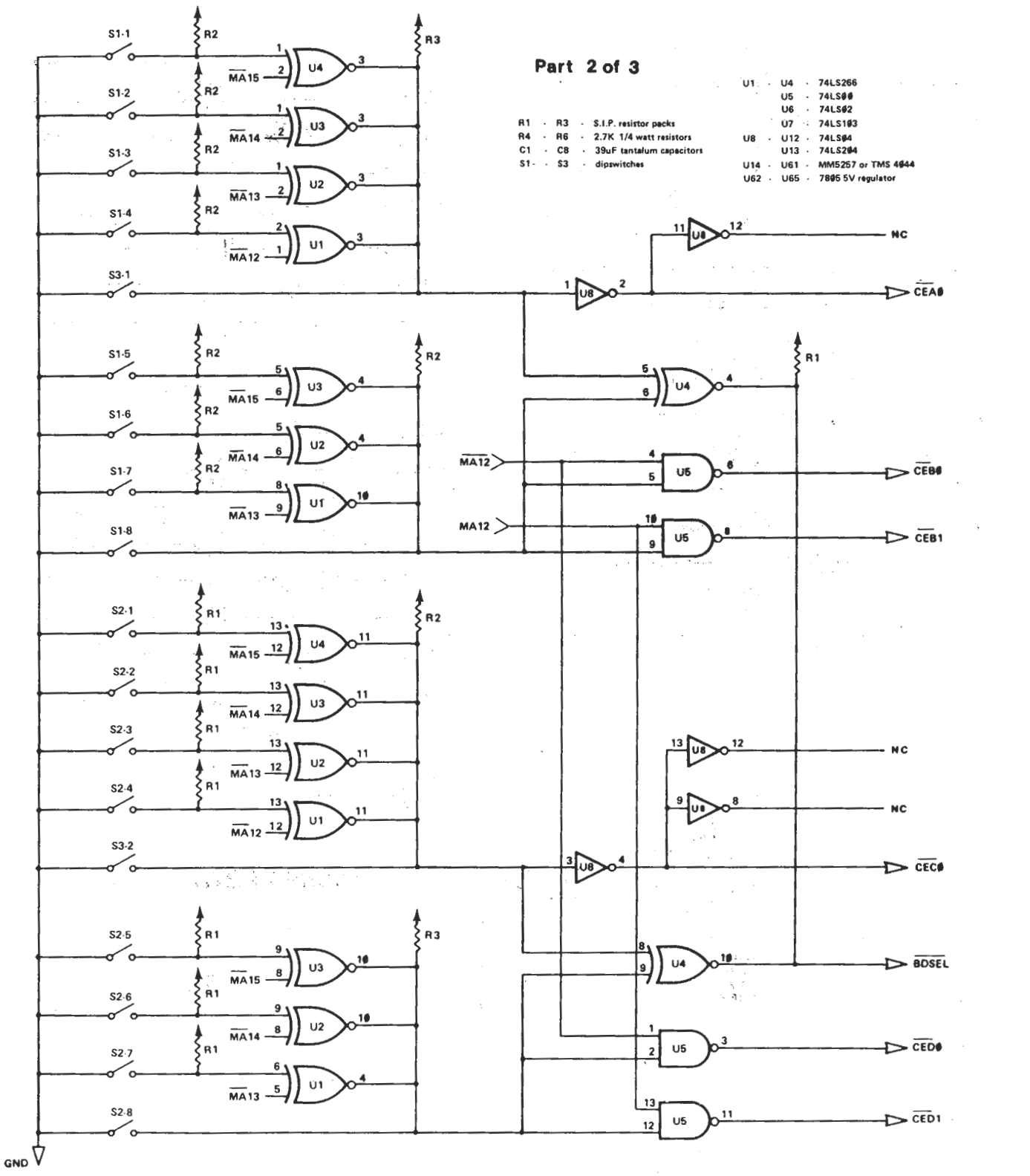
We strive for a board that doesn't just work the first time, but continues to give reliable operation for a long time. If we can be of any help to you in applying this board, or if you have any questions, please let us know. As always, we solicit your comments, letters, and new product suggestions.

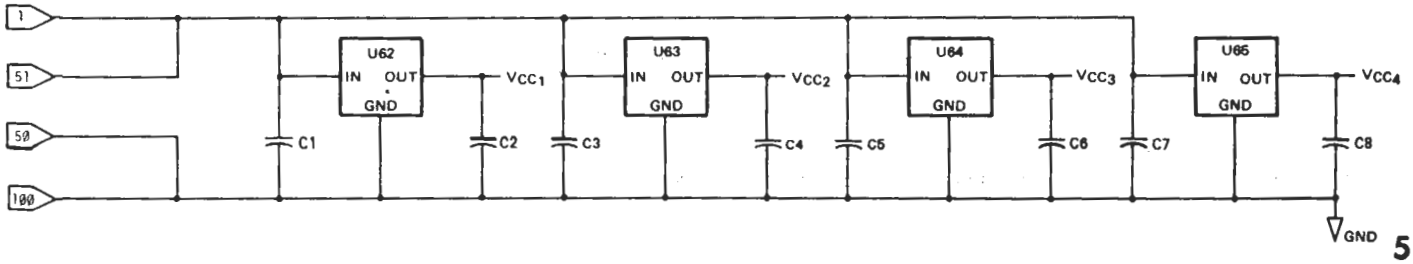
HAPPY COMPUTING!




# Econoram VII A T.M.

## Part 1 of 3


Part 2 of 3
R1 - R3 - S.I.P. resistor packs
R4 - R6 - 2.7K 1/4 watt resistors
C1 - C8 - 39uF tantalum capacitors
S1- - S3 - dipswitches
U1 - U4 - 74LS266
U5 - 74LS00
U6 - 74LS02
U7 - 74LS193
U8 - U12 - 74LS04
U13 - 74LS204
U14 - U61 - MM5257 or TMS 4044
U62 - U65 - 7805 5V regulator
S1-1
S1-2
S1-3
S1-4
S3-1
S1-5
S1-6
S1-7
S1-8
S2-1
S2-2
S2-3
S2-4
S3-2
S2-5
S2-6
S2-7
S2-8
R1
R2
R3
MA15
MA14
MA13
MA12
NC
CEA0
CEB0
CEB1
CEC0
BDSEL
CED0
CED1
GND


1
51
50
100
U62
U63
U64
U65
IN
OUT
GND
VCC1
VCC2
VCC3
VCC4
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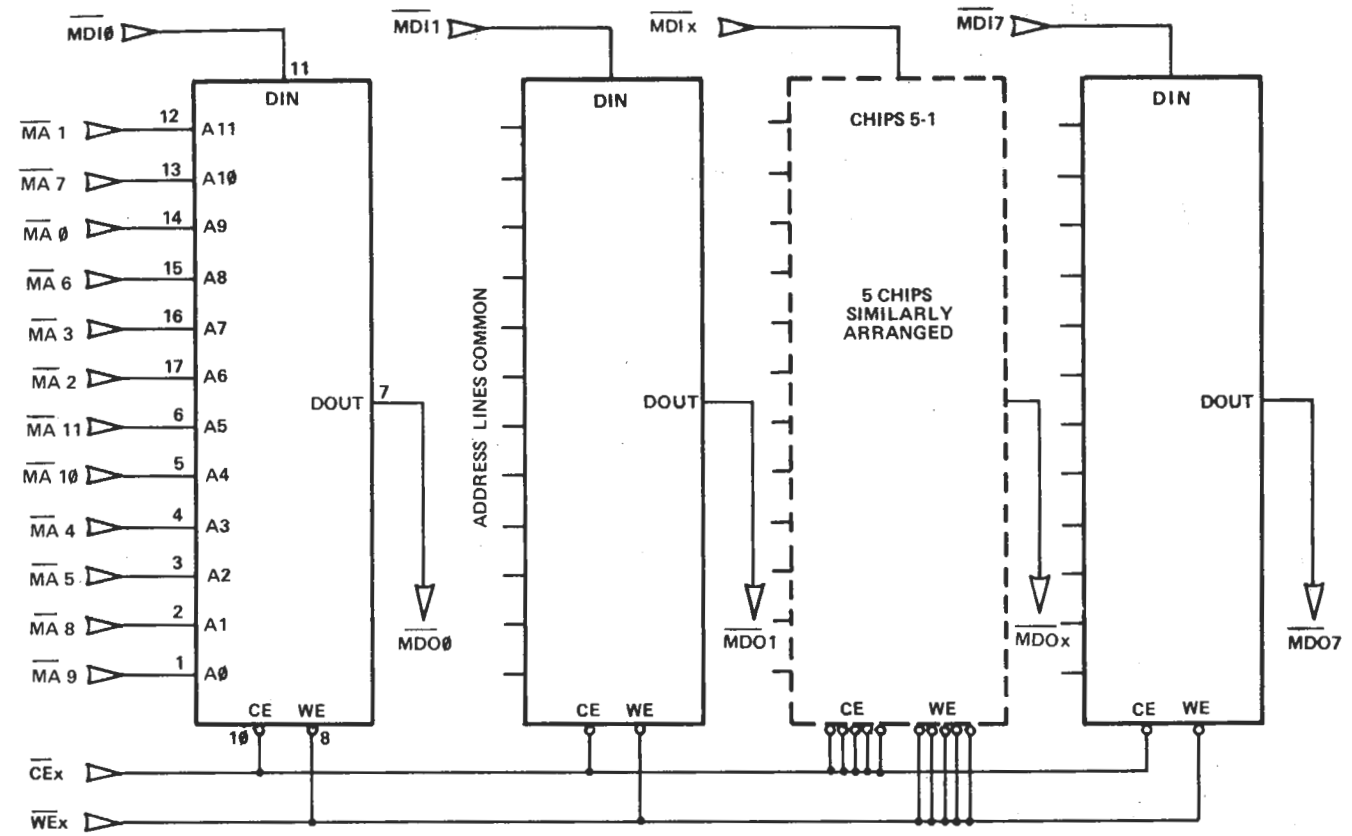
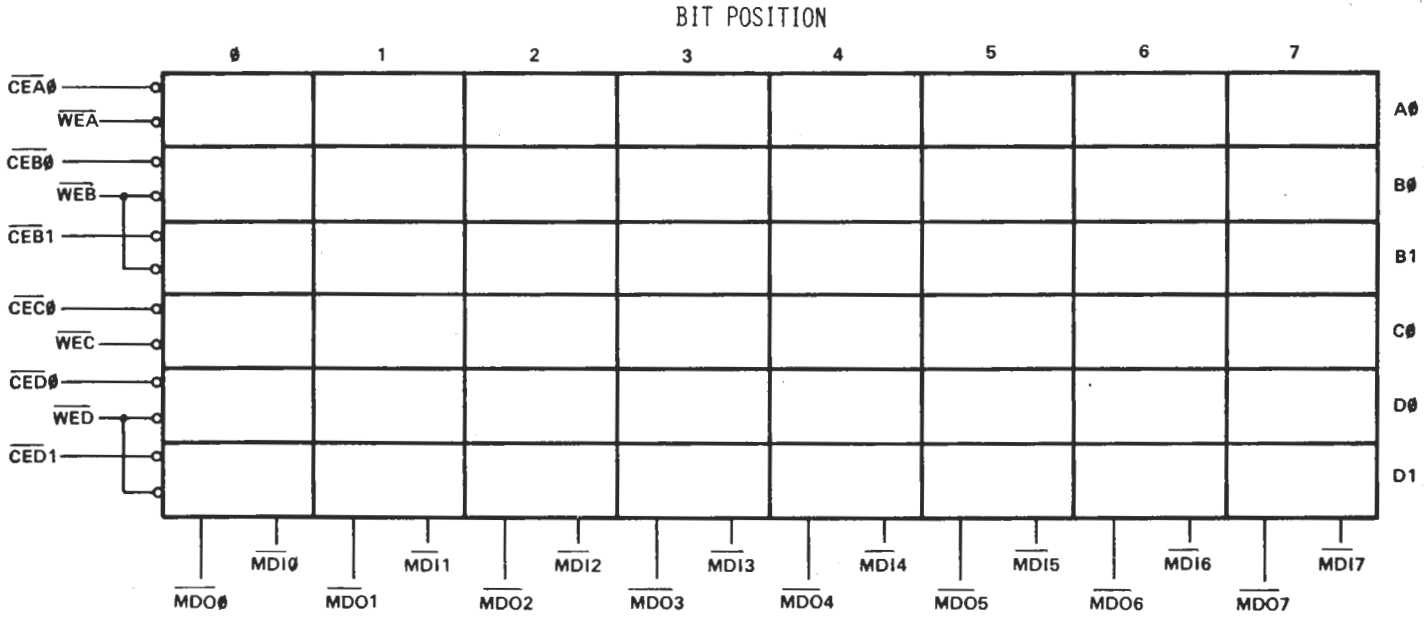
C2
C3
C4
C5
C6
C7
C8
GND


MDI0
MDI1
MDIx
MDI7
DIN
DOUT
CHIPS 5-1
5 CHIPS
SIMILARLY
ARRANGED
ADDRESS LINES COMMON
MA 1
MA 7
MA 0
MA 6
MA 3
MA 2
MA 11
MA 10
MA 4
MA 5
MA 8
MA 9
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
CE
WE
MDO0
MDO1
MDOx
MDO7
CEx
WEx


BIT POSITION
CEA0
WEA
CEB0
WEB
CEB1
CEC0
WEC
CED0
WED
CED1
A0
B0
B1
C0
D0
D1
MDI0
MDI1
MDI2
MDI3
MDI4
MDI5
MDI6
MDI7
MDO0
MDO1
MDO2
MDO3
MDO4
MDO5
MDO6
MDO7