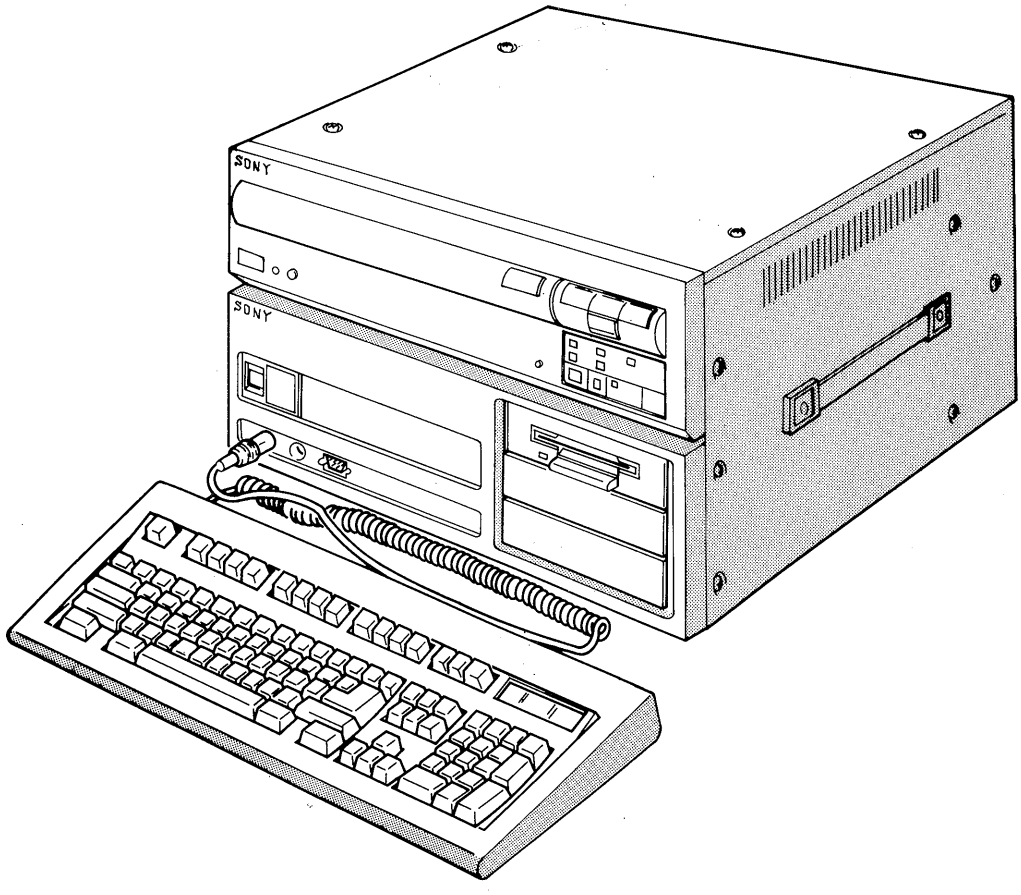
VIW-3015A

SERVICE MANUAL



使用時は添付資料も参照のこと
Refer to the additional documents

Sony VIEW System

SONY®

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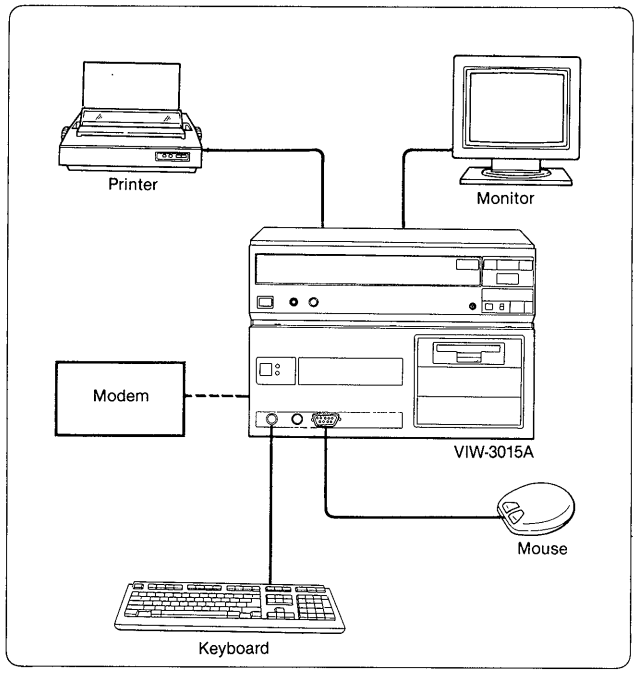
CHAPTER 1
OPERATION

1-1. SYSTEM OUTLINE

1-1-1. Features

The Sony VIEW (Visual Information Enhanced Workstation) system is an advanced video information (including graphic and text) system.
The VIW-3015A consists of a 16-bit microcomputer with a keyboard and a videodisc player.
The computer can control the videodisc player through the commands entered directly from the keyboard or through an operation program from a micro floppydisk.
Some peripheral devices which facilitate operation are optionally available.



*The Sony CPD-1303A/1302A Trinitron character display is recommended.

Two media system

This system employs a micro floppydisk for storage of the system program and application software and a videodisc for video information. The computer with the system program and an application software loaded can control the entire system. The procedure for playback of a videodisc is totally managed by the program loaded.

16-bit microprocessor as the center of the system

The computer employs the Intel 80286 as its CPU. The 80286 is a highly integrated 16-bit microprocessor which is compatible with the Intel 8086. The 80286 provides two modes: the real address mode and the protected mode. The real address mode (8086 mode) operates in the 1M byte real address area. The protected mode provides a 1G-byte virtual address area which includes a 16M-byte real address area.
The IBM AT BUS offers the following two features: (1) a de facto standard, and (2) a compatibility with most commercially available circuit boards.

IBM Video Graphics Array (VGA) compatible

Using the internal high scan superimposer board, the computer supports all color display modes that are employed in VGA Personal System/2. In addition, Expanded color display mode (640.480 dots, 256 colors) is also readily available.

Superimposition of computer images over videodisc images

The system includes a circuit which superimposes graphics or characters generated by the computer over video images reproduced by the videodisc player. This function also allows selection of the superimposed image, the computer generated image and the video image for display on the monitor screen, thus providing a variety of displays.
Digital superimposer system creates sharp graphics images with no switching noise. Transparent color specification has two types: the single color or the multi color (up to 256 colors).

Large memory for user programs

The 80286 processes 16M bytes of memory area and the computer has 640K bytes of RAM as its standard main memory. With the built-in 3.5 inch micro floppydisk drive unit, a large volume of data can be stored as each floppydisk can hold 1.4M bytes of data.

A variety of built-in I/O interfaces

The computer is equipped with various built-in connectors and interfaces: for pointing devices, for RS-232C interfaces, for the printer and so forth. One optional micro floppydisk or two optional hard disk drive units can be installed in the computer in addition to the built-in 3.5-inch micro floppydisk drive unit for a maximum of three storage devices.

Flexible display system

When you install the SMI-3085 in the VIW-3015A, the computer also supports the high resolution graphics modes that are unique to Sony, in addition to VGA compatible display modes.

1-1-2. System Expansion

Following optional devices are prepared for the VIW-3015A.

Device name	Application
Floppydisk drive unit SMI-3014 (capacity: 1.4M bytes formatted)	One 3.5 inch micro floppydisk drive which incorporates a disk controller, is already installed in the computer. The SMI-3014 provides additional storage capacity. It can be conveniently mounted inside the computer.
Internal hard disk drive unit SMI-3018	The SMI-3018 internal hard disk drive, controlled by the SMI-3034, can be installed in the computer. This unit provides additional storage capacity and allows a higher rate of data access. It can be conveniently mounted inside the computer.
Hard disk controller board SMI-3034	This unit controls the SMI-3018 and other 5.25-inch hard disk drives for the IBM PC/AT.
IEEE-488 board SMI-3032	This unit consists of the IEEE-488 interface bus unit. The IEEE-488 interface bus controls the high-level automatic measurement systems.
Dual RS-232C board SMI-3031	This unit adds two RS-232C ports, which operate in the asynchronous mode.
SFA/Digital data decorder board SMI-3080	This unit decodes SFA (Still Frame Audio) and digital data recorded in the videodiscs.
High resolution graphics superimposer SMI-3085	This board kit enables the high resolution graphics display unique to Sony.

Device name	Application
Trinitron character display CPD-1302A/1303A	For display of the information from the computer and the videodisc player.
Printer for IBM PCs	For program listing and printing out of processing results.
Mouse SMI-3062	For quick and easy control of a cursor.
IEEE-488 interface cable SMK-0032 Short IEEE-488 cable SMF-0033	For connection between the IEEE-488 board and various peripheral devices.
RS-232C cable SMF-3031	For connection between the Dual RS-232C board and various devices.
Monitor cable CTG-PSII	For connection between the computer and the Trinitron character display.
Printer cable SMF-2120	For connection between the computer and a printer.

1-2. WARNING

To prevent fire or shock hazard, do not expose the unit to rain or moisture.

To avoid electrical shock, do not open the cabinet. Refer servicing to qualified personnel only.

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

The shielded interface cable recommended in this manual must be used with this equipment in order to comply with the limits for a computing device pursuant to Subpart J of Part 15 of FCC rules.

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IBM is a registered trademark of International Business Machine Corporation.
IBM PC/AT is a trademark of IBM Corporation.
VGA is a trademark of IBM Corporation.

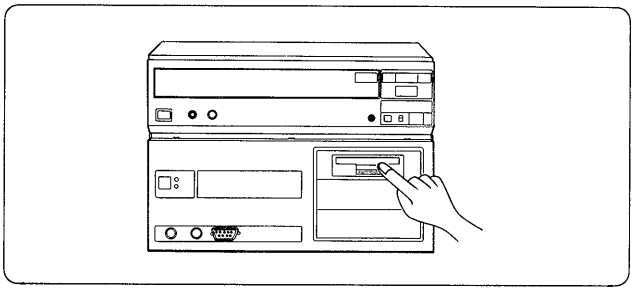
The export of this product is subject to the authorization of the government of the exporting country.

1-3. BEFORE OPERATION

1-3-1. Preparation

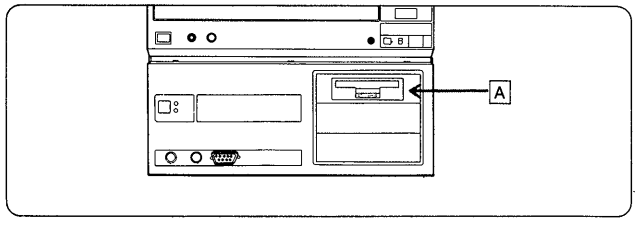
After unpacking the computer, remove the inserted drive protector and affix the drive label using the following procedures, before connection and operation.

Removing the drive protectors



Note: Store the removed drive protector in a safe place, since you may need it when moving the computer.

Affixing the drive labels



Setting up the computer using the Maintenance and Utility Disk

The computer must be set up using the provided Maintenance and Utility Disk when it is used for the first time after purchase or when the system configuration is changed, such as after installing optional devices like SMI-3018 internal hard disk drive unit. Please refer to Chapter 1-5 "SOFTWARE INFORMATION" for details.

1-3-2. Precautions

On safety

- The unit operates on 120 V AC, 50/60 Hz.
- Should any solid object or liquid fall into the cabinet, unplug the unit and have it checked by qualified personnel before operating it any further.
- Unplug the unit from the wall outlet if it is not to be used for an extended period of time.
- To disconnect the cord, pull it out by the plug. Never pull the cord itself.

On installation

- The computer consists of high-precision electronic parts. Do not drop it or bump it against other objects. Do not place it in a location subject to vibration or on an unstable base.
- Do not install the unit near a heat source such as a radiator or an air duct, or in a place subject to direct sunlight, excessive dust, and/or moisture.
- Do not place electronic equipment near the computer or the floppydisk unit. They may malfunction if affected by an electromagnetic field. The floppydisk unit is especially sensitive because it uses weak magnetic signals; never place electronic equipment, such as a TV set, near it.
- Provide adequate air circulation to prevent internal heat build-up. Do not place the unit on surfaces (rugs, blankets) or near materials (curtains, draperies) that may block the ventilation slots.
- Use only the specified peripheral equipment; otherwise, trouble may result. Before connecting peripheral equipment, be sure to turn the power off or the internal IC chip may be damaged.

On cleaning

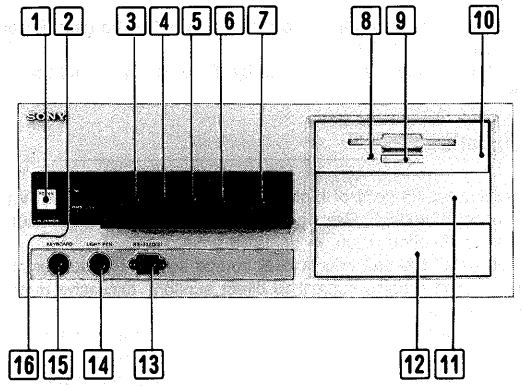
- Clean the cabinet and keyboard with a soft, dry cloth, or a soft cloth lightly moistened with a mild detergent solution. Do not use any type of solvent, such as alcohol or benzine, which might damage the finish.

If trouble occurs, unplug the unit, and contact an authorized Sony representative.

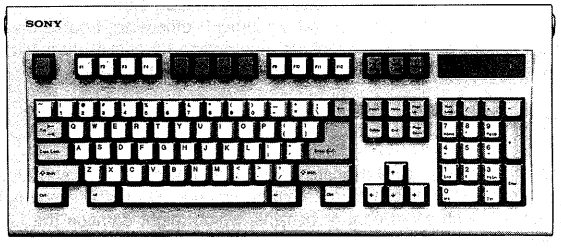
1-3-3. Location and Function of Parts and Controls

As for the videodisc player, refer to the LDP-1500 Service Manual.

Front Panel



Keyboard



1 POWER switch
Press this switch to turn on the computer. To stand by, press the switch again. This switch is active only when the main POWER switch on the rear panel is kept on.

2 POWER ON indicator
While the computer's power is on, this indicator lights.

3 VOLUME (sound volume) control[1)]
This control adjusts the volume from the built-in speaker. When you use the SMI-3085, this control also adjusts the volume from the speaker of the monitor.

4 COLOR control[1)]
When you use the SMI-3085, this control adjusts the color intensity of the external video picture during superimpose operation. Clockwise rotation makes the picture more vivid; counterclockwise rotation makes it paler.

5 HUE control[1)]
When you use the SMI-3085, this control adjusts the hue of the external video picture during superimpose operation. Clockwise rotation makes the color tones more greenish; counterclockwise rotation makes them more purplish. Adjust to the most natural skin tones.

6 STARTING DEV (starting device) selector[1)]
This switch is used to select one of the following devices for loading the software:
FD - AUTO: Micro floppydisk
HD : Hard disk
* : This position is invalid.

7 RESET button[1)]
Press this button if there is a program overrun in order to reset the computer to the initial state and start the diagnostics.

8 In-use indicator
When a micro floppydisk drive reads or writes data, this indicator lights. Do not press the eject button while this indicator is lit.

9 Eject button
Press this button to remove a floppydisk.

10 Micro floppydisk drive A
The floppydisk drive for a 3.5-inch micro floppydisk. Affix the provided label A on the disk drive.

11 Space for optional micro floppydisk drive B or optional hard disk drive
Remove this panel to install either one optional micro floppydisk or one optional internal hard disk drive unit in this space.

12 Space for optional hard disk drive
Remove this panel to install an optional internal hard disk drive unit in this space.

13 RS-232C(2) connector
Connect a pointing device such as SMI-3062 mouse and other RS-232C devices. This port is accessed as "COM2".

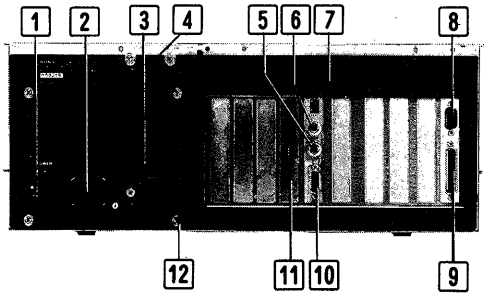
14 LIGHT PEN jack (5-pin DIN jack)
Connect SMI-3061 light pen to this connector to provide input from the display screen.
A light pen can be used only when the SMI-3085 is installed.

15 KEYBOARD jack (5-pin DIN jack)
Connect a supplied keyboard to this connector.

16 HARD DISK indicator
When a hard disk unit is installed in the computer and when a hard disk drive reads or writes data, this indicator lights.

1) The controls numbered from 3 to 7 are behind the cover. To open the cover, press it.

Rear Panel



(1) MAIN POWER switch
The main switch to turn on and off the computer. When the computer is not used for a long period of time, turn off this switch.

(2) AC IN (inlet) connector
The supplied AC power cord, whose other connector is connected to a wall outlet, is connected here.

(3) AC OUT (outlet) connector
Connect to the videodisc player AC inlet.
This outlet supplies AC power to other equipment whose power consumption is no more than 2.3 A. Power is supplied to the connected equipment if the main POWER switch of the rear panel and the POWER switch of the front panel is turned on.

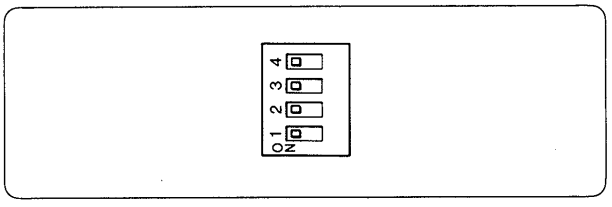
(4) DISPLAY BOARD switch
This switch selects the board for the display of computer characters and graphics. This switch can be set only while the power is off.

- **A:** (Default position) All slots are active. Do not set in this position when the SMI-3085 is installed.
- **B:** The output from the MONITOR connector (10) is disabled and the output from the SMI-3085 when it is installed is enabled.
- **C:** The output from the SMI-3085 when it is installed is disabled and the output from the MONITOR connector (10) is enabled.

(5) AV OUT connector (AV jack)
This connector outputs unprocessed audio and video signals from the AV IN connector (6).

(6) AV IN connector (AV jack)
This connector accepts audio (R, L) and video signals from a videodisc player or the SMI-3080 SFA/Digital Data Decoder Board.

(7) DIP switch
Set switches 3, 4 according to your system needs. Switches 1, 2 must be set ON (default).
Set switch 3 to the position which provides your monitor with the preferable HUE.
Set switch 4 ON to terminate input video signals at 75Ω. Or set OFF to output signals from the AV OUT connector to other devices such as a monitor.



(8) RS-232C(1) connector (9-pin connector)
The asynchronous communication connector. Connect such devices as modems. This port is accessed as "COM1".

(9) PRINTER connector (25-pin connector)
Connect a printer of the standard 8-bit parallel data transfer type (Centronics).

(10) MONITOR connector (15-pin connector)
This connector supplies the display output to a monitor, such as the CPD-1302A/1303A.

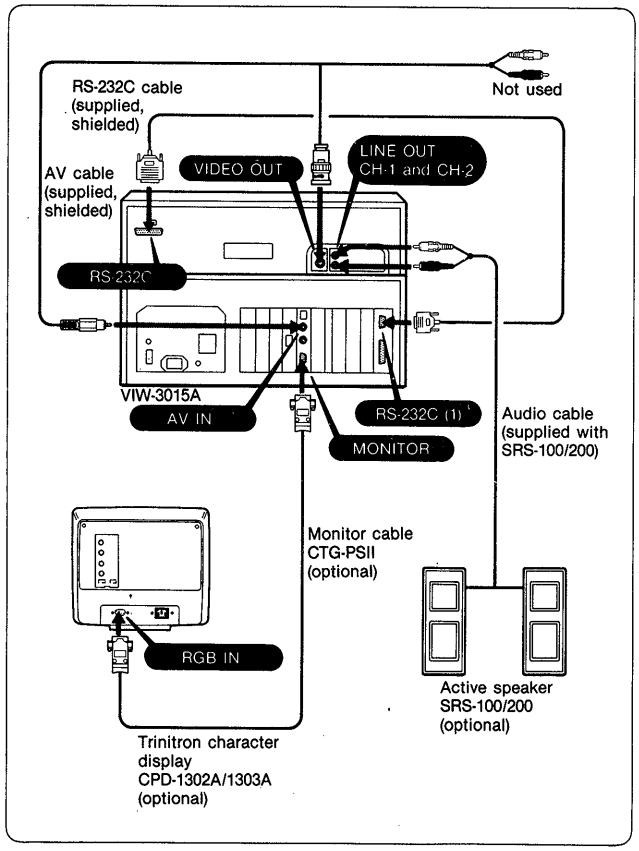
(11) DIP switch
Keep all switches in the default positions.
(Switches 1 to 3: OFF, Switch 4: ON)

(12) Ground terminal
To reduce hum, connect this terminal to an earth ground with a ground wire.

1-3-4. System Connection

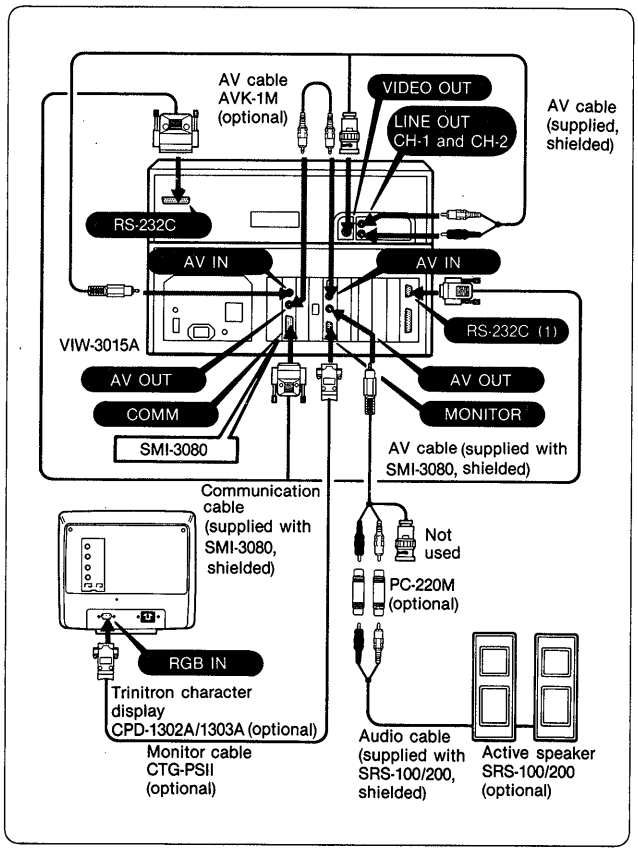
- Before connection, make sure that the power of the microcomputer and the videodisc player is turned off.
- To assure the connection, insert the connectors firmly.

Basic connection



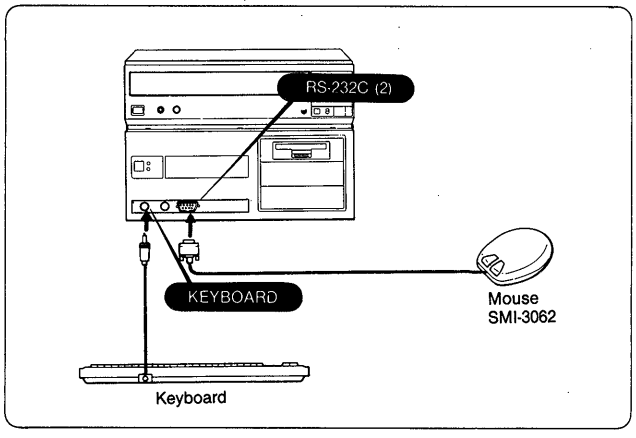
When your system uses the CPD-1302A, set the RGB input selector on the CPD-1302A to ANALOG.

Connection when the SMI-3080 is installed in the VIW-3015A



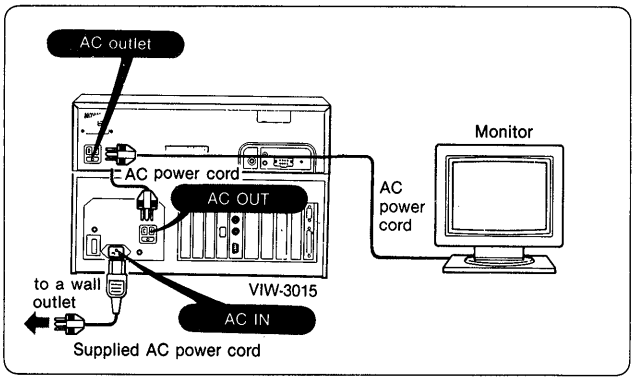
When your system uses the CPD-1302A, set the RGB input selector on the CPD-1302A to ANALOG.

Connection of the Keyboard and Pointing Devices

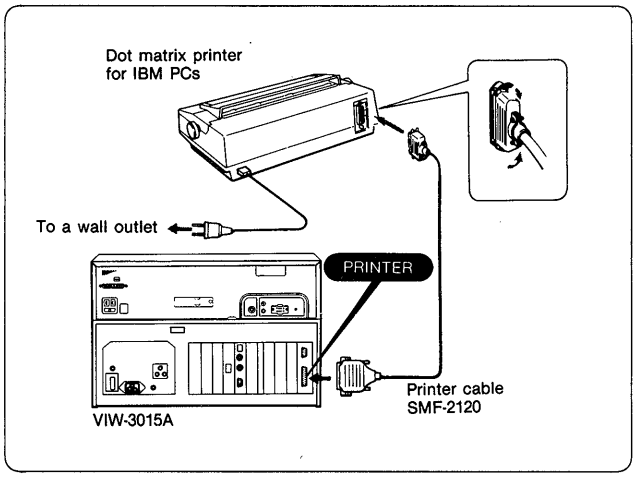


Power connection

Connect the power cords of each component as follows. The power of the system is turned on and off by simply pressing the POWER switch of the micro computer. The POWER switches of the videodisc player and the monitor should be kept in the ON position.



Connecting a Printer



1-4. BASIC OPERATION

1-4-1. Starting Up the System

When you use the system for the first time, the system must be prepared by loading the set-up program from the supplied Maintenance and Utility Disk (see Chapter 1-5 "SOFTWARE INFORMATION").

To start the system, prepare the Sony SMW-3001B MS-DOS 3.20 and load MS-DOS following procedures shown below.
When you use MS-DOS for the first time after purchase, create a backup copy of the MS-DOS system disk (see MS-DOS User's Guide for details).

To load MS-DOS

Load MS-DOS using the following procedures when the MS-DOS system disk is not inserted in the floppydisk drive. Omit Step 4 when the system disk is already inserted in the drive.

1 Turn on the power of the connected components, such as a monitor.

2 Set the STARTING DEV switch on the front panel of the computer to FD-AUTO.

3 Turn on the power of the computer.
This will also turn on the power of the videodisc player and the monitor.

The self-diagnostics program is executed and RAM size will be displayed on the screen as follows:

RAM 00640K bytes

If any error is detected during the self-diagnostics, an error message is displayed. Follow the advice listed on "Self diagnostics program" in such a case. To resume operation, press the F1 key. Then the message will appear.

Insert system disk and press F1 key

Contact an authorized Sony representative, if the above message doesn't appear.

4 Insert the MS-DOS system disk into the floppydisk drive A and press F1 key.

Except for the automatic start program (autoexec.bat) of MS-DOS, the MS-DOS command is awaited.

As for operation after MS-DOS is loaded, refer to the respective manual of the software.

Self-diagnostics Program

When the computer is turned on or reset, the self-diagnostics program is executed. If an error is detected, the error message and code associated to the error condition is displayed. The error code and actions to be taken are listed below.

Error code	Description
03,13,1D	Incorrect system configuration set-up. Set up the correct system configuration using the Maintenance and Utility Disk.
0C	Incorrect main memory size setting. Set up the correct main memory size using the Maintenance and Utility Disk.
1C	Incorrect extended RAM size setting. Set up the correct extended RAM size using the Maintenance and Utility Disk.
0E	Incorrect display board setting. Set up the initial display mode setting using the Maintenance and Utility Disk.
32	Built-in micro floppydisk failure. Turn off the power of VIW-3015A, and then turn it on again. If the error recurs, contact an authorized Sony representative.
33	Built-in micro floppydisk failure. Turn off the power of VIW-3015A, and then turn it on again. If the error recurs, contact an authorized Sony representative. If only one floppydisk drive is installed, cancel the second floppydisk drive setting using the Maintenance and Utility Disk.
34,35	Built-in hard disk drive failure. Turn off the power of VIW-3015A, and then turn it on again. If the error recurs, contact an authorized Sony representative. If no hard disk drive is installed, cancel the hard disk drive setting using the Maintenance and Utility Disk.
01,02,04,05, 0B,0D,11,12, 15,52,0F,31	System failure. Turn off the power of VIW-3015A, and then turn it on again. If the error recurs, contact an authorized Sony representative.
06	Check the connection of the keyboard. If it is connected to the computer properly, turn off VIW-3015A and turn it on again. If the error recurs, contact an authorized Sony representative.
21,22,23,24, 25,26,27,28 29,2A,2B	Check the DIP switch setting on the I/O board referring to page 86. If they are set correctly, contact an authorized Sony representative. These errors occur only when the SMI-3085 high resolution graphics superimposer is installed.
50	Optional ROM is out of order.

If the computer does not operate normally even though error messages and codes are not displayed, detailed diagnostics are required. Please contact an authorized Sony representative when you cannot eliminate an error.

To Start the System Monitor

Load the System Monitor program when you want to modify the display mode or dump the memory contents using the basic commands stored in the system ROM of the computer at the machine language level.

Loading system monitor program

1 Turn on the power of the connected components.

2 Turn on the power of the computer.
The following message is displayed:

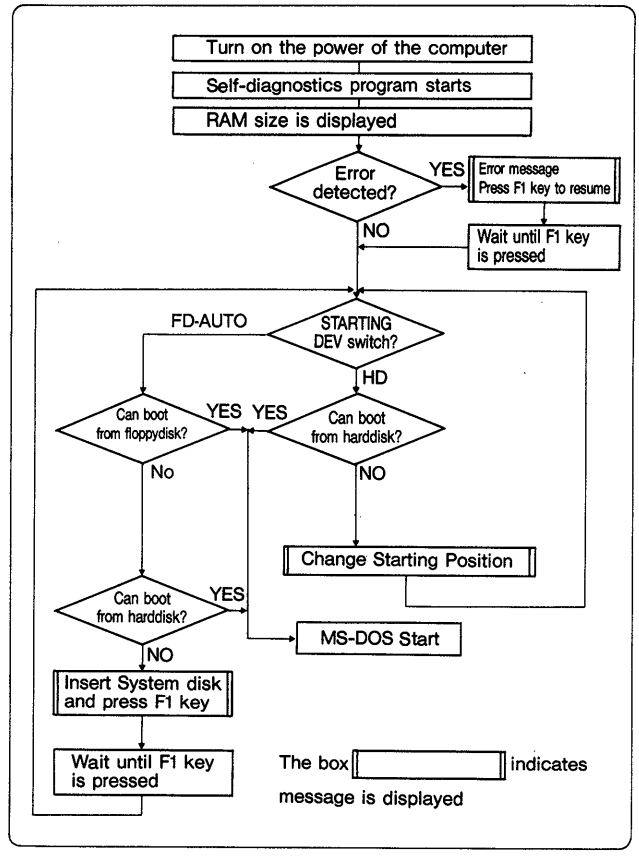
```
RAM XXXXXX bytes
```

3 Press [Esc] key until the following message appears.

```
ROM Version Number
  SONY: System ROM1 (F000) = * * * *
        System ROM2 (E000) = * * * *
System Monitor Program
Copyright Sony Corp. 1988
0000>
```

Now, you can execute an operation such as a memory dump using the system monitor commands. Please refer to the optional SML-3001 Hardware and BIOS Manual for details on System Monitor.

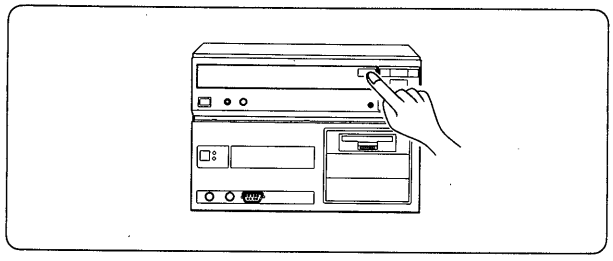
Operational Flowchart



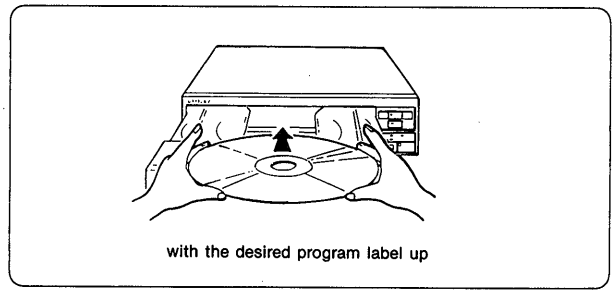
1-4-2. To Use a Videodisc

When using a videodisc, insert it as follows:

1 Press the OPEN/CLOSE button on the videodisc player to open the disc compartment.



2 Place the video disc on the table.



with the desired program label up

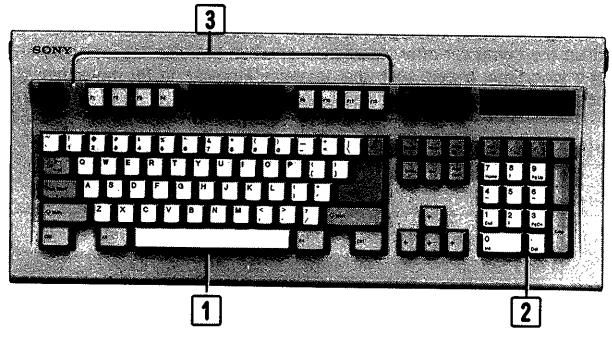
3 Press the OPEN/CLOSE button again. The compartment closes, and the STANDBY indicator lights.

To remove the disc

Press the OPEN/CLOSE button to stop the playing of the disc, no matter what mode the player is in. The disc will stop rotating, and the disc compartment will be ejected.

1-4-3. Keyboard Operation

Keyboard Arrangement



(1) Main keyboard
Alphanumeric characters are arranged in the standard typewriter keyboard layout.
The keyboard has character input keys (such as A to Z, 0 to 9, +, ?, <, >) which are displayed as they are entered, and control keys (such as Ctrl, Esc) which perform a certain task when they are pressed.

(2) Ten-key
The ten-key consists of numeric keys (0 to 9), arithmetic symbols (+, -, •, *, /), and ENTER key (↵). Numeric keys are arranged in the standard calculator layout.

(3) Function keys
The keyboard has 12 function keys, from F1 to F12. The function of these keys are defined by the software. Therefore, their functions vary depending on the software used. Please refer to the respective software manual for details.

Key Functions

This section describes the functions of the control keys defined by the BIOS of the computer. Other key functions vary depending on the MS-DOS and application programs. Please refer to each software manual for details on them.

Ctrl
control key
When this key is pressed together with another character key, a control code is generated. Because the valid control codes and their function depend on the software used, see the manual of the software for detailed information on the control codes.

⇧
Shift key
When this key is pressed together with a character input key, the corresponding symbol in the shift position (upper symbol on the key) or the corresponding capital letter (of the letter on the key) is entered.

Alt
alternate key
When this key is pressed together with the number key, the ASCII code of the key pressed can be entered as a decimal value.
Example: Alt + 6 5 → A (41H = 65)

Caps Lock
capital lock key
When this key is pressed, the indicator lights and all letters are entered in capitals. The small letter is entered when the Shift key is pressed after pressing this key. When the key is pressed again, it will unlock. This key will not affect any special characters and numeric keys.

↵
Enter key
Press this key to indicate the end of the input of a line of data or commands from the keyboard. Press this key every time you finish entering a line. The cursor moves to the next line, and the entry of the next data or command is awaited.

←
back space key
When this key is pressed, the cursor is moved one space to the left and the character in that position is deleted.

Print Screen
When this key is pressed, the display on the screen will be printed out.

Ctrl + Alt + Delete
When the Ctrl, Alt, and Delete keys are pressed simultaneously, the computer system is reset.

1-5. SOFTWARE INFORMATION

1-5-1. Associated Software and Manual

The VIEW system which incorporates the High Scan Superimposer Board (Consists the superimposer board and the VGA board) is called the "VIEW/VGA system". The VIW-3015A is the VIEW/VGA system. The following is a list of software available for the control of VIEW/VGA system or the development of applications. These have a compatible software interface with IBM InfoWindow.

- SMW-3001B MS-DOS Version 3.20
  Operating system designed for use with Sony VIEW system.

- SMW-3060 VIEW/VGA Control Program
  A driver which controls the VIEW/VGA system.

- SMW-3061 VIEW/VGA Software Development Kit
  Software utilities, library and manual for the development of VIEW/VGA applications.

- Maintenance and Utility Disk (Supplied with the VIW-3015A)
  This disk contains the following software

Maintenance program[1]:	Set up program, Diagnostics test program
Superimpose driver:	INT10EX.SYS, INT10EX.COM
MS-DOS utility:	VMODE.COM, LDPSUP.EXE
Microsoft Windows utility:	VGASUPER.EXE
Microsoft Windows driver:	PVGA256.DRV, PVGA256.LGO, PVGA256.GRB, WINDOWS.TXT

  Install the Microsoft Windows driver when using the display mode 5F. See the WINDOWS. TXT file for details on installation.

- SML-3001 Hardware and BIOS Manual
  This manual provides technical information on the computer for a system programmer. Primarily, Interrupt and ROM BIOS call are described.

Note:
The explanation of the display on the SML-3001 is for the optional SMI-3085 High Resolution Graphics Superimposer. As for the explanation of the display in the VIEW/VGA system, refer to "Superimpose Driver BIOS Specifications" in this manual and/or the manual of SMW-3061.

1) The maintenance program is a "hidden" file. So when you execute the DIR command of MS-DOS, the file name will not be displayed.

1-5-2. How to Use Maintenance and Utility Disk

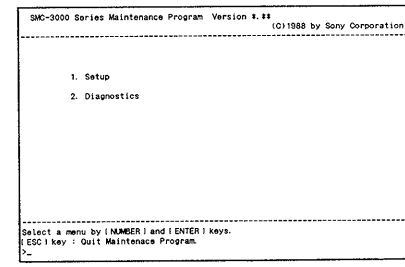
To execute the Set-up program or the Diagnostics test program, load the Maintenance program as follows.
To execute another program, load MS-DOS using the MS-DOS system disk and execute the desired program.

1 Insert the Maintenance and Utility Disk into floppydisk drive A.

2 Set the STARTING DEV switch on the front panel of the computer to FD-AUTO.

3 Turn on the connected devices and then turn on the computer.

The self-diagnostics program (see page 1-8 "Self-diagnostics Program") is executed. If no error is detected, the program in the Maintenance and Utility Disk is loaded and the following selection screen is displayed.



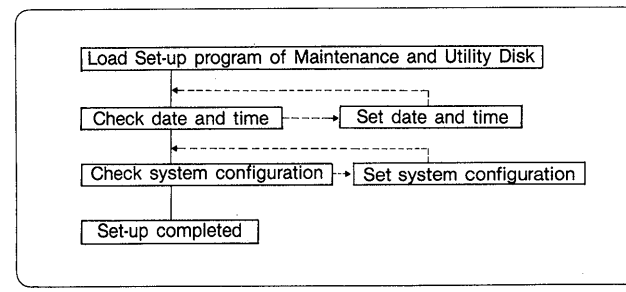
For operation after the Maintenance program is loaded, refer to the sections "Set-up Program" when the system is just installed or modified, and "Diagnostics Test Program" when the diagnostics of the system components is required.

1-5-3. Set-up Program

When the VIW-3015A is used for the first time after purchase, or when the system configuration is changed after installing optional devices such as SMI-3014 floppydisk drive unit, the system must be set-up using the supplied Maiantenance and Utility Disk. Otherwise, every time when the power is turned on, the self-diagnostics program may display error messages. The following illustration shows the flow of the setting up operations.

Note:
This computer incorporates a rechargeable battery which provides power to the RAM used for storing the set-up program data. When you first start up the computer after installation or when you use the computer after a long time, please keep the computer's power on for more than eight hours to charge the back-up battery.

Setting up procedures



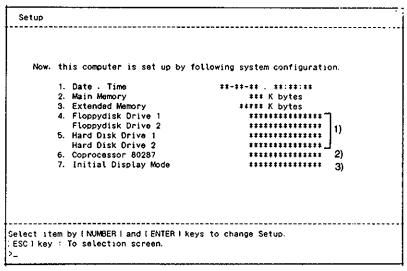
Set-up Operation

Set-up the computer as follows:

1 Load the Maintenance and Utility Disk in accordance with the procedures in the section "How to Use Maintenance and Utility Disk".

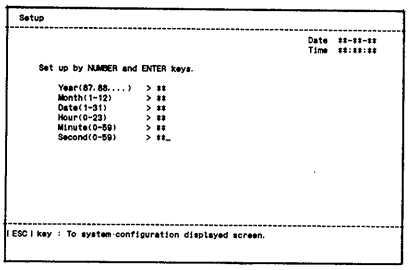
2 Enter "1" at selection screen and press Enter.

The following set-up menu is displayed.



Note 1): The connected disk drive type or "Not Installed" is indicated.
Note 2): "Installed" or "Not Installed" is indicated.
Note 3): "Sony Mode (BWC2)" or "COC2" is indicated.

3 Enter "1" and press Enter *.
The following date and time setting screen is displayed. Enter the current year at the year prompt using numeric keys and press Enter. In the same manner, enter month, date, hour, minute, and second.



4 Press Esc key.
The set-up menu (see step 2) will reappear.

5 The item numbers (2) to (7) of the set-up menu indicate the current system configuration.
Confirm the indicated value of each item.

- The main memory size (2) will be indicated as 512K bytes for the SMC-2000 mode and 640K bytes for the SMC-3000 mode.
- The extended memory size (3) and whether or not the co-processor 80287 is installed (6) is detected by the software and indicated in accordance with the results.
- The type of floppydisk drive (4) and hard disk drive (5) are indicated in accordance with the current set-up. However, the indications may differ from the existing configuration. If so, set the type correctly.
- You can select the initial display mode (7) from two modes: Sony Mode (BWC2) or COC2.

6 You can reset item (7) (Initial Display Mode) as required. To reset, enter "7" and press Enter to specify the desired mode. Press Esc to return to the set-up menu.

Note:
When you use a VGA board as display board, set to Sony Mode (BWC2).

7 Press Esc to end the set-up program.
The selection screen will reappear.

When the set-up operation is completed

To perform the diagnostics test:
Enter "2" at the selection screen (see step 1) and press Enter. See the following sections for details on the diagnostics test.

To load MS-DOS:
Remove the Maintenance and Utility Disk from drive A:, insert the MS-DOS system disk and press Esc key.
MS-DOS will be loaded.

* Press Enter if the current date and time need not be changed. The cursor moves to the next setting item.

1-5-4. Diagnostics Test Program

The VIW-3015A and the peripheral devices can be diagnosed by the Maintenance and Utility Disk. This diagnostics test program performs a more detailed check of each device than the self-diagnostics program that is automatically executed when the computer is turned on. Moreover, this program formats (physical format of the hard disk drive unit), and performs a read test of storage devices such as a hard disk drive unit.

The diagnostics test covers the following four categories:
1. Printed circuit board
2. Display device
3. External storage device
4. Input/output device (printer, keyboard, mouse)

The diagnostics test programs follow the hierarchical structure shown in the next page.

Note:
The devices indicated with an asterisk on the screen during the diagnostics test program are the optional devices. Therefore, such devices cannot be tested unless they are installed.

Hierarchical structure of the diagnostics test menu

1. Board Diagnostics
   - 1-1. System Board Diagnostics
     - 1-1-1. Once
     - 1-1-2. Multiple Times
   - 1-2. Display Board Diagnostics
     - 1-2-1. Once
     - 1-2-2. Multiple Times
   - 1-3. Hard Disk Controller Board Diagnostics
   - 1-4. Extended RAM Board Diagnostics
     - 1-4-1. Once
     - 1-4-2. Multiple Times
   - 1-5. Starting Device Switch Diagnostics
2. Display Device Diagnostics
   - 2-1. Display Color Diagnostics
   - 2-2. Display Mode Diagnostics
     - 2-2-1. Automatic Mode
     - 2-2-2. Manual Mode
   - 2-3. PCG Diagnostics
   - 2-4. Adjust Screen Position
3. External Storage Device Diagnostics
   - 3-1. Floppydisk Drive Diagnostics
     - 3-1-1. Read
     - 3-1-2. Read/Write
   - 3-2. Hard Disk Drive Diagnostics
     - 3-2-1. Read
     - 3-2-2. Format
   - 3-3. Videodisc Player Diagnostics
4. Input/Output Device Diagnostics
   - 4-1. Printer Diagnostics
   - 4-2. Keyboard Diagnostics
   - 4-3. Mouse Diagnostics
     - 4-3-1. Using RS-232C(1)
     - 4-3-2. Using RS-232C(2)
     - 4-3-3. Using RS-232C(3)
     - 4-3-4. Using RS-232C(4)

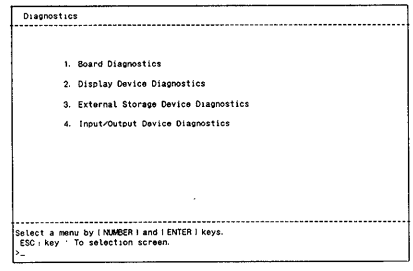
Diagnostics Test Operation

To display the diagnostics test menu

1 Load the Maintenance program in accordance with the procedures in the section "How to Use the Maintenance and Utility Disk".

2 Enter "2" (2. Diagnostics) at selection screen and press Enter.

The following main menu is displayed.



3 Enter the item number and press Enter.
The specified diagnostics test menu will be displayed.
Refer to the following sections for details on each item.

Board Diagnostics

The diagnostics performed for the printed circuit board are as follows:

System board diagnostics
Tests the following items.
- CPU 80286
- Co-processor 80287
- Timer, Interrupt Controller
- Printer Interface
- RS-232C Chip
- Address Gate A20
- Shutdown Function
- Main Memory
- PSG, Beep (sound)

Display board diagnostics
Tests the following items.
- Video RAM
- Color Register
- Palette RAM
- Transparent Color
- DIP Switches
- I/O Addresses

Note:
- Disconnect the equipment from the RS-232C connectors before you perform the system board diagnostics.
- During the display board diagnostics, the screen flickers. However, this is not a system malfunction; it occurs because of the test.

Hard disk controller board diagnostics
Tests the hard disk controller.

Extended RAM board diagnostics
The extended RAM board is not provided by Sony Corporation. When you install a commercially available extended RAM board, perform the read and write test of the board using this program. When the test is completed successfully, the extended RAM size is indicated.

Starting device switch diagnostics
Tests the starting device setting (FD-AUTO, HD, *).

Operation

Enter "1" (1. Board Diagnostics) at the main menu and press [Enter].
The following screen appears.
Perform the diagnostics test as follows.

```
1. Board Diagnostics

      1-1. System Board Diagnostics
        2. Display Board Diagnostics
  *     3. Hard Disk Controller Board Diagnostics
  *     4. Extended RAM Board Diagnostics
        5. Starting Device Switch Diagnostics

  * : Option

Select a menu by [ NUMBER ] and [ ENTER ] keys.
[ ESC ] key : To main menu.
>_
```

1 Enter the sub-digit of the menu item and press [Enter]. For example, enter "1" to test the system board, and then press [Enter].

The following screen appears, asking you whether the test should be performed once or repeatedly.

```
1-1. System Board Diagnostics

      1-1-1. Once Diagnostics
        2. Multiple Times Diagnostics

      Note.  Be sure no device is installed to RS-232C connectors.

Select a menu by [ NUMBER ] and [ ENTER ] keys.
[ ESC ] key : To menu of 1.
>_
```

The multiple times diagnostics has 10-second intervals between each test. When the "C" key is pressed during the interval, the next test starts immediately regardless of the elapsed time from the previous test.
To stop the diagnostics test, press [Esc] key.

2 Enter "1" to test once or "2" to repeat test, and press [Enter].

Example:

```
1-1-1. System Board Diagnostics (Once)

CPU 80286          : Operation ..... OK
                     Clock Frequence ..... OK 8MHz
NPX 80287          : Operation ..... OK
                     Clock Frequence ..... OK 6MHz
                     Correspond to
                     Exception Error ..... OK
TIMER              : Period ..... OK
                     Interrupt Controller .. OK ** times
Printer Interface  : ..... OK
RS-232C Chip       : RS-232C(1) ..... NG
                     RS-232C(2) ..... OK
Address Gate A20   : ..... NG
Shutdown Function  : ..... OK
Main Memory        : ..... OK *** K bytes
PSG.BEEP           : ..... END

[ ESC ] key : To menu of 1-1.
>_
```

The diagnostics test starts while displaying the test items.
When the test is completed successfully, "OK" is displayed. If an error is detected, "NG" is displayed.
Neither "OK" nor "NG" is displayed for the PSG, or bell sound. Confirm the result by the sound.

3 Press [Esc] to return to the menu 1-1 screen.

Press [Esc] to return to the previous higher menu level in the hierarchy structure. For example, if [Esc] is pressed at the menu 1-1, the menu 1 (1. Board Diagnostics) reappears.

Display Device Diagnostics

The diagnostics tests performed for the display device are as follows:

Display color diagnostics
The color bar with the sixteen available colors is displayed.

Display mode diagnostics
In the Automatic mode, the screen is displayed one by one.
In the Manual mode, test the display mode according to screen instructions using the following keys.

[N]/[P] keys:	Next/Previous screen
[G] key:	Sets Genlock mode (automatic or internal)
[S] key:	Sets superimposing mode (computer graphics only, superimpose, or video image only)
[T] key:	Sets transparent color mode (single transparent color or multiple transparent color)
[↑][↓][←][→] and [Enter] keys:	Select a color palette using the cursor keys, and press [Enter] to set/remove it as the transparent color. Pressing the [Enter] key acts as a toggle switch to turn on/off the transparent color.
[Esc] key:	Ends the test.

PCG diagnostics
Every time [Enter] key is pressed the PCG page 0 and 1 is displayed alternately.

Adjust screen position
Adjust screen position for each display mode.
This operation is carried out when modifying the relative location between the computer graphics and video images.

Operation

Enter "2" (2. Display Device Diagnostics) at the main menu and press [Enter].
The following menu appears.
Perform the diagnostics test as follows.

```
2. Display Device Diagnostics

      2-1. Display Color Diagnostics
        2. Display Mode Diagnostics
        3. PCG Diagnostics
        4. Adjust Screen Position

Select a menu by [ NUMBER ] and [ ENTER ] keys.
[ ESC ] key : To main menu.
>_
```

Enter the sub-digit of the menu item and press [Enter].
For example, enter "4" to perform the "2-4. Adjust Screen Position", and press [Enter].

The following submenu is displayed.

```
2-4. Adjust Screen Position

      2-4-1. Load display parameters
        2. Adjust screen position
        3. Save display parameters
        4. End. Return to menu of 2.

Select a menu by [ NUMBER ] and [ ENTER ] keys.
>_
```

Loading parameters from a file

You can replace the current display parameters with those saved in a parameter file. (Refer also to "Saving parameters in a file" for details on creating a parameter file.)

1 Enter "1" (Load display parameters) and press [Enter].

2 Specify the parameter file name and press [Enter].

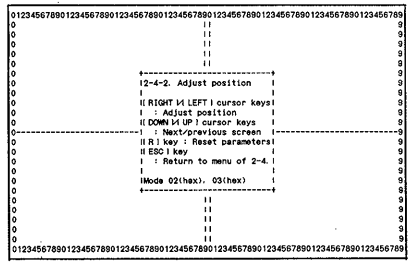
3 When loading is completed, press [Esc] and return to the submenu.

Specifying a new screen position

1 Select "2" (Adjust screen position) and press [Enter].

2 Adjust the screen position using the right/left cursor keys. Pressing [R] resets the screen position of the currently selected display mode to the default setting. This does not affect settings of the other display modes.

3 When the desired screen position is set, press the up/down cursor keys to change the display mode and repeat the step 2.



4 When the screen positions of all display modes are set, press [Esc] to return to the submenu.

Saving parameters in a file

1 You can save the display parameters in a file for later use. Select "3" (Save display parameter) to save the parameters in a file.

2 The system prompts you to enter a file name. Enter the desired file name to store the parameters. (Keep the file name within 8 character-long without specifying any file attribute. The system automatically attaches a ".DPF" attribute to the file name.)

3 Press [Esc] and return to the submenu.

Notes:
- Refer to "Loading parameters from a file" for procedures of loading the saved parameters in the diagnostic program.
- The parameter file can be loaded also when activating the Superimpose Driver from MS-DOS.

Example:
Loading a display parameter file called "USER.DPF" to adjust screen positions.

A>INT10EX USER

To return to the menu 2

Enter "4" in the submenu. The screen returns to the menu 2.

External Storage Device Diagnostics

The diagnostics tests performed for the external storage device are as follows:

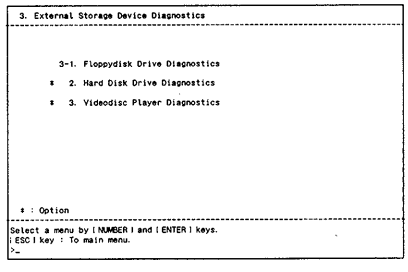
Floppydisk drive diagnostics
Performs the Read test and Read/Write test.
When Read/Write test is selected, it also performs the physical formatting the disk. Consequently, all data on the disk is erased. Therefore, it is recommended that you make a copy of the data on another disk before executing this program.

Hard disk drive diagnostics
Performs the Read test and physical formatting the hard disk. When the formatting is performed, all data written on the disk is erased. Therefore, it is recommended that you make a copy of the data on a floppydisk before executing this program. When the formatting is also performed, the Read/Write test is performed automatically.

Videodisc player diagnostics
Tests the performance of the computer for controlling the videodisc player via RS-232C or IEEE-488.

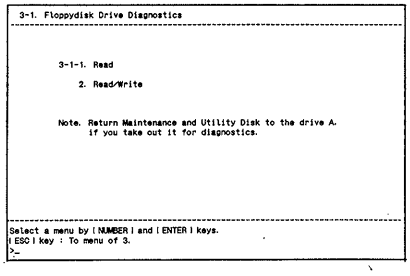
Operation

Enter "3" (3. External Storage Device Diagnostics) at the main menu and press [Enter].
The following menu appears.
Perform the diagnostics test as follows.



1 Enter the sub-digit of the menu item and press [Enter].
For example, enter "1" to test the floppydisk drive, and then press [Enter].

The following screen appears:



2 Enter the item number and press [Enter].
Follow the instructions on the screen for the rest of the operation.

Note:
An error may be detected due to scratches on the floppydisk during the floppydisk drive diagnostics. To be sure, test with another floppydisk.

Input/Output Device Diagnostics

The diagnostics tests performed for the I/O device are as follows:

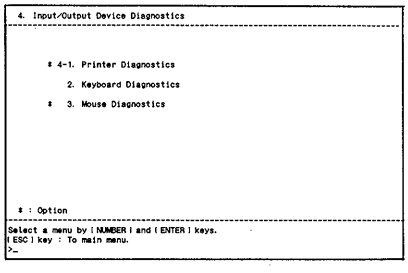
Printer diagnostics
Tests for printing alphanumeric characters.

Keyboard diagnostics
Displays the characters associated to each key on the keyboard. Press a key and see whether the corresponding character is displayed.

Mouse diagnostics
Tests the mouse and RS-232C interface when a mouse is connected to RS-232C connectors (1) to (4) respectively.

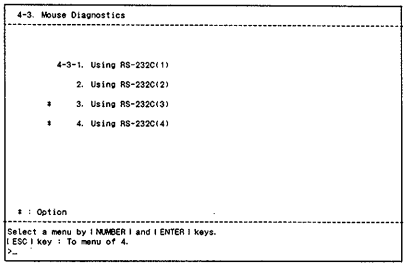
Operation

Enter "4" (4. Input/Output Device Diagnostics) at the main menu and press [Enter].
The following menu appears.
Perform the diagnostics test as follows.



1 Enter the sub-digit of the menu item and press [Enter].
For example, enter "3" to test the mouse (RS-232C interface), and then press [Enter].

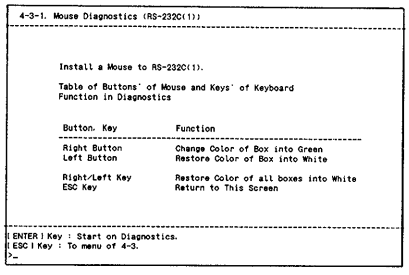
The following screen appears:



Note:
The test item will not be displayed when the "2. Keyboard Diagnostics" is selected. Press a key and see whether the corresponding character is displayed on the screen.

2 Enter the item number and press [Enter].
Follow the instructions on the screen for the rest of the operation.

Example:



Notes:
- Press [Enter] to perform the mouse diagnostics at the above screen.
- During the mouse diagnostics, the color of the box at the cursor position changes when the respective key or button is pressed. The mouse and RS-232C interface are normal when the color changes in accordance with the above screen description.

3 To quit the test, proceed as follows.
The printer diagnostics terminate automatically.
To quit the keyboard diagnostics, press [Esc] key and then press [Enter] key.
To quit the mouse (RS-232C interface) diagnostics, press [Esc] key.

1-5-5. Software Drivers

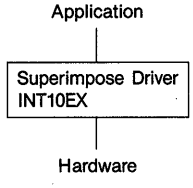
To use the superimpose function, a software driver is needed. The user can select one of the two available drivers—the Superimpose Driver supplied in the Maintenance and Utility Disk and optional SMW-3060 VIEW/VGA Control Program—which best suits individual needs.
The superimpose driver is not needed when using the SMW-3060 VIEW/VGA Control Program.

Superimpose Driver

This driver is provided both as a device driver and a external command, having the same BIOS functions to control the High Scan Superimposer. (See "Superimpose Driver BIOS Specifications" for details.)
Find the following two files in the Maintenance and Utility Disk.

- INT10EX.SYS
- INT10EX.COM

This driver is used to create an original video interactive system.
Refer to "Superimpose Driver BIOS Specifications" for the default display settings implemented by this driver.



How to Install Superimpose Driver

INT10EX.SYS

To install the INT10EX device driver, include this statement in the CONFIG.SYS file.

DEVICE = INT10EX.SYS

When MS-DOS starts up, the driver is automatically loaded in the memory and remains there until the power is turned off.

INT10EX.COM

Start this as an ordinary external command.

A>INT10EX

The driver is loaded in the memory and remains there until the power is turned off.

Notes:
- The INT10EX.COM driver must be executed before other TSR (Terminate and Stay Resident) programs are installed.
- When the Superimpose Driver is installed, display mode is automatically set to the Superimposed VGA 3+ mode.
- Refer to "Superimpose Driver BIOS Specifications" for the driver's default display settings.
- Superimposing is possible only with display modes listed in page 1-22.

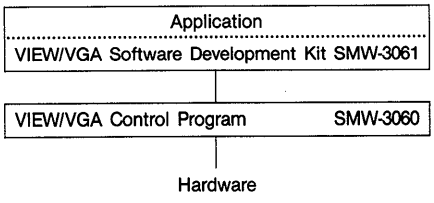
VIEW/VGA Control Program

This driver is included in the optional SMW-3060 VIEW/VGA Control Program. Utilities and library contained in the SMW-3061 VIEW/VGA Software Development Kit assume the use of this driver for running an application developed by the user.

This driver is necessary when running a VIEW/VGA application created for IBM InfoWindow.

Functionally speaking, the VIEW/VGA Control Program includes the Superimpose Driver. For details on the installation, refer to the SMW-3060 manual. Details on the software specification are found in the SMW-3061 VIEW/VGA Software Development Kit manual.

Note:
When the VIEW/VGA System is put in the "active" or "suspend" state by the VIEW/VGA Control Program, utility programs contained in the Maintenance and Utility Disk cannot be executed. Set the VIEW/VGA System in "inactive" state before executing any of the utilities.



1-5-6. Running a Generic VGA Software without Using Superimposing Functions

To run a generic software supporting VGA display mode (written for IBM PS/2 or other computers incorporating a VGA board) without using superimposing functions, it is necessary to use the superimposer's through mode.

Note:
Superimposing of video images input from a videodisc player and computer graphics created by a generic VGA software is possible by using the LDPSUP.EXE. For details, see "Controlling Superimposer and Videodisc Player" on page 1-18.

When INT10EX.SYS is installed

1. Delete the statement "DEVICE = INT10EX.SYS" from the CONFIG.SYS file using an editor.
2. Press RESET button.
   (Or turn off the power of the computer and turn it on.)
3. The system starts up in the Normal VGA 3+ color display mode.
4. If necessary, use VMODE.COM to set the display mode to CGA or EGA (3 or 3*) for specific applications not supporting the VGA display mode. (The VMODE command is included in the Maintenance and Utility Disk. Refer to "Set Display Mode" on page 1-17 for details.)
5. Run the software.

When INT10EX.SYS is not installed

1. Turn on the power to the computer.
   The system starts up in the Normal VGA 3+ color display mode.
2. If necessary, use VMODE.COM to set the display mode to CGA or EGA (3 or 3*) for specific applications not supporting the VGA display mode. (The VMODE command is included in the Maintenance and Utility Disk. Refer to "Set Display Mode" on page 1-17 for details.)
3. Run the software.

Note:
Do not execute neither the Superimpose Driver (INT10EX.COM) nor VIEW/VGA Control Program.

1-5-7. MS-DOS Utilities

Set Display Mode (VMODE.COM)

The VMODE.COM is used to specify display and superimpose settings. It is also used to select the genlock mode (auto or internal), activate/deactivate the mute function, or reset all display settings to default.

The superimpose mode, as well as genlock setting and mute function, are significant only when the Superimpose Driver or VIEW/VGA Control Program is installed.

How to use the VMODE.COM

A>VMODE [<option>[<parameter>]]

- When both <option> and <parameter> are omitted, a list of the available options and parameters are displayed.
- When <option> is specified and <parameter> omitted, the parameter required by the specified option is displayed.
- When <option> is omitted and <parameter> specified, the system assumes DSP (selects a display mode) is specified.

There are six options available for the VMODE.COM.

DSP Selects a display mode (3, 3* or 3+)
SUP Selects a superimpose mode.
GEN Selects a genlock mode.
MUT Activates/deactivates the mute function.
RST Resets all display settings to default.
MOD Selects a display mode. (This option allows selection of a display other than those covered by the DSP option.)

DSP

Syntax VMODE [DSP[:]]<mode>

Function Selects a display mode specified by <mode>. Three display modes are available as follows. (To select a display mode other than these three, use the MOD option.)

C CGA, 3 (hex)
E EGA, 3* (hex)
V VGA, 3+ (hex) (default)

Example VMODE DSP:E
or
VMODE E

Sets the display mode to 3* (hex), EGA.

SUP

Syntax VMODE SUP[:]<superimpose>

Function Selects a superimpose mode specified by <superimpose>. Three superimpose modes are available as follows.

C Computer graphics only (default)
S Superimpose (both computer graphics and video images are displayed)
V Video images only

Example VMODE SUP:S

Sets the superimpose mode to superimpose.

GEN

Syntax VMODE GEN[:]<genlock>

Function Selects a genlock mode either automatic or internal specified by <genlock>.

A Automatic (default)
I Internal

When video signals are unstable in such events as scanning, resultant frequent switching of synchronization may distort the screen image. To avaoid this, set the genlock mode to internal.

Note:
Video images run horizontally when the genlock mode is set to internal.

Example VMODE GEN:I

Sets the genlock mode to internal

MUT

Syntax VMODE MUT[:]<mute>

Function Activates/deactivates the mute function.

Y Mute ON (default)
N Mute OFF

Turn on this function to blackens the screen when switching screen modes using the VGA BIOS call (INT10H, AH = 00H). This function is convenient when screen flickering is disturbing during the transition of display modes. Once turned on, the mute function automatically blackens the screen for approximately one second every time the display mode is changed by the VGA BIOS call.

Example VMODE MUT:N

Turns the mute function OFF.

RST

Syntax VMODE RST[:]

Function This resets all screen settings to default. When the Superimpose Driver or VIEW/VGA Control Program is installed, the screen settings are reset to the default specified at the time of installation. When neither is installed, the display mode is set to 3+ (hex).

Default display settings (when the Superimpose Driver of VIEW/VGA Control Program is installed)

- Display mode: 3+
- Genlock: Automatic
- Superimpose: Computer graphics only
- Transparent mode: Single transparent color mode (color number 0 is transparent)
- Mute: On
- Display output: Enable

MOD

Syntax VMODE MOD[:]<mode>

Function Selects a display mode specified by <mode>.
Use of this option allows the user to select one of all the display modes supported by the VIEW/VGA System.
Refer to page 80 for available display modes.

Example VMODE MOD:1+

Sets the display mode to 1+ (hex).

Note The system may not function normally when a display mode other than listed on page 80 is specified.
Internally, the system stores the lower two digits of <mode> in the AL register and executes "Set display mode" (INT10H, AH = 00H).
Although supported by the VIEW/VGA System, those display modes larger than 6 (hex) may not provide compatible environment for some of the MS-DOS commands.

Example of VMODE.COM execution

When the optional SMI-3080 SFA/Digital Data Decoder Board is installed together with the High Scan Superimposer, the SMI3080.EXE diagnostic program, supplied in the SMI-3080 Utility Disk, can be used to check the superimposing of computer graphics and video images on the VIEW/VGA System.

1 Install either the Superimpose Driver or VIEW/VGA Control Program.

A>INT10EX

2 Set the superimpose mode to "superimpose."

A>VMODE SUP:S

3 Execute SMI3080 specifying COM port and baud rate parameters.

A>SMI3080 1, 1200

Refer to the SMI-3080 Operating Instructions for details on the SMI3080.EXE diagnostics program.

Controlling Superimposer and Videodisc Player (LDPSUP.EXE)

The LDPSUP.EXE is a TSR (Terminate and Stay Resident) program which controls the High Scan Superimposer and videodisc player (LDP-1200/1500/1550/2000 series).
This program allows graphics drawn by a commercially available painting software to be overlaid with video images from a videodisc player.

The LDPSUP.EXE has the following functions.

Videodisc player control
CLEAR, INDEX ON/OFF, SEARCH, CH-1/2 ON/OFF, SCAN, FAST, STEP (STILL), PLAY

High Scan Superimposer control
Superimpose mode setting
- Computer graphics only
- Video images only
- Superimpose (overlaying computer graphics and video images)

Transparent color setting
Specifies one of the available colors (16 or 256 colors) as the transparent color

Note:
The LDPSUP.EXE is a special program to be used with a generic software supporting VGA diaplay mode. Without using this program, computer graphics created by the generic VGA software cannot be superimposed. For procedures of running a VGA software separately from the superimposing functions, refer to "Running a Generic VGA Software without Using Superimposing Functions" on page 1-16.

Installation

1 Install either the Superimpose Driver or VIEW/VGA Control Program.

2 Execute the LDP.EXE specifying COM port, baud rate and hot key parameters.

A>LDPSUP <n>,<b>[,[<shift>][,<key>]]

n: COM port (RS-232C connector) number to which the videodisc player's control cable is connected. COM ports 1 through 4 are supported. (Ports 3 and 4 are only available on SMI-3031 Dual RS-232C Board.)
This parameter cannot be omitted.

b: Baud rate (1200, 2400, 4800 or 9600) for the RS-232C port specified by the "n" parameter.
This parameter cannot be omitted.

shift: The shift status key, pressed together with the alphabet key specified by the "key" parameter, to invoke the program. Specify A(lt), C(trl) or S(hift). When omitted, the default Alt key is assumed.

key: The key, pressed together with the shift status key specified by the "shift" parameter, to invoke the program.
Alphabet keys A through Z can be specified. When this parameter is omitted, the default "L" key is assumed.

Examples:

A>LDPSUP 1, 1200

RS-232C port 1, set to 1200 baud, is selected for videodisc player control, with the default [Alt]+[L] as the hot key to invoke the program.

A>LDPSUP 2,4800,,E

RS-232C port 2, set to 4800 baud, is selected for videodisc player control, with [Alt]+[E] as the hot key.

A>LDPSUP 1,9600,C,A

RS-232C port 1, set to 9600 baud, is selected for videodisc player control, with [Ctrl]+[A] as the hot key.

To control only the High Scan Superimposer without controlling the videodisc player, specify the following parameters.

A>LDPSUP 0 [,[<shift>][,<key>]]

Notes:
- Be sure to specify the RS-232C port number to which the videodisc player's control cable is connected.
- The RS-232C port can be used only for videodisc player control once it is specified in the LDPSUP.EXE parameter until the computer is reset (turned off).
- The LDPSUP.EXE may not function properly when used together with other TSR programs. In that case, change the order of installing these TSR programs including the LDPSUP.EXE. If changing the installation order does not improve the situation, it is necessary to give up using these TSR programs.
- Entering "LDPSUP <n>,<b>," or "LDPSUP 0," results in an error.

Removing from the memory

The LDPSUP.EXE program can be removed from the memory provided that there is no memory resident program installed after that.

To remove the LDPSUP.EXE program from the memory, enter as follows.

A>LDPSUP OFF

Note:
If other TSR programs have been installed after LDPSUP.EXE, all these memory resident programs must be removed in the reverse order of installation before removing LDPSUP.EXE. In other words, the last installed program must be removed first. Removing LDPSUP without taking this procedure creates an empty "hole" in the memory and the system may not function properly.

Error messages

Port number is invalid
Appears when a number other than 0 through 4 or number is entered fot the COM port parameter ("n"). It is also displayed when the required separator "." is not entered following the valid COM port number (1, 2, 3 or 4), or a string other than "OFF" is entered.

Port is not present
Appears when the specified COM port is not present.

Baud rate is invalid
Appears when the specified baud rate is incorrect. (1200, 2400, 4800 or 9600 must be specified.)

Key code is invalid
Appears when a key other than [Shift], [Alt] or [Ctrl] is specified as the shift status key, or a key other than alphabets A through Z as the hot key.

RS-232C communication error
Appears when the clear command sent to the videodisc player could not be executed.

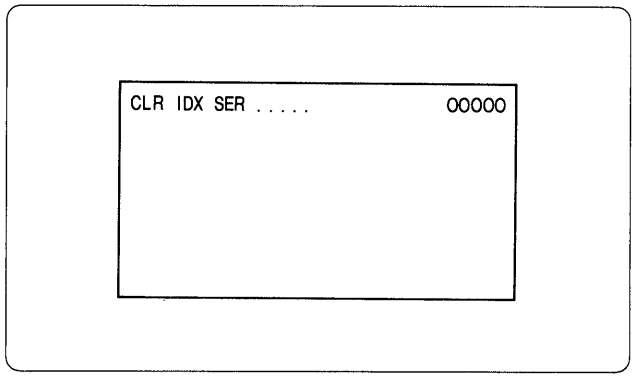
Superimpose driver is not installed
Appears when neither the Superimpose Driver nor VIEW/VGA Control Program has been installed.

LDPSUP is not resident
Appears when an attempt is made to remove the LDPSUP.EXE although it is not resident in the memory.

How to invoke

Press the hot key (the shift status key and alphabet key) specified in the command parameter. (Default is [Alt]+[L].)

Available control commands of the program are displayed at the top row of the screen.



Control commands

The table below shows control commands provided by the LDPSUP.EXE. Note that these commands are effective only after the program is activated by the hot key.

1 Select a command using the right/left cursor keys.
The color of the selected command changes.

2 Press a corresponding key to execute the command.
The command is executed.

Commands	Key to press	Function
CLR	ENTER	Clears command (error status is also cleared.)
IDX	ENTER	Switches index on/off
SER	Number, ENTER	Performs frame search for the frame specified using the number keys.
AUD	ENTER	Switches audio channels 1 and 2. (ON, ON) → (ON, OFF) → (OFF, ON) → (OFF, OFF) → (ON, ON) → .....
SCN	R or F	Performs reverse/forward scan until next command is entered.
FST	R or F	Performs reverse/forward fast until next command is entered.
STP	R or F	Performs reverse/forward step (1 frame at a time).
PLY	R or F	Performs reverse/forward play until next command is entered.
COM	ENTER	Displays only computer graphics.
VID	ENTER	Displays only video images.
SUP	ENTER	Overlays computer graphics on video images.
T_N	Number, ENTER	Makes the specified color (having the palette number designated using the number keys) transparent.
T_C	DOWN/UP cursor	Increases/decrease the palette number for transparent color specification.
(Quit)	Esc	Quits from LDPSUP.

The commands can also be invoked by pressing the following keys instead of selecting with the right/left cursor keys.

For example, the following operations have the same meaning.
Pressing the C key ↔ Selecting the CLR command with the right/left keys and pressing the ENTER key.

Key to press (invoke)	Command	Key to press (control)
C	CLR	ENTER
I	IDX	ENTER
S	SER	—
A	AUD	ENTER
F1/F2	SCN	R/F
F3/F4	FST	R/F
F5/F6	STP	R/F
F7/F8	PLY	R/F
X	COM	ENTER
Y	VID	ENTER
Z	SUP	ENTER
T	T_N	—
U	T_C	—

The following key operations have the same meaning.
Pressing the X key ↔ Pressing the V key when the superimpose mode is "superimpose."
Pressing the Y key ↔ Pressing the V key when the superimpose mode is "computer only."
Pressing the Z key ↔ Pressing the V key when the superimpose mode is "video only."

How to quit

Press [Esc] to quit the program. The LDPSUP program remains resident in the memory until it is removed from the memory or the computer is reset (turned off). It can be invoked again by pressing the hot key.

Notes:

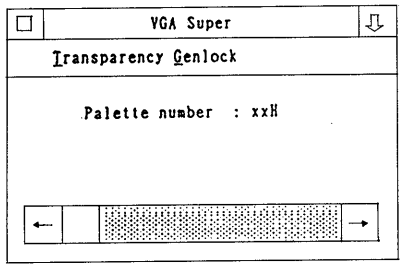
- When LDPSUP is invoked by pressing the hot key, the following attributes are set to the videodisc player and the superimposer.
  - Audio channels 1 and 2 ON.
  - Index ON
  - Frame mode
  - Single transparent color mode
  - Genlock automatic
    - (The external sync mode is selected when an external video signal is input, while the internal sync mode is selected when no external video signal is input.)
  - Superimpose mode
    - (Computer graphics are overlaid on the video images.)
- Ten keys cannot be used in LDPSUP to input numbers.
- Moving the mouse while LDPSUP is active may cause some garbage on the screen. That garbage may not disappear even after quitting from LDPSUP.

1-5-8. Microsoft Windows Utility

The VGASUPER.EXE is a utility program used to control the transparency and genlock of the High Scan Superimposer in the Microsoft Windows environment.
Before operating the Microsoft Windows, the Superimpose Driver or VIEW/VGA Control Program must be installed.

How to start

To start this utility program, select and execute VGASUPER on the MS-DOS Executive Window.



Changing the transparent color

Click [←] or [→] on the screen to increase or decrease the color palette number until the desired color palette number is displayed on the screen.

Changing the superimpose mode and genlock mode

To change the superimpose mode, select the transparency menu in the video mode by placing the mouse cursor on the menu icon and clicking the mouse. Then select the desired superimpose mode. The following three modes are available.

Mode	Description
Computer	Only computer graphics are displayed.
Video	Only video images from the videodisc player are displayed.
Super	Computer graphics are overlaid on video images.

To change the genlock mode, point the desired icon and click the mouse.

Note:
Once "video" is selected, icons are not displayed. In this case, simply click the mouse or press the space bar. This changes the superimpose mode from "video" to "computer."

1-5-9. Superimpose Driver BIOS Specifications

When the Superimpose Driver is installed, the following new functions are added to INT 10H call for the High Scan Superimposer.

INT10H AH = FEH BH = FFH

BL = 00H Set superimpose mode and genlock mode.
01H Set transparent mode.
02H Set transparent color (single transparent).
03H Set transparent colors (multiple transparent).
04H Set mute function.
05H Set display output.
06H Reset display settings.
07H Get version number.
80H Inquire superimpose mode and genlock mode settings.
81H Inquire transparent mode settings.
82H Inquire transparent color (single transparent).
83H Inquire transparent colors (multiple transparent).
84H Inquire mute function setting.
85H Inquire display output setting.

INT 10H

INT 10H AH = 0FEH BH = 0FFH: High Scan Superimposer Functions

BL = 00H Set superimpose mode and genlock mode

[Entry] AL = [g000 00ss]
g = genlock automatic/internal (0/1)
ss = 00: Computer graphics only
01: Superimpose
10: Video image only
11: Reserved

[Return] None

BL = 01H Set transparent color mode

[Entry] AL = [0000 000m]
m = 0: Single transparent color mode
1: Multiple transparent color mode

[Return] None

BL = 02H Set transparent color

[Entry] CX = Transparent color palette number (0000H to 00FFH)

[Return] None

[Note] This is a function for the single transparent color mode. Whatever you change the display mode, the transparent color palette number do not change.

BL = 03H Set transparent colors

Entry SI = Start palette number
CX = Length
ES:DX = Pointer to the transparency data buffer. Each bit specifies the following.
0: Not transparent
1: Transparent

Return None

Note Transparency of the colors in the specified palette number range is changed. This is a function for the multiple transparent color mode.
SI must be from 0000H to 00FFH and the sum of SI and CX must be within 0100H.
When you change the display mode, transparency of the color in the palette change. So set the transparent colors again if you need.

Example When SI = 0003H, CX = 000AH, ES = 5000H, DX = 0000H and the byte pointers pointing 5000:0000(H) = 36H and 5000:0001(H) = 80H, this function causes the following.
- Colors whose palette number 3, 4, 7, 10 and 12 are set non-transparent.
- Colors whose palette number 5, 6, 8, 9 and 11 are set transparent.
- Transparency setting of the colors having a palette number smaller than 3 or greater than 12 remains as is.

Color number (decimal):	3	4	5	6	7	8	9	10	11	12	-	-
Data:	0	0	1	1	0	1	1	0	1	0	0	0

BL = 04H Set mute function (on/off)

Entry AL = [0000 000m]
m = mute function off/on (0/1)

Return None

Function With the mute function turned on, output from the High Scan Superimposer is muted when the display mode setting function call (INT 10H, AH = 00H) is executed.
No image is displayed for approximately one second.
With the mute function turned off, the image may flicker when the display mode is changed.

BL = 05H Set display output

Entry AL = [0000 000m]
m = Display output enable/disable (0/1)

Return None

Function With the display output disabled, output from the High Scan Superimposer (both RGB and video outputs) is disabled.

BL = 06H Reset display settings

Entry None

Return None

Function Resets all display settings to default.

BL = 07H Get version number

Entry None

Return BL = FEH: Superimpose Driver is installed.
Others: Superimpose Driver is not installed.
When BL = FEH, AL indicates the version number of the Superimpose Driver (BCD format). The upper nibble is the integer part while the lower nibble the fraction.

Function Confirms whether the Superimpose Driver is installed, and gets the version number if installed.

BL = 80H Inquire superimpose mode and genlock mode settings

Entry None

Return AL = [gXXX XXss]
X = Reserved
g = Genlock automatic/internal (0/1)
ss = 00: Computer graphics only
01: Superimpose
10: Video images only
11: Reserved

BL = 81H Inquire transparent mode setting

Entry None

Return AL = [XXXX XXXm]
X = Reserved
m = 0: Single transparent color mode
1: Multiple transparent color mode

BL = 82H Inquire transparent color setting

Entry None

Return CX = Transparent color palette number (0000H to 00FFH)

Note This is a function for the single transparent color mode.

BL = 83H Inquire transparent color settings

Entry SI = Start palette number
CX = Length
ES:DX = Pointer to the transparency data buffer.

Return None

Note This is a function for the multiple transparent color mode.

BL = 84H Inquire mute function (on/off) setting

Entry None

Return AL = [XXXX XXXm]
x = Reserved
m = Mute function off/on (0/1)

BL = 85H Inquire display output setting

Entry None

Return AL = [XXXX XXXm]
x = Reserved
m = Display output enable/disable (0/1)

Default display settings

When the Superimpose Driver or VIEW/VGA Control Program is installed, the display modes are set as follows.
- Display mode: 3+
- Genlock: Automatic
- Superimpose: Computer graphics only
- Transparency: Single transparent color mode (color number 0 is transparent)
- Mute: On
- Display output: Enable

Note:
All functions retain the values used when called except for the AX register, flags, and registers to which returned values are passed.
For INT10H functions other than those added by the Superimpose Driver, refer to the following IBM publications.
- IBM Personal System/2™ Display Adapter Technical Reference, April 1987 (IBM part number 68X2251 S68X-2251-0)
- IBM Personal System/2™ and Personal Computer BIOS Interface Technical Reference, April 1987 (IBM part number 68X2260 S68X-2260-00)

1-6. TECHNICAL DATA

1-6-1. Display Mode

The VIW-3015A features two VGA setups:
Normal VGA and Superimposed VGA. The table below shows various display modes in both VGA modes.

Normal VGA

When the power is turned on, the computer system starts in this VGA setup. The Normal VGA setup is compatible with the VGA display adapter used by the IBM Personal System/2™. In this setup, computer graphics cannot be superimposed on video images.

Superimposed VGA

This VGA setup is invoked when the Superimpose Driver ("INT10EX" in the supplied Maintenance and Utility Disk) is installed. All display modes under the Superimpose VGA setup are made compatible with 31.5 kHz horizontal and 60 Hz vertical frequencies to allow superimposing of computer graphics on video images. The monitor's display area is slightly smaller than the Normal VGA setup. The ratio between the display area's horizontal width and vertical height also differs.
For details, refer to the Software Information.

Mode	Type	Colors[1]	Characters	Display buffer start (hex)	Dots per character	Max. pages	Resolution
0, 1	Character	16	40×25	B8000	8× 8	8	320×200[2]
0*, 1*	Character	16	40×25	B8000	8×14	8	320×350
0+, 1+	Character	16	40×25	B8000	9×16	8	360×400
2, 3	Character	16	80×25	B8000	8× 8	8	640×200[2]
2*, 3*	Character	16	80×25	B8000	8×14	8	640×350
2+, 3+	Character	16	80×25	B8000	9×16	8	720×400
4, 5	Graphics	4	40×25	B8000	8× 8	1	320×200[2]
6	Graphics	2	80×25	B8000	8× 8	1	640×200[2]
D	Graphics	16	40×25	A0000	8× 8	8	320×200[2]
E	Graphics	16	80×25	A0000	8× 8	4	640×200[2]
10	Graphics	16	80×25	A0000	8×14	2	640×350
11	Graphics	2	80×30	A0000	8×16	1	640×480
12	Graphics	16	80×30	A0000	8×16	1	640×480
13	Graphics	256	40×25	A0000	8× 8	1	320×200[2]
5F[3]	Graphics	256	80×30	A0000	8×16	1	640×480

* : Enhanced mode of the IBM Enhanced Graphics Adapter
\+ : Enhanced mode of the IBM Personal System/2 VGA Display Adapter
1) Selectable from 262, 144 colors for simultaneous display
2) 200-line vertical resolution modes are double-scanned to display 400 lines on the screen.
3) Enhanced mode of the internal high scan superimposer board.

1-6-2. Specifications

Refer to the LDP-1500 Service Manual for specifications of the videodisc player.

CPU

Processor used	Intel 80286
Clock frequency	8 MHz
Co-processor	80287 (option)
Wait	One wait for memory access 4 wait for I/O access
Interrupt	External interrupts (software initiated) INT instructions Instruction exceptions
Resetting	Automatic at power on/Manual

Memory

RAM	640K bytes (resident)
Video RAM	512K bytes
ROM	128K bytes Initial program loader, System monitor, Diagnostics program, and I/O driver
DMA	7 channel programmable DMA Transmission rate: 1M bytes/sec. max. (CPU: 8 MHz) Channel 0: Floppydisk interface

CRT display

Screen configuration	Superimposition of VGA display screens over the video images.
RGB video output	RGB analog signal, 0-0.7 V, 75 ohms
Horizontal sync signal frequency	31.5K Hz
Vertical sync signal frequency	60 Hz For all superimposed VGA mode, and mode 11, 12 and 5F in normal VGA mode 70 Hz For normal VGA mode (except mode 11, 12 and 5F)

I/O interface

Keyboard	5-pin DIN jack TTL level, serial transfer
RS-232C	9-pin connector Port 1: Controller 8250, asynchronous mode only Baud rate: Programmable up to 9600 baud
Printer	25-pin connector TTL level, 8-bit parallel transfer
Floppydisk	Controller: μPD72065C Drive: Sony 3.5-inch micro floppydisk drive 2HD Type Disk used: 3.5-inch micro floppydisk double side, 80 tracks/side
Light pen	5-pin DIN jack
PSG	Controller: SN-76489AN (3 tones and a noise)
Timer/Calendar	HD146818 (with backup function)

General

Power requirement	120V AC ±10%, 50/60 Hz
Power consumption	5.9 A (OUTLET 1.7 A) max.
Operating conditions	Temperature: 5°C to 35°C (41°F to 95°F) Humidity: 25% to 80%
Storage temperature	−20°C to +60°C (−4°F to 140°F)
Dimensions	Approx. 424×297×455 mm (w/h/d) (16¾×11⅞×17⅞ inches) main unit only, including projecting parts and controls
Weight	Approx. 23.2 kg (51 lb 2 oz) With a keyboard: 1.7 kg (3 lb 12 oz)

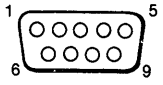
I/O devices

Keyboard	Total number of keys: 101 Function keys: 12

Design and specifications subject to change without notice.

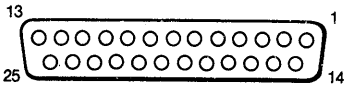
1-6-3. Pin Assignment of the Connector

RS-232 (1)/(2) connector



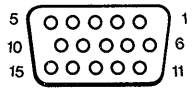
Pin No.	Signal	Pin No.	Signal
1	CD	6	DSR
2	R×D	7	RTS
3	T×D	8	CTS
4	DTR	9	RI
5	GND		

PRINTER connector



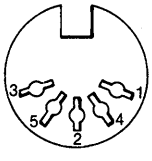
Pin No.	Signal	Pin No.	Signal
1	−STROBE	14	−AUTO FD
2–9	DATA0–7	15	−ERROR
10	−ACK	16	−INIT
11	BUSY	17	−SLCT IN
12	P.E	18–25	GND
13	SLCT		

MONITOR connector



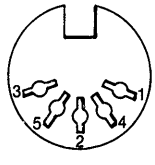
Pin No.	Signal	Pin No.	Signal
1	RED VIDEO	9	GND
2	GREEN VIDEO	10	GND
3	BLUE VIDEO	11	NC
4	NC	12	NC
5	GND	13	HORIZONTAL SYNC
6	RED RETURN (GND)	14	VERTICAL SYNC
7	GREEN RETURN (GND)	15	NC
8	BLUE RETURN (GND)		

LIGHT PEN jack



Pin No.	Signal
1	−LP DATA
2	−LPSW
3	+5V
4	Not used
5	GND

KEYBOARD jack

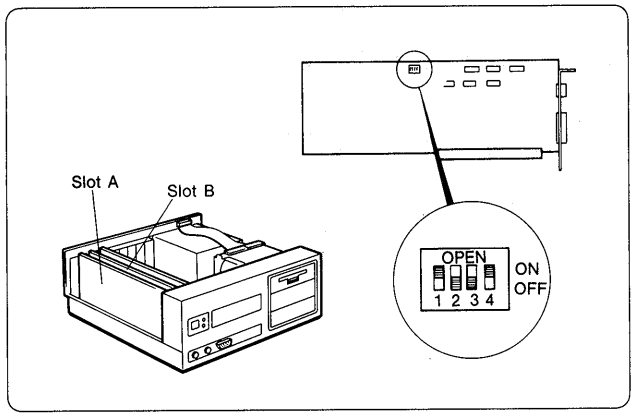


Pin No.	Signal
1	KBCLK
2	KBDATA
3	N C
4	GND
5	+5V

1-6-4. Switch Setting

DIP switch

The default settings of the DIP switches on the I/O board in slot A are as follows:



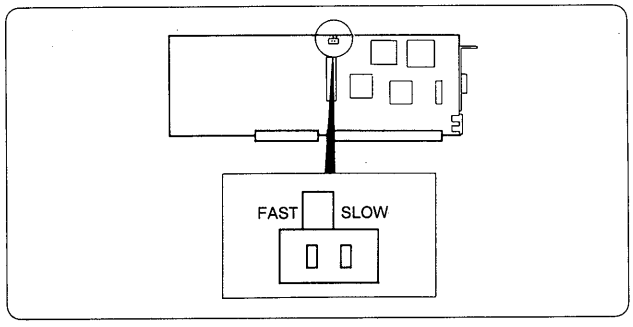
The description of the switches are as follows:

Switch	Description
SW4	Reserved
SW3	ON: A keyboard is not connected. OFF: A keyboard is connected.
SW2	ON: The SMI-3085 is not installed. OFF: The SMI-3085 is installed.
SW1	ON: Output to RS-232C disabled. OFF: Output to RS-232C enabled.

Switch 2 is effective only when the DISPLAY BOARD switch on the rear panel of the computer is set to B position.

Co-processor clock frequency setting

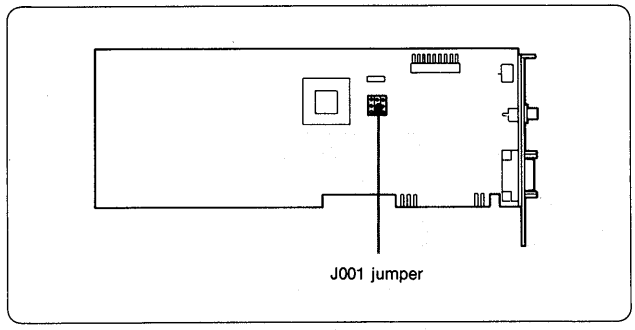
The default setting of the co-processor clock frequency switch on the CPU board in slot B is as follows:

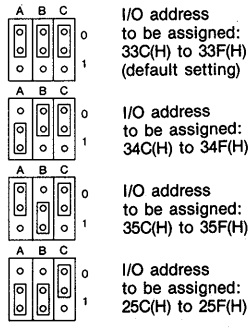


FAST: System clock x 1
SLOW: System clock x 2/3

Superimposer board jumper setting

You can change the I/O addresses of superimpose system. If you want to use the I/O address 33C(H) to 33F(H) at another interface board, change the I/O addresses using J001 jumper on VS-38A board in slot 5.



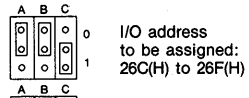


I/O address to be assigned: 33C(H) to 33F(H) (default setting)

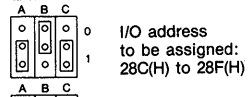
I/O address to be assigned: 34C(H) to 34F(H)

I/O address to be assigned: 35C(H) to 35F(H)

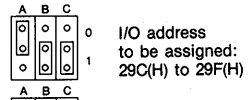
I/O address to be assigned: 25C(H) to 25F(H)



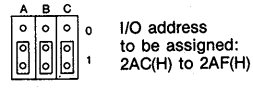
I/O address to be assigned: 26C(H) to 26F(H)



I/O address to be assigned: 28C(H) to 28F(H)



I/O address to be assigned: 29C(H) to 29F(H)



I/O address to be assigned: 2AC(H) to 2AF(H)

Note:
Jumpers other than J001 must be left in the factory setting.

1-7. MS-DOS REFERENCE CARD

BATCH PROCESSING COMMANDS

Command	Function and Format
ECHO	Turns batch echo feature on and off.
	ECHO [ON/OFF <message>]
FOR	Command extension used in batch and interactive file processing.
	FOR %% <c> IN <set> DO <command> (for batch processing) <c> any character except numerics FOR % <c> IN <set> DO <command> (for interactive processing)
GOTO	Command extension used in batch file processing.
	GOTO <label>
IF	Command extension used in batch file processing.
	IF <condition> <command> condition: ERRORLEVEL <number> true if the previous program executed by COMMAND.COM had an exit code of <number> or higher. <string1>= =<string2> true if <string1> and <string2> are identical. EXIST <filename> true if <filename> exists. NOT <condition> true if statement allows conditional execution of commands.
PAUSE	Suspends execution of the batch file.
	PAUSE [<comment>]
REM	Displays remarks during execution of the batch file.
	REM [<command>]
SHIFT	Allows access to more than 10 replaceable parameters in batch file processing.
	SHIFT

CP/M UTILITY COMMANDS

Command	Function and Format
DCPM (NET)	Displays CP/M directory
	DCPM [<drive:>] [<filename>]
ECPM (NET)	Deletes CP/M files with the designated pathname.
	ECPM [<drive:>] <filename>
NCPM (NET)	Changes the file name.
	NCPM [<drive:>] <filename 1> <filename 2>
RCPM (NET)	Read CP/M files to MS-DOS disk.
	RCPM [<drive:>] <filename> [<drive:>] [<filename>] /A copies the file as a text file that ends with the CONTROL-Z code.
WCPM (NET)	Writes CP/M files from MS-DOS disk.
	WCPM [<drive:>] <filename> [<drive:>] [<filename>]

DEBUG COMMANDS

Command	Function
A [<address>]	Assemble
C <range> <address>	Compare
D [<range>] D <address>	Dump
E <address> [<list>]	Enter
F <range> <list>	Fill
G [=<address 1>, <address 2>	Go
H <value> <value>	Hex
I <value>	Input
L [<address> [<drive> <record> <value>]]	Load
N <filename 1> [<filename 2>...]	Name
O <value> <byte>	Output
P [=<address>] [<value>]	Proceed
Q	Quit
R [<register-name>]	Register
S <range> <list>	Search
T [=<address>] [<value>]	Trace
U [<range>] U <address>	Unasemmble
W [<address> [<drive> <record> <value>]]	Write

<drive> A one-digit hexadecimal value to indicate which drive a file will be loaded from or written to.
0 = A, 1 = B, 2 = C, 3 = D

<byte> A two-digit hexadecimal value to be placed in or read from an address or register.

<record> A 1- to 3-digit hexadecimal value used to indicate the logical sector number on the disk.

<value> A hexadecimal value up to four digits used to specify a port number or the number times a command should repeat its functions.

<address> A two-part designation consisting of either an alphabetic segment register designation or a four-digit segment address plus an offset value. If this parameter is omitted, the value set in the CS register is used when G, L, P, T, U or W command is executed. The value set in the DS register is used when any other command is executed.

<range> Two <address>es: for example, <address 1> <address 2> or <address>L<value>.

<list> A series of <byte> value or of <string>s.

<string> Any number of characters enclosed in quote marks.

DEVICE DRIVER AND PARAMETER

Device Driver	Parameter
ANSI console device driver	DEVICE = ANSI.SYS
Extended communication device driver	DEVICE = EXCOM.SYS COM <n> [:] <baud> [, <parity> [, <data> [, <stop> [, <flow>]]]] <n> a communication port number 1, 2, 3 or 4 <baud> baud rate 110, 150, 300, 600, 1200, 2400, 4800 or 9600 <parity> parity N (none), O (odd) or E (even) <data> character length (bits) 7 or 8 <stop> stop bit 1 or 2 <flow> flow control N (no protocol) or X (DC1/DC3) Default: no parity, 8 bits, 1 stop bit and no protocol
Mavica device driver	DEVICE = MAVICA.SYS <n> <n> a communication number 1, 2, 3 or 4
Pointing device driver	DEVICE = MOUSE.SYS [<n>] [, <d>] <n> a communication port number 1, 2, 3 or 4 (default: 2) <d> device name MOUSE, MM1201, BITPAD, or BITPAD2ASC
Touche panel device driver	DEVICE = PANEL.SYS <n>, <d> <n> a communication port number 1, 2, 3 or 4 <d> device name C1200, SFB1000 or CSMART
Videodisc device driver	DEVICE = SETLDP.SYS <n> [, <baud>] <n> a communication port number 1, 2, 3 or 4 <baud> baud rate 1200, 2400, 4800 or 9600
Virtual disk device driver	DEVICE = VDISK.SYS [<disk> [<sector> [<dir>]]] [/E [: <m>]] <disk> virtual disk size in K bytes (decimal value) <sector> sector size in bytes 128, 256 or 512 <dir> a number of directory entries /E Expansion memory is installed. <m> data transfer rate 1 to 8

EDLIN COMMANDS

Command	Function
[<n>] A	Adds the specified number of lines.
[<line 1>], [<line 2>], <line 3>, [<count>] C	Copies a range of lines to a specified line number
[<line 1>] [, <line 2>] D	Deletes a specified range of lines.
[<line>]	Edits a line of text.
E	Ends the editing session.
[<line>] I	Inserts text immediately before the specified line.
[<line 1>] [, <line 2>] L	Lists a range of lines.
[<line 1> [, <line 2>], <line> M	Moves a range of text to the line specified.
[<line 1> [, <line 2>] P	Pages through a file 23 lines at a time.
Q	Quits the editing session.
[<line 1>] [, <line 2>] [?] R <stringl> <Control-Z> <string 2>	Replaces all occurrences of a string of text with a diffrent string of text.
[<line 1>] [, <line 2>] [?] S [<string>]	Searches a range of lines for a string of text.
[<line>] T <drive:> <pathname>	Inserts the contents of a file into the file currently being edited.
[<n>] W	Writes a specific number of lines to disk from the lines that are being edited in memory

<line> indicates a line number.
<line> may be specified one of three ways:

<number>	any number less than 65534
Period (.)	current line number
#	the line after the last line number
Return key	If you type a command and then press Return key without any of line markers, EDLIN uses a default value for each command.

The question mark (?) option tells EDLIN to ask you if the correct strig has been found.
<string> represents text to be found, to be repalced, or to replace other text.

SONY

MS-DOS™ 3.20

SMW-3001A /B

Reference Card

SMC-3000 Series

Sony Corporation
Printed in Japan © 1987/1988

22 (1) /23 (1)

MS-DOS COMMANDS

Command	Function and Format
APPEND	Sets a search path for data files.
	APPEND [<drive:>] [<path>] [; [<drive:>] [<path>] ...]
ASSIGN	Assigns a drive letter to a different drive.
	ASSIGN [X [=] Y [...]] X current drive Y new drive
ATTRIB	Sets or displays attributes of a file.
	ATTRIB [+R|-R] [+A|-A] [<drive:>] <pathname> +R sets a read-only mode. -R disables read-only mode. +A sets the archive attribute of a file. -A clears the archive attribute of a file.
BACKUP	Backs up files from one disk to another.
	BACKUP <drive:> [<pathname>] <drive:> [/S] [/M] [/A] [/D : <date>] /S backs up subdirectories also. /M backs up only those files that have changed since tha last backup. /A adds the files to be backed up to those already on the backup disk. /D backs up only those files that were last modified at or after a certain date.
BREAK	Sets Control-C check.
	BREAK [ON|OFF] ON allows Control-C checking to be extended to any MS-DOS functions. OFF check for Control-C during screen, keyboard, and printer reands/writes only.
CHDIR (CD)	Change directories; displays working directory (CD).
	CHDIR [<pathname>]
CHKDSK (NET)	Scans the directory of a drive and checks for consistency.
	CHKDSK [<drive:>] [<pathname>] [/F] [/V] /F corrects all errors found in the directory. /V displays all files and their paths on a disk.
CLS	Clears the terminal screen.
	CLS
COMMAND	Starts the command processor.
	COMMAND [<drive:> <pathname>] [/P] [/C <string>] [/E : <nnnn>] /P tells COMMAND.COM not to exit to any higher level. /C executes the command or commands specified by <string> and returns. /E specifies the environment size, where <nnnn> is the size in bytes (in decimal).
COPY	Copies the file(s) specified.
	COPY [<drive:>] <pathname> [<drive:>] [<pathname>] [/V] [/A] [/B] /V verify /A the files being processed are ASCII files. /B the files being processed are binary files.
	Appends files.
	COPY <pathname>+<pathname> [+ <pathname> ...] <pathname>
CTTY	Changes the console TTY.
	CTTY <device>
DATE	Displays and sets the date.
	DATE [<date>]

Command	Function and Format
DEBUG	Debugger
	DEBUG [<filename>] [<arglist>] <arglist> a list of filename parameters and switches
DEL (ERASE)	Deletes the file(s) specified (Erase).
	DEL [<drive:>] <pathname>
DIR	Lists requested directory entries.
	DIR [<drive:>] <pathname> [/P] [/W] /P Page Mode /W wide display
DISKCOMP (NET)	Compares disks.
	DISKCOMP [<drive:>] [<drive:>]
DISKCOPY (NET)	Makes a copy of a disk.
	DISKCOPY [<drive:>] [<drive:>]
EDLIN	Line editor
	EDLIN <filename> [/B] /B ignores any Control-z characters in the file.
EXE2BIN	Converts executable files to binary format.
	EXE2BIN [<drive:>] <pathname> [<drive:>] <pathname>
EXIT	Exits command processor and returns to previous level.
	EXIT
FC	Compares files.
	FC [/A] [/B] [/C] [/L] [/LB <n>] [/N] [/T] [/W] [/<nnnn>] <filename 1> <filename 2> /A abbreviates the output of an ASCII comparison. /B forces a binary comparison of both files. /C cause the matching process to ignore the case of letters. /L compares the files in ASCII mode. /LB<n> sets the internal line buffer to <n> lines. /N displays the line numbers on an ASCII comparison. /T does not expand tabs to spaces. /W causes FC to compress tabs and spaces during the comparison. /<nnnn> specifies the number of lines required to match for the file.
FIND	Searches for as constant string of text.
	FIND [/V] [/C] [/N] <"string"> [<drive:>] [<pathname>] /V displays all lines not containing the specified string. /C prints only the count of lines containing the string. /N causes each line to be preceded by its relative line number in the file.
FLD2PIX G	Converts .FLD file to .PIX file.
	FLD2PIX <source pathname> [<destination pathname>]
FORMAT (NET)	Formats a disk to receive an MS-DOS file.
	FORMAT [<drive:>] [/S] [/V] [/9] /S system files and COMMAND.COM are copied. /V sets volume label. /9 disk is formatted for 9 sectors per track.
GRAFTABLE	Loads a table of graphics characters.
	GRAFTABLE

Command	Function and Format
GRAPHICS	Prepares MS-DOS for printing graphics.
	GRAPHICS [<printer> [/R] printer printer to be used to print the display: SMI7020, SMI720, GRAPHICS /R prints black as black and white as white.
HDBOOT	Writes the program that boots MS-DOS from the hard disk onto the floppydisk.
	HDBOOT
HDISK	Sets up the hard disk drive.
	HDISK
JOIN	Joins a disk drive to a pathname.
	JOIN JOIN <drive:> <drive:> <pathname> JOIN <drive:>/D /D turns off the JOIN command
KEYBXX	Supports a foreign keyboard.
	KEYBUK, KEYBGR, KEYBFR, KEYBIT or KEYBSP
LABEL (NEW)	Labels disks.
	LABEL [<drive:>] [<volume label>]
LINK	Linker
	LINK [<objectfiles> [, [<executablefile>] [, [<mapfile>] [, [libraryfile]]]] [<options>]]
MKDIR (MD)	Makes a directory.
	MKDIR [<drive:>] <pathname>
MODE	1. Sets display modes.
	MODE [CON [:]] <mode> [, [<type>] [<HG>]] <mode>

mode	Character/ Graphics	No. of char.	Resolution
40	C/G	40×25	320×200
80	C/G	80×25	640×200
BW40	C/G (monochro)	40×25	320×200
BW80	C/G (monochro)	80×25	640×200
CO40	C/G (color)	40×25	320×200
CO80	C (color)	80×25	640×200
C1	C	40×25	320×200
C2	C	80×25	640×200
G1	G	40×25	320×200
G2	G (monochro)	80×25	640×200
BWC1	C (monochro)	40×25	320×200
BWC2	C (monochro)	80×25	640×200
BWG1	G (monochro)	40×25	320×200
BWG2	G (monochro)	80×25	640×200
COC1	C (color)	40×25	320×200
COC2	C (color)	80×25	640×200
COG1	G (color)	40×25	320×200

<type> G display type: 0, 1, 2 or 3
<HG> G HG mode: 1, 2 or 3

Command	Function and Format
MODE	2. Sets superimpose modes. G
	MODE SUP [:] <cxpt> [, [<gxpt>] [, [<expt>] [, [<bxpt>] [, <priority>]]]] <cxpt> CG transparent color: N (Not), T (Transparent) or P (Partial) <gxpt> HG transparent color: N, T or P <expt> HG extra transparent color: N or T <bxpt> border transparent color: N or T <priority> H (HG > CG > video) or C (CG > HG > video)
	3. Sets genlock and interlace mode. G
	MODE GEN [:] <genlock> <genlock> N (internal, non-interlace), I (internal, interlace), E (external, interlace), A (auto, interlace)
	4. Selects separate mode/combined mode of CG/HG planes. G
	MODE GEN [:] = <sep> <sep> 1 (separate mode) or 2 (combined mode)
	5. Clears the screen by the specified color.
	MODE CLS [:] <plane> [, <color>] <plane> C (CG plane) or H (HG plane) G <color> 0–255
	6. Resets the display mode to its default status.
	MODE RST [:]
	7. Sets asynchronous communication mode.
	MODE COM <n> [:] <baud> [, [<parity>] [, [<data>] [, [<stop>] [, P]]]] <n> a communication port number 1, 2, 3 or 4 <baud> baud rate 110, 150, 300, 600, 1200, 2400, 4800 or 9600 <parity> N (no parity: default), O (odd) or E (even) <data> data length 7 (default) or 8 bits <stop> stop bits 1 (default) or 2 bits P specifies use of a serial printer, and will continuously retry where time-out errors occur.
	8. Specifies parallel printer modes.
	MODE LPT <#> [:] [<n>] [, [<m>] [, P]] <#> a printer port number 1, 2 or 3 <n> characters/line 80, 132 or 158 <m> lines/inch 4, 6 or 8 P will continuously try where time-out error occurs.
	9. Redirects parallel printer output.
	MODE LPT <#> [:] = COM <n> <#> a printer port number 1, 2 or 3 <n> a communication port number 1, 2, 3 or 4
MORE	Sends output to the console one screen at a time.
	MORE
PANELSET	Adjusts the touch screen device driver PANEL.SYS.
	PANELSET
PARK	Moves the hard disk drive's heads to the shipping zone.
	PARK
PATH	Sets a command search path.
	PATH [[<drive:>] [<pathname>] ; [<drive:>] [<pathname>] ...]

Command	Function and Format
PIC2PIX G	Converts a .PIC file to a .PIX file.
	PIC2PIX <source pathname> [<destination pathname>] [/M<mode>] [/T<type>] [/R<switch>] /M<mode> the graphic resolution for the converted picture file 1 (HG1), 2 (HG2) or 3 (HG3) /T<type> the screen size of the display 0 (type 0) or 1 (type 1) /R<switch> the reduction mode ON/OFF 0 (reduction mode OFF) or 1 (ON)
PRINT	Prints files.
	PRINT [/D : <device>] [/B : <size>] [/Q : <value>] [/T] [/C] [/P] [<drive:>] [<pathname>] /D : <device> the print device /B : <size> size in bytes of the internal buffer /Q : <value> the number of files allowed in the print queue. 4 to 32 (default: 10) /T deletes all files in the print queue. /C turns on cancel mode. /P turns on print mode.
PROMPT	Change the MS-DOS command prompt.
	PROMPT [<text>]
RECOVER NET	Recovers a bad disk or file.
	RECOVER [<drive:>] <pathname>
REN (RENAME)	Changes the name of a file.
	REN [<drive:>] <pathname> <pathname>
REPLACE	Updates previous versions of files.
	REPLACE [<drive:>] <pathname> [<drive:>] [<path>] [/A] [/D] [/P] [/R] [/S] [/W] /A adds new files. /D replaces newer files. /P prompts you to replace or add files. /R replaces read-only files. /S searches all directories. /W waits for any keys.
RESTORE	Restores backed up files.
	RESTORE <drive:> [<drive:>] [<pathname>] [/S] [/P] /S restores subdirectories. /P prompts for permission to restore hidden or read-only files.
RMDIR (RD)	Removes a directory.
	RMDIR <pathname>
SELECT	Installs MS-DOS on a new disk.
	SELECT [[<drive:>] <drive:> [<pathname>]] <country> <key> <country> specifies the country code. <key> specifies the keyboard code.
SET	Sets one string value to another in the environment.
	SET [<string> = <string>]
SHARE	Installs file sharing and locking.
	SHARE [/F : <space>] [/L : <locks>] /F : <space> allocates file space in bytes. /L : <locks> allocates the number of locks.
SORT	Sorts data forward or backward.
	SORT [/R] [/ + <n>] /R reverse the sort. / + <n> sorts starting with column n.

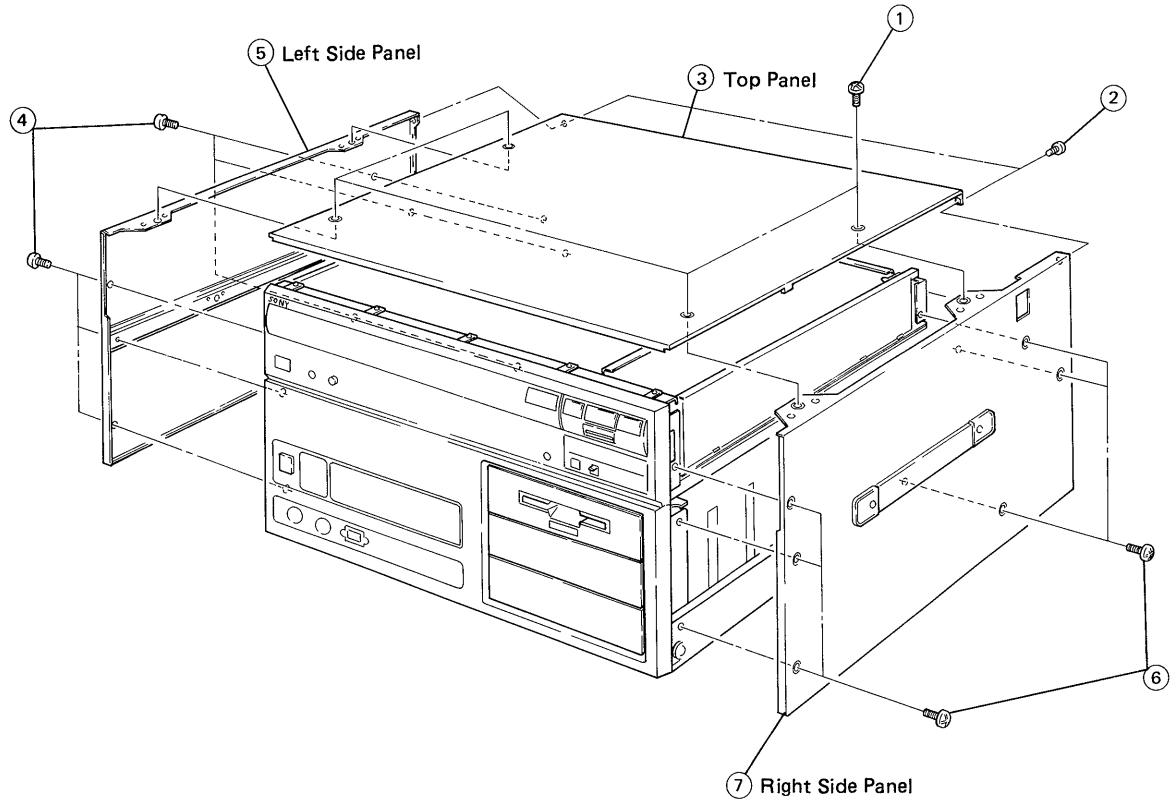
Command	Function and Format
SUBST NET	Substitutes a string for a pathname.
	SUBST [<drive:>] [<pathname>] [/D] /D deletes an associated drive or pathname.
SWITCH G	Selects the use of the main memory of 640K bytes.
	SWITCH [512[/W]|640[/W]] /W waits for the <Enter> key before MS-DOS is loaded again.
SYS NET	Transfers MS-DOS system files.
	SYS <drive:>
TERM	Simulates your computer as a terminal.
	TERM <n> [, <duplex> [, <flow> [, <del>] [, <autolf> [, <mask>]]]] <n> a communication port number 1, 2, 3 or 4 <duplex> communication method F (full dual, default) or H (half dual) <flow> flow control X (DC1/DC3) or N (no protocol) <del> received DEL (7FH) code transaction N (not change), B (change to BS code, default) or 0 (change to NUL code) <autolf> automatic line feed (0AH) transaction N (no auto line feed, default), L (auto line feed at receiption/ sending), R (receive only) or S (send only) <mask> mask MSB M (reset MSB to 0) or N (no mask)
TIME	Displays and sets the time.
	TIME [<hours> : <minutes>]
TREE	Displays directories and file names.
	TREE [<drive:>] [/F] /F displays the names of the files in each directory.
TYPE	Displays the contents of a file on the screen.
	TYPE [<drive:>] <filename>
VER	Prints MS-DOS version number.
	VER
VERIFY	Turns the verify switch on/off when writing to disk.
	VERIFY [ON/OFF]
VOL	Displays disk volume label.
	VOL [<drive:>]
XCOPY	Copies files and subdirectories.
	XCOPY [<drive:>] [<path>] <filename> [<drive:>] [<path>] [<filename>] [/A] [/D : <date>] [/E] [/M] [/P] [/S] [/V] [/W] /A copies new or modified files. /D : <date> copies files on or after the date. /E copies any subdirectories. /M copies new or modified files. /P prompts. /S copies all subdirectories. /V verifies. /W waits for any keys.

CHAPTER 2
SERVICE INFORMATION

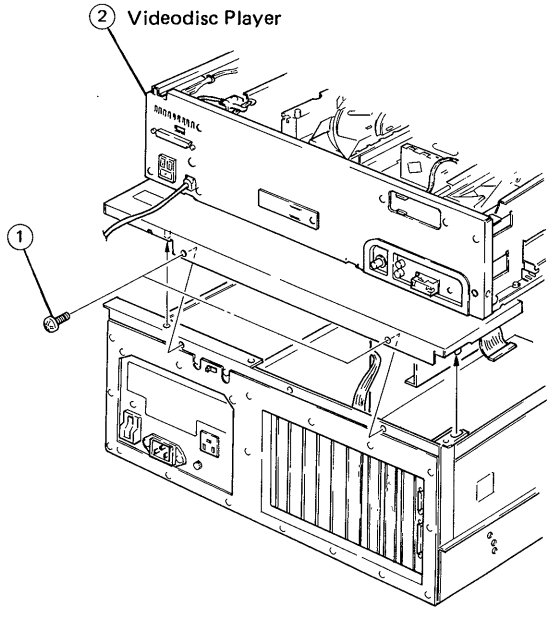
2-1. REMOVAL

Perform the following removal in numerical order given.

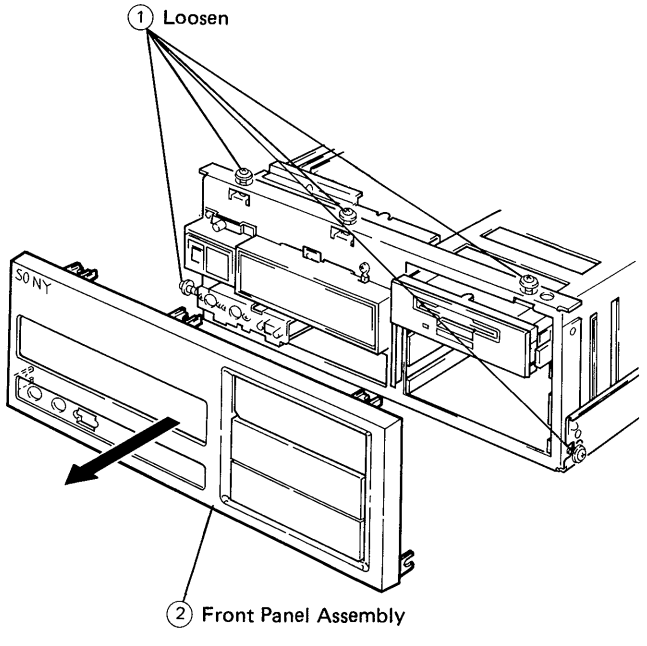
2-1-2. Top Panel and Side Panel Assemblys



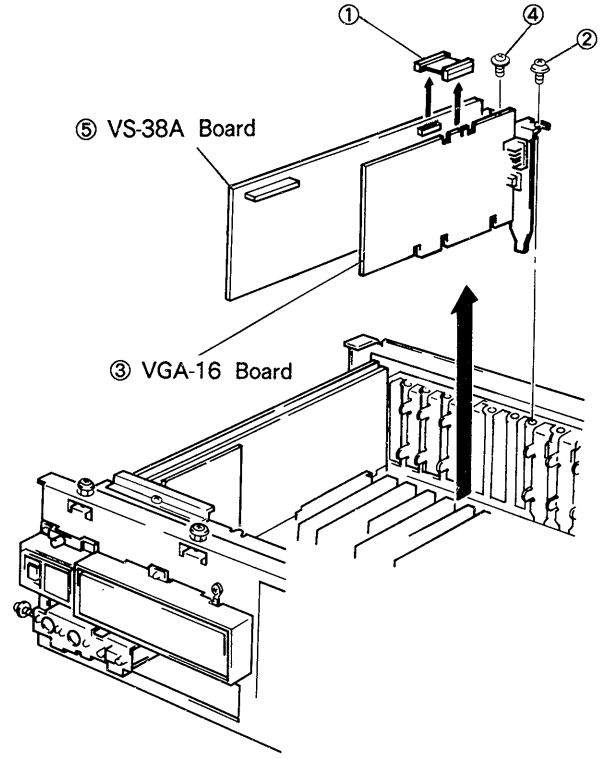
2-1-2. Videodisc Player



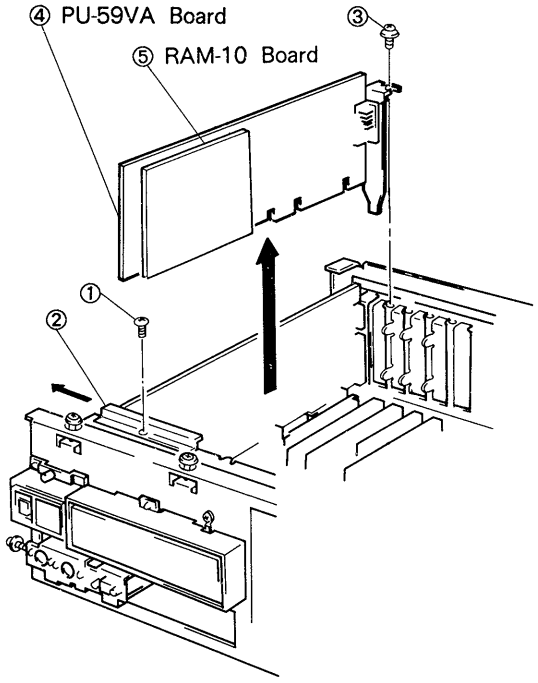
2-1-3. Front Panel Assembly



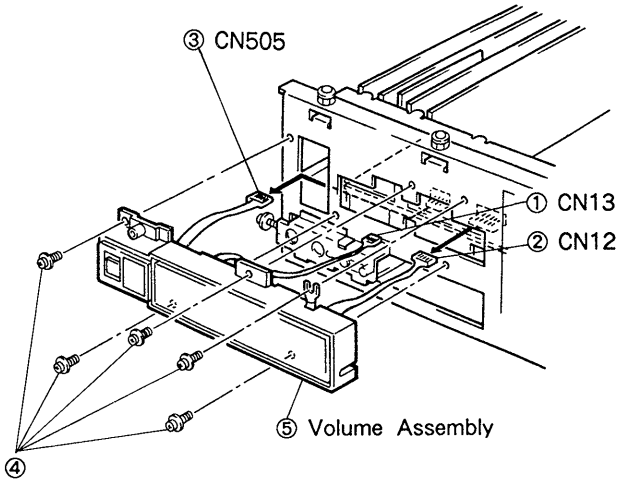
2-1-4. VS-38A Board and VGA-16 Board



2-1-5. PU-59VA Board and RAM-10 Board

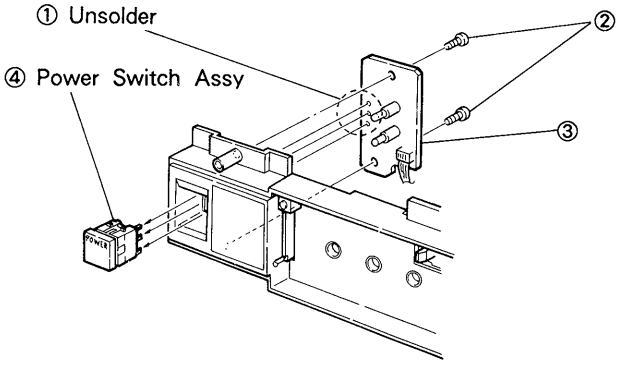


2-1-6. Volume Assembly

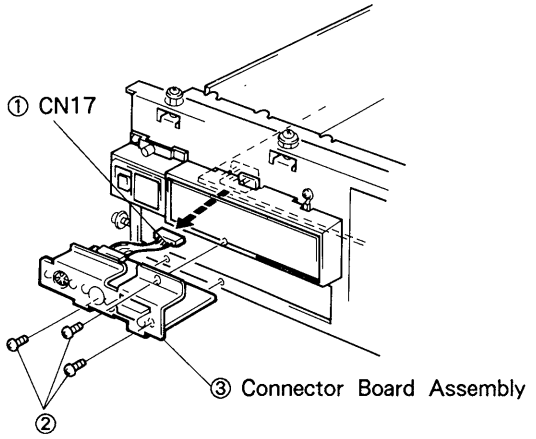


CN505 is connected only when mounting SMI-3085.

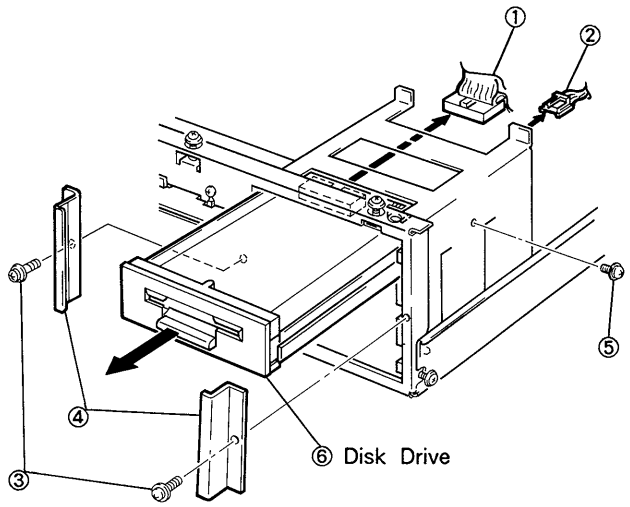
2-1-7. Power Switch Assembly



2-1-8. Connector Board Assembly

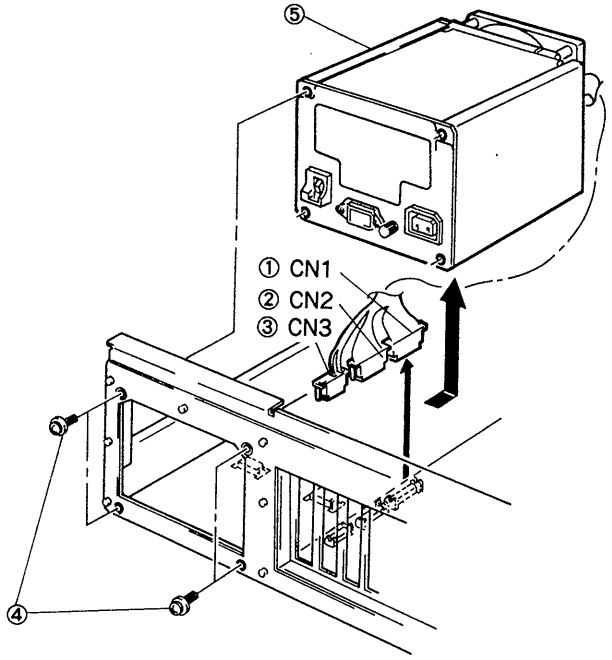


2-1-9. Disk Drives

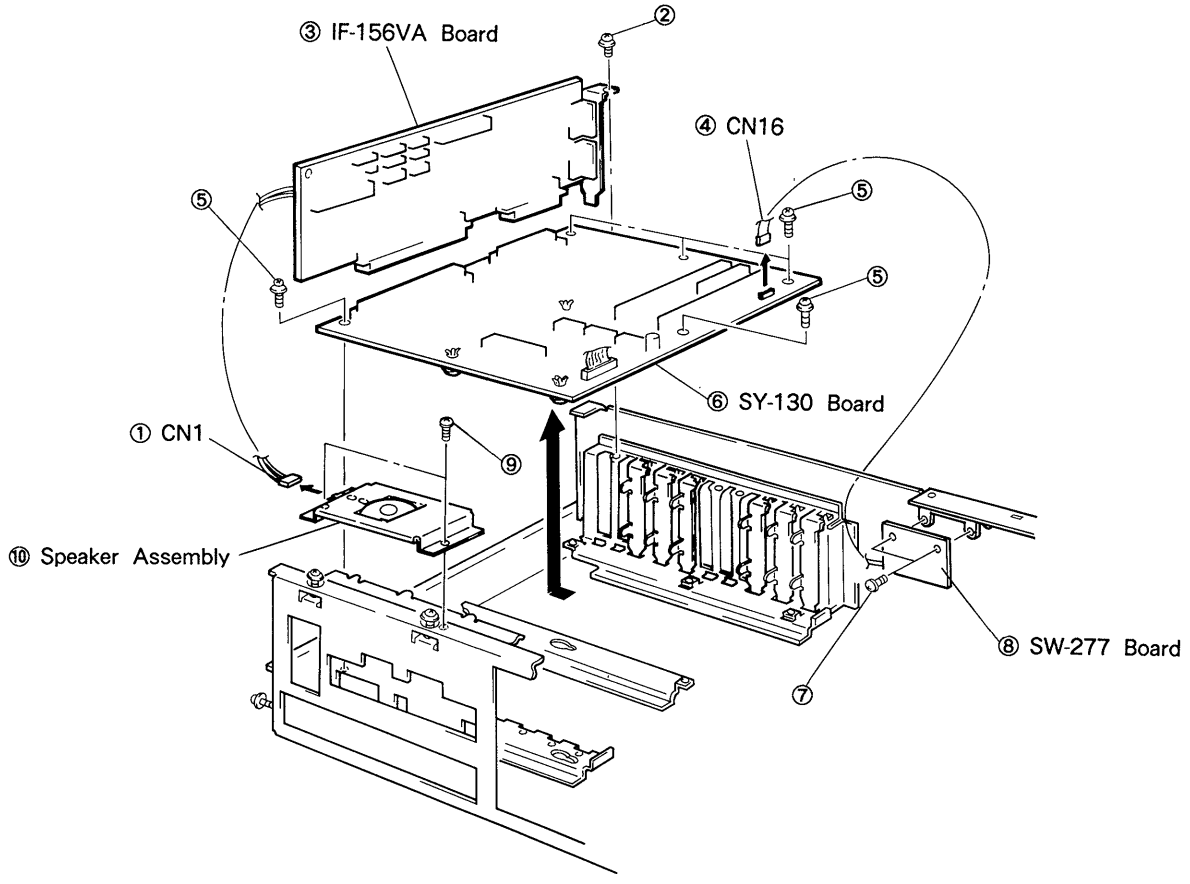


This manner is applicable for additional drives.
Or, refer to the service manual of additional drives.

2-1-11. Power Supply Unit



2-1-10. IF-156VA Board, SY-130 Board, SW-277 Board, and Speaker Assembly



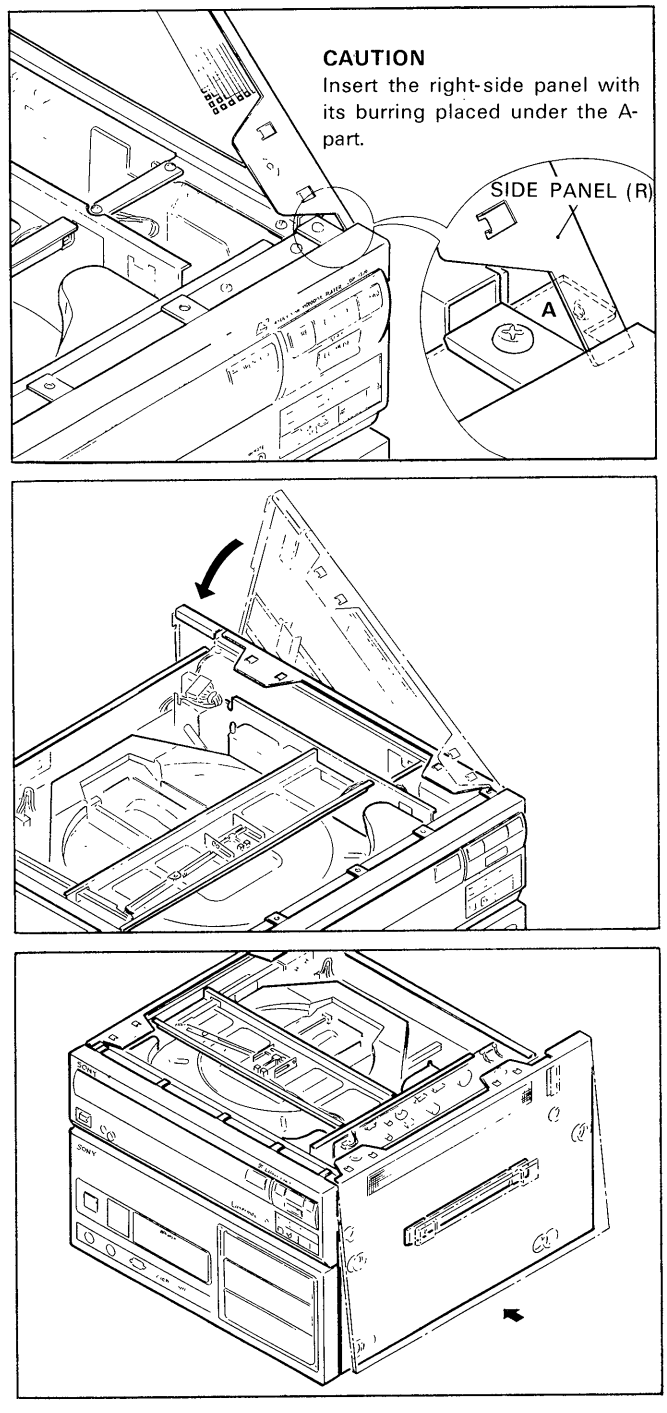
2-2. SERVICE INFORMATION OF VIDEODISC PLAYER

When servicing "videodisc player block" of VIW-3015A, use the LDP-1500 service manual together with this one.
On this VIW-3015A service manual, computer sections are mainly described.

2-3. SERVICE INFORMATION OF VIDEO GRAPHICS ARRAY BOARD

The VGA-16 board is standard equipment for VIW-3015A. When servicing, the board has to be replaced.

2-4. INSTALLING THE RIGHT SIDE PANEL



2-5. REPAIR PARTS

1. Safety Related Components Warning.
   Components identified by shading marked with ⚠ on the schematic diagrams and repair parts list are critical to safe operation. Replace these components with Sony parts whose part numbers appear in this manual or in service bulletins and service manual supplements published by Sony.

2. Replacement Parts supplied from Sony Parts Center will sometimes have a different shape from the original parts. This is due to "accommodating the improved parts and/or engineering changes" or "standardization of genuine parts".
   This manual's repair parts list indicate the parts numbers of "the standardized genuine parts at present".
   Regarding engineering parts changes in our engineering department, refer to Sony service bullentins and service manual supplements.

3. Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.

4. Abbreviations

Ref. No.	Description
C□□, CV□□	CAPACITOR
CN□□	CONNECTOR
CP□□	COMBINATION PARTS
D□□	DIODE
DL□□	DELAY LINE
F□□	FUSE
FL□□	FILTER
IC□□	IC
L□□, LV□□	INDUCTOR
M□□	MOTOR
Q□□	TRANSISTOR
R□□, RV□□	RESISTOR
RB□□	RESISTOR BLOCK
RY□□	RELAY
S□□, SW□□	SWITCH
SB□□	SOLAR BATTERY
T□□	TRANSFORMER
TH□□	THERMISTOR
X□□	CRYSTAL

5. Units for Capacitors, Inductors and Resistors.
   The following units are assumed in schematic diagrams and repair parts list unless otherwise specified:
   Capacitors: μF
   Inductors: μH
   Resistors: ohm

2-6. FIXTURES

J-6093-380-A	EXTENSION BOARD, IF-156
J-6093-490-A	EXTENSION BOARD ASSY (use J-6093-490-1)
J-6093-540-A	EXTENSION BOARD, PU-59
J-6093-570-A	IC EXTRACTION TOOL, 68 PLCC
J-6093-580-A	IC EXTRACTION TOOL, 84 PLCC
J-6200-200-A	KEYTOP EXTRACTION TOOL

CHAPTER 3
THEORY OF OPERATION

3-1. GENERAL DESCRIPTION

On this section, only the microcomputer block is described.

3-1-1. Function of Each Board

Board names and unit names are explained in the alphabetical order.

CP-110 board: KEYBOARD and LIGHT PEN connectors are mounted on this board.

CP-116 board: RS-232C (2) connector at the front panel is mounted on this board.

IF-156VA board: An InterFace board. It contains RS-232C (1) and (2), printer and keyboard interface circuits, as well as PSG (Programmable Sound Generator), timer and RTC (Real Time Clock) circuits.

Keyboard: Based on a bidirectional, clock-synchronized serial communication system.

PU-59VA and RAM-10 boards: A Processor Unit. The PU-59VA board is a computer processor built around a 16-bit CPU. The RAM-10 board has 640K bytes of main system memory. The PU-59VA board has 128K bytes of system ROM.

Switching regulator. Based on a pulse width control system. It has outputs for −12V, −5V, +12V, +5V and PG (Power Good). Upon reception of the P.ON (Power-On $\overline{\text{REMOTE}}$) signal it turns on from a standby state.

SW-198 board: POWER switch and LED for power indicator and hard disk indicator are mounted on this board.

SY-130 board: A SYstem board. There are system buses, video buses and special interface buses, each of which is mounted on this board: It also contains a floppydisk control circuit. A system bus gate circuit is also provided, so that one Sony display board (option) and another display board may be installed in one slot each and operated individually.

VGA-16 board: A Video Graphics Array board. Refer to "IBM Video Graphics Array (VGA) compatible" of Section 1-1-1. This board has Paradise PVGA (Paradise Video Graphics Array), 256K-byte ROM for VGA BIOS, 512K-byte graphics RAM, 6-bit RGB D/A converter with color palette, and 15 pins analog monitor connector. The VIW-3015A, however, contains unused parts. (For details, refer to the chapter 3-6.)

VR-60 board: RESET switch, STARTING DEV select switch, and variable resistor for HUE, COLOR, VOLUME are mounted on this board.

VS-38A board: A Video Superimposer board. Refer to "Superimposition of computer images over videodisc images" of Section 1-1-1. This board has RGB Decoder, 6-bit A/D converters for RGB, Scan converter by 3-FIFO, 2K-byte static RAMs for color palette, 8-bit D/A converters for RGB, 15 pins analog monitor connector, and 2 pieces of gate array.

3-1-2. I/O Map

3-1-2-1. Outline

Since this microcomputer is designed so that it can also use IBM-based computer peripheral functions (optional software/hardware), its I/O addresses are made for use in common.

3-1-2-2. I/O Address Mapping

I/O address	Device
0000H - 001FH	DMA control 1
0020H - 003FH	interrupt control 1
0040H - 005FH	timer
0060H - 006FH	keyboard
0070H - 007FH	RTC; real time clock
0080H - 009FH	DMA page register
00A0H - 00BFH	interrupt control 2
00C0H - 00DFH	DMA control 2
00E0H - 00EFH	reserved
00F0H - 00FFH	arithmetic processor
0100H - 020EH	reserved or not used
020FH	PSG; programmable sound generator
0210H - 02F7H	reserved or not used
02F8H - 02FFH	serial port 2
0300H - 0377H	reserved or not used
0378H - 037FH	parallel port 1
0380H - 03BEH	reserved or not used
03BFH	SONY switch, See 3-3-2.
03C0H - 03CFH	VGA-16 board
03D0H - 03EFH	reserved or not used
03F0H - 03F7H	floppydisk control
03F8H - 03FFH	serial port 2
0400H - FFFFH	reserved or not used
0XXCH - 0XXFH	VS-38A board

"XX" is to be selected out of 25, 26, 28, 29, 33, 34, 35 using the jumper (J001) on the VS-38A board (33 at the time of shipment).

3-1-3. Memory Map

3-1-3-1. Outline

This microcomputer can address 16M bytes of real address space. It incorporates the 16-bit microprocessor 80286.
Addresses exclusively used for the microcomputer are from address 000000H to address 0BFFFFH, from address 0E0000H to address 0FFFFFH, and from address FE0000H to address FFFFFFH. The system ROM is allocated to addresses 0E0000H and up; the code image of the system ROM is allocated to addresses from FE0000H and up; the main memory (system memory) and CG/HG video RAM are allocated to addresses 000000H and up.
The CG/HG video RAM for the VIW-3015A is included in the optional SMI-3085.

3-1-3-2. Memory Address Map

<table>
<tr><td>000000H
09FFFFH</td><td colspan="2">Main memory, 640K bytes</td></tr>
<tr><td>0A0000H
0B7FFFH</td><td>Reserved,
96K bytes</td><td rowspan="2">*HG video RAM
mapping address
128K bytes</td></tr>
<tr><td>0B8000H
0BBFFFH</td><td>*CG video RAM,
16K bytes</td></tr>
<tr><td>0BC000H
0BFFFFH</td><td colspan="2"></td></tr>
<tr><td>0C0000H
0DFFFFH</td><td colspan="2">Reserved
144K bytes</td></tr>
<tr><td>0E0000H
0FFFFFH</td><td colspan="2">System ROM,
128K bytes</td></tr>
<tr><td>100000H
EFFFFFH</td><td colspan="2">Reserved (Expansion memory,
RAM/ROM disk), 14M bytes</td></tr>
<tr><td>F00000H
FDFFFFH</td><td colspan="2">Unused,
896K bytes</td></tr>
<tr><td>FE0000H
FFFFFFH</td><td colspan="2">System ROM code image,
128K bytes</td></tr>
</table>

For the VIW-3015A, the CG/HG video RAM can be used only when the optional SMI-3085 is attached.

3-1-3-3. Main Memory Map

The main memory is placed on the RAM-10 board.

<table>
<tr><td>000000H</td><td>Interrupt vector table</td></tr>
<tr><td>000400H
0006FFH</td><td>Work area</td></tr>
<tr><td>000700H

09F3FFH</td><td>IO. SYS, MS-DOS. SYS,
COMMAND. COM,
Device drivers,
Application programs</td></tr>
<tr><td>09F400H
09FFFFH</td><td>ROM work area</td></tr>
</table>

3-1-3-4. HG Video RAM Map

This section applies only to the SMC-3000VP. Functions discussed here are optional (SMI-3085) for the VIW-3015A.
The HG video RAM (512K bytes) is placed in the HG board (DSC-43V board) and is mapped in units of 64K bytes on the real address space (128K bytes) of the microprocessor 80286 from address 0A0000H to address 0BFFFFH.

Real address	I/O address	Page	HG video RAM
080000H I 08FFFFH	*05B0H	0	64K bytes
		1	64K bytes
090000H I 09FFFFH	*05B1H	2	64K bytes
		3	64K bytes
0A0000H I 0AFFFFH	05B2H	4	64K bytes
		5	64K bytes
0B0000H I 0BFFFFH	05B3H	6	64K bytes
		7	64K bytes

Any particular page is specified by each I/O address.

*; This is usable when the main memory is operated in 512K mode (SMC-2000 mode).

3-1-4. I/O Slots

This microcomputer comes with a total of 10 I/O slots, from Slot A to Slot E and from Slot 1 to Slot 5. These slots are mounted on the SY-130 board.
Slot A is exclusive for the IF (IF-156) board.
Slot B is exclusive for the CPU (PU-59) board.
Slots C, D and E contain video buses and multipurpose 16-bit buses. Video buses are exclusive for Sony display boards, but since these boards are optional (SMI-3085) for the VIW-3015A they can also be used as 8-bit buses in this unit.
Slots 1 and 3 to 5 are used for general-purpose, 16-bit buses (can also be used for 8-bit buses).
Slot 2 can be used for a general-purpose, 8-bit bus.

Slot	SMC-3000VP	VIW-3015A
A	IF-156V board	IF-156VA board
B	PU-59VP board	PU-59VA board
C	DSC-38 board	option
D	DSC-43V or DSC-43VP board	option
E	VS-36 or VS-36P board	option
5	option	VS-38A board
4	option	VGA-16 board
3	option	option
2	option	option
1	option	option

With the DISPLAY BOARD switch (SW-277 Board) on the rear panel the function of the slot can be changed as follows:

DISPLAY BOARD switch	Function
Position A	Normal mode (All slots are active)
Position B	Sony mode (Slot 4 is inactive)
Position C	EGA/VGA mode (Slots C, D, E are inactive)

3-2. PU-59V BOARD AND RAM-10 BOARD

3-2-1. Outline

The PU-59V board, together with the RAM-10 board, called the CPU board.
The system clock (SYSCLK) is 8 MHz.
The PU-59V board contains the following circuits:

- CPU (80286)
- PC/AT compatible set (82C201, 82C202, 82A203, 82A204, 82A205)
- DMA controller (8237A-5), 2 pieces.
- Interrupt controller (8259A), 2 pieces.
- Memory mapper gate array (M60005-0223FP)
- System ROM (27512), 2 pieces.
- 40-pin IC socket for arithmetic processor (80287)

The system clock (SYSCLK) is 8 MHz.
The clock of the arithmetic processor is selected from FAST (SYSCLK) and SLOW (SYSCLK×2/3).
The RAM-10 board contains the following circuits:

- 256K × 1-bit configured D-RAM (MB81256-12), 20 pieces.
- 64K × 4-bit configured D-RAM (MB81464-12), 4 pieces.

Together these constitute a parity bit appended, 640K-byte memory.

3-2-2. Microprocessor IC318

IC318 (80286) is a 16-bit microprocessor having 24-bit address buses and 16-bit data buses. It operates in the following two modes:

- Real-address mode
- Protect mode

The real mode is compatible with the 8086 and can access a 1 M-byte address space with real addresses. In this case, each address is specified by only 20 bits. The protect mode gives the microprocessor 16M bytes of real address space.
Each time a task is performed, the 16M bytes of real address space is mapped to 1 G bytes of virtual address space, so that the microprocessor can operate as if there were 1 G bytes of address space. Furthermore, the microprocessor is provided with a memory management function, protect function and task function to make it capable of handling multi-task/multi-user systems.

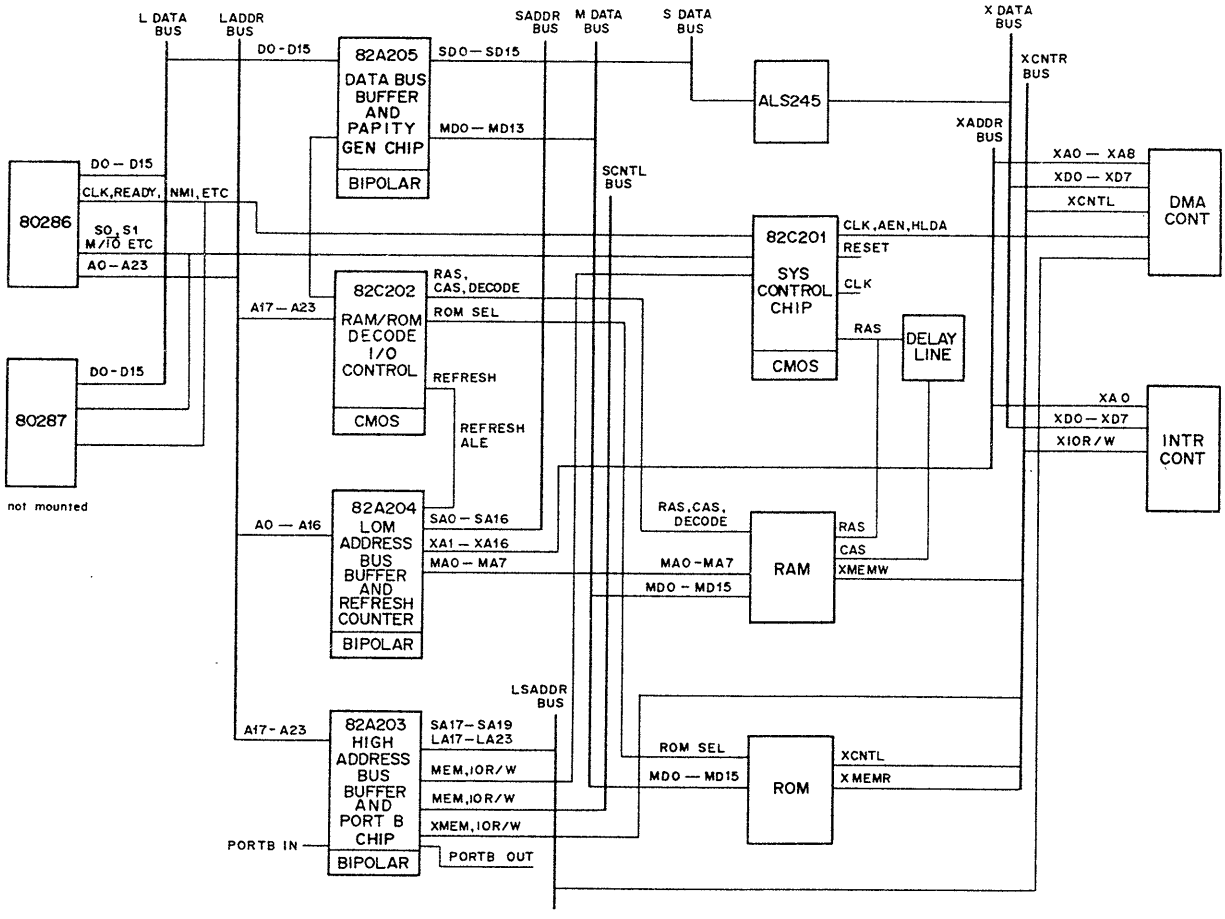


Fig. 3-2-1 PU-59V Board Block Diagram

3-2-3. Clock Generation

The X301 (16 MHz) quartz oscillator and an oscillation circuit in IC323 (82C201) generate a 16 MHz processor clock (PROCCLK). At the same time, the IC323 generates a 8 MHz system clock (SYSCLK) which is synchronized with the T state of the processor, a 4 MHz DMA clock (DMACLK) obtained by halving the frequency of the system clock, and also a 8 MHz peripheral clock (PCLK) obtained by halving the frequency of the processor clock. Furthermore, the X302 (14.31818 MHz) quartz oscillator and an oscillation circuit in the IC323 generate a 14.31818 MHz video clock (OSC), supplied to the system bus, and a 12-frequency-divided 1.19318 MHz clock (OSC/12) which is used for the timer IC226 (8254).

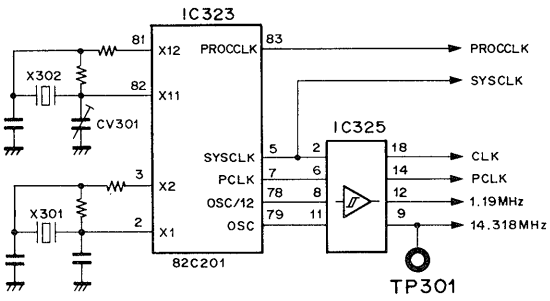


Fig.3-2-3 Clock Generator

3-2-4. PC/AT Compatible Set

This set consists of IC323 (82C201), IC309 (82C202), IC322 (82A203), IC320 (82A204) and IC319 (82A205). Most of the MSI/SSI logic circuits used in the control circuit of IBM PC/AT are integrated into these five LSI chips.

The 82C201 is used to generate various clocks and synchronize the Reset/Ready timing, as well as generate command and control signals, convert data and control wait states, DMA refreshing and the numeric processor, and it also has an NMI error logic function.
The 82C202 is used to decode and latch the ROM/RAM addresses, detect parity errors, and decode the I/O addresses.
The 82A203, located between the local bus and the system bus, is used to buffer high-order addresses (A17-A23), memory read/write signals, and I/O read/write signals, as well as control the buses. It also manages the system control and status port (PORT B).

Port B Status I/O Address Table

I/O Address	Bit	Function
061H	0	timer Ch2 gate speaker (R/W)
	1	speaker data (R/W)
	2	RAM parity check (0=enable) (R/W)
	3	I/O check (0=enable) (R/W)
	4	refresh detect (R)
	5	OUT2 (R)
	6	I/O channel check (R)
	7	parity check (R)

The 82A204 is used to buffer and control between and the control of local address buses (A1-A16), the low-order addresses of the system bus (SA0-SA16), peripheral addresses (XA1-XA16) and memory addresses (MA0-MA7), as well as for generating refresh addresses.
The 82A205 is used to buffer and control between and the control of local data buses (D0-D7), system data buses (SD0-SD15) and memory data buses (MD0-MD15), as well as for generating and checking parity bits.

3-2-5. Memory Mapper Gate Array IC312

IC312 (M60005-0223FP) consists of the SN74LS612 equivalent memory mapper function, as well as the address decoder, data bus controller, etc., which are formed into gate arrays.

3-2-5-1. Address Decoder

Using the $\overline{\text{INTER}}$ signal decoded by the IF-156V board and address signals (XA5-XA8), this device decodes addresses from 0H to FFH at 20H intervals. Decoder outputs are output when the CPUHLDA signal is inactive (low) or when the $\overline{\text{MASTER}}$ signal is active (low).

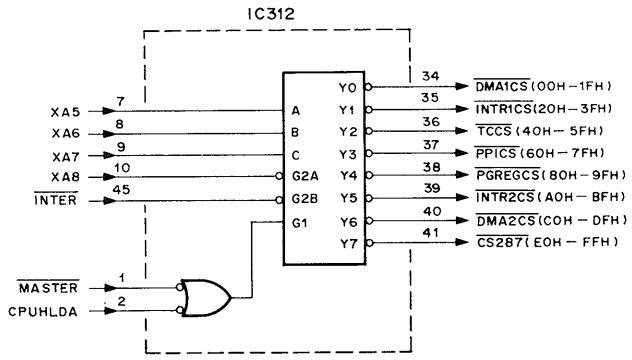


Fig.3-2-5-1 Internal Address Decoder Circuit

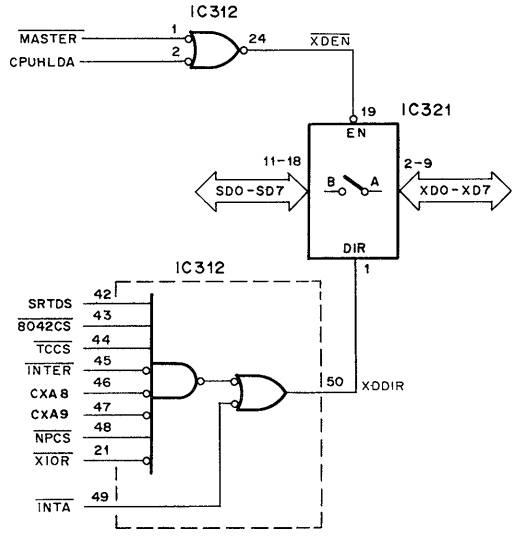


Fig.3-2-5-2 Internal Data Bus Control Circuit

3-2-5-2. Data Bus Controller

See Fig. 3-2-5-2.

This device generates the $\overline{XDEN}$ signal and the XDDIR signal used to control the IC321 (74ALS245), located between the system data buses (SD0-SD7) and peripheral data buses (XD0-XD7).

The $\overline{XDEN}$ signal is used to enable the IC321, which is enabled when the CPUHLDA signal is inactive (low) or when the $\overline{MASTER}$ signal is active (low). (During DMA, the IC is disabled.)

The XDDIN signal controls the direction of data in IC321. When the signal is at high level, data is in the direction from XD to SD; when low, data is in the direction from SD to XD.

The CONT1 (SRTDS), CONT2 ($\overline{8042CS}$) and CONT3 ($\overline{TCCS}$) signals are used to disable the XDDIR signal when access is made to the timer IC226 (8254), keyboard controller IC222 (8742), and real-time clock IC225 (146818) mounted on the IF-156V board. Chip select signals for each device are connected to these control signals. The $\overline{INTER}$ signal is a decode signal (0H-FFH) from the IF-156V board, and the $\overline{NPCS}$ signal is a chip select signal for the arithmetic processor (80287).

3-2-5-3. DMA Page Register

This register is used for the DMA channels to be mapped to the memory page by page during DMA-mode data transfer, and it consists of a SN74LS612 equivalent memory mapper.

Setting of the mapping is performed, when the $\overline{PGREGCS}$ signal is active (low), by reading and writing address data to a page register which is specified by the four low bits (XA0-XA3) of the address. During DMA transfer, page registers are selected by signals $\overline{DACK0}$, $\overline{DACK2}$, $\overline{DACK3}$, $\overline{DACK6}$, $\overline{DACK7}$ and $\overline{HLDADMA2}$ ($\overline{DACK4}$) from the DMA controller (8237A-5) and the $\overline{REF}$ signal, and address information is output to PXA (A16), A17-A19, CA20 and A21-A23. At this time $\overline{PGREGCS}$ is at high level.

Page Register I/O Address Table

Page Register	I/O Address
DMA Ch0	87H
DMA Ch1	83H
DMA Ch2	81H
DMA Ch3	82H
DMA Ch5	8BH
DMA Ch6	89H
DMA Ch7	8AH
Refresh	8FH

During DMA transfer, if 8-bit data is transferred (Ch0-Ch3) addresses A0 through A23 are used, of which A0 to A16 are produced by the DMA controller and A17 to A23 are produced by the page register.

For the transfer of 16-bit data (Ch5-Ch7) A1 through A23 are used, of which A1 to A16 are produced by the DMA controller and A17 to A23 are produced by the page register.

3-2-5-4. External view

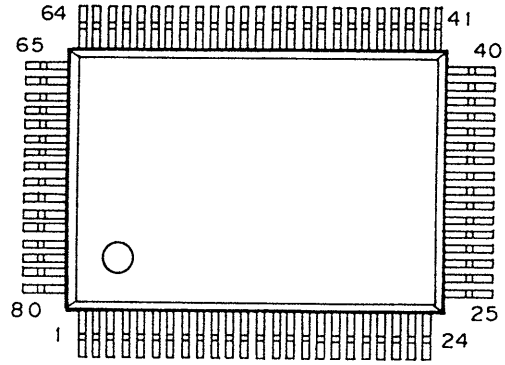


Fig.3-2-5-4 M60005-0223FP Ext. View

3-2-5-5. Pin function table

Pin Function Table 1 of M60005-0223FP

Pin No.	Signal name	I/O	Function
1	$\overline{MASTER}$	I	A Low level indicates that another device on the system bus is active.
2	CPUHLDA	I	Inputs CPU Hold Acknowledge signal. A High level on the CPUHLDA is interpreted as a DMA cycle.
3-11 12, 14-20	XA0 to 16 XD0 to 7	I I/O	Input I/O addresses. Input/output I/O datas (DMA page address).
21	$\overline{XIOR}$	I	Inputs I/O read strobe signal.
23	$\overline{XIOW}$	I	Input I/O write strobe signal.
24	$\overline{XDEN}$	O	Outputs enable signal of XD bus tranceiver (IC321).
25—27 28 29—31 33	A23 to 21 CA20 A19 to 17 PXA (A16)	O O O O	Outputs address (A23 to 16) of DMA page registor.
34	$\overline{DMA1CS}$	O	Outputs chip select signal for DMA controller 1 (IC311).
35	$\overline{INTR1CS}$	O	Outputs chip select signal for interrupte. controller 1 (IC317).
36	$\overline{TCCS}$	O	Outputs chip select signal for timer counter.
37	$\overline{PPICS}$	O	Outputs chip select signal for peripheral interface devices.
38	$\overline{PGREGCS}$	O	Outputs chip select signal for DMA page registor.
39	$\overline{INTR2CS}$	O	Outputs chip select signal for interrupte controller 2 (IC316).
40	$\overline{DMA2CS}$	O	Outputs chip select signal for DMA controller 2 (IC310).
41	$\overline{CS287}$	O	Outputs chip select signal for coprocessor (IC313)

Pin function Table 2 of M60005-0223FP

Pin No.	Signal name	I/O	Function
42—44	CONT1 to 3	I	These are control signal inputs of XDDIR signal (pin 50). Refer to section 3-2-5-2.
45	$\overline{INTER}$	I	Inputs decoded signal of ports 00H to FFH.
46, 47	CXA8 and 9	I	Input XA8 and XA9. These are control signals of XDDIR signal (pin 50).
48	$\overline{NPCS}$	I	This is control signal input of XDDIR signal (pin 50). (same as CONT signal)
49	$\overline{INTA}$	I	Inputs Interrupte Acknowledge signal. This is control signal input of XDDIR signal (pin 50).
50	XDDIR	O	Outputs direction signal of XD bus tranceiver (IC321).
53	$\overline{LCSROM}$	I	Inputs decoded signal of CPU addresses E0000H to FFFFFH.
54	$\overline{ROMCS}$	O	Outputs decoded signal of CPU addresses F0000H to FFFFFH.
58	$\overline{XMRENB}$	O	Enable signal output for the $\overline{MEMR}$ signal generation gate (IC304) during DMA operation.
59	RESET 4	I	Inputs System Reset signal. This is reset of $\overline{XMRENB}$ signal (pin 58)
60	$\overline{MEMRDMA}$	I	Inputs $\overline{MEMR}$ signal of DMA controller (IC310 and IC311).
61	DMACLK	I	Inputs DMA clock. The $\overline{MEMRDMA}$ signal (pin 60) is deplayed for 1 DMA clock pulse, then output from pin 58 ($\overline{XMRENB}$).
63	$\overline{HLDADMA2}$	I	Inputs $\overline{DACK\ 4}$ signal. This is input to select of DMA page registor output.
64	AEN1P	I	Inputs AEN signal of DMA controller 1 (IC311).
65	AEN2P	I	Inputs AEN signal of DMA controller 2 (IC310).
66	AEN	I	Inputs AEN signal of system. This is input to generate $\overline{MHLDA}$ signal.
67	HLDADMA2	O	Outputs inverse pin 63 ($\overline{HLDADMA2}$).
68	$\overline{MHLDA}$	O	Outputs CPU hold acknowlege signal, when MASTER mode.
69, 70	$\overline{AEN\ 1}$	O	A Low level indicates real period of DMA cycle (IC311).
71, 72	$\overline{AEN\ 2}$	O	A Low level indicates real period of DMA cycle (IC310).
74	REF	O	Outputs inverse pin 80 ($\overline{REF}$).
75	$\overline{DACKO}$	I	Inputs $\overline{DACKO}$ signal.
76	$\overline{DACK\ 2}$	I	Inputs $\overline{DACK\ 2}$ signal.
77	$\overline{DACK\ 6}$	I	Inputs $\overline{DACK\ 6}$ signal.
78	$\overline{DACK\ 3}$	I	Inputs $\overline{DACK\ 3}$ signal.
79	$\overline{DACK\ 7}$	I	Inputs $\overline{DACK\ 7}$ signal.
80	$\overline{REF}$	I	Inputs refresh signal.

These are input to select of DMA page registor output.

3-2-6. DMA Controller

IC310 and IC311 are DMA controllers (8237A-5), by cascade connection, which support seven DMA channels.

DMA Channel Table

Controller	Channel	Device
1 IC311	Ch0	SONY I/O
	Ch1	SONY I/O
	Ch2	floppydisk controller
	Ch3	SONY I/O
2 IC310	Ch4	cascade for IC311
	Ch5	SONY I/O
	Ch6	SONY I/O
	Ch7	SONY I/O

The IC311 is assigned channels 0 to 3, and it is used for the transfer of 8-bit data. Each channel can transfer data in units of 64K bytes to and from address space of 16M bytes.
The IC310 is assigned channels 4 to 7, and it is used for the transfer of 16-bit data. Each channel can transfer data in units of 128K bytes to and from address space of 16M bytes. In this case, however, data transfer cannot be performed in the boundary of odd-numbered addresses. Address XA0 is forced to the low level.

DMA controller I/O Address Table

I/O Address		R/W	Function	
IC311	IC310		IC311	IC310
000H	0C0H	R/W	Ch0 address	Ch4 address
001H	0C2H	R/W	Ch0 word counter	Ch4 word counter
002H	0C4H	R/W	Ch1 address	Ch5 address
003H	0C6H	R/W	Ch1 word counter	Ch5 word counter
004H	0C8H	R/W	Ch2 address	Ch6 address
005H	0CAH	R/W	Ch2 word counter	Ch6 word counter
006H	0CCH	R/W	Ch3 address	Ch7 address
007H	0CEH	R/W	Ch3 word counter	Ch7 word counter
008H	0D0H	R	status register	
		W	command register	
009H	0D2H	W	request register	
00AH	0D4H	W	signal mask register	
00BH	0D6H	W	mode register	
00CH	0D8H	W	clear byte register	
00DH	0DAH	R	temporary register	
		W	master clear	
00EH	0DCH	W	clear master register	
00FH	0DEH	W	all mask register	

3-2-7. Interrupt

A total of 16-level system interrupts can be used that include the NMI (nonmaskable interrupt) of the CPU and 15 levels of interrupt obtained by cascade connection of IC316 and IC317 interrupt controllers (8259A). The NMI interrupt request signal includes a parity error signal and an I/O channel check signal.

Interrupt Channel Table

Level	Device	Signal	Function
1	CPU	MMI	Memory parity error and I/O channel error
2	IC317	IRQ0	Timer output 0
3	IC317	IRQ1	Keyboard (output buffer full)
	IC317	IRQ2	IC316 slave interrupt
4	IC316	IRQ8	Real-time clock
5	IC316	IRQ9	Software redirect to INT 0AH (IRQ2)
6	IC316	IRQ10	SONY I/O
7	IC316	IRQ11	SONY I/O
8	IC316	IRQ12	SONY I/O
9	IC316	IRQ13	Coprocessor (80287)
10	IC316	IRQ14	SONY I/O
11	IC316	IRQ15	SONY I/O
12	IC317	IRQ3	RS-232C (COM2)
13	IC317	IRQ4	RS-232C (COM1)
14	IC317	IRQ5	SONY I/O
15	IC317	IRQ6	Floppydisk controller
16	IC317	IRQ7	Printer, light pen, etc.

Interrupt Controller I/O Address Table

I/O Address		R/W	Function*
IC317	IC316		
020H	0A0H	R	IRR, ISR
		W	OCW2, OCW3, ICW1
021H	0A1H	R	IMR
		W	OCW1, ICW2, ICW3, ICW4

*: Please refer to Component Data Catalog of the IC.

3-2-8. Arithmetic Processor IC313

The PU-59V board comes with an optional 40-pin socket for connection of the 80287 arithmetic processor (coprocessor) that expedites numeric operation. The 80287 operates with the same clock as the CPU, and the clock can be selected between FAST, one time the system clock (8 MHz), and SLOW, 2/3 times the system clock.
Although the 80287 arithmetic processor operates in parallel with the CPU, when viewed from the CPU it functions as one of the I/O devices.

Arithmetic Processor I/O Address Table

I/O Address	Function
0F0H	arithmetic processor busy signal clear (R)
0F1H	arithmetic processor reset (R)
0F8H-0FFH	arithmetic processor control (R/W)

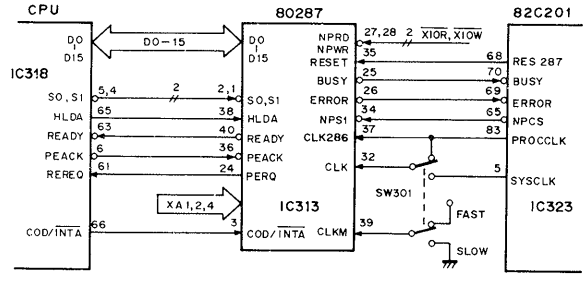


Fig.3-2-8

3-2-9. System ROM

IC314 and IC315 constitute the system ROM (D27512), to which 128K bytes of memory address from address 0E0000H to address 0FFFFFH are allocated.
For the $\overline{CE}$ input of the ROM, the $\overline{LCSROM}$ signal that is decoded by the IC309 (82C202) is used; for the $\overline{OE}$ input, the $\overline{XMEMR}$ signal is used.

3-2-10. Number of Wait Cycles

One bus cycle requires three clock cycles, including one wait. The 8-bit I/O for 8-bit devices requires six clock cycles, including four wait cycles; and the 16-bit I/O for 8-bit devices requires 12 clock cycles, including 10 wait cycles.

3-2-11. Main Memory on RAM-10 Board

The parity bit appended 640K-byte main memory consists of 20 pieces of 256K × 1-bit D-RAM (MB81256-12) and four pieces of 64K × 4-bit D-RAM (MB81464-12), both of which are mounted on the RAM-10 board. Memory addresses are from 0H to 09FFFFH. The refresh cycle is 16.8 μS, which is triggered by channel 1 of the timer IC226 (IF-156V board).

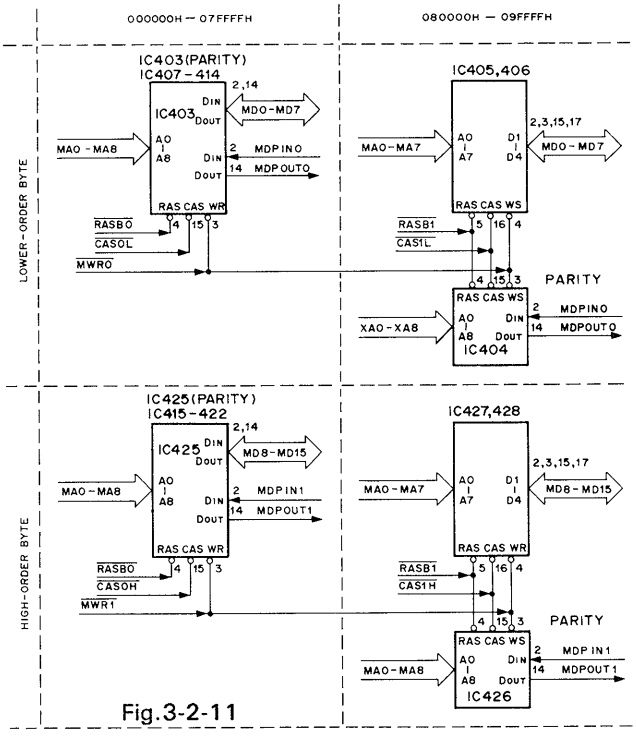


Fig.3-2-11

3-2-12. Memory Control Circuit

The RAS0, 1 signals and the CAS0, 1 signals (latch output) address-decoded by IC309 (82C202) are enabled by the RAS (RAM select) signal generated by IC307 (74F00), DL301 and IC301 (74F10) and the RASENBL and CASENBL signals.

The RAS0 and CAS0 signals select the RAM (low-order bank) in memory addresses of 0H through 07FFFFH. Note, however, that according to the $\overline{XA0}$ and XBHE signals the CAS0 signal selects even-number bytes ($\overline{XA0}$ = "1") or odd-number bytes (XBHE = "1") in the low-order bank.

The RAS1 and CAS1 signals select the RAM (high-order bank) in memory addresses of 080000H through 0AFFFFH. Note, however, that according to the $\overline{XA0}$ and XBHE signals the CAS1 signal selects even-number bytes or odd-number bytes in the high-order bank in the same way as the CAS0 signal.

In the memory addresses A1-A16, after being latched by the ALE signal in the IC320 (82A204), are divided into row addresses and column addresses by the ADDRSEL signal and then sent to the RAM through memory address buses (MA0-MA7).

Also, refresh addresses are generated by a refresh counter in the IC320 and then sent to the RAM through memory address buses.

The IC302 (74F153) is a multiplexer for the memory address line MA8. Because the main memory uses 256K × 1-bit D-RAMs, 18-bit address wires are required. Accordingly, when the memory is accessed $\overline{SA18}$ and $\overline{SA17}$ are output via MA8 to the row and column addresses, respectively, by the ADDRSEL signal.

When the memory is refreshed, because 256 refresh cycles are performed every 4 ms, the required address wires are MA0 to MA7, and MA8 is not used (at this time, MA8 = "0").

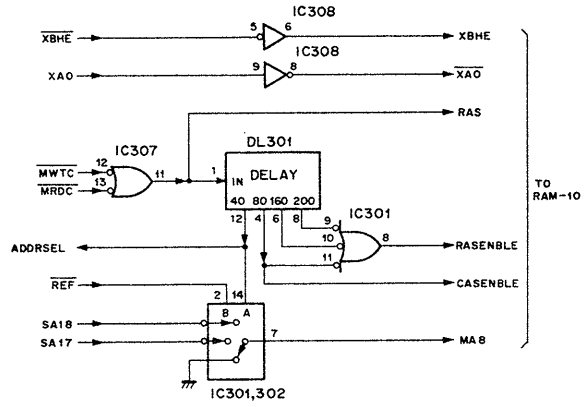


Fig.3-2-12-1

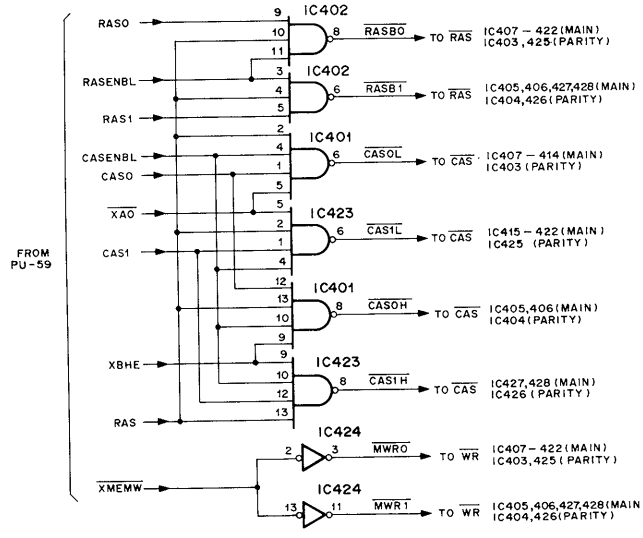


Fig.3-2-12-2

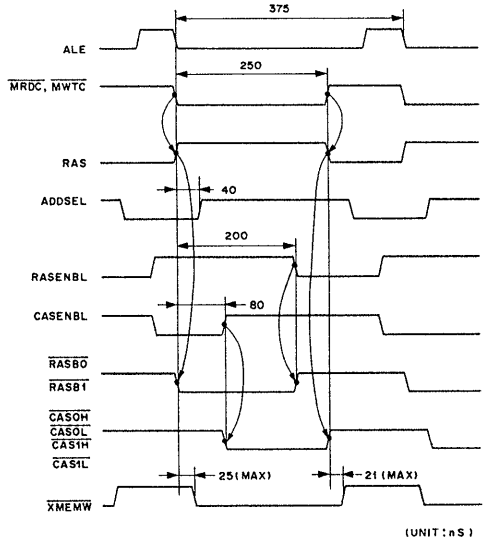


Fig.3-2-12-3

Fig.3-2-12-3 shows the data in 8 MHz system clock (SYSCLK).

3-3. IF-156V BOARD

3-3-1. Outline

The IF-156V board called the IF (Interface) board.
This board contains the following circuits:

- Timer (8254)
- Real-time clock (146818), also called the RTC.
- Keyboard controller (8742)
- Centronics-based printer interface
- Asynchronous RS-232C interface (8250), 2 channels
- Programmable sound generator (SN76489), also called the PSG.
- I/O address decoder (μPD65005G-095-12)
- Audio amplifier

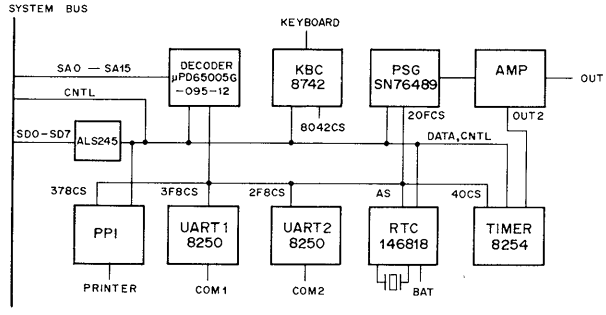


Fig. 3-3-1 IF-156V Board Block Diagram

3-3-2. I/O Address Decoder Gate Array IC233

See fig. 3-3-2.

IC233 (μPD65005G-095-12) is a gate array designed to perform address decoding as its primary function. By decoding address signals (SA0 to SA15) from the system bus, it generates various I/O port signals. As its secondary functions, the device generates I/O read/write control signals ($\overline{ATEN}$, $\overline{SOEN}$, MAEN) using the 3BFH port, as well as clocks (3.6864 MHz) for IC220 PSG (SN76489), and clocks (1.8432 MHz) for IC202 and IC223 (8250) of anynchronous serial communications interface. These clocks are generated by the X202 (3.6864 MHz) quartz oscillator and internal oscillation circuit. The 3BFH port is provided to prevent collision of the IBM-system I/O address in which only 10 low-order bits are decoded with the present system's fully decoded I/O address. This port is called the SONY switch, and it is switched over by data in bit 0.

When the power is turned on, the SONY switch is in the OFF state.

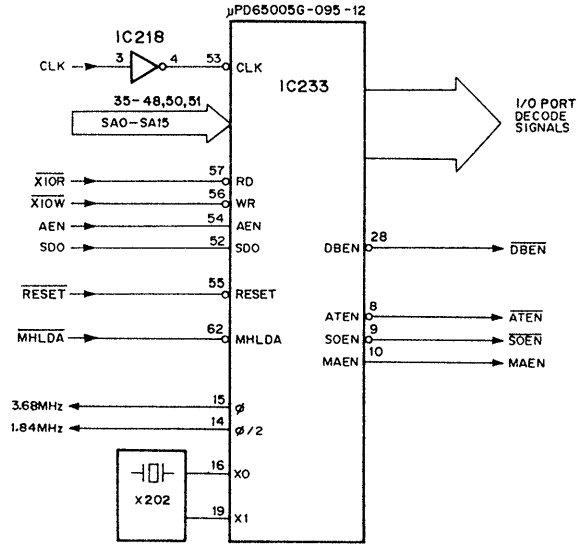


Fig.3-3-2-1

When accessing I/O adresses 0000H through 7FFFH the signals $\overline{ATEN}$ and $\overline{SOEN}$ both become low active, irrespective of te SONY switch setting.

I/O Address 8000H – FFFFH

SONY switch	$\overline{ATEN}$	$\overline{SOEN}$
"1" ON	Low	Low
"0" OFF	Low	Low

When accessing I/O adresses 8000H through FFFFH the signals $\overline{ATEN}$ and $\overline{SOEN}$ will be as shown below, depending on the SONY switch setting.

I/O Address 0000H – 7FFFH

SONY switch	$\overline{ATEN}$	$\overline{SOEN}$
"1" ON	High	Low
"0" OFF	Low	High

I/O read/write signals are changed by the $\overline{ATEN}$ and $\overline{SOEN}$ signals as described in section 3-3-3.

I/O Address Decoder (μPD65005G-095-12)
Pin Function Table

Pin No.	Signal name	I/O	Function
3	$\overline{378CS}$	O	decoded signal of 378H to 37FH (printer interface)
4	$\overline{20FCS}$	O	decoded signal of 20FH (PSG interface)
5	$\overline{6FCS}$	O	not used (decoded signal of 060H to 06FH)
6	$\overline{IOCS}$	O	decoded signal of 060H to 06FH, 20FH, 2F8 to 2FFH, and 378H to 37FH (data bus control)
7	$\overline{INTER}$	O	decoded signal of 000H to 0FFH (CPU board I/O interface)
8	$\overline{ATEN}$	O	IBM PC/AT mode enable
9	$\overline{SOEN}$	O	SONY mode enable
10	MAEN	O	master mode enable
11	$\overline{DOSTR}$	O	not used (COM1 write strobe)
12	$\overline{DISTR}$	O	not used (COM1 read strobe)
13	$\overline{3F8CS}$	O	decoded signal of 3F8H to 3FFH (COM1 interface)
14	$\phi/2$	O	1.8432MHz (for COM1 and COM2 clock)
15	ϕ	O	3.6864MHz (PSG clock)
16	X0	I	oscillator input (X202)
19	X1	O	oscillator output (X202)
20	RTCAS	O	RTC address strobe
21	$\overline{RTCWR}$	O	RTC data write strobe
22	$\overline{RTCDS}$	O	RTC data read strobe
23	RTCCS	O	decoded signal of 070H to 07FH (RTC interface)
24	$\overline{XRD}$	O	not used
25	$\overline{XWR}$	O	not used
26,58	GND		0V
27	VDD		+5V
28	$\overline{DBEN}$	O	**data bus enable (timer, RTC, floppy-disk drive, COM1)**
29	$\overline{40CS}$	O	decoded signal of 040H to 05FH (timer interface)
30	$\overline{3D0CS}$	O	decoded signal of 3D0H to 3DFH
31	$\overline{500CS}$	O	decoded signal of 500H to 51FH
32	$\overline{3F0CS}$	O	decoded signal of 3F0H to 3F7H (floppydisk drive interface)
35—48	A0—A13	I	system bus address (SA0—SA13)
50,51	A14,A15	I	system bus address (SA14, SA15)
52	SD0	I	**input data of part 3BFH**
53	$\overline{CLK}$	I	system clock
54	AEN	I	address enable (CPU board)
55	$\overline{RESET}$	I	reset drive
56	$\overline{IOW}$	I	I/O write signal (CPU board)
57	$\overline{IOR}$	I	I/O read signal (CPU board)
59	$\overline{60CS}$	O	not used (decoded signal of 060H)
60	$\overline{61CS}$	O	decoded signal of 061H (data buffer disable)
61	$\overline{62CS}$	O	not used (decoded signal of 062H)
62	$\overline{MHLDA}$	I	HLDA under master mode (CPU board)
63	$\overline{2F8CS}$	O	decoded signal of 2F8H to 2FFH (COM2 interface)

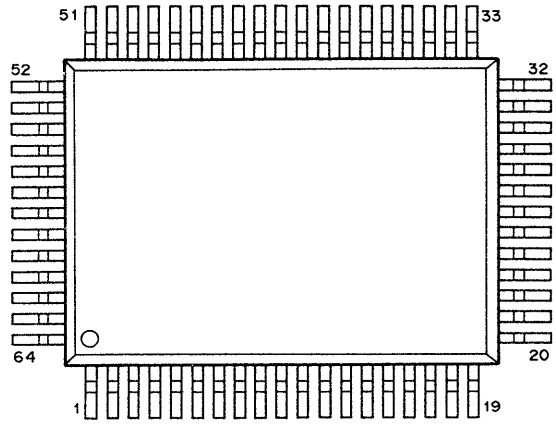


Fig.3-3-2-2 μPD65005G-095-12 Ext.View

3-3-3. I/O Read/Write Control

See fig. 3-3-3.
The $\overline{IOR}$ signal and the $\overline{IOW}$ signal from the CPU board are controlled by the $\overline{ATEN}$ signal and the $\overline{SOEN}$ signal.
When the $\overline{ATEN}$ signal is active (low), the $\overline{AIOR}$ signal and the $\overline{AIOW}$ signal of the system bus are enabled. When the $\overline{SOEN}$ signal is active (low), the $\overline{SIOR}$ signal and the $\overline{SIOW}$ signal of the video bus are enabled.

The MAEN signal is a signal that indicates HLDA when the system is put into master mode operation by the $\overline{MASTER}$ signal of the system bus, and it is used to switch the directions of the $\overline{AIOR}$ and $\overline{AIOW}$ signals of the system bus. It is designed for use with SMI-3038 (LAN controller board), etc.

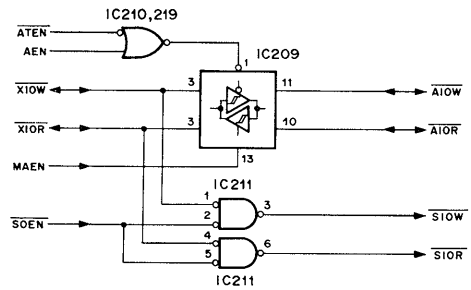


Fig. 3-3-3

3-3-4. Timer IC226

IC226 (8254) is a 3-channel programmable timer, all three channels of which are driven by the 1.19318 MHz clock from the CPU board. The clock observable with TP206.

Channel	Function
0	timer interrupt (every approx. 54.9 mS period)
1	memory refresh interrupt (every approx. 16.8μS period)
2	beep sound generation

Timer I/O Address Table

I/O Address	bit	Function
040H	0—7	counter 0 data (R/W)
041H	0—7	counter 1 data (R/W)
042H	0—7	counter 2 data (R/W)
043H		control word register (W)
	0	count binary/decimal
	1—3	mode specify
	4, 5	number of counter load
	6, 7	counter specify

3-3-5. Real Time Clock (RTC) IC225

See fig. 3-3-5.

IC225 (146818) comes with clock and calendar functions to indicate the year, month and date, as well as days of the week and time, and it has a built-in 50-byte user RAM.

The device uses a 32.768 kHz quartz oscillator for the clock, and for interrupt it outputs IRQ8 signals via IC216 (74LS04). It is protected against power outage by a NiCd rechargeable battery, which is mounted on the SY-130 board, and it has a nominal voltage of 3.6V. The battery is recharged by a trickle charging method.

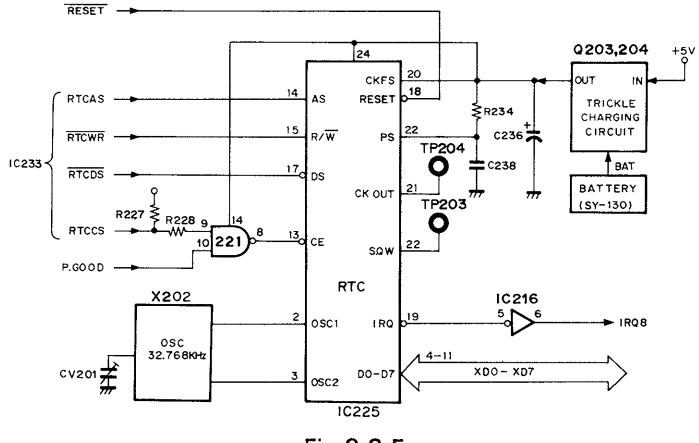


Fig.3-3-5.

Real Time Clock I/O Address Table

I/O Address	Bit	Function
070H	0—6	RTC address specify (W)
071H	0—7	data (R/W)

3-3-6. Keyboard Controller IC222

IC222 (8742) is a keyboard controller with a single-chip microcomputer, and it functions to control the keyboard and generate A20 gate signals.

The keyboard controller has two 8-bit input/output ports and two test inputs. P10-P17 are the input ports and P20-P27 are the output ports. The test inputs are connected, respectively, to the clock and data from the keyboard.

Input Port Table

Bit	Definition
0—3	unfixed
4	fixed to high (second 256K-byte RAM switch)
5	fixed to high (manufacturing jumper)
6	fixed to high (display type switch)
7	fixed to high (keyboard inhibit switch)

Output Port Table

Bit	Definition
0	system reset
1	gate A20
2, 3	unfixed
4	output buffer full
5	unused
6	keyboard clock, output
7	keyboard data, input

Furthermore, it has an 8-bit status register (I/O address 64H) to report keyboard status, as an 8-bit output buffer to return scan codes and the execution results of commands, and an 8-bit input buffer used for commands and command data to be set.

Keyboard Controller I/O Address Table

I/O Address	Bit	Function
060H	0—7	I/O buffer (R/W)
064H		status register (R)
	0	output buffer full
	1	input buffer full
	2	system flag
	3	command or data
	4	inhibit
	5	transmit time out
	6	receive time out
	7	parity error
	0—7	command register (W)

Access to the input/output ports is accomplished via the input/output buffers of the I/O address 60H by outputting commands to the I/O address 64H.

3-3-7. Printer Interface

See fig. 3-3-7.
This interface consists of Centronics-based 8-bit input/output ports, through which data is transferred at the TTL level. The connector is a 25-pin D-sub connector (CN201) which has various signal wires to indicate the paper end (PE), paper feed control (AUTO FD) and on-line/off-line (SLCT IN) status, in addition to control signals such as ACK, BUSY and STROBE. On the basis of the 378CS signal from the I/O address decoder IC233, it decodes I/O addresses from 378H to 37BH with IC235 (74LS155). I/O addresses from 378H to 37AH are used with the printer interface.
Port 37BH is the status port. See section 3-3-9.
The interrupt signal IRQ7 is generated from the ACK signal form the printer via IC234 (74LS125) and IC238 (74LS04). The interrupt can be masked by '0''of bit 4 in port 37AH.

Printer Interface I/O Address Table

I/O Address	Bit	Function
378H, 37CH	0—7	data (R/W)
379H, 37DH		status 1 (R)
	3	0 = error
	4	1 = select
	5	1 = paper end
	6	1 = acknowledge
	7	0 = busy
		data mode (W)
	7	input/output
37AH, 37EH		status 2 (R), command (W)
	0	1 = strobe
	1	1 = auto feed
	2	0 = printer initializing
	3	1 = printer select
	4	1 = INT enable

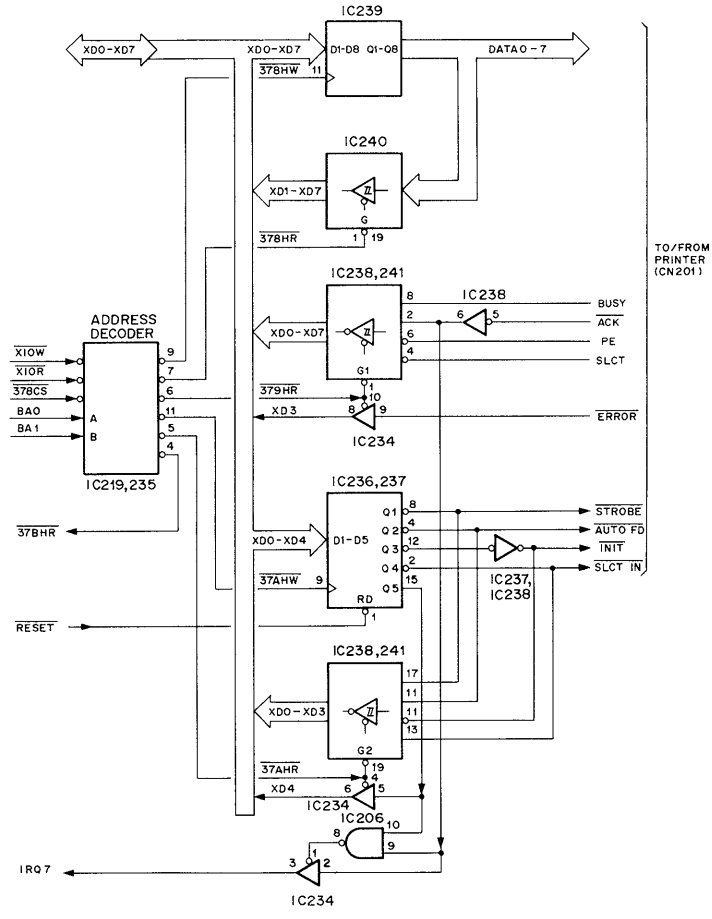


Fig.3-3-7 Printer Interface

3-3-8. Serial Interface COM1 and COM2

IC202 and IC223 are asynchronous serial communications ICs (8250). IC223 is assigned to COM1 and IC202 is assigned to COM2.

The 8250 comes with a baud rate generator so it can respond to various formats with regard to the data length, parity and stop bit. It uses a 1.8432 MHz clock generated in the I/O address decoder IC233. Interrupt signals from COM1 and COM2 are connected, respectively, to IRQ4 and IRQ3 via IC203. COM2 can be disabled by JP201.
The connector for COM1 is located on the IF-156V board (CN202), whereas the connector for COM2 is mounted on the front panel.

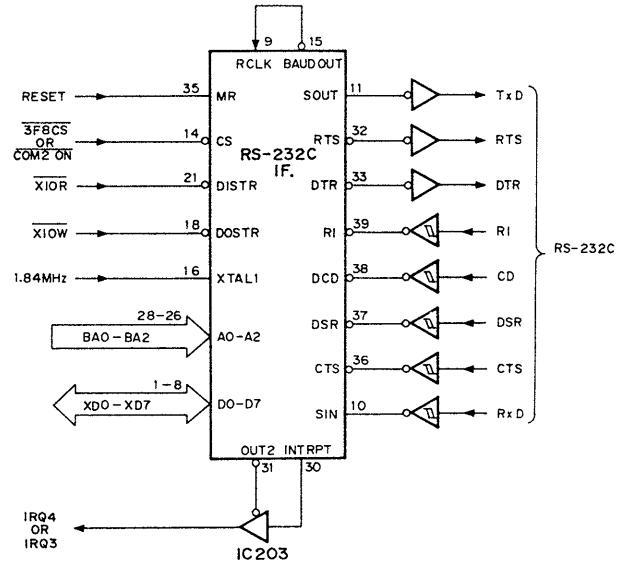


Fig.3-3-8

Serial Interface I/O Address Table

I/O Address		Bit	Function
COM1	COM2		
3F8H	2F8H	0—7	(DLAB=0) receiver buffer register (R)
		0—7	(DLAB=0) transmitter holding register (W)
		0—7	(DLAB=1) divisor latch data LSB (R/W)
3F9H	2F9H		(DLAB=0) interrupt enable register (W)
		0	enable received data available interrupt
		1	enable transmitter holding register empty interrupt
		2	enable receiver line status interrupt
		3	enable modem status interrupt
		0—7	(DLAB=1) divisor latch data MSB (R/W)
3FAH	2FAH		interrupt identification register (R)
		0	interrupt pending=0
		1	interrupt ID bit (0)
		2	interrupt ID bit (1)
3FBH	2FBH		line control register (R/W)
		0	word length select bit 0
		1	word length select bit 1
		2	number of stop bits
		3	parity enable
		4	even parity select
		5	stick parity
		6	set break
		7	divisor latch access bit (DLAB)
3FCH	2FCH		modem control register (R/W)
		0	data terminal ready (DTR)
		1	request to send (RTS)
		2	output 1
		3	output 2
		4	loop
3FDH	2FDH		line status register (R)
		0	data ready
		1	overrun error
		2	parity error
		3	framing error
		4	break interrupt
		5	transmitter holding register empty
		6	transmitter empty
3FEH	2FEH		modem status register (R)
		0	delta clear to send
		1	delta data set ready
		2	trailing edge of ring indicator
		3	delta data carrier detect
		4	clear to send (CTS)
		5	data set ready (DSR)
		6	ring indicator (RI)
		7	data carrier detect (DCD)
3FFH	2FFH	0—7	scratch pad register data (R/W)

3-3-9. Status Port

IC204 (SN74LS244) is an 8-bit status port, and it can read information on the setting of SW201 (4-bit DIP switch) from I/O address 37BH. The SW201 is connected to bit 2 through bit 5 of the I/O address 37BH.
The gate signal of the IC204 is produced by IC235 (74LS155). The setting of the SW201 when shipped from the factory is ON, OFF, OFF and ON from bit 2.

Status I/O Address Table

I/O Address	Bit	Read function
37BH	0,1	starting device select*
	2	1 = terminal output to COM1
	3	1 = video system board and high-resolution graphics board are mounted
	4	1 = keyboard is connected
	5	1 = reserved
	6	sound status
	7	fixed to low

*; Starting Device Select

Bit 0	Bit 1	Starting device
0	0	floppydisk
0	1	hard disk
1	1	videodisc

ST-1 is bit 0.
ST-2 is bit 1.

(Switching is performed by S101 on VR-60 board.)

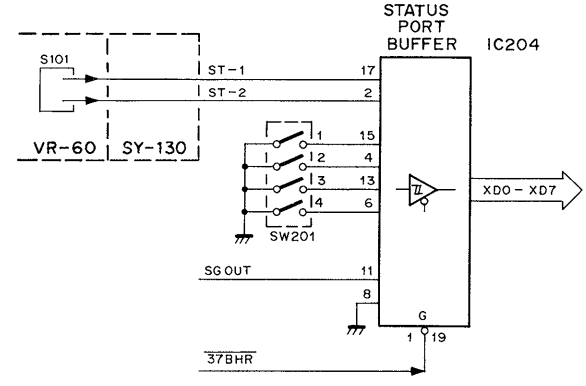


Fig.3-3-9

3-3-10. Muting Circuit

Q201, 202 and 205 are the muting transistors provided to prevent the generation of indeterminate sounds from the PSG when the power is turned on, or system reset (because the PSG does not have a reset terminal).
The P.GOOD signal from the switching regulated power supply or the $\overline{\text{RES SW}}$ signal from RESET switch on the VR-60 board is used as the muting signal.

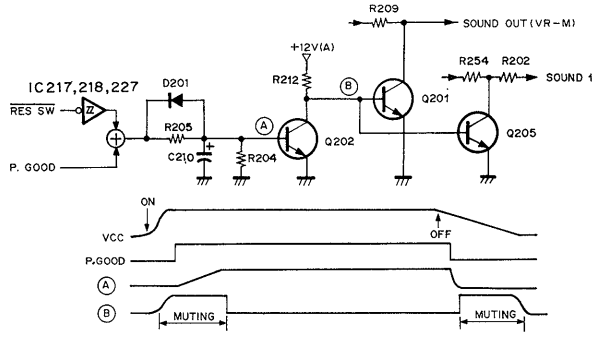


Fig.3-3-10

3-3-11. Data Bus Buffer IC242

IC242 (74ALS245) is a data bus buffer of the IF-156V board. Data flow is switched by the $\overline{\text{AIOR}}$ signal. When the $\overline{\text{AIOR}}$ signal is active (low), data is transferred from XD to SD; when the signal is inactive (high), data is transferred from SD to XD.
The Enable signal of the IC242 is produced by IC231 (74ALS11) and IC232 (74LS32) in such a way that it becomes active (low) when data is read or written to peripheral devices mounted on the IF-156V board.

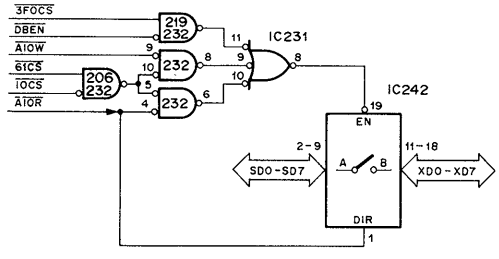


Fig.3-3-11

3-3-12. Programmable Sound Generator (PSG)

IC220 is PSG (SN76489), which outputs a sound with the frequency and sound volume as set to it.
The output of PSG is combined with output (OUT2) from the timer IC226 (8254).
And then, past the IC207 (2/2) (4558). is output from the IC207 (1/2) to the video bus (SOUND1). A muting circuit is provided for the outputs of IC207, (1/2) and (2/2).
IC201 (LM386) is the speaker amplifier. This IC is only mounted to the IF-156VA board of VIW-3015A, and the speaker is only incorporated to VIW-3015A.

PSG I/O Address Table

I/O Address	Bit	Function
20FH	0-7	data (W)
	0	system reset status (R)
	6	ready (R)

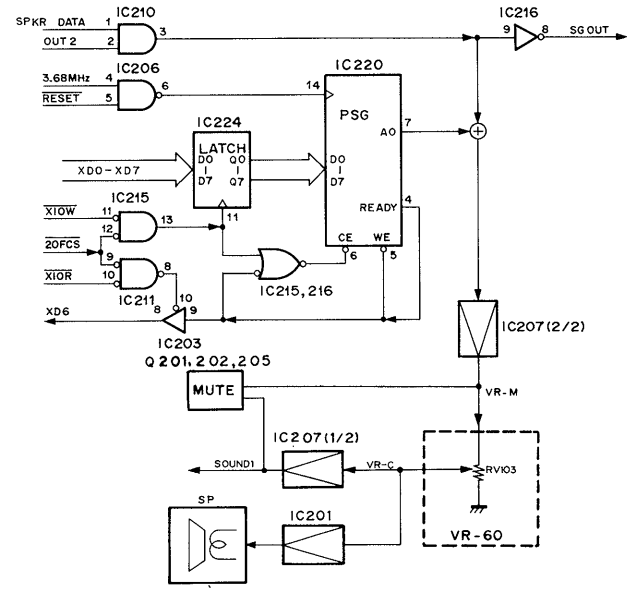


Fig.3-3-12-1

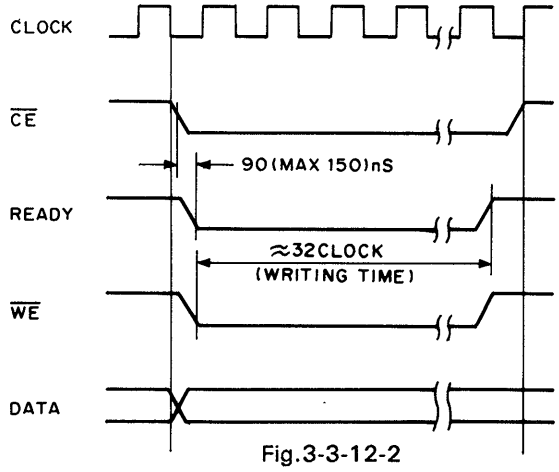


Fig.3-3-12-2

3-4. SY-130 BOARD

3-4-1. Outline of SY-130 Board

The SY-130 board is a mother board which functionally connects the boards in other slots. (Refer to Section 3-1-4.)
Also on this board, there is a floppydisk control circuit, back-up battery for RTC (IF-156V board), and gate circuit for selecting display board. The SY-130 board called the SY (System) board.

3-4-2. Outline of Floppydisk Control Circuit

This circuit is comprised of floppydisk controller (FDC), VFO (data separator), gate array, floppydiskk drive (FDD) interface buffer etc. This circuit is capable of controlling two internal FDDs. The data transmission speed of this circuit is capable of handling 125, 150, and 250Kbps FDD with the FM (single density) recording method, and 250, 300, and 500Kbps FDD with the MFM (double density) record method.
However, if the jumper wires settings on the SY-130 board are not changed, it cannot handle FDD having other than the same type interface (IBM AT compatible) as the standard installed FDD*1.
The FDD interface of the SMC-3000VP or the VIW-3015A is as follows.

Pin	Signal name	Pin	Signal name
1	NC	2	2HD/$\overline{2DD}$ *2
3	RETURN	4	$\overline{IN\ USE}$ *2
5	RETURN	6	NC
7	RETURN	8	$\overline{INDEX}$
9	RETURN	10	$\overline{DRIVE\ SEL\ A}$
11	RETURN	12	$\overline{DRIVE\ SEL\ B}$
13	RETURN	14	NC
15	RETURN	16	$\overline{MOTOR\ ON}$
17	RETURN	18	$\overline{DIR}$
19	RETURN	20	$\overline{STEP}$
21	RETURN	22	$\overline{WRITE\ DATA}$
23	RETURN	24	$\overline{WRITE\ GATE}$
25	RETURN	26	$\overline{TRACK\ 0}$
27	RETURN	28	$\overline{WRITE\ PROT}$
29	RETURN	30	$\overline{READ\ DATA}$
31	RETURN	32	$\overline{HEAD\ SEL}$
33	RETURN	34	$\overline{DSK\ CHG}$

*1: The standard installed FDD in the SMC-3000VP, VIW-3015A, and SMI-3014 (option) FDD unit is MFD-73W-51D (MP-F73W-51D).
*2: 5.25-inch FDD made by some manufacturers can use this signal. It cannot be used with any 3.5-inch FDDs.

3-4-3. I/O Port

1. Port 3F2H Write

Bit No.	Function
0,1	drive select*
2	"0" = FDC reset
3	"1"=interrupte request and DMA request signal enable
4	"1"=drive-A motor on
5	"1"=drive-B motor on
6	"1"=drive-C motor on
7	"1"=drive-D motor on

* : Drive Select

Bit 0	Bit 1	Drive name
0	0	A
1	0	B
0	1	C
1	1	D

2. Port 3F4H Read (FDC main status register)

Bit No.	Function
0-3	unused
4	FDC busy
5	non-DMA mode
6	data input/output
7	master request

3. Port 3F4H Write (FDC control)
standby control
software reset

4. 3F5H Port (FDC data register)
Read : data or status
Write : command or data

5. Port 3F7H Read

Bit No.	Function
0-6	unused
7	floppydisk change

6. Port 3F7H Write (floppydisk control register)

Bit No.	Function
0,1	data transfer rates select*
2-7	unused

* : Data Transfer Rates Select

Bit 1	Bit 0	Data transfer rates
0	0	500K bps (MFM)
1	0	300K bps (MFM)
0	1	250K bps (MFM, defult)

3-4-4. Gate Array IC3

The FDC, VFO, and FDD are controlled from the system bus by the gate array IC3 (μPD65005G-126-12).
Refer to Fig. 3-4-16 of page 26 for the dimension.

Terminal Functions of μPD65005G-126-12

Terminal No.	I/O	Terminal name	Explanation/connection
1,2	—	NC	No connection.
3	O	DSC	Drive select C output.
4	O	DSD	Drive select D output.
5	O	MONC	Motor-on C output.
6	O	MONC	Motor-on D output.
7	I	DCHC	Disk change C input.
8	O	NFCR	(Used for FDD of SONY interface). Outputs a disk change reset signal to drives A and B.
9	I	DCHA	Disk change A or B input.
10	O	HDD	Outputs a drive density switching signal (High/$\overline{\text{Normal}}$). When the data rate is 500Kbps, high; when 250Kbps, low.
11	O	DSA	Drive select A output.
12	O	DSB	Drive select B output.
13	O	MONA	Outputs OR of motor-on A and motor-on B.
14	O	NDIR	Direction signal output.
15	O	NSTP	Step-seek signal output.
16	O	NWDT	Write data output.
17,18	—	NC	No connection.
19	O	NWGT	Write gata output.
20	I	ITRK	Track 0 signal input.
21	I	IWPT	Write protect signal input.
22	I	RC	Used for the circuit to prevent from writing by mistake to FDD when the power is on.
23	I	WE	Write enable signal input.
24	I	IWDT	Write data input.
25	I	ISTP	Fault reset or step-seek signals input.
26	—	GND	0V.
27	—	V_{DD}	+5V.
28	I	SEEK	Mode signal input, $\overline{\text{RW}}$/SEEK.
29	I	IDIR	Direction signal input.
30	O	MIST	FDD select signal output, mini/$\overline{\text{standard}}$.
31	O	FDSW	FDD type select signal output.
32	O	ORST	FDC reset signal output.
33,34	—	NC	No connection.
35	O	NCS	FDC chip select signal output, ports 3F4H and 3F5H.
36	O	NODK	$\overline{\text{DACK}}$ signal (pin 46) gate output.
37	O	OTC	TC signal (pin 41) gate output.
38	I	ICLK	Clock input, 4 or 8MHz.
39	O	OWPT	Write protect signal output.
40	O	OTRK	Track 0 signal output.
41	I	ITC	Terminal count (T/C) signal input.
42	I	NRS	System reset signal input.
43	I	N3FO	Ports 3F0H to 3F7H decoded signal ($\overline{\text{3FOCS}}$) input.
44	I	NIOW	I/O write strobe signal ($\overline{\text{AIOW}}$) input.
45	I	NIOR	I/O read strobe signal ($\overline{\text{AIOR}}$) input.
46	I	NIDK	DMA acknowledge signal (DACK2) input.
47	I	ISA2	System bus address line 2 input.
48	I	ISA1	System bus address line 1 input.
49	—	NC	No connection.
50	I	ISA0	System bus address line 0 input.
51	O	ODCH	Disk change signal output.
52	O	NDEN	Becomes low when port 3F7H is read.
53	O	NIEN	Enable interrupt signal request signal and DMA request.
54	I	ID0	System bus data line 0 input.
55	I	ID1	System bus data line 1 input.
56	I	ID2	System bus data line 2 input.
57	I	ID3	System bus data line 3 input.
58	—	GND	0V.
59	I	ID4	System bus data line 4 input.
60	I	ID5	System bus data line 5 input.
61	I	ID6	System bus data line 6 input.
62	I	ID7	System bus data line 7 input.
63	O	NOG	Data bus buffer enable signal.
64	—	NC	No connection.

The main functions are as follows.

(1) Decoder section
The latch signal for the various registers in the gate array, FDC chip select signal, data buffer gate signal for the system bus, etc., are created by the three address signals (ISA0 to ISA2) and the $\overline{\text{3FOCS}}$ signal decoded by the IF-156V.

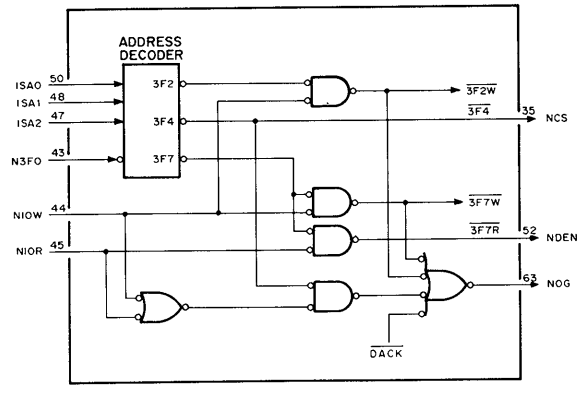


Fig. 3-4-1.

(2) Register 1 (Digital Output Register)
This is an 8-bit register which enables the FDD select signal, motor ON signal, and system bus INT and DRQ signals by writing to the port 3F2H.

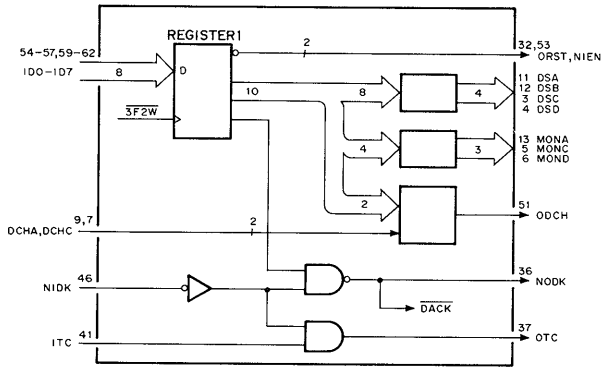


Fig. 3-4-2.

(3) Register 2 (Floppydisk Control Register)
This is a 2-bit register for designating the VFO data transmission speed by writing to the port 3F7H.

Register (2)		Gate array output			Data transfer rates (bps)
Bit 1	Bit 2	FDSW	MIST	HDD	
0	0	0	0	1	500K
0	1	0	1	0	300K
1	0	1	1	0	250K

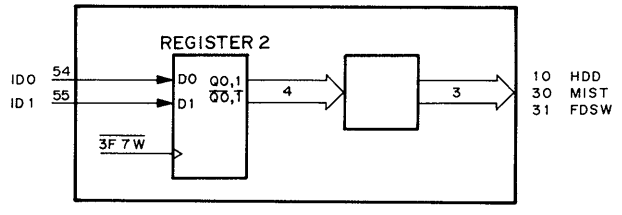


Fig. 3-4-3.

(4) Delay, write error prevention circuit
The FDC write data signal is delayed to match the timing of the FDD interface (IBM specifications). There is also a gate which prevents writing errors to the FDD when the power is turned ON.

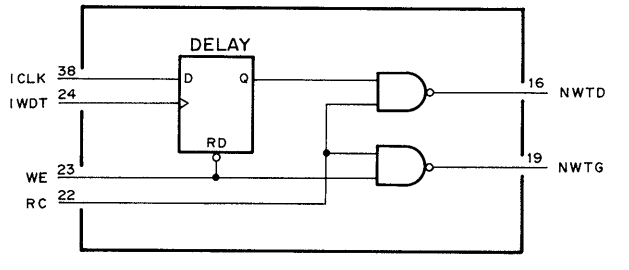


Fig. 3-4-4.

(5) Gate circuit
Controls the direction (DIR) signal, step (STEP) signal sent to the FDD from the FDC, and track 0 (TRACK 0) signal and write protect (WRITE PROT) signal sent to the FDC from the FDD by the SEEK/$\overline{RW}$ signal from the FDC (indicates FDD reading/writing and seek).
The NFCR output is a disk change reset (fault clear) signal for FDD with Sony interface. It is not connected (JW16) as it is not used by the IBM specification FDD which is installed as standard.

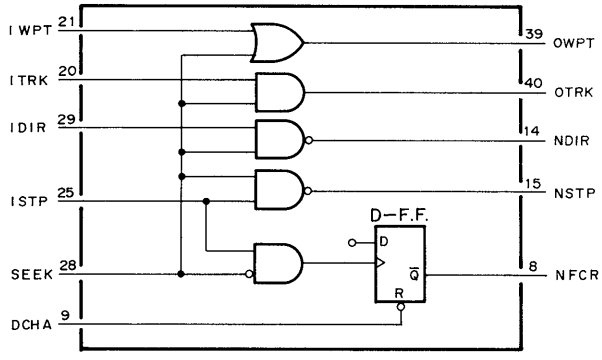


Fig. 3-4-5.

3-4-5. FDC IC4

FDC μPD72065C (IC4) is a floppydisk controller for the IBM track format.
The FDC is located at ports 3F4H and 3F5H.
The chip select signal is decoded in the IC3 gate array.
The FDC reset signal is output by setting bit 2 of the port 3F2H to "0".
The DRQ and INT signals are enabled by setting bit 3 of the port 3F2H "1", and are output to the system bus through IC9 (74LS125).

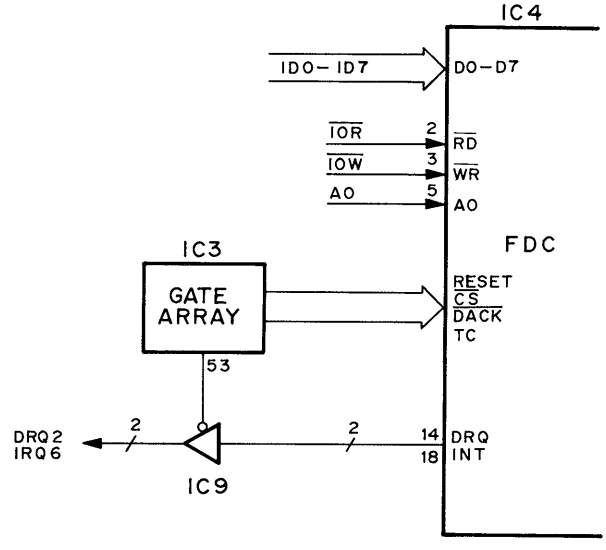


Fig. 3-4-6.

The following is a description of the pin functions of the μPD72065C.

Terminal Functions of μPD72065C

Terminal name	I/O	Function	State when reset
RESET	I	Reset Puts FDC into idle state. • Drive interface outputs are made to low, except for WDATA (indeterminate). • On the main system side, INT DRQ is made to low, while DB7 to DB0 are changed to input state.	—
$\overline{RD}$	I	Read A control signal for the main system to read data from FDC to data bus.	
$\overline{WR}$	I	Write A control signal for the main system to write data from data bus to FDC.	
$\overline{CS}$	I	Chip select Validates $\overline{RD}$ and $\overline{WR}$ signals.	
A_0	I	Address zero A signal used to select the status register or data register in FDC via address bus. When it is 0, status register is selected; if 1, data register is selected.	
DB_7-DB_0	I/O	Data bus A bidirectional 3-state data bus.	Input
DRQ	O	Data request A signal to request data transfer in DMA mode.	Low
$\overline{DACK}$	I	Data acknowledge A signal to acknowledge the DMA cycle.	—
TC	I	Termination clock A signal to specify the termination of data transfer.	
INDEX	I	Index A signal indicating that the read/write head of a drive is positioned on the physical starting point of track on disk.	
INT	O	A request signal to the main system for the processing of transferred data and execution results.	Low
ϕ	I	Phi A clock input. Standard floppy: 8 MHz; mini-floppy: 4 MHz	—
WCLK	I	Write clock A timing signal for transferred data at write time. However, this clock must have also been entered when reading data. The leading edge of this clock pulse must be synchronized with that of the phi clock. FM: $16\phi_{CY}$; MFM: $8\phi_{CY}$ (ϕ_{CY}=period of ϕ input)	
WINDOW	I	Window A signal, generated in the VFO circuit, which is used to sample the clock bit and data bits of RDATA. Whether a clock bit or data bit is determined by FDC.	—
RDATA	I	Read data Data read from the drive and this signal consists of a clock bit and data bits. Unless both WINDOW and RDATA are entered when reading data, the drive is dead locked.	
SYNC	O	Sync A signal to indicate the operating mode of FDC. If 1, FDC is reading data; if 0, it is inhibited from reading operation.	
WE	O	Write enable A signal to instruct the drive to write data.	Low
MFM	O	A signal to specify the operating mode of VFU circuit. If 1, VFO is in MFM mode; if 0, it is in FM mode.	
SIDE	O	Side A signal to select the head 1 or 0 of a double-sided disk drive. If 0, head 0 is selected; if 1, head 1 is selected.	
WDATA	O	Write data Data written to drive, consisting of clock bit and data bits.	Indeterminate

Terminal Functions of μPD72065C

Terminal name	I/O	Function	State when reset
FLT/TRK0	I	Fault/track zero When $\overline{RW}$ is specified by the $\overline{RW}$/SEEK signal, it becomes FLT, and a signal is entered that indicates whether or not the drive is in fault state. When SEEK is specified by the $\overline{RW}$/SEEK signal, it becomes TRK0, and a signal is entered that indicates whether or not the read/write head of the drive is positioned at cylinder 0.	—
WPRT/2SIDE	I	Write protect/2 side When RW is specified by the $\overline{RW}$/SEEK signal, it becomes WPRT, and a signal is entered that indicates whether or not the disk is write inhibited. When SEEK is specified by the $\overline{RW}$/SEEK signal, it becomes 2SIDE, and a signal is entered that indicates whether or not a double-sided disk is placed in the drive.	
READY	I	Ready A signal indicating that the drive is in ready state.	
HDLD	O	Head load A signal which puts the read/write head of the drive into load state.	
FLTR/STEP	O	Fault read/step When $\overline{RW}$ is specified by the $\overline{RW}$/SEEK signal, it becomes FLTR, canceling the fault state of the drive. When SEEK is specified by the $\overline{RW}$/SEEK signal, it becomes STEP, generating the seek pulse.	Low
LCT/DIR	O	LCT/Direction When $\overline{RW}$ is specified by the $\overline{RW}$/SEEK signal, it becomes LCT, indicating that the read/write head of the drive has selected the 43rd or subsequent cylinder. When SEEK is specified by the $\overline{RW}$/SEEK signal, it becomes DIR, specifying the direction of the seek operation. If 0, the centrifugal direction is specified; if 1, the centripetal direction is specified.	
$\overline{RW}$/SEEK	O	Read write/Seek A signal used to discriminate those among drive interface signals which serve dual purposes, read/write and seek. When 0, it indicates $\overline{RW}$; when 1, it indicates SEEK.	
V_{DD}	—	Positive power supply	—
GND	—	GND potential	

3-4-6. VFO IC5

IC5 μPD71066CT is a VFO (data selector) for data transmission speeds of 500, 300, 250, 150, and 125 Kbps.

Internally, it has the following main six functions.

(1) Clock generator block
A signal corresponding to the use mode of the VFO is output to pins FDCCLK and WCLK by the 16 MHz/19.2 MHz externally connected crystal oscillator or external clock (crystal oscillator used here).

(2) Input data generator block
R (Reference signal from one-shot circuit) and V (Comparison symmetry signal from RDIN pin) signals input to the phase comparator are generated from input data. The block also switches whether the analog one-shot circuit or the digital one-shot circuit be used.

(3) Charge pump and filter switching
According to the signal that switches PLL time constants, the charge pump on the LPF2 side is enabled or disabled, thereby controlling the PLL time constant.

(4) Output data generator block
A WINDOW signal (RCLK) and READ DATA signal (RDOUT) are generated that correspond to each mode and each FDC.

(5) SYNC byte detector block
The SYNC field part is detected within a duration of 16 pulses and over to 20pulses, irrespective of the FM or MFM recording.

(6) IDENT field detector block
By detecting whether the SYNC field detected in the SYNC byte detector block is the ID part or the data part, it sets the PLL time constant.

The following is a description of the pin functions of the μPD71066CT.

Terminal Functions of μPD71066CT See Fig. 3-4-8 (page 3-22) for Pin No.

<table>
<tr><th>Terminal name</th><th>Input/Output</th><th>Function</th></tr>
<tr><td>AOSR</td><td></td><td>Analog One-Shot Register.
Fixed resistor connecting terminal (used for the analog one-shot circuit).</td></tr>
<tr><td>RDIN</td><td>Input</td><td>Read Data In
Input terminal for the read data from FDD (pull-up resistor built in)</td></tr>
<tr><td>MIN/STD</td><td>Input</td><td>Mini/Standard Floppy
Terminal for switching between 5-inch FDD and 8-inch FDD (pull-up resistor built in).
5-inch FDD: Open (or high)
8-inch FDD: Low</td></tr>
<tr><td>RGATE</td><td>Input</td><td>Read Gate
Input terminal for the signal which specifies whether the read operation from the FDC is to be allowed or inhibited (pull-up resistor built in).
<table>
<tr><th>FDCSW2</th><th>RGATE</th><th>Read Operation</th></tr>
<tr><td>High</td><td>High</td><td>Allowed</td></tr>
<tr><td>High</td><td>Low</td><td>Inhibited</td></tr>
<tr><td>Low</td><td>High</td><td>Inhibited</td></tr>
<tr><td>Low</td><td>Low</td><td>Allowed</td></tr>
</table></td></tr>
<tr><td>MFM/FM</td><td>Input</td><td>Terminal for switching between double-density and single-density recording systems (pull-up resistor built in).
<table>
<tr><th>FDCSW2</th><th>MFM/FM</th><th>Recording System</th></tr>
<tr><td>High</td><td>High</td><td>MFM recording</td></tr>
<tr><td>High</td><td>Low</td><td>FM recording</td></tr>
<tr><td>Low</td><td>High</td><td>FM recording</td></tr>
<tr><td>Low</td><td>Low</td><td>MFM recording</td></tr>
</table></td></tr>
<tr><td>SYNCSW</td><td>Input</td><td>Sync Switch
Terminal for selecting whether or not the gain switching of PLL (detection of SYNC field) is to be performed with an internally generated signal or external signal (SYNC terminal) (pull-up resistor built in).
SYNCSW = Open (or high); Internal sync
SYNCSW = Low: External sync</td></tr>
<tr><td>SYNC</td><td>Input</td><td>• Input terminal for the signal which switches the gain of PLL between the ID field and the data field when FDCSW1 = open (or high) and, at the same time, SYNCSW = open (or high).
• When SYNCSW = low,
Input terminal for the SYNC field detect signal from FDC which switches the gain of PLL.
<table>
<tr><th>SYNC</th><th>PLL time constant</th></tr>
<tr><td>High</td><td>Small</td></tr>
<tr><td>Low</td><td>Large</td></tr>
</table>
(Pull-up resistor built in)</td></tr>
<tr><td>RDOUT</td><td>Output</td><td>Read Data Out
Terminal to output read data synchronized with the read clock (RCLK), which is generated by the read data signal from FDD.</td></tr>
<tr><td>RCLK</td><td>Output</td><td>Read Clock
Terminal to the output clock for sampling the read data output.</td></tr>
<tr><td>FDCCLK</td><td>Output</td><td>Floppy Disk Clock
Terminal for output of the FDC clock.</td></tr>
<tr><td>WCLK</td><td>Output</td><td>Write Clock
Terminal for output of the write clock to FDC.</td></tr>
<tr><td>X1, X2</td><td></td><td>Terminal for the connection of quartz for the clock generation (16 MHz quartz).
If external clock input, input to X2 terminal.</td></tr>
</table>

Terminal Functions of μPD71066CT See Fig. 3-4-8 (page 3-22) for Pin No.

Terminal name	Input/Output	Function
X3, X4		Terminal for the connection of quartz for the clock generation (19.2 MHz quartz). If external clock input, input to X4 terminal.
TOUT	Output	Timer Out Timer circuit output terminal (μPD71066 only).
TCC		Timer Circuit Constant Terminal for the connection of RC used to set the timer circuit time constant (μPD71066 only).
$\overline{\text{RESET}}$	Input	Reset Input terminal for low-level active system reset (pull-up resistor built in).
CVC		Terminal for the connection of the capacitor for the VCO circuit oscillation.
FDDSW	Input	FDD Switch Terminal for switching FDD types (pull-up resistor built in). • FDDSW = Open (or high) 500/250/125 Kbps data transfer rate FDD • FDDSW = Low 500/250/300/150 Kbps data transfer rate FDD
VCOIN	Input	Input terminal for the low-pass filter output signal to the VCO circuit.
FDCSW1	Input	• When FDCSW2 = open (or high), FDC select terminal. FDCSW1 / FDC Open (or high) / μPD765A/7265 Low / μPD7260 • When FDCSW2 = low, timer circuit trigger input terminal (pull-up resistor built in).
LPF2 LPF1	Output	Terminal for the connection of the Low-Pass Filter
FDCSW2	Input	FDC select terminal (pull-up resistor built in). FDCSW2 / FDC Open (or high) / μPD765A/7265/7260 Low / FD179X series
AOSC		Analog One-Shot Capacitance Terminal for the connection of the fixed capacitor (used for the analog one-shot circuit).
V_{DD}		Terminal for positive power supplies.
GND		GND potential terminal.
AV_{DD}		Positive power supply terminal for the analog circuits
AGND		GND potential terminal for the analog circuits.

Setting of Data Transfer Rates

Setting of the control terminal			Clock output frequency from VFO			Data transfer rates (Kbps)
FDDSW	MIN/STD	MFM/FM	FDCCLK	RCLK	WCLK	
1	1	1	4MHz	250kHz	500kHz	250
1	1	0	4MHz	125kHz	250kHz	125
0	1	1	4.8MHz	300kHz	600kHz	300
0	1	0	4.8MHz	150kHz	300kHz	150
0	0	1	8MHz	500kHz	1MHz	500
0	0	0	8MHz	250kHz	500kHz	250

3-4-7. Connection Between FDC and VFO

R106 and C108 represent a resistor and capacitor for the analog one-shot circuit, which are used only when the data transfer rate is 500Kbps. They are set in such a way that the steady phase (t_{STW}: between RCLK-RDOUT) is 950 nsec.

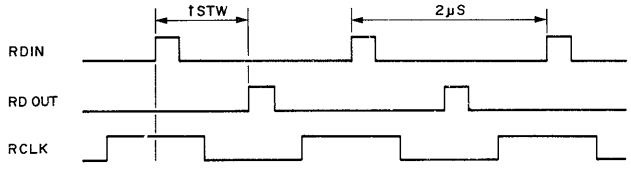


Fig. 3-4-7.

R107, R108, R110, C107 and C110 are the constants of LPF1 and 2. The switching of LPF is automatically performed upon the detection of the SYNC field in the IC. R110 determines the lock range of PLL Currently it has such a width that 250 Kbps signals can be read when transferred at a rate of 300 Kbps.
The oscillation frequency of VCO is fine-tuned by R109. RGATE="H" and RDIN="L", and the setting is made in such a way that it is matched to the data transfer rate setting by the signal of the RCLK terminal. 500 kHz it 500 Kbps.

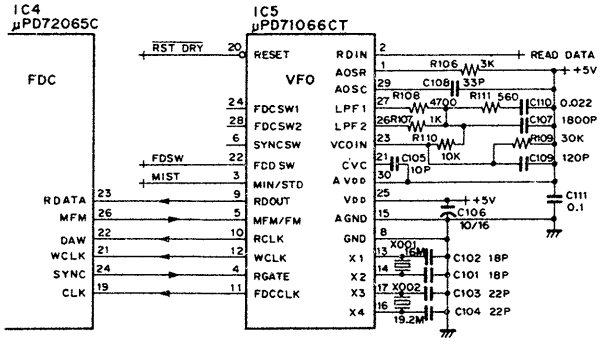


Fig. 3-4-8.

3-4-8. Timing on Drive Interface

Fig. 3-4-10 through 3-4-14 show the timing diagram of each command on the drive interface side.

(1) Fig. 3-4-10 indicates the following timing: Read data, Read deleted data, Read diagnostic, Read ID, Scan equal, Scan low or equal, Scan high or equal.
When writing data up to the 2nd byte of the C-phase (Command-phase) is finished, the SIDE signal is output.
The contents of these signals correspond to the contents of the HD bit.
When all of the remaining parameters (except the READ ID command) have been written, 0 is output to the $\overline{RW}$/SEEK signal.
Then the MFM signal is set as needed.
When all this is done whether or not in head load state is checked, and if in head load state (i.e., the HDLD signal is in one state) the SYNC signal is set and the drive immediately starts reading the disk. If the head is not loaded, it is first loaded in position (HDLD signal = 0 to 1) and after an elapse of head load time (specified by the SPECIFY command), the SYNC signal is set and the drive starts reading the disk.
When the ID part that is specified by IDR of the C-phase is detected, the CRC byte at the last of the ID part is read. Upon reading this byte, the SYNC signal is reset, thus inhibiting the drive from reading the disk. This inhibited area is 24 bytes in length for the MFM mode. It is provided to avoid reading data in a discontinued spot in the boundary between GAP 2 caused when writing and SYNC.
When the read inhibit section thus prescribed is finished, the SYNC signal is set and the drive starts reading the disk. Here the SYNC byte is detected and subsequently the drive reads the data part. When reading the CRC byte in the data part is finished, the SYNC signal is reset in order to avoid the discontinued spot in the boundary with the subsequently written GAP 3. The length of the reset section here is the value of the GSL byte specified by the C-phase. After the number of bytes specified by the GSL byte have gone by, the SYNC signal is set and the drive begins to read the ID part of the next sector.
When read up to the last sector, the HDLD signal is reset unless a new read/write command is given to the same cylinder of the same device within the head unload time (specified by the SPECIFY command). The SIDE signal is reset after the HDLD signal is reset.
If any new read/write command is given to the same cylinder of the same device within the head unload time, the HDLD signal remains set so the time to load the head can be saved.

Track Format (MFM)

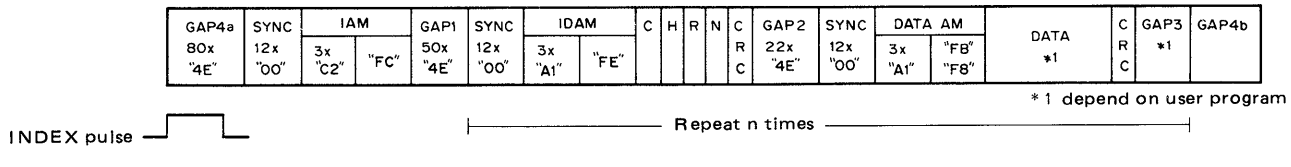


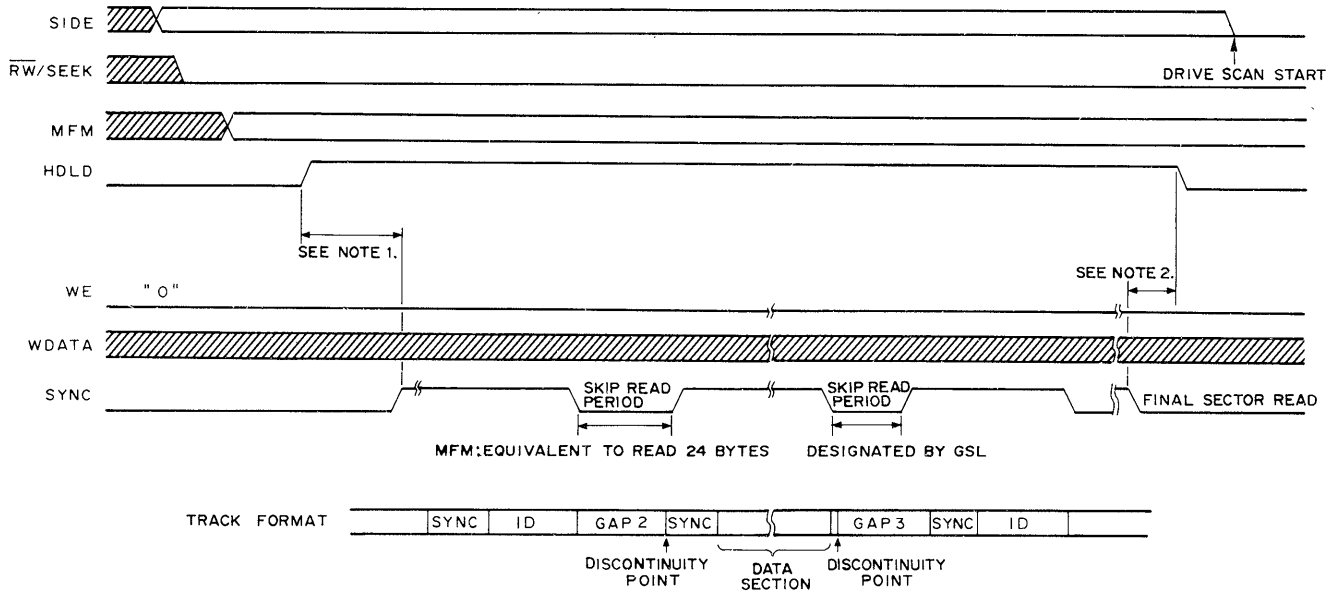
Fig. 3-4-9

(2) Fig. 3-4-11 shows the timing of the WRITE DATA and WRITE DELETED DATA commands.
The SIDE, $\overline{RW}$/SEEK, MFM and HOLD signals are output in the same way as the READ commands (see Fig. 3-4-9). However, the READY signal is checked.
After the HDLD signal has been set the SYNC signal is set and the ID part of the desired sector is detected, and when reading the CRC byte is finished the SYNC signal is reset. Operations up to here are the same as with the READ commands.
When the SYNC signal has been reset the WE signal is set after an elapse of a certain time (the width of GAP 2), causing the SYNC bytes (12 bytes for MFM) to be written. Here a discontinued spot is created in the boundary between the previously written GAP 2 and the newly written SYNC byte.
Subsequent to the SYNC byte, the drive writes to the data part, and after writing the CRC byte in the data part is finished one byte of gap is written and the WE signal is reset. Here too a discontinued spot is created. While the WE signal is being output, WDATA signal is output.
After writing the CRC byte in the data part is finished (after an elapse of the time specified by the GSL byte) the SYNC signal that had been reset during write operation is set, and the drive begins to read the ID part of the next sector.

(3) Fig. 3-4-12 shows the timing of the WRITE ID command. Unlike WRITE DATA, no sector is specified. After detection of the INDEX signal, the WE signal is set and immediately the drive starts writing from the gap at the track starting point and all the format for one track is written. However, the data that is written to the data part is the one specified by the D byte for all bytes.
When all formats have been written up to the last sector (specified by the SC byte) the drive writes gaps until the INDEX signal is detected again.

(4) Fig. 3-4-13 shows the timing of the SEEK and RECALIBRATE commands.
The $\overline{RW}$/SEEK output is made to 1, and the DIR signal and the STEP signal are output. The period in which time the STEP signal is output to one FDD is the time specified by SRT (Step Rate Time) of the SPECIFY command.

(5) Fig. 3-4-14 shows the timing of the SENSE DEVICE STATUS command. When writing the 2nd byte in the C-phase is finished, the SIDE signal is output.
Subsequently 0 is output to the $\overline{RW}$/SEEK signal, while at the same time the WPRT signal is checked. And then the $\overline{RW}$/SEEK signal is made to 1 and the TRK0 signal is checked.



NOTE 1. This interval is specified by HLT of SPECIFY command and also not concerned with SYNC detection. Under head load condition, there is no head load wait when read/write command is given to the same cylinder of same device continuously.

NOTE 2. This interval is specified by HLT of SPECIFY command.
New read/write command is given to the same cylinder of the same device with the head unload time, the HDLD signal remains set.

Fig. 3-4-10 READ DATA, READ DELETED DATA, READ DIAGNOSTIC, READ ID, SCANING

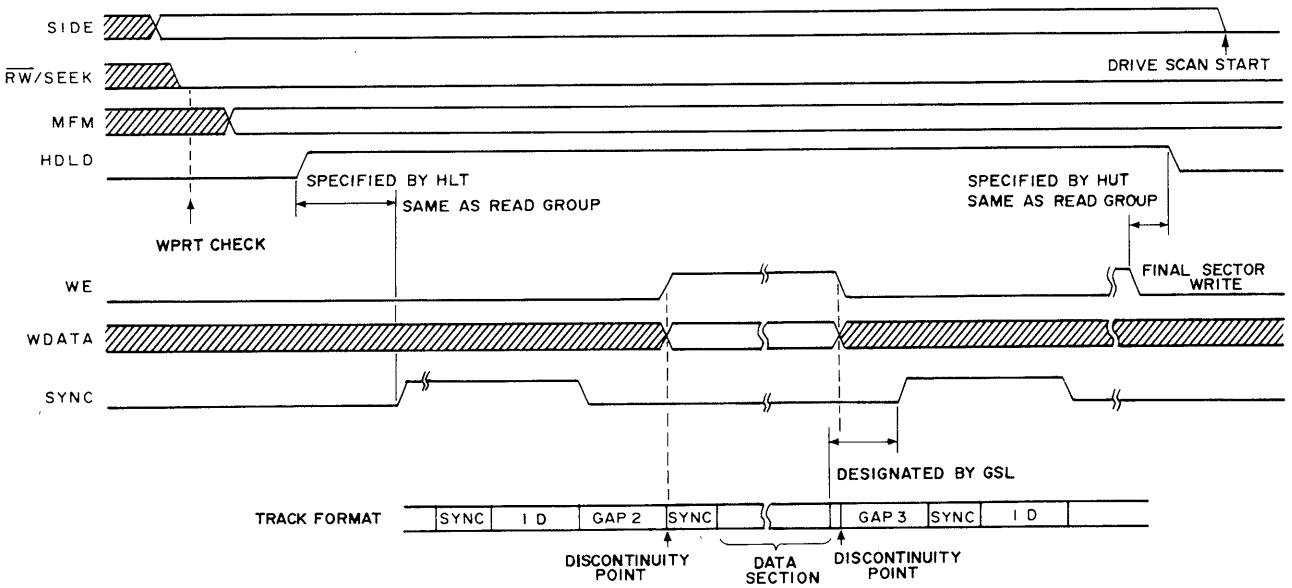


Fig. 3-4-11 WRITE DATA, WRITE DELETED DATA

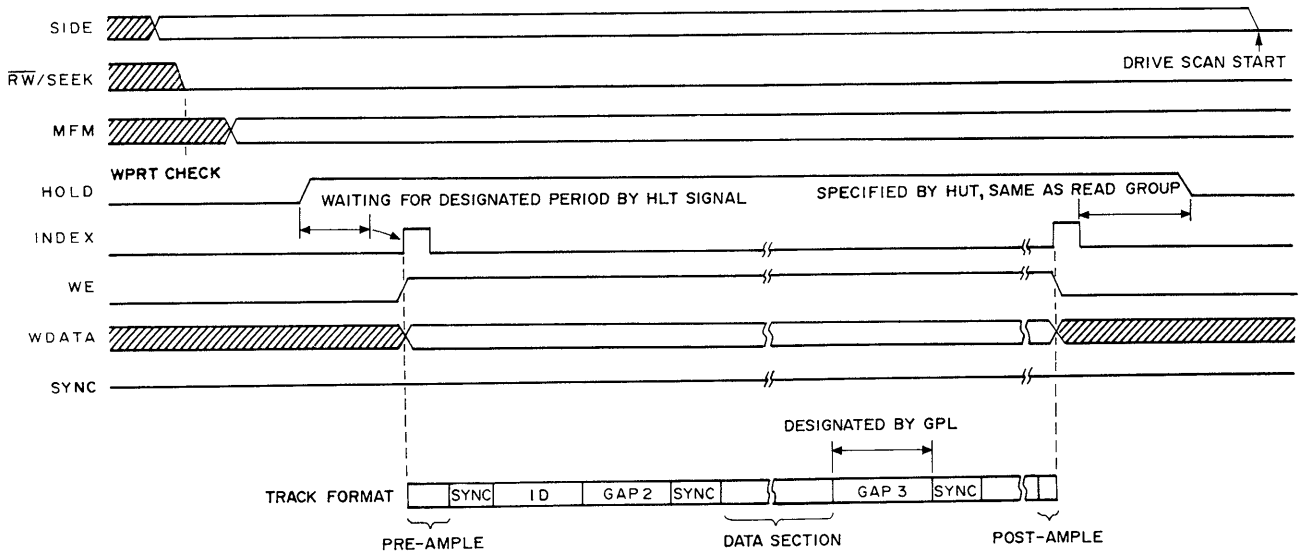


Fig. 3-4-12 WRITE ID

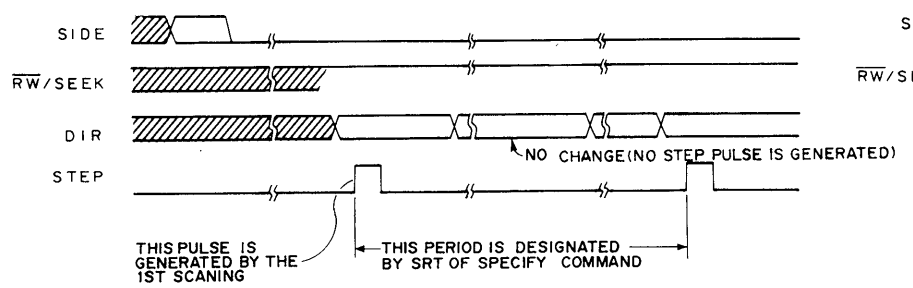


Fig. 3-4-13 SEEK, RECALIBRATE

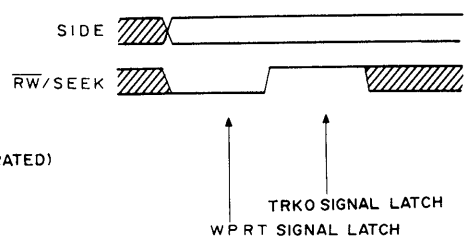


Fig. 3-4-14 SENSE DEVICE STATUS

3-4-9. FDD Interface Signals

See the table in Section 3-4-2.

1. Signals from FDC to FDD

- $\overline{\text{DRIVE SEL A}}$, $\overline{\text{DRIVE SEL B}}$
  Drive select signal for FDD. Selected when low.

- $\overline{\text{MOTOR ON}}$
  Motor-on signal for FDD. Turned on when low.
  $\overline{\text{MOTOR ON}}$ is output when the motor of drive A is turned on or when the motor of drive B is turned on. Accordingly, motors of both drives in internal FDD are turned on.

- $\overline{\text{DIR}}$
  $\overline{\text{STEP}}$ signal which specifies the direction for the head of FDD to move. Stepped out when high; stepped in when low.

- $\overline{\text{STEP}}$
  A pulse signal to move the head of FDD. (by 1 track)

- $\overline{\text{WRITE GATE}}$
  Write enabled when low. Write disabled when high.

- $\overline{\text{WRITE DATA}}$
  A pulse signal to specify the contents of data record on a floppydisk..

- $\overline{\text{HEAD SEL}}$
  Side 0 when high. Side 1 when low.

- $\overline{\text{IN USE}}$
  When low, FDD is under the control of FDC.

- 2HD/$\overline{\text{2DD}}$
  Used when 2HD (dual-speed) FDD is used. When high, 360 rpm. When low, 300 rpm.

2. Signals from FDD to FDC

- $\overline{\text{TRACK 0}}$
  When low, the head of FDD is at track 0 (the outermost track).

- $\overline{\text{INDEX}}$
  Index hole detection pulse signal in the floppydisk.

- $\overline{\text{READ DATA}}$
  Reproduction pulse signal of record datas on a floppydisk.

- $\overline{\text{WRITE PROT}}$
  When low, a floppydisk is write-protected.

- $\overline{\text{DSK CHG}}$
  When low, a floppydisk has been removed from FDD.

3-4-10. Display Board Select

There are gates for some of the signals on the system bus and **video bus to allow other display boards (such as EGA/VGA) to be used with Sony display boards installed in slots C, D, and E. IC10 (74F02), IC11 through IC13 (each 74F32) and IC14 (74LS32) are these gates.**

The DISPLAY BOARD switch (S1) on the SW-277 board controls this gate circuit. The BS-1 and BS-2 signals from this switch enable/disable the bus signals.

See also Fig. 3-4-15 of page 3-26.

DISPLAY BOARD switch	signal name	
	BS-1	BS-2
Position A	Low	Low
Position B	Low	High
Position C	High	Low

Position A: Normal mode. All slots are active.

Position B: Sony mode. Slot 4 is inactive. The signals which actually disable slot 4 are the following.

disable signal name	level	remarkes
$\overline{\text{AIOR}}$, $\overline{\text{AIOW}}$, $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$	High	Signals only for Slot 4
$\overline{\text{REFRESH}}$	Low	

Position C: EGA mode. Slots C, D, and E are inactive. The signals which actually disable slots C, D, and E are the following.

disable signal name	level	remarkes
$\overline{\text{AIOR}}$, $\overline{\text{AIOW}}$, $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$, $\overline{\text{AEN}}$	High	Signals only for Slot C, D, and E
$\overline{\text{REFRESH}}$	Low	
M/$\overline{\text{HG}}$*	High	Signal only for Slot B
$\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, BLANKING*	High	Signals only for Slots C and D
L ON*, R ON*	High	Signals only for Slot E

* Signals on video bus

Note 1: At position A, boards other than display boards can be inserted and used in slot 4.

Note 2: Even at position C, the ausio output (CN607 and CN608) on the DSC-43V board in slot D can still be obtained.
As only ausio is output from the analog RGB output (CN508) on the VS board in slot E, this allows for only sound to be heard when monitors with a built-in speaker are connected.
In case the SMI-3085 is attached to the VIW-3015A.

Note 3: Refer to section 1-2-3 regarding the DISPLAY BOARD switch.

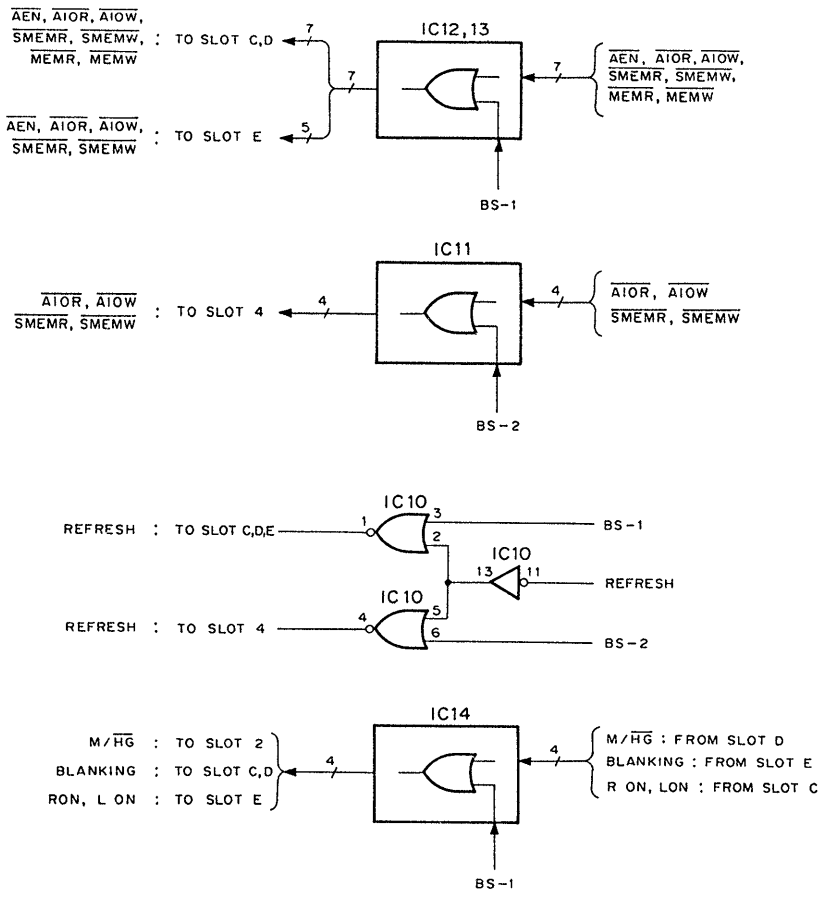


Fig.3-4-15. Display Board Bus Select

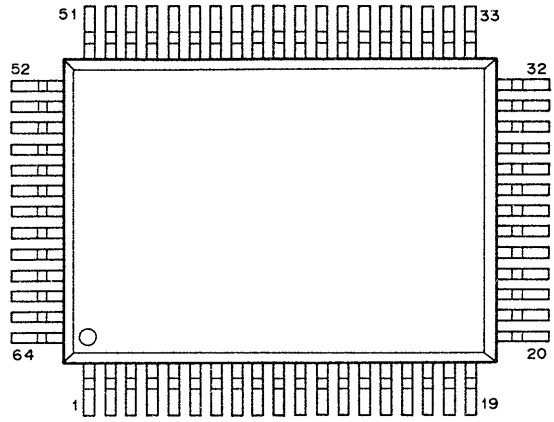
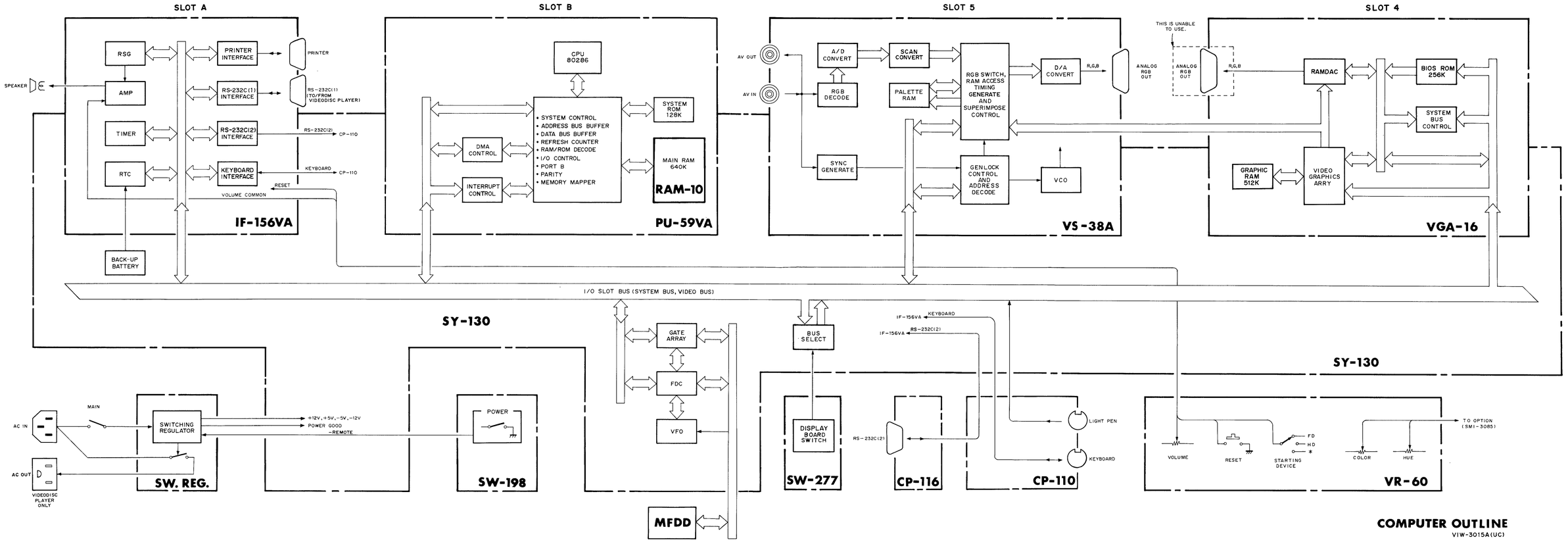


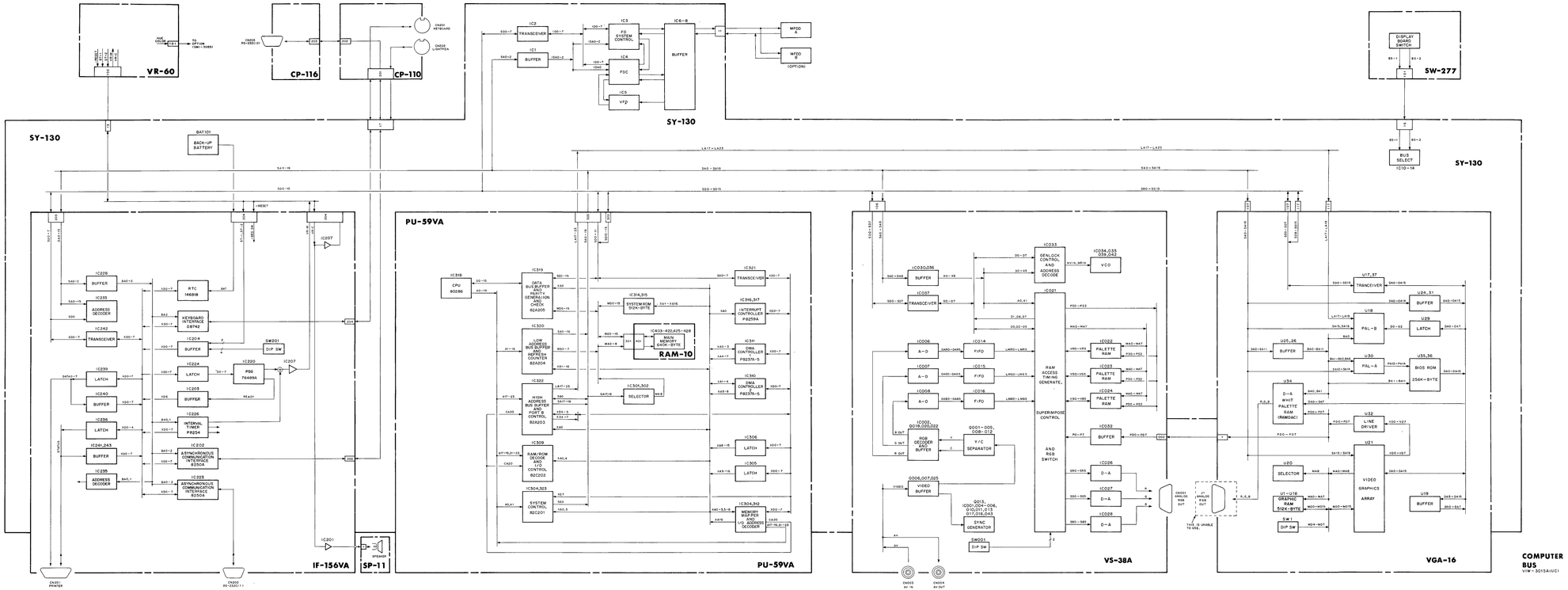
Fig.3-4-16. μPD65005G-126-12 Ext. View

CHAPTER 4
BLOCK DIAGRAM

4-1. COMPUTER OUTLINE

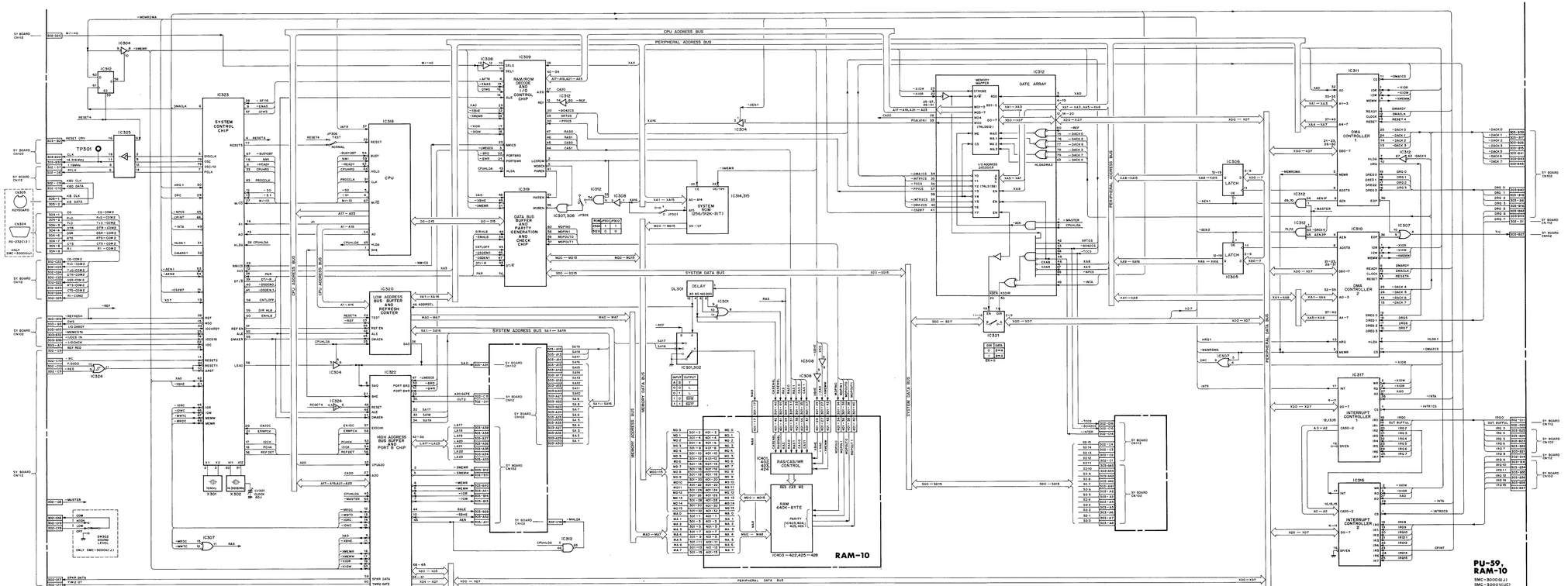


4-2. COMPUTER BUS

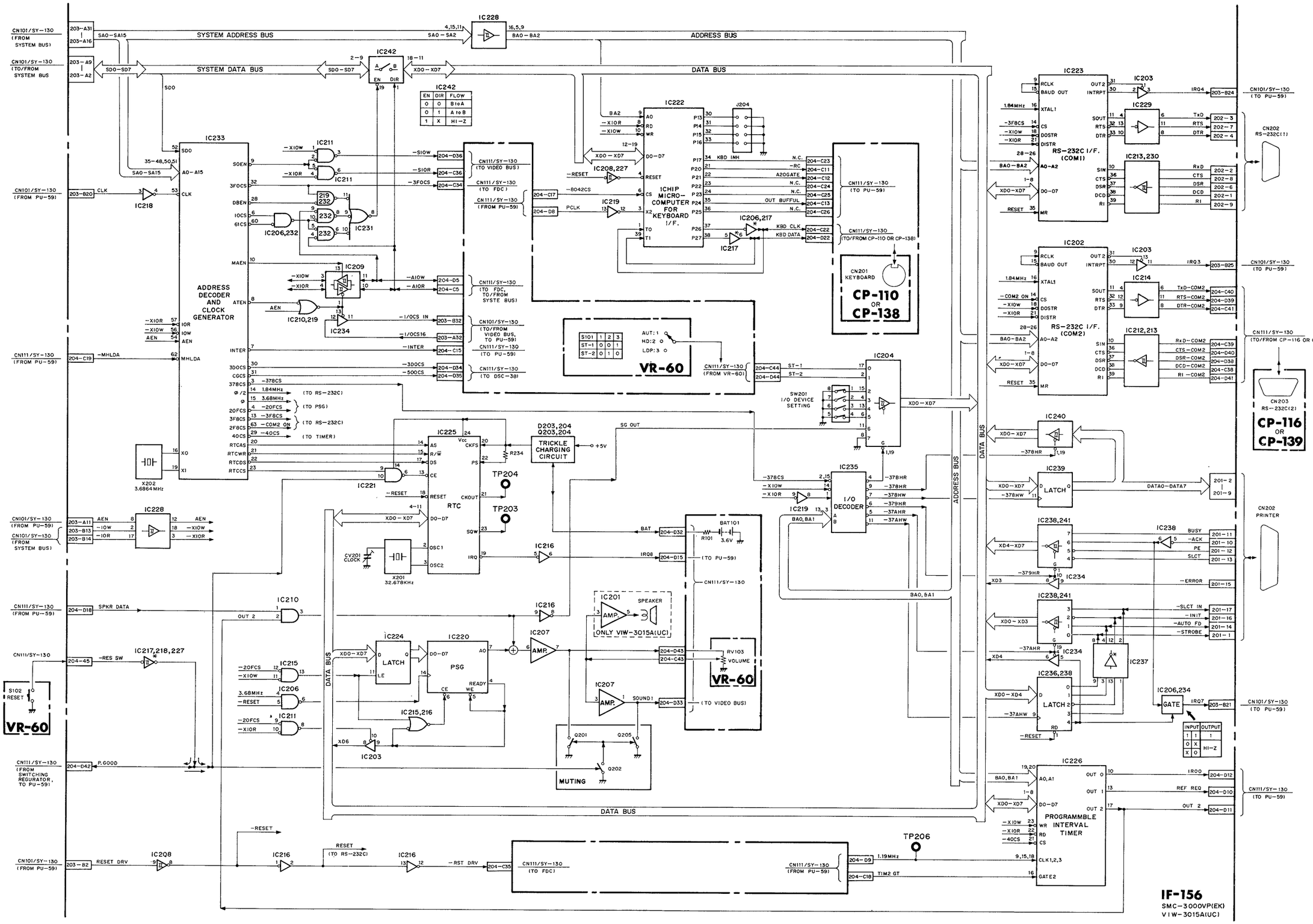


PU-59VA, RAM-10 PU-59VA, RAM-10

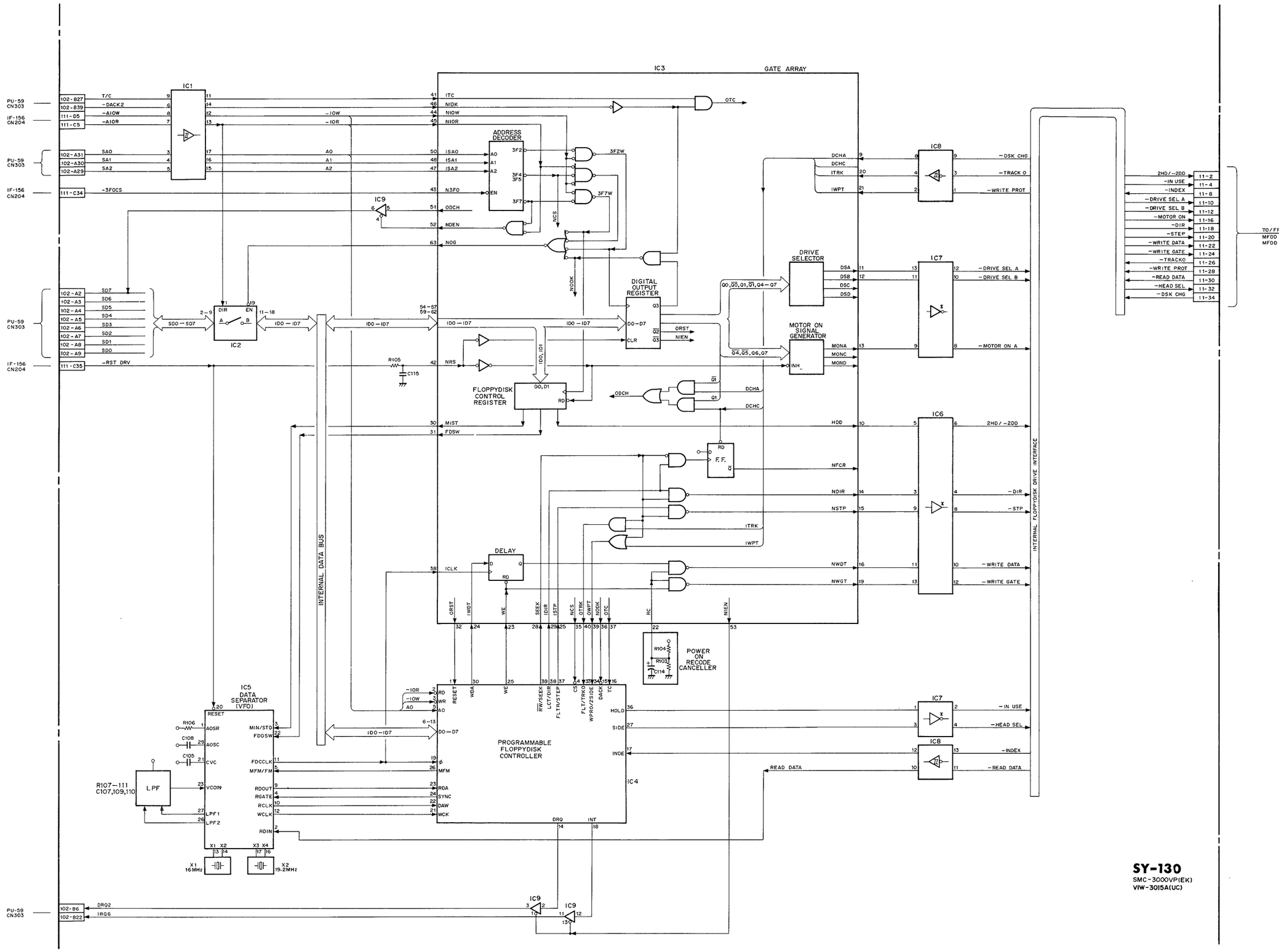
4-3. PU-59VA BOARD, RAM-10 BOARD



4-4. IF-156VA BOARD

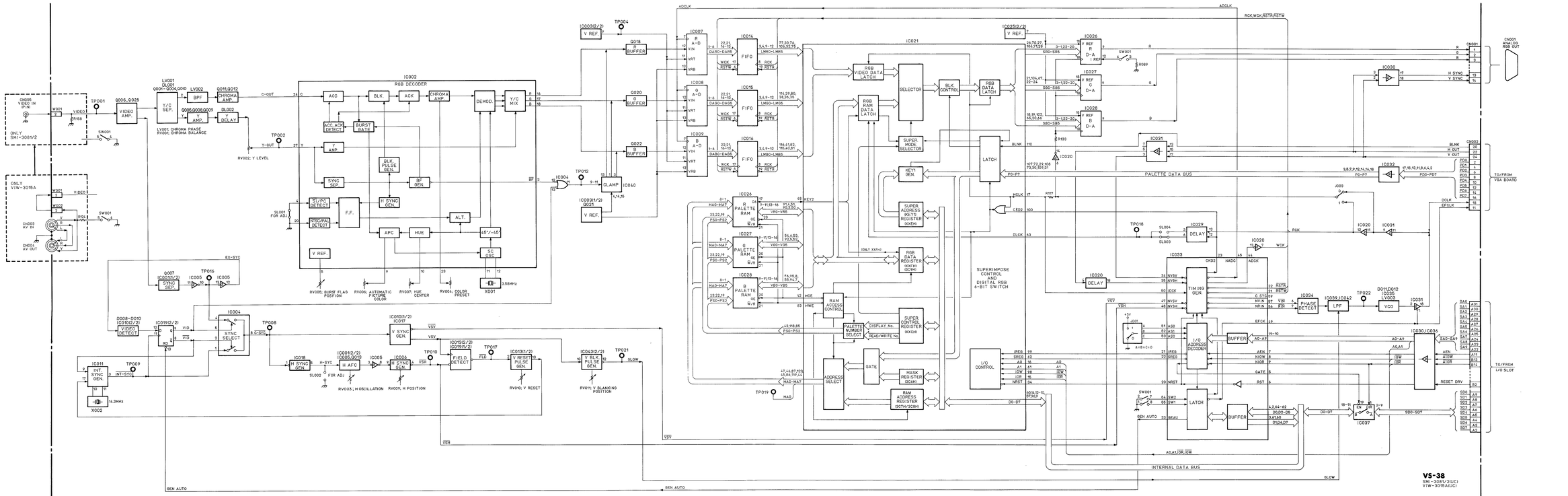


4-5. SY-130 BOARD



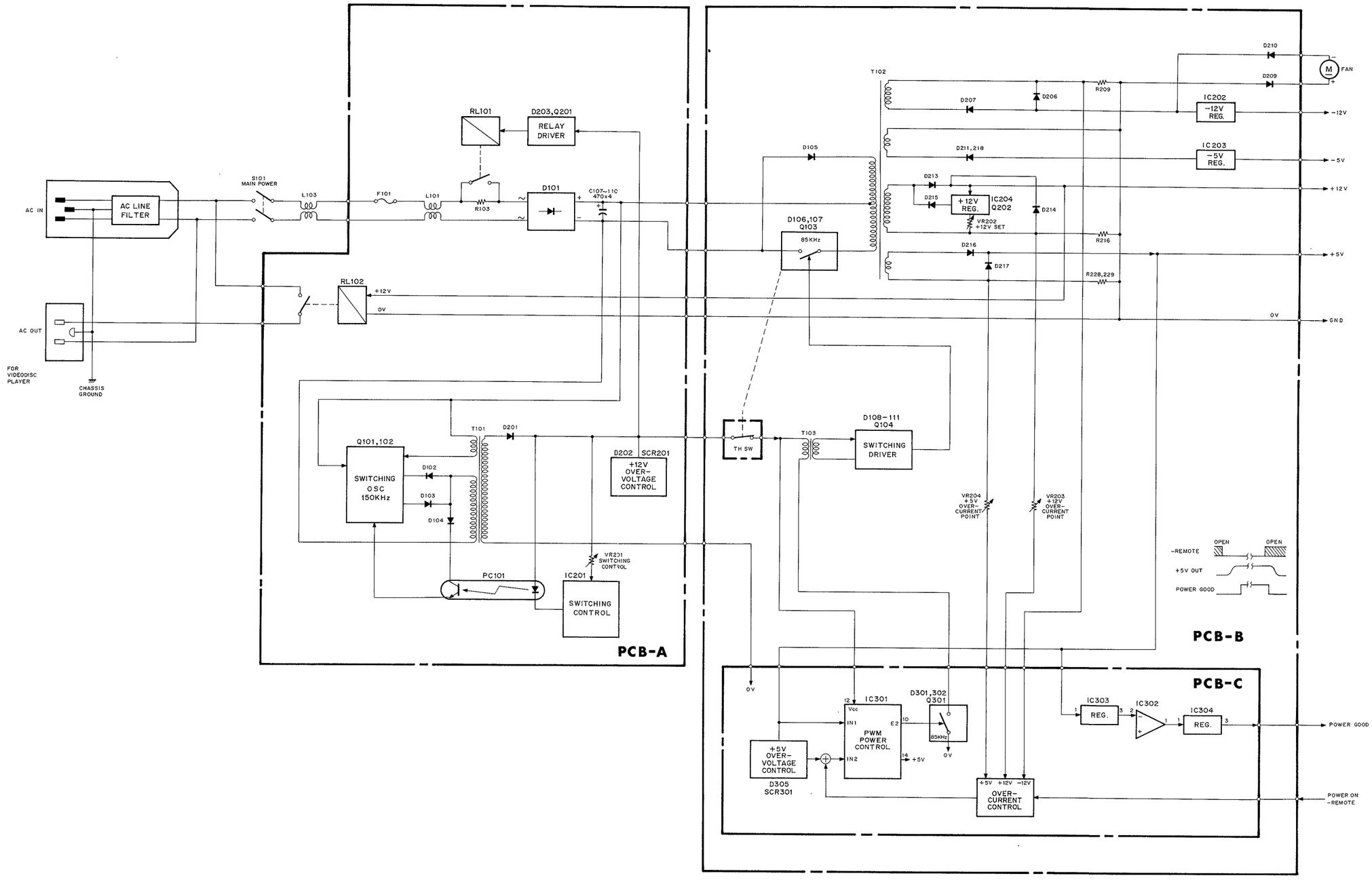
VS-38A VS-38A

4-6. VS-38A BOARD



SW. REG.	SW. REG.

4-7. SWITCHING REGULATOR



SR-93
SWITCHING REG.

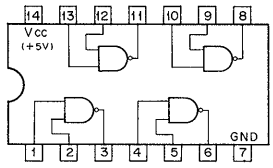
SMC-3000V(UC)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(UC),(J)
VIW-3020/1(U)

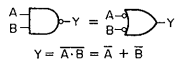
CHAPTER 5
SCHEMATIC DIAGRAM

5-1. SEMICONDUCTOR PIN ASSIGNMENTS

74F00PC (FSC)
SN74ALS00AN (TI)

TTL 2-INPUT POSITIVE-NAND GATE
– TOP VIEW –





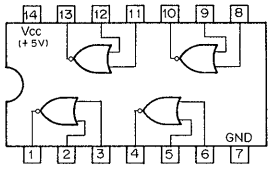
$Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

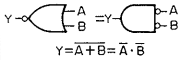
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

0; LOW LEVEL
1; HIGH LEVEL

MC74F02N (MOTOROLA)
SN74ALS02N (TI)
SN74LS02N (TI)

TTL 2-INPUT POSITIVE-NOR GATE
– TOP VIEW –





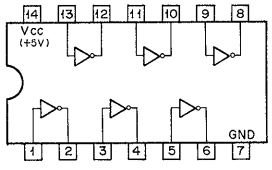
$Y = \overline{A+B} = \overline{A} \cdot \overline{B}$

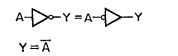
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

0:LOW LEVEL
1;HIGH LEVEL

74F04PC (FSC)
N74LS04D (SIGNETICS) FLAT PACKAGE
SN74ALS04BN (TI)
SN74LS04N (TI)

TTL INVERTER
– TOP VIEW –





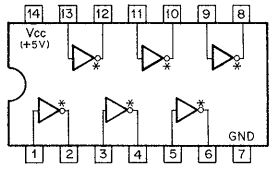
$Y = \overline{A}$

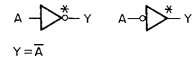
A	Y
0	1
1	0

0;LOW LEVEL
1;HIGH LEVEL

SN7405N (TI)

TTL INVERTER WITH OPEN-COLLECTOR
– TOP VIEW –





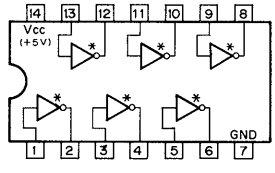
$Y = \overline{A}$

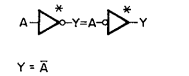
A	Y
0	1
1	0
*	OPEN COLLECTOR

0;LOW LEVEL
1;HIGH LEVEL
*; OPEN COLLECTOR

HD74LS06P (HITACHI)
SN7406N (TI)
SN74LS06N (TI)

TTL INVERTER BUFFER/DRIVER WITH OPEN-COLLECTOR
– TOP VIEW –





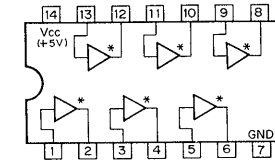
$Y = \overline{A}$

A	Y
0	1
1	0
*	OPEN COLLECTOR

0;LOW LEVEL
1;HIGH LEVEL
*;OPEN COLLECTOR

SN7407N (TI)

TTL BUFFER/DRIVER WITH OPEN-COLLECTOR
– TOP VIEW –

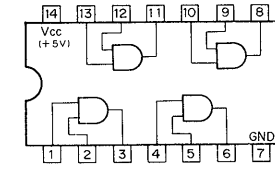


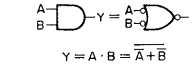
A	Y
0	0
1	*

0 ; LOW LEVEL
1 ; HIGH LEVEL
* ; OPEN COLLECTOR

74F08PC (FSC)
MC74F08N (MOTOROLA)
SN74ALS08N (TI)

TTL 2-INPUT POSITIVE-AND GATE
– TOP VIEW –





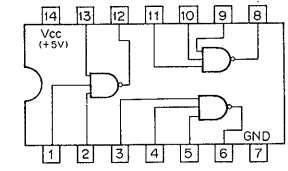
$Y = A \cdot B = \overline{\overline{A} + \overline{B}}$

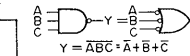
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

0; LOW LEVEL
1; HIGH LEVEL

74F10PC (FSC)
MC74F10N (MOTOROLA)

TTL 3-INPUT POSITIVE NAND GATE
– TOP VIEW –





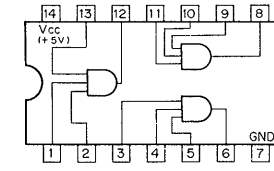
$Y = \overline{ABC} = \overline{A} + \overline{B} + \overline{C}$

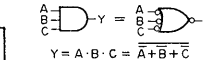
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

0 : LOW LEVEL
1 : HIGH LEVEL

SN74ALS11AN (TI)

TTL 3-INPUT POSITIVE-AND GATE
– TOP VIEW –





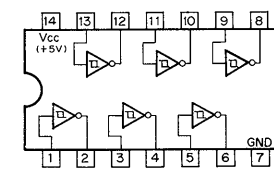
$Y = A \cdot B \cdot C = \overline{\overline{A} + \overline{B} + \overline{C}}$

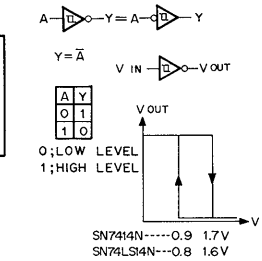
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

0;LOW LEVEL
1;HIGH LEVEL

SN74LS14N (TI)

TTL SCHMITT TRIGGER INVERTER
– TOP VIEW –





$Y = \overline{A}$

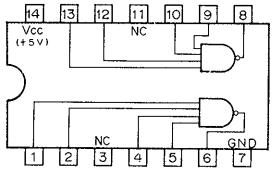
A	Y
0	1
1	0

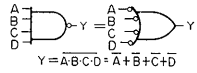
0;LOW LEVEL
1;HIGH LEVEL

SN7414N-----0.9 1.7V
SN74LS14N---0.8 1.6V

MC74F20N (MOTOROLA)

TTL 4-INPUT POSITIVE NAND GATE
– TOP VIEW –



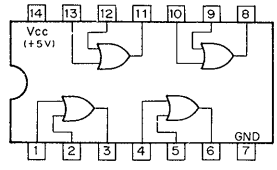


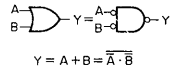
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
:	:	:	:	:
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

0 ; LOW LEVEL
1 ; HIGH LEVEL

74F32PC (FSC)
MC74F32N (MOTOROLA)
SN74ALS32N (TI)
SN74LS32N (TI)

TTL 2-INPUT POSITIVE-OR GATE
– TOP VIEW –



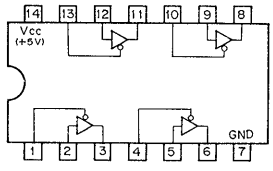


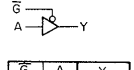
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

0 ; LOW LEVEL
1 ; HIGH LEVEL

MC74LS125AD (MOTOROLA) FLAT PACKAGE
SN74LS125AN (TI)

TTL BUS BUFFER GATES WITH 3-STATE OUTPUTS
– TOP VIEW –



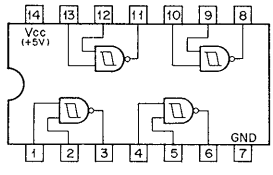


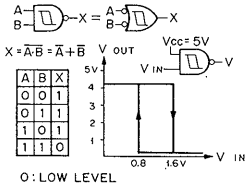
G	A	Y
0	0	0
0	1	1
1	X	HI – Z

0 ; LOW LEVEL X ; DON'T CARE
1 ; HIGH LEVEL HI-Z ; HIGH IMPEDANCE

SN74LS132N (TI)

TTL 2-INPUT NAND SCHMITT TRIGGER
– TOP VIEW –



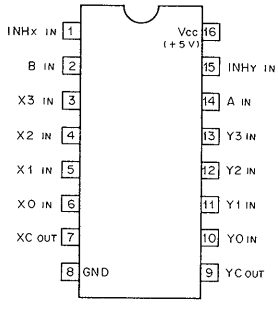


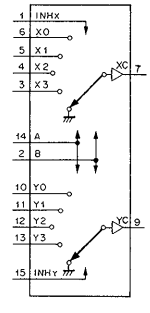
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

0 ; LOW LEVEL
1 ; HIGH LEVEL

MC74F153N (MOTOROLA)

TTL 4-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER
– TOP VIEW –



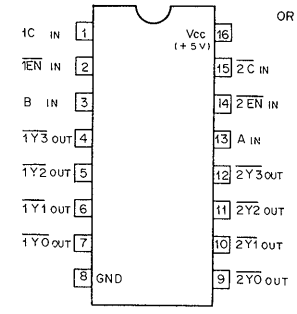


CONTROL IN			ON CHANNEL
INH	B	A	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	GND

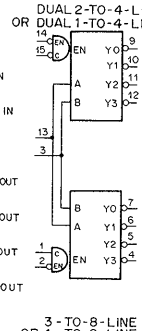
0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

SN74LS155N (TI)

TTL DUAL 2-TO-4-LINE DECODER/DEMULTIPLEXER
– TOP VIEW –



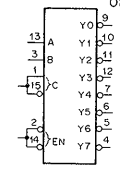
DUAL 2-TO-4-LINE DECODER
OR DUAL 1-TO-4-LINE DEMULTIPLEXER



INPUTS				OUTPUTS			
EN	C	B	A	Y3	Y2	Y1	YO
0	0	0	0	1	1	1	0
0	0	0	1	1	1	0	1
0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	1
X	1	X	X	1	1	1	1
1	X	X	X	1	1	1	1

EN	C	B	A	Y3	Y2	Y1	YO
0	1	0	0	1	1	1	0
0	1	0	1	1	1	0	1
0	1	1	0	1	0	1	1
0	1	1	1	0	1	1	1
X	0	X	X	1	1	1	1
1	X	X	X	1	1	1	1

3-TO-8-LINE DECODER
OR 1-TO-8-LINE DEMULTIPLEXER

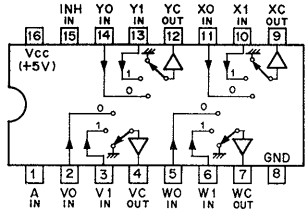


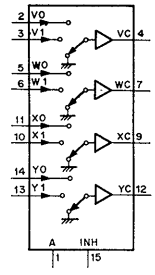
INPUTS				OUTPUTS							
EN	C	B	A	Y7	Y6	Y5	Y4	Y3	Y2	Y1	YO
0	0	0	0	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	0	1	1	1	1
0	1	0	1	1	1	0	1	1	1	1	1
0	1	1	0	1	0	1	1	1	1	1	1
0	1	1	1	0	1	1	1	1	1	1	1
1	X	X	X	1	1	1	1	1	1	1	1

0 ; LOW LEVEL 1 ; HIGH LEVEL X ; DON'T CARE

SN74LS157NS (TI) FLAT PACKAGE

TTL 2-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER
– TOP VIEW –



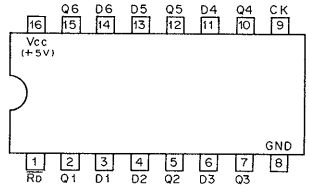


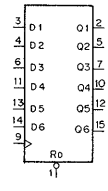
CONT. IN		ON CHANNEL
INH	A	
0	0	0
0	1	1
1	X	GND

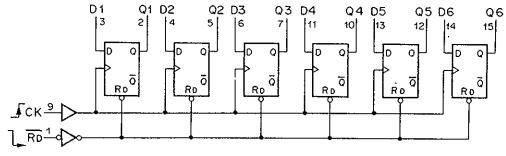
0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

MC74LS174D (MOTOROLA) FLAT PACKAGE
SN74LS174N (TI)

TTL D-TYPE FLIP-FLOP WITH DIRECT RESET
– TOP VIEW –







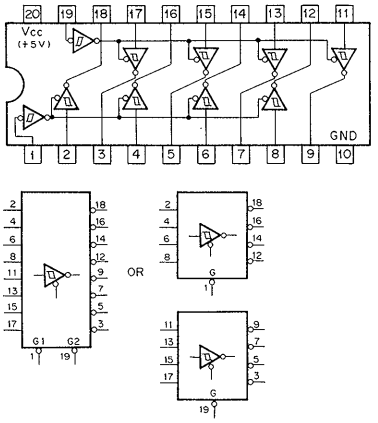
EACH FLIP-FLOP

INPUTS			OUT
$\overline{RD}$	CK	D	Q
0	X	X	0
1	↓	0	0
1	↓	1	1
1	0	X	Q0

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

74F240N (FSC)
SN74LS240N (TI)

TTL 3-STATE SCHMITT TRIGGER INVERTER/LINE DRIVER
– TOP VIEW –

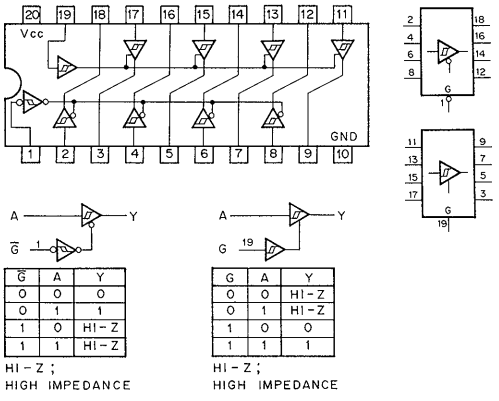


$\overline{G}$	A	Y
0	0	1
0	1	0
1	X	HI-Z

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE

74F241PC (FSC)

TTL 3-STATE SCHMITT TRIGGER BUFFER/LINE DRIVER
– TOP VIEW –



$\overline{G}$	A	Y
0	0	0
0	1	1
1	0	HI-Z
1	1	HI-Z

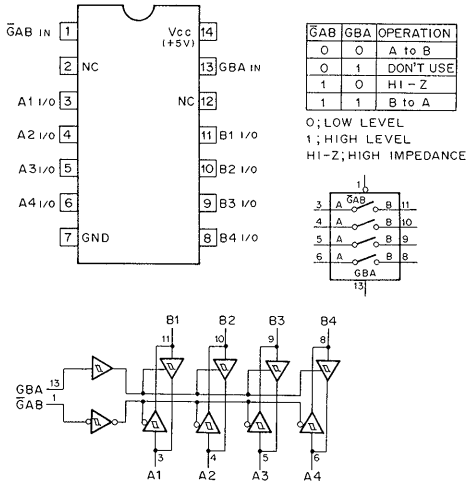
HI-Z ;
HIGH IMPEDANCE

G	A	Y
0	0	HI-Z
0	1	HI-Z
1	0	0
1	1	1

HI-Z ;
HIGH IMPEDANCE

74F243PC (FSC)

TTL BUS TRANSCEIVERS WITH 3-STATE OUTPUT
– TOP VIEW –

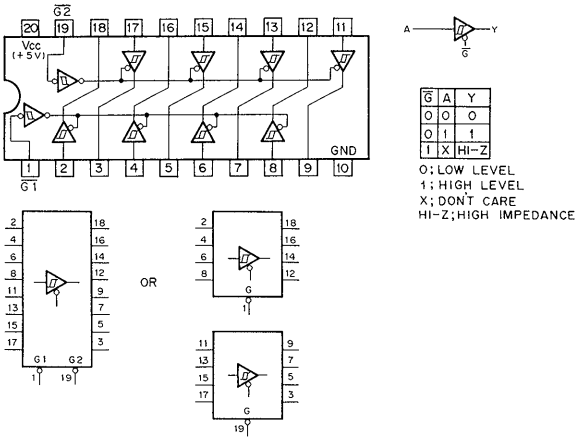


GAB	GBA	OPERATION
0	0	A to B
0	1	DON'T USE
1	0	HI-Z
1	1	B to A

0 ; LOW LEVEL
1 ; HIGH LEVEL
HI-Z ; HIGH IMPEDANCE

N74LS244DW (SIGNETICS) FLAT PACKAGE
SN74ALS244AN (TI)
SN74F244DW (TI) FLAT PACKAGE
SN74LS244N (TI)

TTL 3-STATE SCHMITT TRIGGER BUFFER/DRIVER
– TOP VIEW –

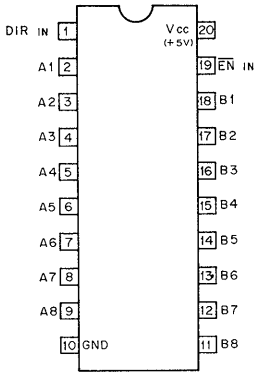


$\overline{G}$	A	Y
0	0	0
0	1	1
1	X	HI-Z

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE

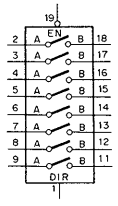
N74LS245DW (SIGNETICS) FLAT PACKAGE
SN74ALS245AN (TI)
SN74LS245N (TI)
SN74LS245NS (TI) FLAT PACKAGE

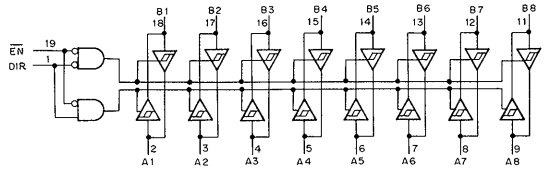
TTL BILATERAL SCHMITT TRIGGER BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
– TOP VIEW –



$\overline{EN}$	DIR	OPERATION
0	0	B to A
0	1	A to B
1	X	HI-Z

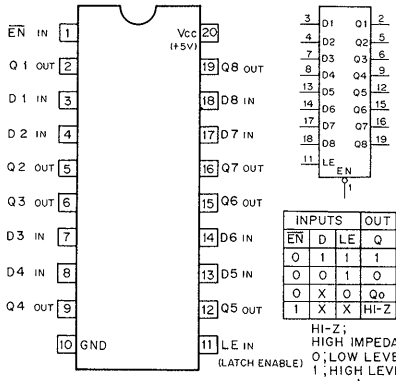
0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE





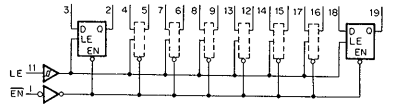
SN74LS373N (TI)

TTL 3-STATE OUTPUTS OCTAL LATCHES
– TOP VIEW –



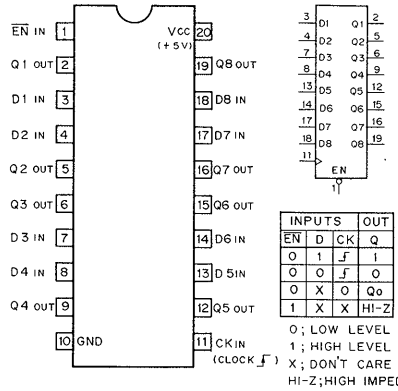
INPUTS			OUT
EN	D	LE	Q
0	1	1	1
0	0	1	0
0	X	0	Qo
1	X	X	HI-Z

HI-Z; HIGH IMPEDANCE
0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE



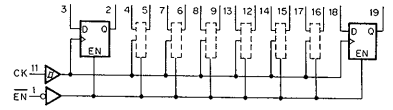
SN74LS374N (TI)

TTL 3-STATE OUTPUTS OCTAL D-TYPE FLIP-FLOP
– TOP VIEW –



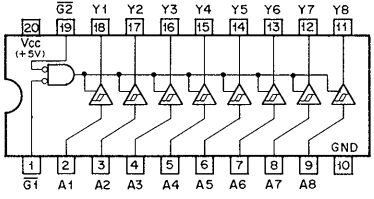
INPUTS			OUT
EN	D	CK	Q
0	1	↑	1
0	0	↑	0
0	X	0	Qo
1	X	X	HI-Z

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE



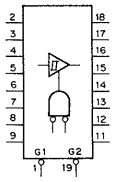
SN74LS541N (TI)

TTL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS
– TOP VIEW –



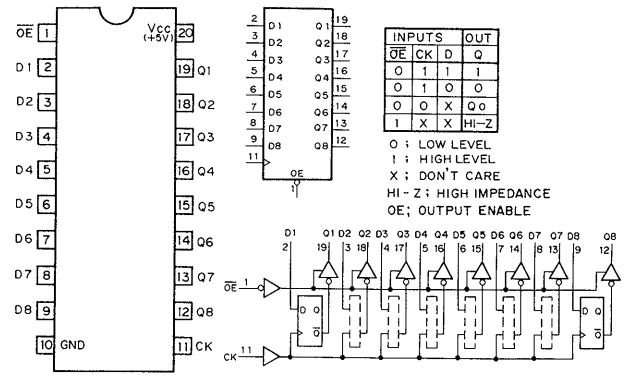
G1	G2	A	Y
0	0	0	0
0	0	1	1
1	X	X	HI-Z
X	1	X	HI-Z

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE



SN74ALS573BN (TI)

TTL 3-STATE OUTPUTS OCTAL D-TYPE LATCHES
– TOP VIEW –

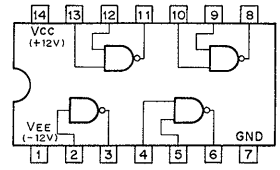


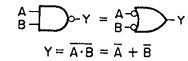
INPUTS			OUT
OE	CK	D	Q
0	↑	1	1
0	↑	0	0
0	0	X	Qo
1	X	X	HI-Z

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE
OE; OUTPUT ENABLE

SN75188N (TI)

2-INPUT (1-INPUT) POSITIVE-NAND LINE DRIVER
– TOP VIEW –



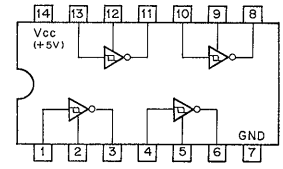


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

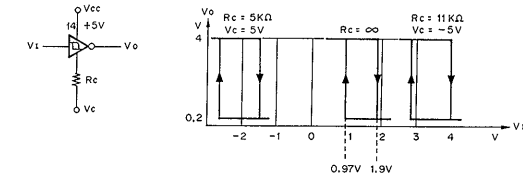
0:LOW LEVEL
1:HIGH LEVEL

SN75189AN (TI)

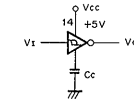
QUADRUPLE LINE RECEIVER
– TOP VIEW –



INPUT THRESHOLD SHIFTING

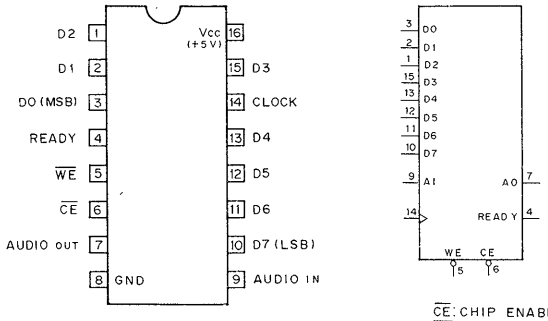


INPUT NOISE FILTERING



SN76489AN (TI)

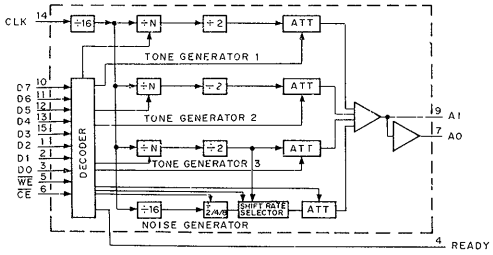
IIL PROGRAMMABLE SOUND GENERATION CONTROLLER
– TOP VIEW –



$\overline{CE}$	$\overline{WE}$	READY
1	X	1
0	1	0
0	0	0 (DURING 32 CLOCKES INPUT) → 1

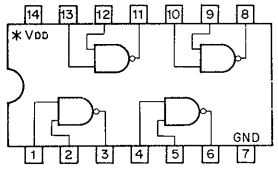
$\overline{CE}$: CHIP ENABLE
$\overline{WE}$: WRITE ENABLE
A1: AUDIO INPUT
AO: AUDIO OUTPUT

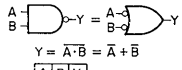
0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE



SN74HC00N (TI)
TC74HC00P (TOSHIBA)

C-MOS 2-INPUT NAND GATE
– TOP VIEW –





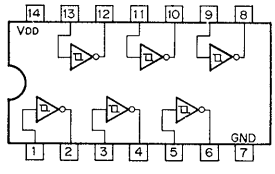
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

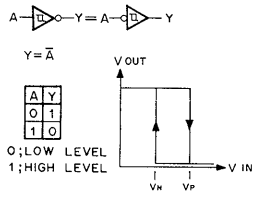
0; LOW LEVEL
1; HIGH LEVEL

*VDD HC; +2to+6V

SN74HC14N (TI) (V_{DD} = +2 to +6V)

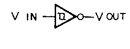
C-MOS SCHMITT TRIGGER INVERTER
– TOP VIEW –





A	Y
0	1
1	0

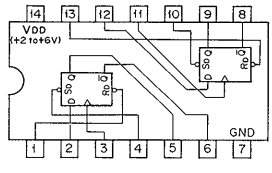
0; LOW LEVEL
1; HIGH LEVEL



VDD	VN	VP
2.0V	0.75V	1.25V
4.5V	1.9V	2.7V
6.0V	2.6V	3.6V

SN74HC74N (TI)

C-MOS D-TYPE FLIP FLOP WITH DIRECT SET/RESET
– TOP VIEW –

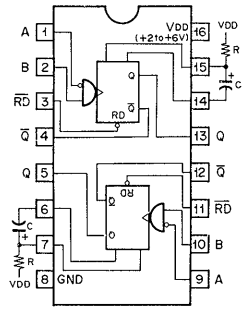


INPUTS				OUTPUTS	
$\overline{Sn}$	$\overline{Rn}$	CK	D	Qn+1	$\overline{Qn+1}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Qn	$\overline{Qn}$

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
1*; NONSTABLE

TC74HC123P (TOSHIBA)

C-MOS DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR
– TOP VIEW –



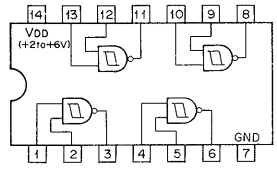
INPUT			OUTPUT	
$\overline{RD}$	A	B	Q	$\overline{Q}$
0	X	X	0	1
1	1	X	0	1
1	X	0	0	1
1	0	↑	⎍	⎍
1	↓	1	⎍	⎍
↓	0	1	⎍	⎍

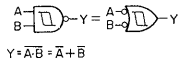
0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE

OUTPUT PULSE WIDTH = 0.46CR

MC74HC132N (MOTOROLA)
TC74HC132P (TOSHIBA)

C-MOS 2-INPUT NAND SCHMITT TRIGGER
– TOP VIEW –



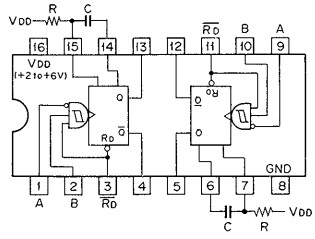


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

0; LOW LEVEL
1; HIGH LEVEL

TC74HC221P (TOSHIBA)

C-MOS MONOSTABLE MULTIVIBRATOR WITH SCHMITT TRIGGER INPUT
– TOP VIEW –



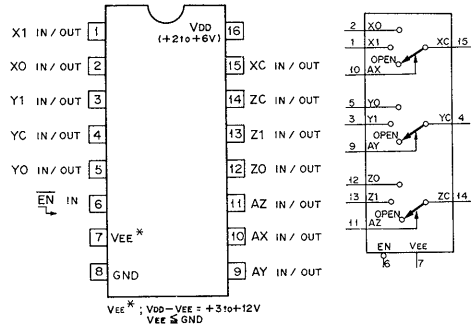
INPUTS			OUTPUTS	
$\overline{RD}$	A	B	Q	$\overline{Q}$
0	X	X	0	1
X	1	X	0	1
X	X	0	0	1
1	0	↑	⎍	⎍
1	↓	1	⎍	⎍
↑	0	1	⎍	⎍

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE

OUTPUT PULSE WIDTH = 0.7CR

TC74HC4053AP (TOSHIBA)

C-MOS 2-CHANNEL MULTIPLEXER/DEMULTIPLEXER
– TOP VIEW –



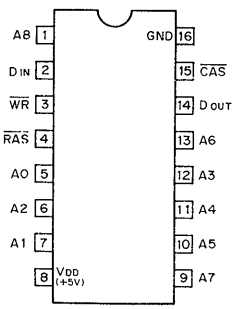
VEE* ; VDD−VEE = +3to+12V
VEE ≦ GND

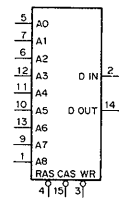
CONT. INPUTS		ON
$\overline{EN}$	A (X,Y,Z,)	CHANNEL
0	0	0
0	1	1
1	X	OPEN

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE.

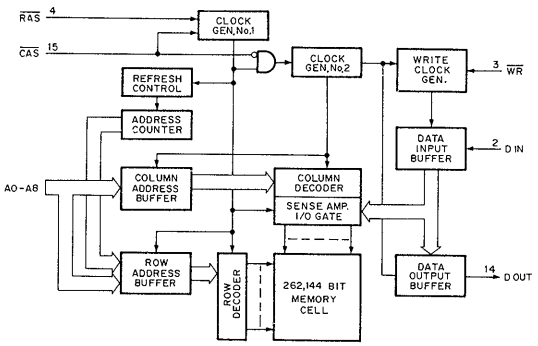
HM50256P-12 (HITACHI) (ACCESS TIME = 120nS)
MB81256-12P (FUJITSU) (ACCESS TIME = 120nS)

N-MOS 262,144-WORD BY 1-BIT DYNAMIC RAM
– TOP VIEW –



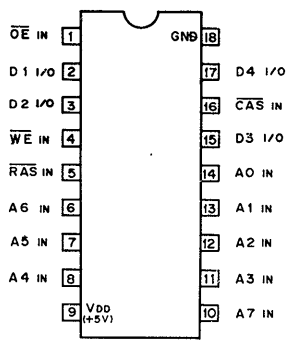


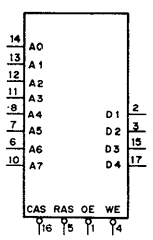
A0–A8 ; ADDRESS INPUT
$\overline{CAS}$; COLUMN ADDRESS STROBE
DIN ; DATA INPUT
Dout ; DATA OUTPUT
$\overline{RAS}$; ROW ADDRESS STROBE
$\overline{WR}$; WRITE ENABLE



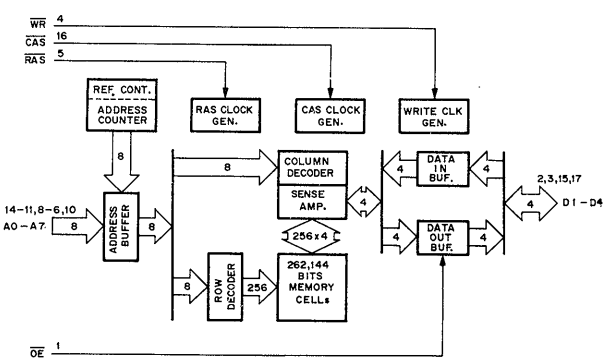
M5M4464P-10 (MITSUBISHI) (ACCESS TIME = 100nS)
MB81464-10 (FUJITSU) (ACCESS TIME = 100nS)
MB81464-12 (FUJITSU) (ACCESS TIME = 120nS)
MSM41464-10RS (OKI) (ACCESS TIME = 100nS)
uPD41464C-10 (NEC) (ACCESS TIME = 100nS)

N-MOS 262144-BIT (65536x4) DYNAMIC RAM
– TOP VIEW –



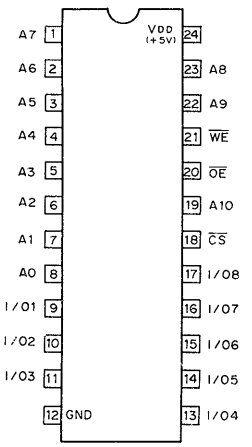


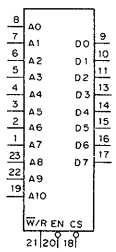
A0–A7 ; ADDRESS INPUT
$\overline{CAS}$; COLUMN ADDRESS STROBE
D1–D4 ; DATA IN/OUT
$\overline{OE}$; OUTPUT ENABLE
$\overline{RAS}$; ROW ADDRESS STROBE
$\overline{WE}$; WRITE ENABLE



TMM2018AP-25 (TOSHIBA)

N-MOS 16384 (2048x8)-BIT STATIC RAM
– TOP VIEW –

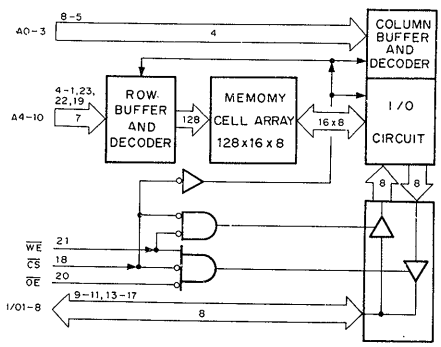




INPUTS			FUNCTION
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	
0	0	1	WRITE
0	1	0	READ
0	1	1	DISABLE (OUTPUT=HI-Z)
1	X	X	DISABLE (OUTPUT=HI-Z)

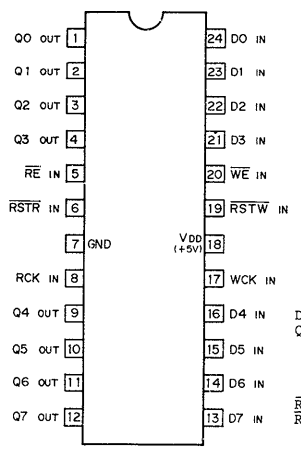
0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE

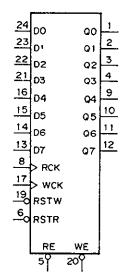
A0–10; ADDRESS INPUTS
I/O1–8; DATA INPUTS/OUTPUTS
$\overline{CS}$; CHIP SELECT INPUT
$\overline{OE}$; OUTPUT ENABLE INPUT
$\overline{WE}$; WRITE ENABLE INPUT



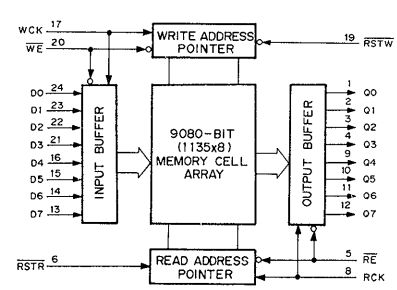
uPD42102C-3 (NEC) (ACCESS TIME = 21nS)

C-MOS 9080-BIT (1135x8) FIFO MEMORY
– TOP VIEW –



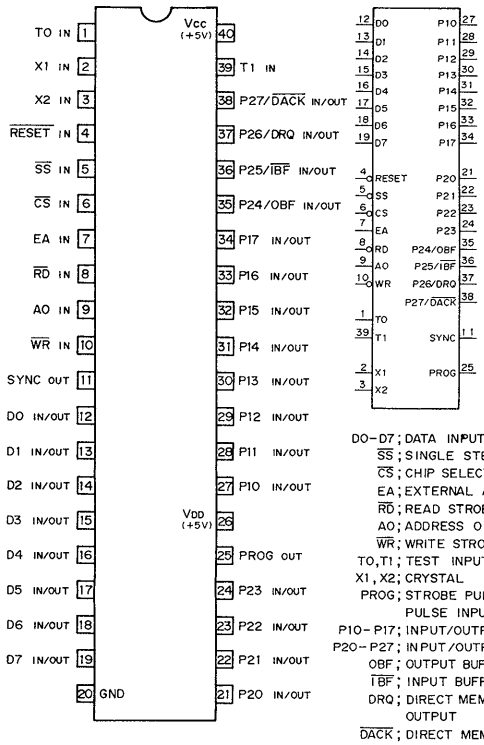


D0–7; DATA INPUTS
Q0–7; DATA OUTPUTS
WCK; WRITE CLOCK INPUT
RCK; READ CLOCK INPUT
$\overline{WE}$; WRITE ENABLE INPUT
$\overline{RE}$; READ ENABLE INPUT
$\overline{RSTW}$; RESET WRITE INPUT
$\overline{RSTR}$; RESET READ INPUT

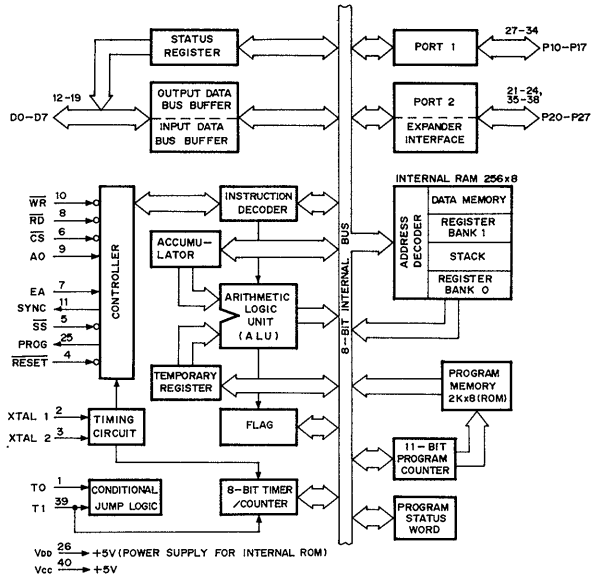


D8742 (INTEL)
P8742AH (INTEL)

N-MOS SINGLE CHIP 8-BIT MICROCOMPUTER
– TOP VIEW –

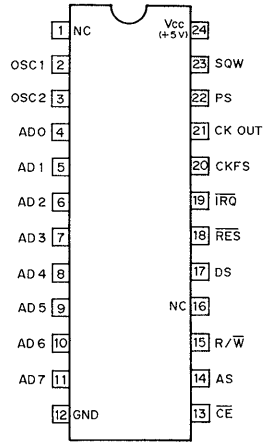


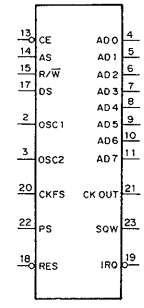
DO–D7 ; DATA INPUTS/OUTPUTS
SS ; SINGLE STEP INPUT
CS ; CHIP SELECT INPUT
EA ; EXTERNAL ADDRESS INPUT
RD ; READ STROBE INPUT
AO ; ADDRESS O INPUT
WR ; WRITE STROBE INPUT
TO,T1 ; TEST INPUTS
X1, X2; CRYSTAL
PROG ; STROBE PULSE OUTPUT/PROGRAM PULSE INPUT
P10–P17 ; INPUT/OUTPUT PORT 1
P20–P27 ; INPUT/OUTPUT PORT 2
OBF ; OUTPUT BUFFER FULL FLAG OUTPUT
IBF ; INPUT BUFFER FULL FLAG OUTPUT
DRQ ; DIRECT MEMORY ACCESS REQUEST OUTPUT
DACK ; DIRECT MEMORY ACCESS ACKNOWLEGDE OUTPUT



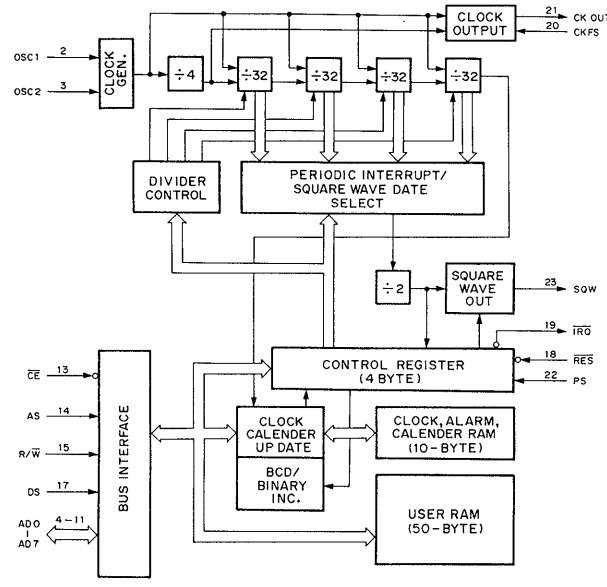
MC146818P (MOTOROLA)

C-MOS REAL TIME CLOCK + RAM
– TOP VIEW –



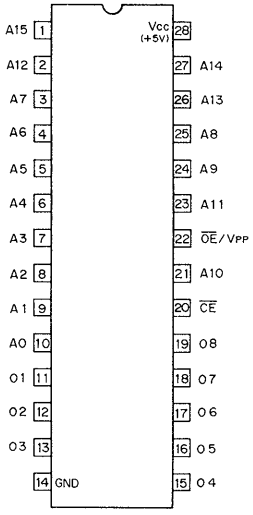


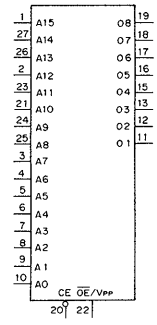
AD0–AD7 ; MULTIPLEXED ADDERSS/DATA BUS
AS ; MULTIPLEXED ADDERSS STROBE
CE ; CHIP ENABLE
CKFS ; CLOCK OUT FREQUENCY SELECT
CK OUT ; CLOCK OUT
DS ; DATA STROBE
IRQ ; INTERRUPT REQUEST (OPEN DRAIN)
OSC 1,2 ; CRYSTAL/EXTERNAL CLOCK INPUT
PS ; POWER SENSE
R/W ; READ/WRITE
RES ; RESET
SQW ; SQUARE WAVE



D27512J-2 (INTEL) (ACCESS TIME = 200nS)

N-MOS 512K-BIT ERASABLE PROM
– TOP VIEW –





A0-A15 ; ADDRESS BUS LINES
$\overline{CE}$; CHIP ENABLE
O1-O8 ; DATA OUTPUTS(INPUTS)
$\overline{OE}$; OUTPUT ENABLE
Vpp ; PROGRAM POWER SUPPLY

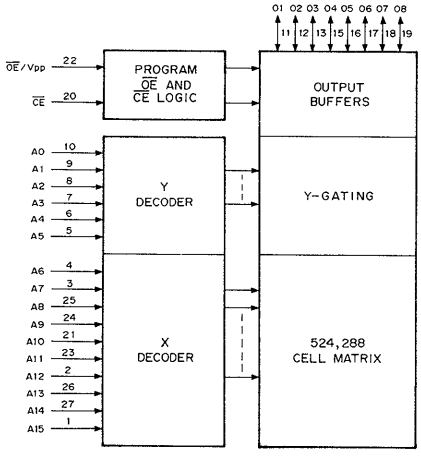
OPERATING MODES

CE	OE/Vpp	A0-A15	Vcc	O1-O8	MODE
0	0	X	+5V	OUTPUT	READ
0	1	X	+5V	HIGH-Z	OUTPUT DISABLE
1	X	X	+5V	HIGH-Z	STANBY
0	12.5V	X	+6V	INPUT	INTELIGENT PROGRAMMING
1	12.5V	X	+6V	HIGH-Z	PROGRAM INHIBIT
0	0	*1	+6V	CODE	INTELIGENT IDENTIFIER*2

*1; A1-A8,A10-A13 = 0 0; LOW LEVEL
A14,A15 = 1 1; HIGH LEVEL
A9 = 12.0±0.5V X; DON'T CARE

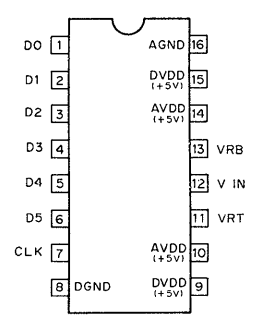
*2; INTELIGENT IDENTIFIER MODE

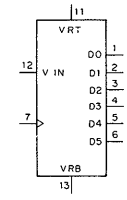
IDENTIFIER CODE	A0	O8	O7	O6	O5	O4	O3	O2	O1	DATA
MANUFACTURER	0	1	0	0	0	1	0	0	1	89H
DEVICE	1	0	0	0	0	1	1	0	1	0DH



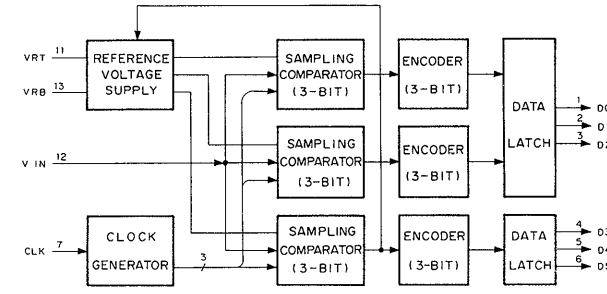
CXD1172P (SONY)

6 BITS 20 MSPS VIDEO A/D CONVERTER
– TOP VIEW –



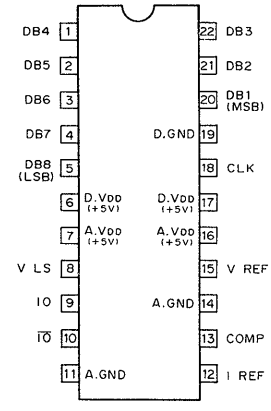


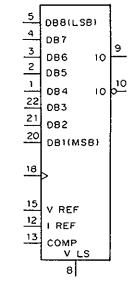
AGND; ANALOG GROUND
AVDD; ANALOG POWER SUPPLY
CLK; CLOCK INPUT
D0-5; DIGITAL DATA OUTPUTS (LSB to MSB)
DGND; DIGITAL GROUND
DVDD; DIGITAL POWER SUPPLY
V IN; ANALOG VOLTAGE INPUT
VRB; BOTTOM REFERENCE VOLTAGE INPUT
VRT; TOP REFERENCE VOLTAGE INPUT



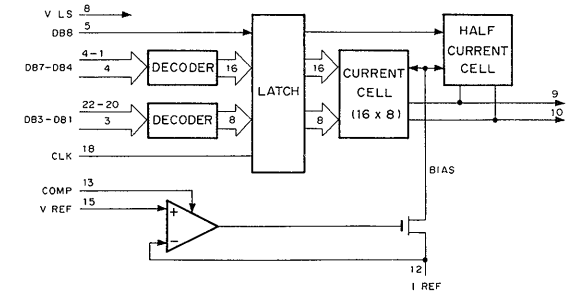
uPD6902C (NEC)

C-MOS 8-BIT D/A CONVERTER
– TOP VIEW –



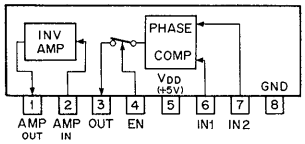


A.GND; ANALOG GROUND
A.VDD; ANALOG POWER SUPPLY
COMP; PHASE COMPENSATION
CLK; CLOCK INPUT
DB1-8; DIGITAL DATA INPUTS (MSB to LSB)
D.GND; DIGITAL GROUND
D.VDD; DIGITAL POWER SUPPLY
IO; ANALOG CURRENT OUTPUT
I REF; FULL SCALE CURRENT
V LS; VOLTAGE LEVEL SELECT ($\overline{C\text{-}MOS}$/TTL)
V REF; REFERENCE VOLTAGE



CX23065 (SONY)

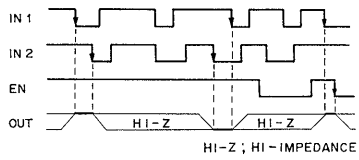
N-MOS PHASE COMPARATOR WITH INVERSION AMPLIFIER
– PRINTED SIDE VIEW –



EN	OUT
1	ACTIVE
0	HIGH IMPEDANCE

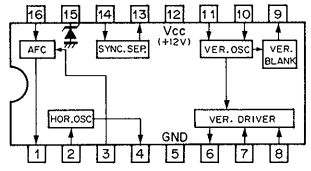
1; HIGH LEVEL
0; LOW LEVEL

TIMING CHART



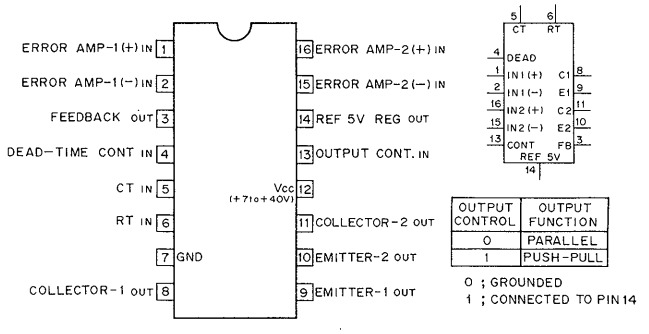
LA7801 (SANYO)

SYNCHRO, DEFLECTION CIRCUIT FOR COLOR TV
– TOP VIEW –



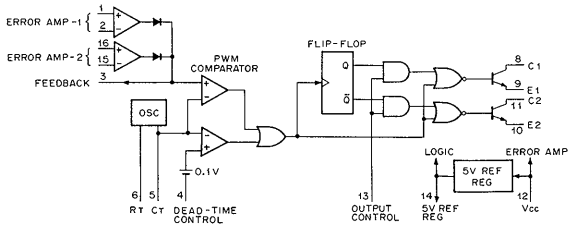
MB3759 (FUJITSU)

PWM POWER CONTROL
– TOP VIEW –



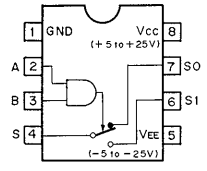
OUTPUT CONTROL	OUTPUT FUNCTION
0	PARALLEL
1	PUSH-PULL

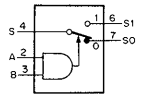
0 ; GROUNDED
1 ; CONNECTED TO PIN 14



TL601CP (TI)

P-MOS ANALOG SWITCH
– TOP VIEW –



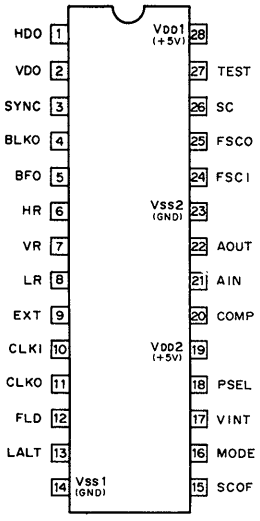


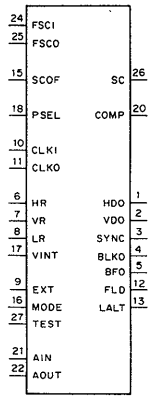
CONT IN		ON CHANNEL
A	B	
0	0	SO
0	1	SO
1	0	SO
1	1	S1

0; LOW LEVEL
1; HIGH LEVEL

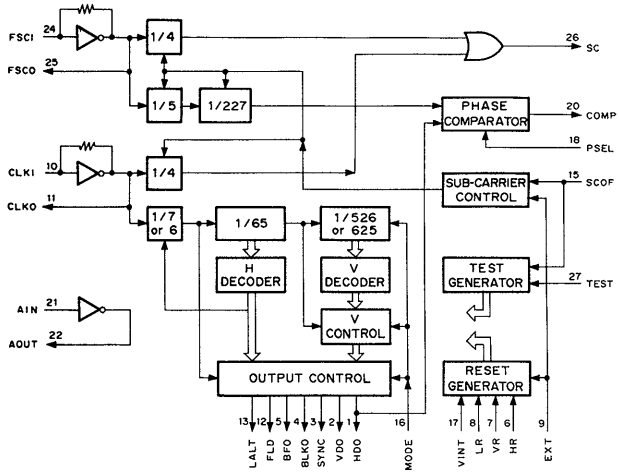
CXD1030M (SONY) FLAT PACKAGE

C-MOS SYNCHRONOUS SIGNAL GENERATOR
– TOP VIEW –





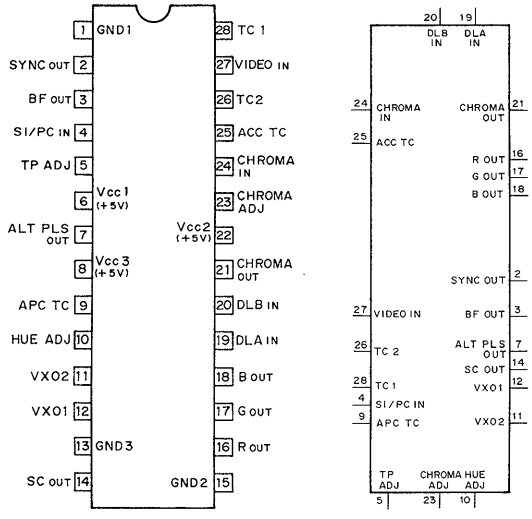
PIN No.	SYMBOL NAME	ABBREVATION
1	HDO	HORIZONTAL DRIVE PULSE OUTPUT
2	VDO	VARTICAL DRIVE PULSE OUTPUT
3	SYNC	COMPOSITE SYNCHRONOUS PULSE OUTPUT
4	BLKO	COMPOSITE BLANKING PULSE OUTPUT
5	BFO	BURST FLAG PULSE OUTPUT
6	HR	H RESET INPUT
7	VR	V RESET INPUT
8	LR	LINE ALTERNATE RESET INPUT
9	EXT	INTERNAL/EXTERNAL MODE SELECT
10	CLKI	CLOCK INPUT (NTSC:14.31818MHz, PAL:14.1875MHz)
11	CLKO	CLOCK OUTPUT
12	FLD	FIELD PULSE OUTPUT
13	VSS1	GND
14	LALT	LINE ALTERNATE PULSE OUTPUT
15	SCOF	SUB-CARRIER INPUT (ON/OFF)
16	MODE	NTSC/PAL MODE SELECT
17	VINT	INITIALRISE INPUT
18	PSEL	PHASE COMPARATE POLARITY SELECT
19	VDD2	+5V of INVERTER for FILTER
20	COMP	OUTPUT of PHASE COMPARATOR
21	AIN	INPUT of INVERTER for FILTER
22	AOUT	OUTPUT of INVERTER for FILTER
23	VSS2	GND of INVERTER for FILTER
24	FSCI	4fsc CLOCK INPUT
25	FSCO	4fsc CLOCK OUTPUT
26	SC	SUB-CRRIER OUTPUT
27	TEST	TEST INPUT (NORMALLY LOW LEVEL)
28	VDD1	+5V

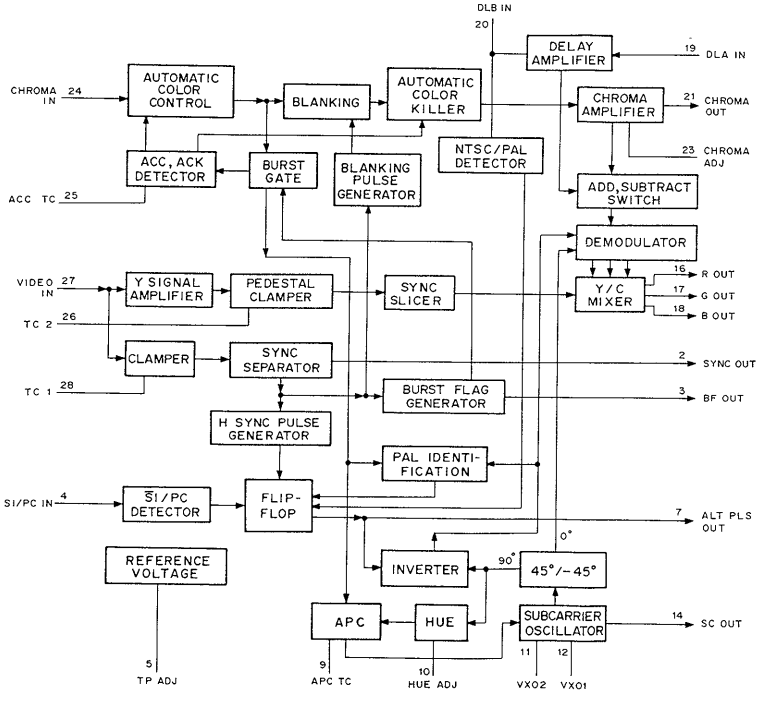


V7020 (SONY)

NTSC/PAL DECODER

– TOP VIEW –

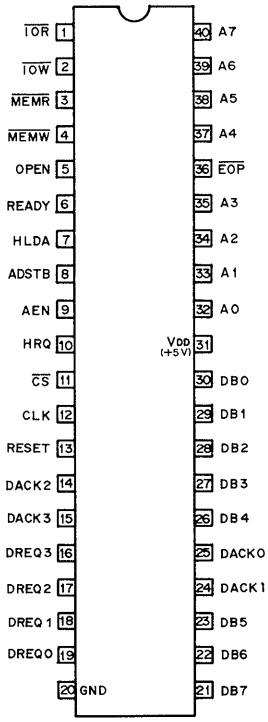


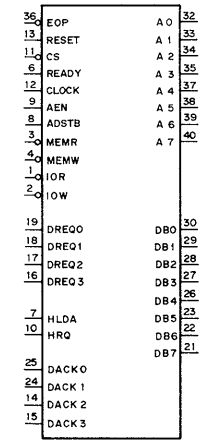


FUNCTION TABLE

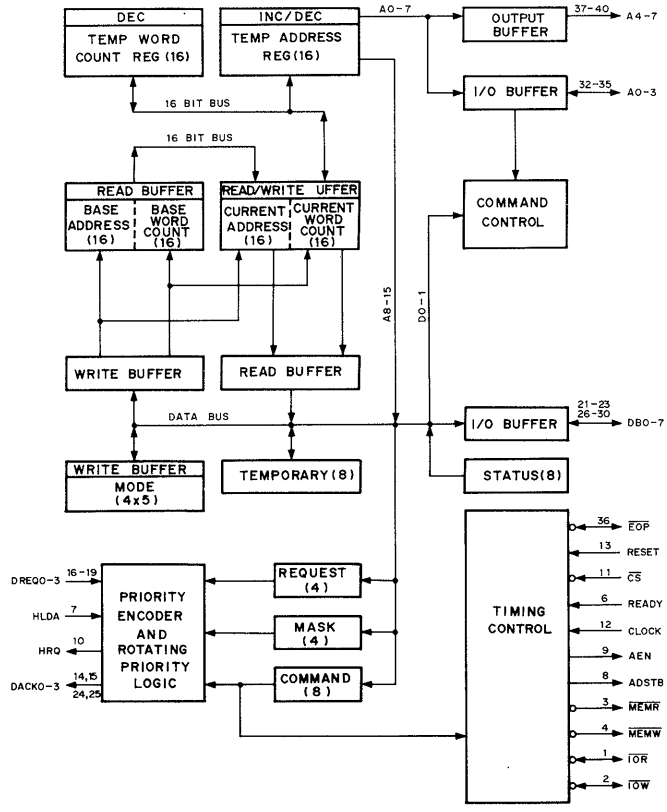
PIN NO.	SYMBOLIC NAME	DESCRIPTION
1	GND1	GROUND FOR Y SIGNAL AMPLIFIER AND SYNCHRONIZING SIGNAL SEPARATOR
2	SYNC OUT	SYNCHRONIZING SIGNAL OUTPUT(TTL LEVEL)
3	BF OUT	BURST FLAG OUTPUT (TTL LEVEL)
4	SI/PC IN	SUPERIMPOSE OR PERSONAL COMPUTER SELECTION SIGNAL INPUT SI MODE:LOW, PC MODE:HIGH
5	TP ADJ	BURST FLAG POSITION ADJUSTMENT
6	Vcc1	Vcc FOR Y SIGNAL AMPLIFIER AND SYNCHRONIZING SIGNAL SEPARATOR
7	ALT PLS OUT	LINE ALTERNATION PULSE OUTPUT NTSC MODE:LOW, PAL MODE:LINE ALTERNATION PULSE
8	Vcc3	Vcc FOR APC,HUE, AND VXO STAGES
9	APC TC	AUTOMATIC PHASE CONTROL TIME CONSTANT
10	HUE ADJ	HUE ADJUSTMENT
11	VXO2	
12	VXO1	CRYSTAL OSILLATOR
13	GND3	GROUND FOR APC,HUE, AND VXO STAGES
14	SC OUT	SUBCARRIER SIGNAL OUTPUT
15	GND2	GROUND FOR DEMODULATOR AND Y/C MIXER
16	R OUT	RED SIGNAL OUTPUT
17	G OUT	GREEN SIGNAL OUTPUT
18	B OUT	BLUE SIGNAL OUTPUT
19	DLA IN	DELAY AMPLIFIER INPUT
20	DLB IN	MODE SELECTION AND DELAY AMPLIFIER GAIN BIAS NTSC MODE: V20≦0.8V PAL MODE: 2.0V≦V20≦2.8V V20 IS THE VOLTAGE MUST BE APPLIED
21	CHROMA OUT	CHROMA SIGNAL OUTPUT
22	Vcc2	Vcc FOR DEMODULATOR AND Y/C MIXER
23	CHROMA ADJ	MODE SELECTION AND CHROMA AMPLIFIER GAIN ADJUSTMENT BLACK AND WHITE MODE: V23≦0.8V COLOR MODE : 2.0V≦V23≦3.0V V23 IS THE VOLTAGE MUST BE APPLIED
24	CHROMA IN	CHROMA SIGNAL INPUT
25	ACC TC	AUTOMATIC COLOR CONTROL TIME CONSTANT
26	TC2	TIME CONSTANT FOR PEDESTAL CLAMPER
27	VIDEO IN	VIDEO SIGNAL INPUT
28	TC1	TIME CONSTANT FOR SYNCHRONIZING SIGNAL SEPARATOR

P8237A-5 (INTEL)
N-MOS PROGRAMMABLE DMA CONTROLLER
— TOP VIEW —

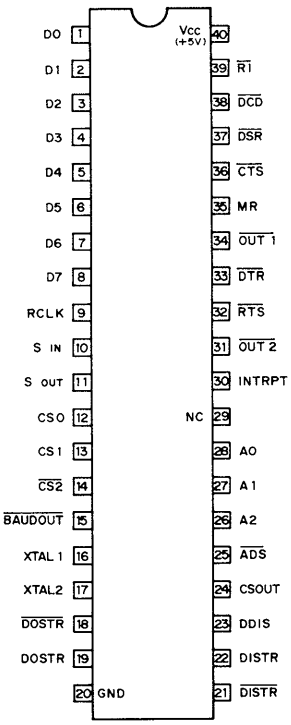


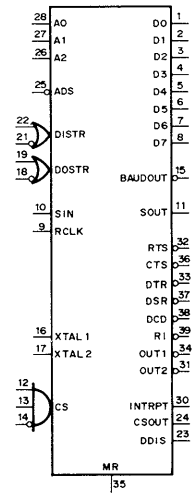


A0~7	;	ADDRESS
ADSTB	;	ADDRESS STROBE
AEN	;	ADDRESS ENABLE
CLK	;	CLOCK
$\overline{CS}$	;	CHIP SELECT
DACK0-3	;	DMA ACKNOWLEDGE
DB0-7	;	DATA BUS
DREQ0-3	;	DMA REQUEST
$\overline{EOP}$	;	END OF PROCESS
HLDA	;	HOLD ACKNOWLEDGE
HRQ	;	HOLD REQUEST
$\overline{IOR}$	;	I/O READ
$\overline{IOW}$	;	I/O WRITE
$\overline{MEMR}$	;	MEMORY READ
$\overline{MEMW}$	;	MEMORY WRITE



INS8250AN (NS)
ASYNCHRONOUS COMMUNICATION INTERFACE
— TOP VIEW —

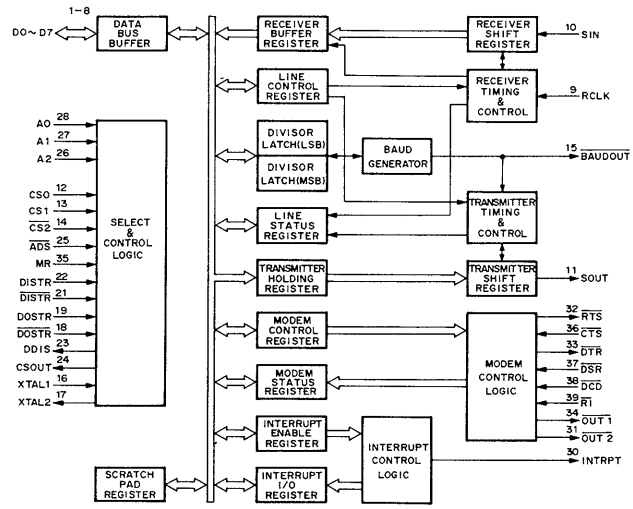




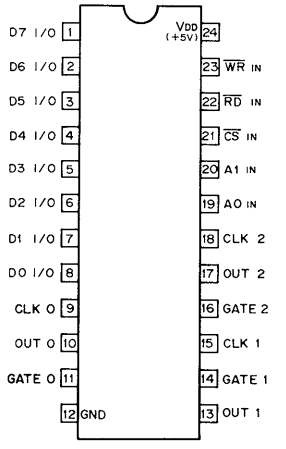
A0-2	;	REGISTER SELECT
ADS	;	ADDRESS STROBE
BAUDOUT	;	BAUD OUT
CS0-2	;	CHIP SELECT 0-2
CSOUT	;	CHIP SELECT OUT
CTS	;	CLEAR TO SEND
D0-7	;	DATA BUS 0-7
DCD	;	DATA CARRIER DETECT
DDIS	;	DRIVER DISABLE
DISTR	;	DATA INPUT STROBE
DOSTR	;	DATA OUTPUT STROBE
DSR	;	DATA SET READY
DTR	;	DATA TERMINAL READY
INTRPT	;	INTERRUPT
MR	;	MASTER RESET
OUT1, 2	;	OUTPUT1, 2
RCLK	;	RECEIVER CLOCK
RI	;	RING INDICATOR
RTS	;	REQUEST TO SEND
SIN	;	SERIAL INPUT
SOUT	;	SERIAL OUTPUT
XTAL1, 2	;	CRYSTAL1, 2

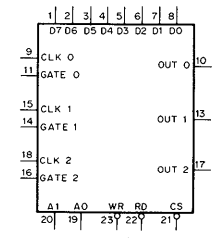
DLAB	A2	A1	A0	REGISTER
0	0	0	0	RECEIVER BUFFER(READ), TRANSMITTER HOLDING REGISTER(WRITE)
0	0	0	1	INTERRUPT ENABLE
X	0	1	0	INTERRUPT IDENTIFICATION(READ ONLY)
X	0	1	1	LINE CONTROL
X	1	0	0	MODEM CONTROL
X	1	0	1	LINE STATUS
X	1	1	0	MODEM STATUS
X	1	1	1	SCRATCH PAD
1	0	0	0	DIVISOR LATCH(LEAST SIGNIFICANT BYTE)
1	0	0	1	DIVISOR LATCH(MOST SIGNIFICANT BYTE)

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE



P8254 (INTEL)
N-MOS PROGRAMMABLE INTERVAL TIMER
— TOP VIEW —



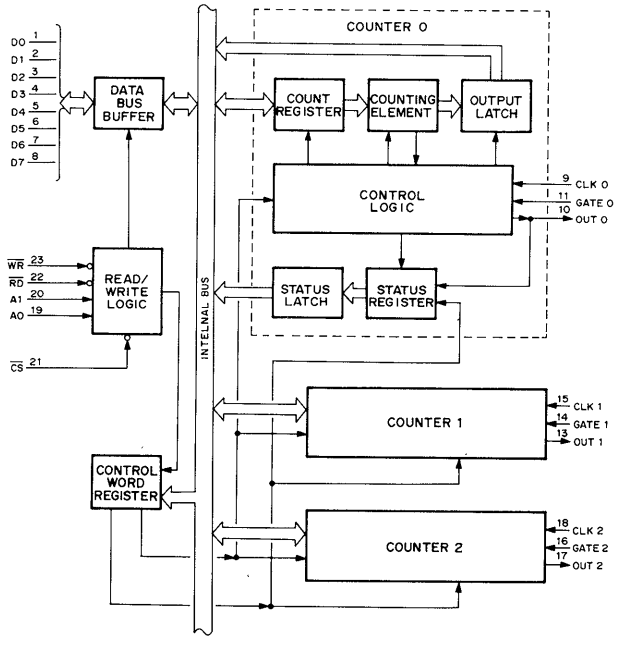


D7-D0 ; 8-BIT DATA I/O
CLK n ; COUNTER CLOCK INPUT
GATE n; COUNTER GATE INPUT
OUT n ; COUNTER CLOCK OUTPUT
$\overline{RD}$; READ COUNTER or STATUS
$\overline{WR}$; WRITE COMMAND or DATA
$\overline{CS}$; CHIP SELECT
A1,A0 ; SELECTED FUNCTION

FUNCTION TABLE

INPUTs					FUNCTION
-CS	-RD	-WR	A1	A0	
0	1	0	0	0	WRITE into COUNTER 0
0	1	0	0	1	WRITE into COUNTER 1
0	1	0	1	0	WRITE into COUNTER 2
0	1	0	1	1	WRITE CONTROL WORD
0	0	1	0	0	READ from COUNTER 0
0	0	1	0	1	READ from COUNTER 1
0	0	1	1	0	READ from COUNTER 2
0	0	1	1	1	NO OPERATION(HI-Z)
1	X	X	X	X	NO OPERATION(HI-Z)
0	1	1	X	X	NO OPERATION(HI-Z)

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE



CONTROL WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SCn; SELECT COUNTER

SC1	SC0	OPERATION
0	0	COUNTER 0
0	1	COUNTER 1
1	0	COUNTER 2
1	1	*READ-BACK COMMAND

RWn; READ/WRITE

RW1	RW0	OPERATION
0	0	COUNTER LATCHING
0	1	LSB ONLY
1	0	MSB ONLY
1	1	LSB FIRST then MSB

Mn; MODE

M2	M1	M0	MODE
0	0	0	0
0	0	1	1
X	1	0	2
X	1	1	3
1	0	0	4
1	0	1	5

BCD; BINARY DECODED DECIMAL

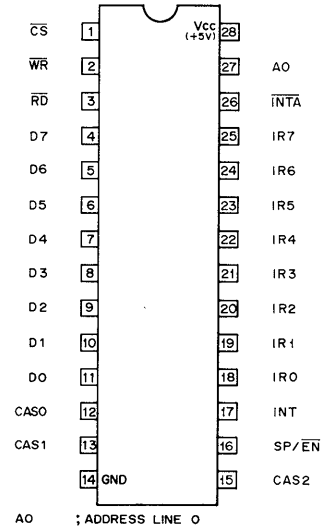
BCD	OPERATION
0	16-BIT BAINRY COUNTER
1	BCD COUNTER(4-DECODED)

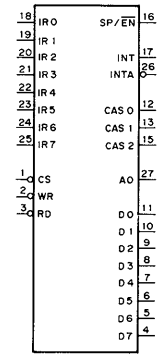
***; READ-BACK COMMAND FORMAT**

D7	D6	D5	D4	D3	D2	D1	D0
1	1	-LC	-LS	C2	C1	C0	RE

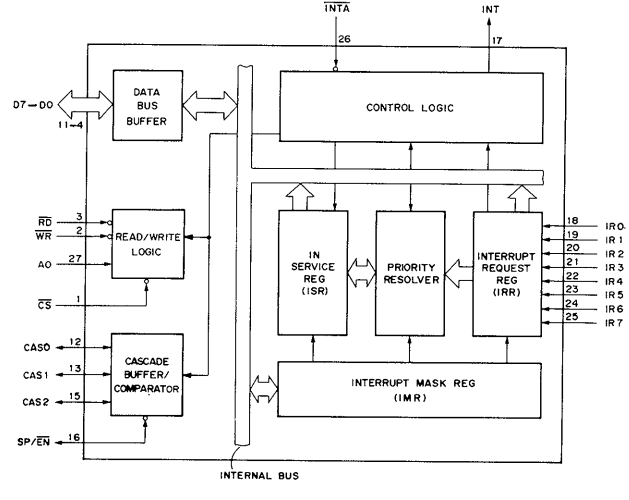
-LC; LATCH COUNT of SELECTED COUNTER(S)
-LS; LATCH STATUS of SELECTED COUNTER(S)
C2; SELECTED COUNTER 2
C1; SELECTED COUNTER 1
C0; SELECTED COUNTER 0
RE; RESERVED for FUTURE EXPANSION: MUST BE 0

P8259A (INTEL)
N-MOS PROGRAMMABLE INTERRUPT CONTROLLER
— TOP VIEW —

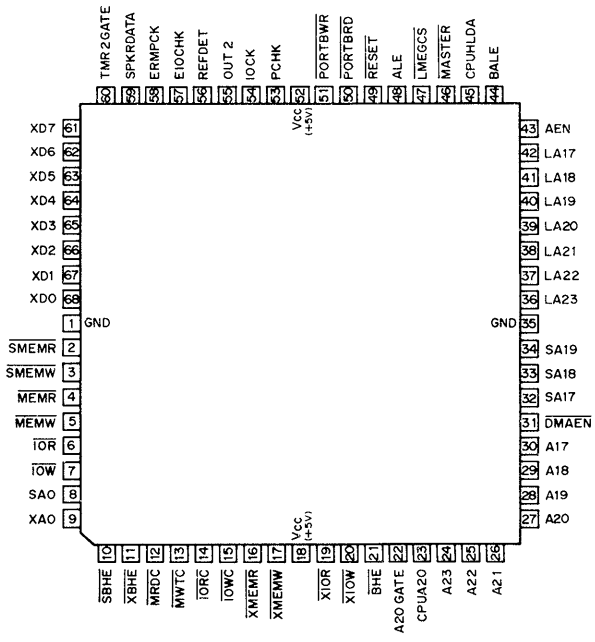


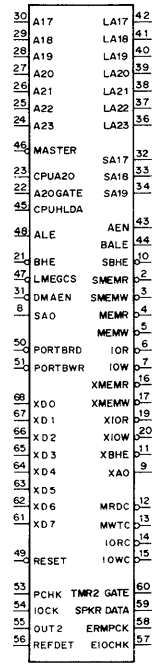


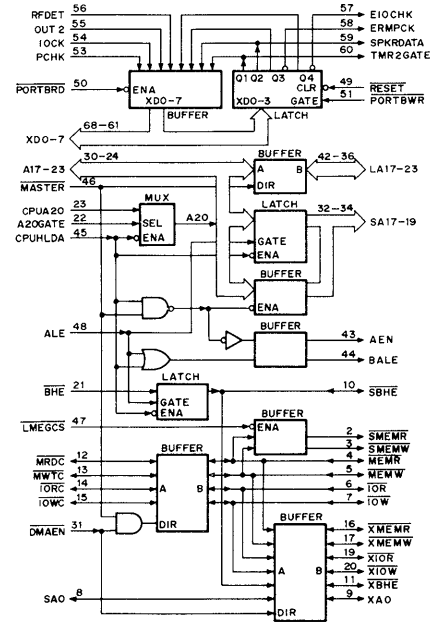
A0 ; ADDRESS LINE 0
CAS0-2; CASCADE LINES 0-2
$\overline{CS}$; CHIP SELECT
D0-D7 ; BIDIRECTIONAL DATA BUS 0-7
INT ; INTERRUPT
$\overline{INTA}$; INTERRUPT ACKNOWLEDGE
IR0-7 ; INTERRUPT REQUEST 0-7
$\overline{RD}$; READ
SP/$\overline{EN}$; SLAVE PROGRAM/$\overline{ENABLE\ BUFFER}$
$\overline{WR}$; WRITE



P82A203 (CHIPS)
TTL HIGH ADDRESS BUS BUFFER AND PORT B CHIP
— TOP VIEW —

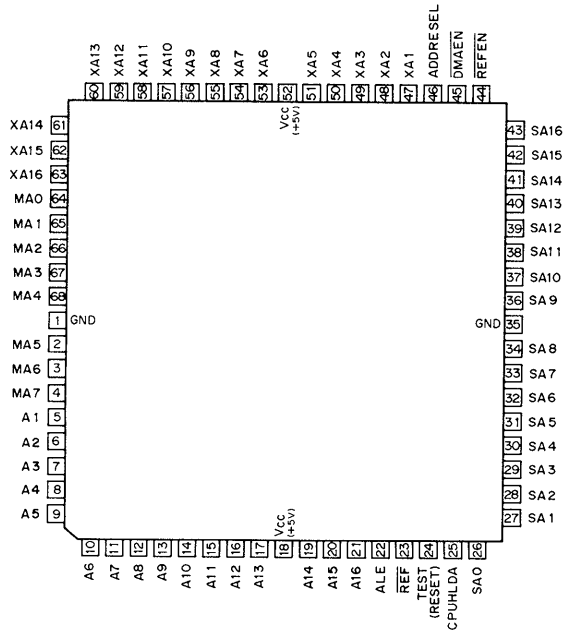


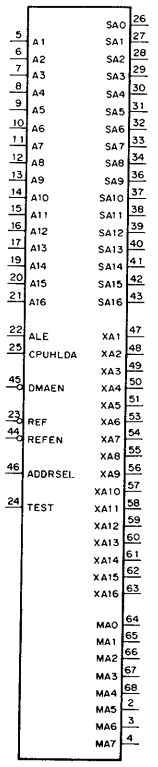


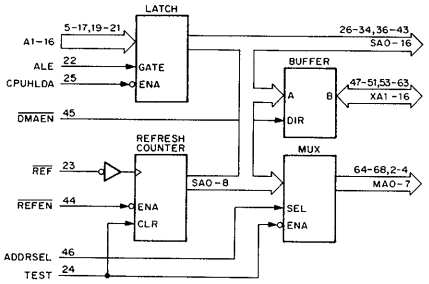



```
A17-23    ; CPU ADDRESS BUS
A20GATE   ; ADDRESS 20 GATE
AEN       ; ADDRESS ENABLE
ALE       ; ADDRESS LATCH ENABLE
BALE      ; BUFFERED ADDRESS LATCH ENABLE
BHE       ; BUS HIGH ENABLE
CPUA20    ; CPU ADDRESS 20
CPUHLDA   ; CPU HOLD ACKNOWLEDGE
DMAEN     ; DMA ADDRESS ENABLE
EIOCHK    ; ENABLE I/O CHECK
ERMPCK    ; ENABLE RAM PARITY CHECK
IOCK      ; I/O CHANNEL CHECK
IOR       ; I/O READ (EXPANSION BUS)
IORC      ; I/O READ CYCLE
IOW       ; I/O WRITE (EXPANSION BUS)
IOWC      ; I/O WRITE CYCLE
LA17-23   ; LOCAL SYSTEM ADDRESS BUS
LMEGCS    ; LOW MEGABYTE CHIP SELECT
MASTER    ; MASTER
MEMR      ; MEMORY READ COMMAND (LOCAL MEMORY)
MEMW      ; MEMORY WRITE COMMAND (LOCAL MEMORY)
MRDC      ; MEMORY READ CYCLE
MWTC      ; MEMORY WRITE CYCLE
OUT2      ; OUTPUT FROM THE TIMER 2 (8254)
PCHK      ; PARITY CHECK
PORTBRD   ; PORT B READ
PORTBWR   ; PORT B WRITE
REFDET    ; REFRESH DETECT
RESET     ; RESET (PORT B LACTH)
SA0       ; ADDRESS 0 (CPU BUS)
SA17-19   ; SYSTEM ADDRESS BUS (EXPANSION BUS)
SBHE      ; BUS HIGH ENABLE (EXPANSION BUS)
SMEMR     ; MEMORY READ COMMAND (EXPANSION BUS)
SMEMW     ; MEMORY WRITE COMMAND (EXPANSION BUS)
SPKRDATA  ; SPEAKER DATA
TMR2GATE  ; TIMER 2 GATE SIGNAL ENABLE
XA0       ; ADDRESS 0 (LOCAL I/O BUS)
XBHE      ; BUS HIGH ENABLE (PERIPHERAL BUS)
XD0-3     ; DATA BUS (INPUT/OUTPUT)
XD4-7     ; DATA BUS (OUTPUT)
XIOR      ; I/O READ (PERIPHERAL BUS)
XIOW      ; I/O WRITE (PERIPHERAL BUS)
XMEMR     ; MEMORY READ (PERIPHERAL BUS)
XMEMW     ; MEMORY WRITE (PERIPHERAL BUS)
```

P82A204 (CHIPS)
TTL LOW ADDRESS BUS BUFFER AND REFRESH COUNTER
— TOP VIEW —

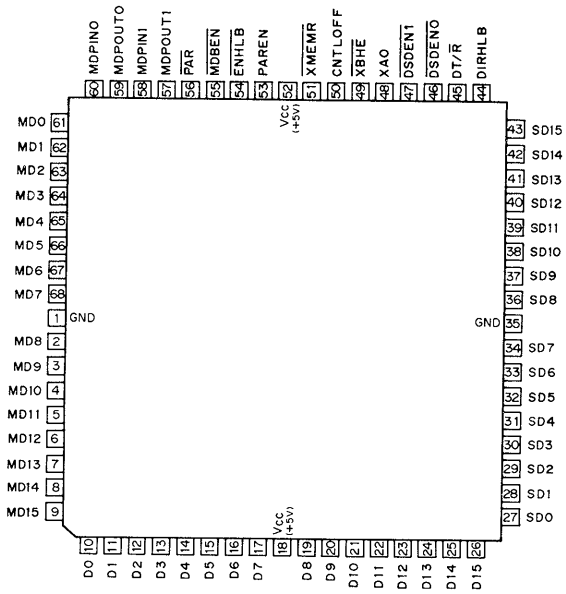


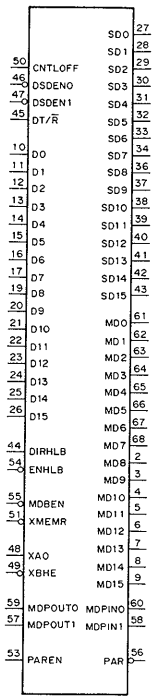




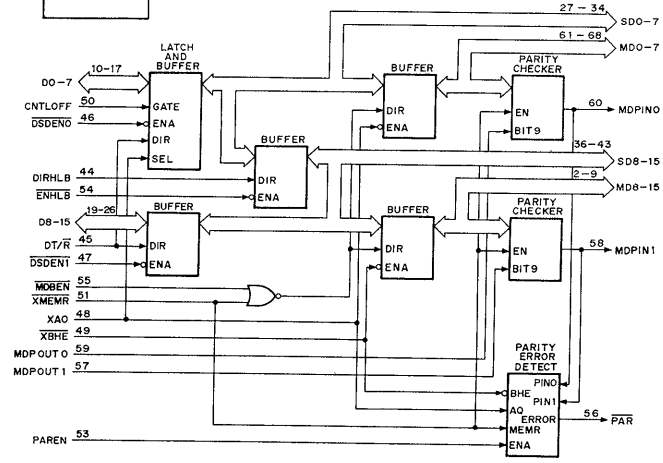
A1-16 ; MEMORY ADDRESS BUS INPUT
ADDRSEL ; ADDRESS SELECT
ALE ; ADDRESS LATCH ENABLE
CPUHLDA ; CPU HOLD ACKNOWLEDGE
$\overline{\text{DMAEN}}$; DIRECT MEMORY ACCESS ENABLE
MA0-7 ; MEMORY ADDRESS BUS OUTPUT
$\overline{\text{REF}}$; REFRESH
$\overline{\text{REFEN}}$; REFRESH ENABLE
SA0 ; SYSTEM ADDRESS 0 (REFRESH ADDRESS)
SA1-16 ; SYSTEM ADDRESS BUS
TEST ; WHEN "1",RESET THE REFRESH COUNTER
AND TRI-STATES MA0-7
WHEN "0",IN NORMAL OPERATION
XA1-16 ; PERIPHERAL ADDRESS BUS

P82A205 (CHIPS)
TTL DATA BUS BUFFER AND PARITY GENERATION AND CHECK CHIP
— TOP VIEW —



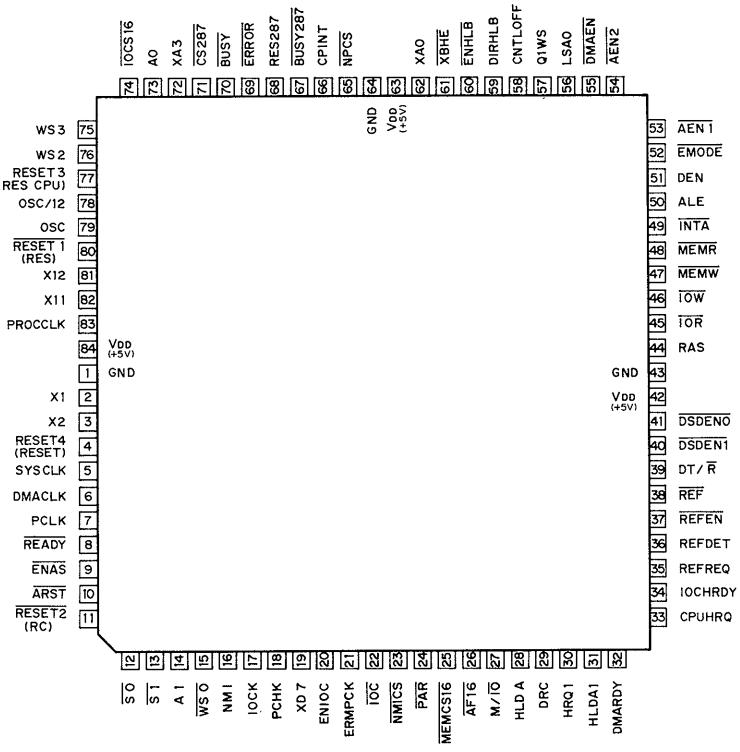


CNTLOFF ; CONTROL OFF
D0-15 ; CPU DATA BUS
$\overline{\text{DIRHLB}}$; DIRECTION OF HIGH TO LOW BYTE
$\overline{\text{DSDEN}}$0-1 ; DATA STROBE ENABLE
$\overline{\text{DT/R}}$; DATA TRANSMIT/$\overline{\text{RECEIVE}}$
$\overline{\text{ENHLB}}$; ENABLE HIGH TO LOW BYTE SIGNAL
$\overline{\text{MD0-15}}$; MEMORY DATA BUS
$\overline{\text{MDBEN}}$; MEMORY DATA BUS ENABLE
MDPIN0-1 ; MEMORY DATA PARITY IN
$\overline{\text{MDPOUT0-1}}$; MEMORY DATA PARITY OUT
$\overline{\text{PAR}}$; PARITY (ERROR)
PAREN ; PARITY ENABLE
SD0-15 ; SYSTEM DATA BUS
XA0 ; ADDRESS 0
$\overline{\text{XBHE}}$; BUS HIGH ENABLE
$\overline{\text{XMEMR}}$; MEMORY READ



P82C201 (CHIPS)
P82C201-10 (CHIPS)

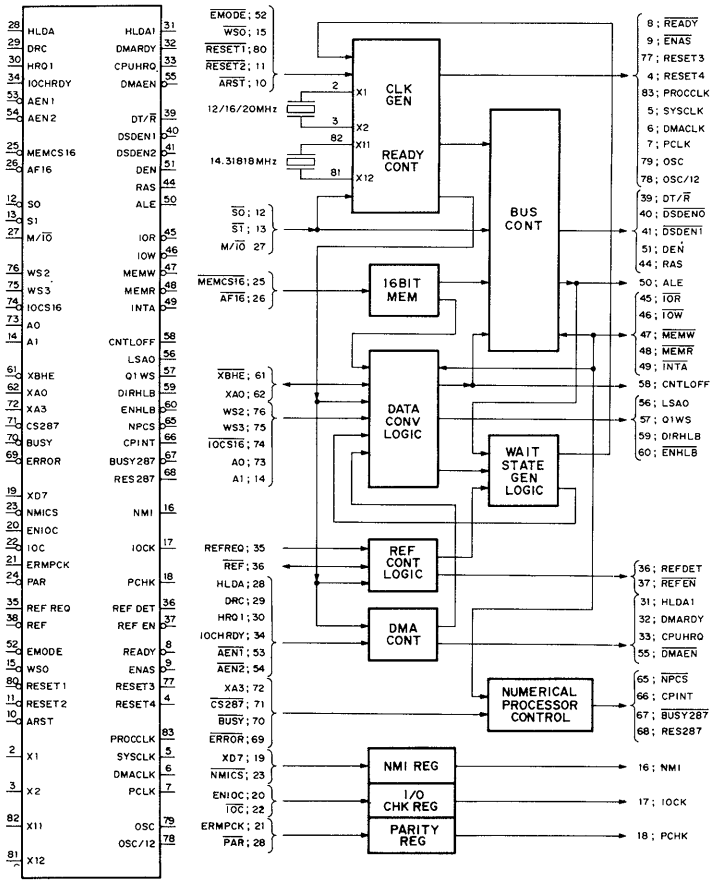
C-MOS SYSTEM CONTROL CHIP
– TOP VIEW –



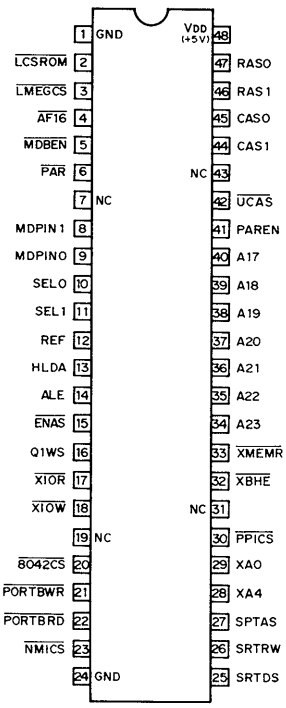
A0 (I) ; ADDRESS 0. FROM CPU.
A1 (I) ; ADDRESS 1. FROM CPU.
AEN1 (I) ; ADDRESS ENABLE 1. FOR 8-BIT DATA TRANSFERS.
AEN2 (I) ; ADDRESS ENABLE 2. FOR 16-BIT DATA TRANSFERS.
AF16 (I) ; FOR 16-BIT MEMORY ACCESSES ARE MADE.
ALE (O) ; ADDRESS LATCH ENABLE.
ARST (I) ; ASYNCHRONOUS RESET.
BUSY (I) ; BUSY. FROM 80287.
BUSY287 (O) ; BUSY 80287. FOR CPU.
CNTLOFF (O) ; CONTROL OFF.
CPINT (O) ; COPROCESSOR INTERRUPT. FROM 80287.
CPUHRQ (O) ; CPU HOLD REQUEST. TO CPU.
CS287 (I) ; CHIP SELECT 80287. FOR 80287.
DEN (O) ; DATA ENABLE. FOR LOCAL DATA BUS.
DIRHLB (O) ; DIRECTION FOR HIGH TO LOW BYTE.
/FROM 8-BIT PERIPHERAL BUS.
DMACLK (O) ; DMA CLOCK. FOR DMA CONTROLLER.
DMAEN (O) ; DMA ADDRESS ENABLE.
DMARDY (O) ; DMA READY. FOR DMA CONTROLLER.
DRC (I) ; DMA READY CLOCK. FOR DMA CONTROLLERS.
DSDEN0 (O) ; DATA STROBE DATA ENABLE. LOW BYTE(D0-7) DATA BUS.
DSDEN1 (O) ; DATA STROBE DATA ENABLE. HIGH BYTE(D8-15) DATA BUS.
DT/R (O) ; DATA TRANSMIT/RECEIVE. FOR LOCAL DATA BUS.
EMODE (I) ; EARLY MODE.
ENAS (O) ; ENABLE ADDRESS STROBE. FOR MC146818.
ENHLB (O) ; ENABLE HIGH TO LOW BYTE.
ENIOC (I) ; ENABLE I/O CHECK.
ERMPCK (I) ; ENABLE RAM PARITY CHECK.
ERROR (I) ; ERROR. FROM 80287.
HLDA (I) ; HOLD ACKNOWLEDGE. FROM CPU.
HLDA1 (O) ; HOLD ACKNOWLEDGE 1. FOR DMA CONTROLLER.
HRQ1 (I) ; HOLD REQUEST 1. FROM DMA CONTROLLER.
INTA (O) ; INTERRUPT ACKNOWLEDGE. FOR INTERRUPT CONTROLLERS.
IOC (I) ; I/O CHECK. FROM I/O DEVICE.
IOCHRDY (I) ; I/O CHANNEL READY. FROM I/O DEVICE.
IOCK (O) ; I/O CHECK. FOR CPU.
IOCS16 (I) ; I/O CHIP SELECT 16.
/TO AN I/O DEVICE FOR 16-BIT ACCESS.
IOR (I/O) ; I/O READ. FOR I/O DEVICES.
IOW (I/O) ; I/O WRITE. FOR I/O DEVICES.
LSA0 (O) ; ADDRESS 0. FOR SYSTEM BUS.
M/IO (I) ; MEMORY I/O SELECT. FROM CPU.
MEMCS16 (I) ; MEMORY CHIP SELECT.
/WHEN 16-BIT MEMORY ACCESSES ARE MADE.
MEMR (I/O) ; MEMORY READ COMMAND. INSTRUCTS A MEMORY DEVICE.
MEMW (I/O) ; MEMORY WRITE COMMAND. INSTRUCTS A MEMORY DEVICE.
NMI (O) ; NON-MASKABLE INTERRUPT. TO NMI OF CPU.
NMICS (I) ; NON-MASKABLE INTERRUPT CHIP SELECT. TO CPU.
NPCS (O) ; NUMERICAL PROCESSOR CHIP SELECT. FOR 80287.
OSC (O) ; OSCILLATOR OUTPUT. FOR VIDEO CLOCK.
OSC/12 (O) ; OSCILLATOR DIVIDE BY 12. FOR COUNTER TIMER.
PAR (I) ; PARITY ERROR.
PCHK (O) ; PARITY CHECK. FOR CPU.
PCLK (O) ; PERIPHERAL CLOCK(=PROCCLK/2).
/FOR PERIPHERAL CONTROLLERS.
PROCCLK (O) ; PROCESSOR CLOCK. FOR CPU.
Q1WS (O) ; ONE WAIT STATE. FOR SLOWER I/O DEVICES.
RAS (O) ; ROW ADDRESS SELECT. FOR MEMORY ACCESSES.
READY (O) ; READY OUTPUT.
REF (I/O) ; REFRESH. FOR DYNAMIC RAMS.
REFEN (O) ; REFRESH ENABLE.
REFDET (O) ; REFRESH DETECT.
REFREQ (I) ; REFRESH REQUEST. FROM 8254.
RES287 (O) ; RESET 80287. FOR 80287
RESET1 (I) ; RESET 1(RES). FROM POWER GOOD SIGNAL.
RESET2 (I) ; RESET 2(RC). FROM 8042.
RESET3 (O) ; RESET 3(RES CPU). TO RESET OF CPU.
RESET4 (O) ; RESET 4(RESET). FOR THE SYSTEM.
S0,S1 (I) ; BUS CYCLE STATUS. FROM CPU.
SYSCLK (O) ; SYSTEM CLOCK(=PROCCLK/2). FOR PERIPHERAL DEVICES.
WS0 (I) ; ZERO WAIT STATE OPTION.
WS2 (I) ; TWO WAIT STATE OPTION.
WS3 (I) ; THREE WAIT STATE OPTION.
X1 (I) ; CRYSTAL CONNECTION OR CLOCK INPUT FOR CPU CLOCK.
X11 (I) ; CRYSTAL CONNECTION OR CLOCK INPUT FOR VIDEO CLOCK.
X12 (I) ; CRYSTAL CONNECTION FOR VIDEO CLOCK.
X2 (I) ; CRYSTAL CONNECTION FOR CPU CLOCK.
XA0 (I/O) ; ADDRESS 0.
XA3 (I) ; ADDRESS 3. FOR CHIP SELECT AND RESET FOR 80287.
XBHE (I/O) ; BUS HIGH ENABLE. FOR HIGH BYTE DATA BUS.
XD7 (I) ; PERIPHERAL DATA BUS BIT 7. FOR CPU.

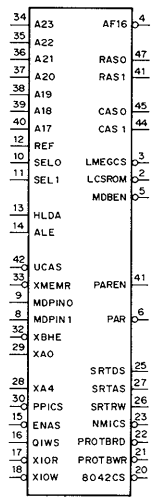
M/IO	-S1	-S0	TYPE OF BUS CYCLE
0	0	0	INTERRUPT ACKNOWLEDGE
0	0	1	I/O READ
0	1	0	I/O WRITE
0	1	1	NONE ; IDLE
1	0	0	HALT OR SHUTDOWN
1	0	1	MEMORY READ
1	1	0	MEMORY WRITE
1	1	1	NONE ; IDLE

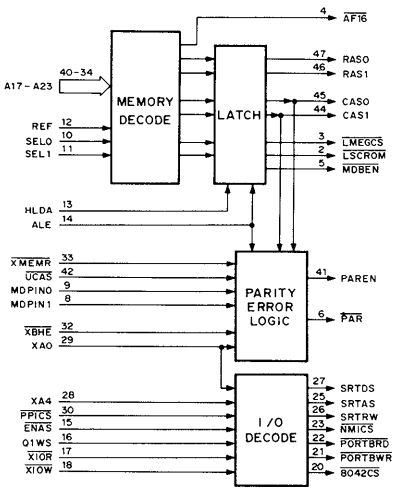
0 ; LOW LEVEL
1 ; HIGH LEVEL



P82C202 (CHIPS)
C-MOS RAM/ROM DECODE I/O CONTROL CHIP
— TOP VIEW —








```
8042CS      ; 8042 CHIP SELECT
A17-A23     ; ADDRESS BUS INPUTS
AF16        ; A WORD MEMORY ACCESS
ALE         ; ADDRESS LATCH ENABLE
CAS0-1      ; COLUMN ADDRESS SELECT
ENAS        ; ENABLE ADDRESS STROBE
HLDA        ; HOLD ACKNOWLEDGE
LCSROM      ; ROM CHIP SELECT
LMEGCS      ; LOW MEG CHIP SELECT
MDBEN       ; MEMORY DATA BUS ENABLE
MDPIN0,1    ; MEMORY DATA PARITY INPUT
NC          ; NO CONNECTION
NMICS       ; NMI CHIP SELECT
PAR         ; PARITY
PAREN       ; PARITY ENABLE
PORTBRD     ; PORT B READ
PORTBWR     ; PORT B WRITE
PPICS       ; PROGRAMMABLE PERIPHERAL INTERFACE CHIP SELECT
Q1WS        ; 1 WAIT STATE
RAS0-1      ; ROW ADDRESS SELECT
REF         ; REFRESH
SEL0-1      ; RAM SELECT
SRTAS       ; REAL TIME CLOCK ADDRESS STROBE
SRTDS       ; REAL TIME CLOCK ADDRESS DATA STROBE
SRTRW       ; REAL TIME CLOCK READ/WRITE
UCAS        ; USER CAS
XA0         ; ADDRESS 0
XA4         ; ADDRESS 4
XBHE        ; BUS HIGH ENABLE
XIOR        ; I/O READ
XIOW        ; I/O WRITE
XMEMR       ; MEMORY READ
```

SELECT INPUT		RAM ADDRESS RANGE		RAM TYPE	
SEL0	SEL1	RAS0/CAS0	RAS1/CAS1	BANK0	BANK1
0	0	000000H-01FFFFH	020000H-03FFFFH	64K	64K
1	0	000000H-07FFFFH		256K	NONE
0	1	000000H-07FFFFH	080000H-09FFFFH	256K	64K
1	1	000000H-07FFFFH	100000H-17FFFFH	256K	256K
X	X	ROM LOW ADDRESS RANGE : 0E0000H - 0FFFFFH			
X	X	ROM HIGH ADDRESS RANGE : FE0000H - FFFFFFH			

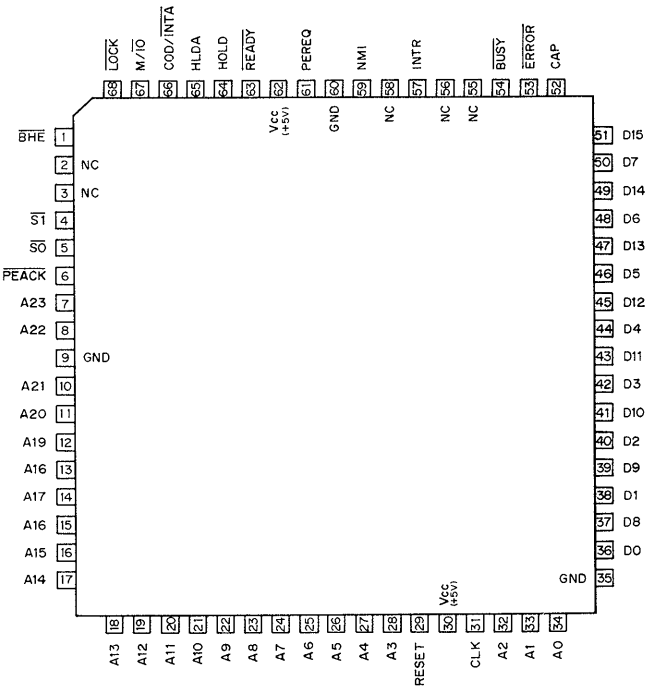
INPUTS					OUTPUTS						
PPI-CS	XA0	XA4	X-IOR	X-IOW	NMI-CS	PORT-BRD	PORT-BWR	8042-CS	SRT-DS	*1 SRT-AS	SRT-RW
1	X	X	X	X	1	1	1	1	1	0	1
0	0	0	X	X	1	1	1	0	1	0	1
0	1	0	0	1	1	0	1	1	1	0	1
0	1	0	1	0	1	1	0	1	1	0	1
0	0	1	1	0	0	1	1	1	1	1	1
0	1	1	1	0	1	1	1	1	1	0	0
0	1	1	0	1	1	1	1	1	0	0	1

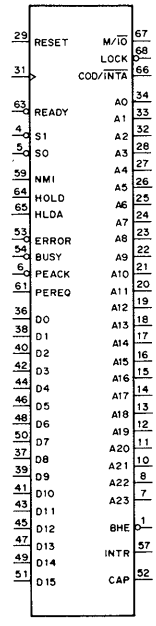
X ; DON'T CARE
0 ; LOW LEVEL
1 ; HIGH LEVEL

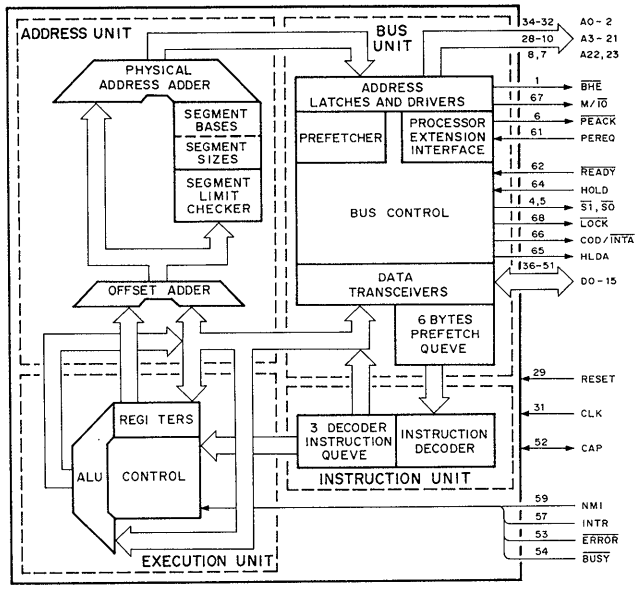
*1 This condition assumes Q1WS and ENAS are true.

N80286-8 (INTEL) (CLOCK RATE = 8MHz)
16 BIT MICROPROCESSOR
— TOP VIEW —

N80286-8(1/4)








```
A0-A23    (O)  ; ADDRESS LINES 0-23
BHE       (O)  ; BUS HIGH ENABLE
BUSY      (I)  ; PROCESSOR EXTENSION BUSY
CAP       (I)  ; SUBSTRATE FILTER CAPACITOR
CLK       (I)  ; SYSTEM CLOCK
COD/INTA  (O)  ; CODE/INTERRUPT ACKNOWLEDGE
D0-D15  (I/O)  ; DATA LINES 0-15
ERROR     (I)  ; PROCESSOR EXTENSION ERROR
HLDA      (O)  ; BUS HOLD ACKNOWLEDGE
HOLD      (I)  ; BUS HOLD REQUEST
INTR      (I)  ; INTERRUPT REQUEST
LOCK      (O)  ; BUS LOCK
M/IO      (O)  ; MEMORY or I/O SELECT
NMI       (I)  ; NON-MASKABLE INTERRUPT REQUEST
PEACK     (O)  ; PROCESSOR EXTENSION OPERAND ACKNOWLEDGE
PEREQ     (I)  ; PROCESSOR EXTENSION OPERAND REQUEST
READY     (I)  ; BUS READY
RESET     (I)  ; SYSTEM RESET
S0,S1     (O)  ; BUS CYCLE STATUS
```

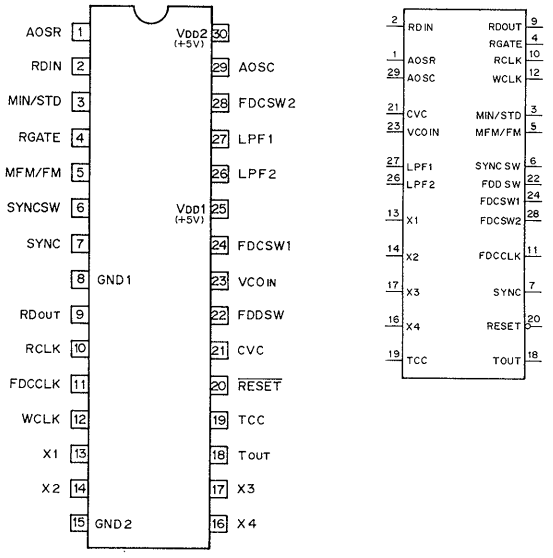
-BHE AND A0 ENCODINGS		
-BHE VALUE	A0 VALUE	FUNCTION
0	0	WORD TRANSFER
0	1	BYTE TRANSFER ON UPPER HALF OF DATA BUS(D8-15)
1	0	BYTE TRANSFER ON UPPER HALF OF DATA BUS(D0-7)
1	1	WILL NEVER OCCUR

80286 BUS CYCLE STATUS DEFINITION				
COD/INTA	M/IO	S1	S0	BUS CYCLE INITISTED
0	0	0	0	INTERRUPT ACKNOWLEDGE
0	0	0	1	WILL NOT OCCUR
0	0	1	0	WILL NOT OCCUR
0	0	1	1	NONE ; NOT A STATUS CYCLE
0	1	0	0	IF A1="1" THEN HALT ; ELSE SHUTDOWN
0	1	0	1	MEMORY DATA READ
0	1	1	0	MEMORY DATA WRITE
0	1	1	1	NONE ; NOT A STATUS CYCLE
1	0	0	0	WILL NOT OCCUR
1	0	0	1	I/O READ
1	0	1	0	I/O WRITE
1	0	1	1	NONE ; NOT A STATUS CYCLE
1	1	0	0	WILL NOT OCCUR
1	1	0	1	MEMORY INSTRUCTION READ
1	1	1	0	WILL NOT OCCUR
1	1	1	1	NONE ; NOT A STATUS CYCLE

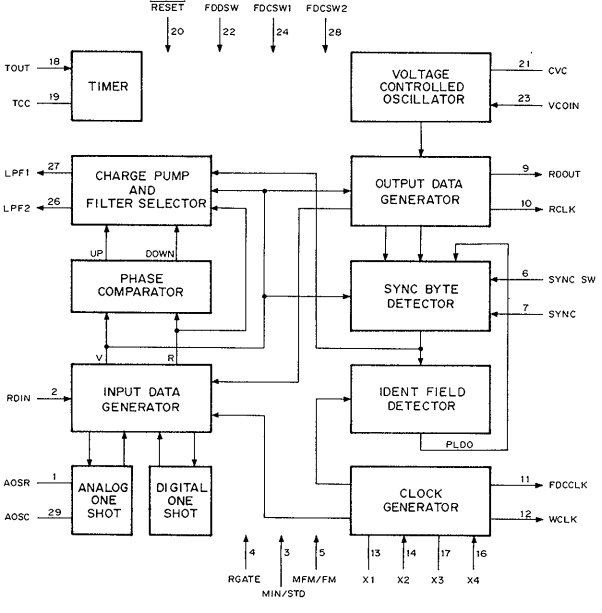
0 ; LOW LEVEL
1 ; HIGH LEVEL

uPD71066CT (NEC)

C-MOS VFO (FLOPPY DISK DATA SEPARATOR)
– TOP VIEW –

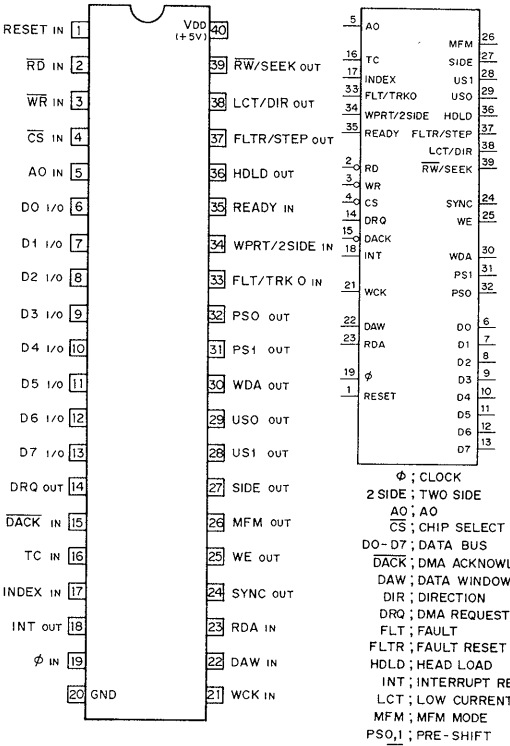


AOSR ; ANALOG ONE SHOT RESISTANCE CONNECTION
AOSC ; ANALOG ONE SHOT CAPACITOR CONNECTION
CVC ; CONNECTED CAPACITOR for VCO
FDCCLK ; CLOCK OUTPUT for FDC
FDCSW1, 2 ; FDC SELECT INPUTS
FDDSW ; FDD TYPE SELECT INPUT
GND1 ; DIGITAL GROUND
GND2 ; ANALOG GROUND
LPF1, 2 ; LOW PASS FILTER OUTPUT
MIN/STD ; MINI/STANDARD FDD SELECT INPUT
MFM/FM ; DOUBLE/SINGLE DENSITY SELECT INPUT
RCLK ; SAMPLING CLOCK for READ DATA OUT
RDIN ; READ DATA INPUT of FDD
RDOUT ; READ DATA OUTPUT (SYNCHRONOUS RCLK)
RESET ; SYSTEM RESET INPUT
RGATE ; READ ENABLE INPUT of FDC
SYNC ; PLL GAIN SELECT/SYNC FIELD DETECT INPUT
SYNCSW ; INTERNAL/EXTERNAL SYNC SELECT INPUT
TCC ; CONNECTED RC for TIME CONSTANT
TOUT ; TIMER OUTPUT
VCOIN ; INPUT of LPF OUT for VCO
VDD1 ; DIGITAL VDD
VDD2 ; ANALOG VDD
WCLK ; FDC WRITE CLOCK OUTPUT
X1 ; CRYSTAL(16MHz) CONNECTION
X2 ; CRYSTAL(16MHz) CONNECTION
or EXTERNAL CLOCK INPUT
X3 ; CRYSTAL(19.2MHz) CONNECTION
X4 ; CRYSTAL(19.2MHz) CONNECTION
or EXTERNAL CLOCK INPUT

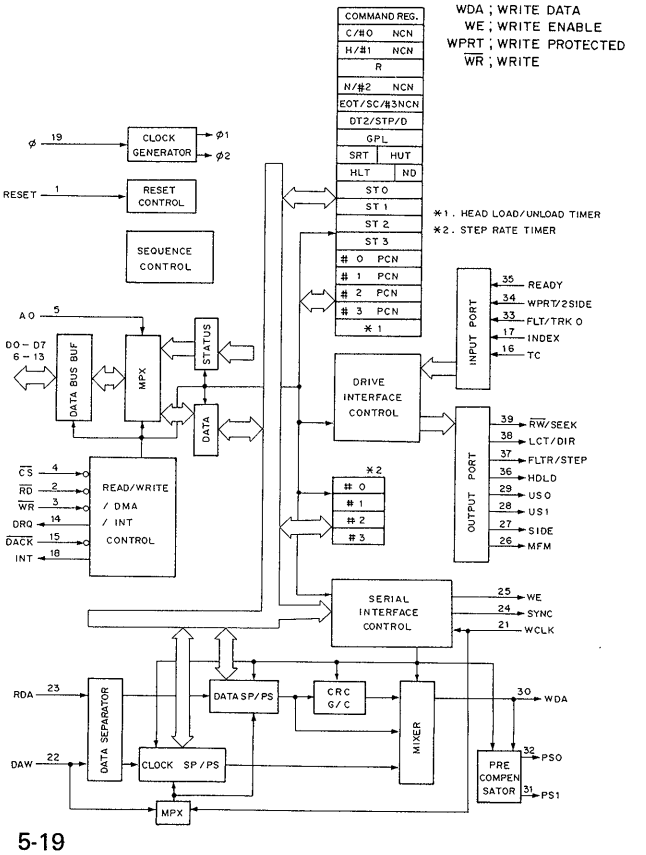


uPD72065C (NEC)

C-MOS PROGRAMMABLE FLOPPY DISK CONTROLLER
– TOP VIEW –

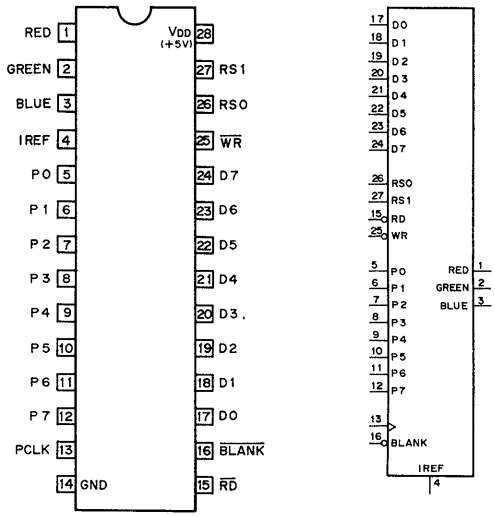


Φ ; CLOCK
2 SIDE ; TWO SIDE
AO ; AO
CS ; CHIP SELECT
DO-D7 ; DATA BUS
DACK ; DMA ACKNOWLEDGE
DAW ; DATA WINDOW
DIR ; DIRECTION
DRQ ; DMA REQUEST
FLT ; FAULT
FLTR ; FAULT RESET
HDLD ; HEAD LOAD
INT ; INTERRUPT REQUEST
LCT ; LOW CURRENT
MFM ; MFM MODE
PSO,1 ; PRE-SHIFT
RD ; READ
RDA ; READ DATA
RW/SEEK ; READ WRITE/SEEK
SIDE ; SIDE SELECT
SYNC ; VFO SYNCHRONIZE
TC ; TERMINAL COUNT
TRK 0 ; TRACK 0
USO,1 ; UNIT SELECT
WCK ; WRITE CLOCK
WDA ; WRITE DATA
WE ; WRITE ENABLE
WPRT ; WRITE PROTECTED
WR ; WRITE

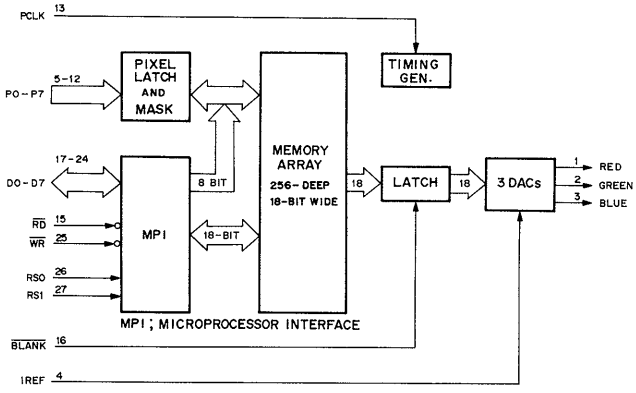


IMS G171P- ? ? (INMOS)

C-MOS COLOR LOOK-UP TABLE (6-BIT DAC, 8-BIT PIXEL)
– TOP VIEW –



$\overline{\text{BLANK}}$; VIDEO BLANKING SIGNAL INPUT. ACTIVE LOW.
BLUE ; ANALOG BLUE OUTPUT
PCLK ; PIXEL CLOCK INPUT
D0-D7 ; PROGRAM DATA INPUTS/OUTPUTS
GREEN ; ANALOG GREEN OUTPUT
IREF ; REFERENCE CURRENT INPUT
P0-P7 ; PIXEL ADDRESS INPUTS
$\overline{\text{RED}}$; ANALOG RED OUTPUT
$\overline{\text{RD}}$; REGISTER READ STROBE INPUT. ACTIVE LOW.
RS0,RS1 ; REGISTER SELECT INPUTS
$\overline{\text{WR}}$; REGISTER WRITE STROBE INPUT. ACTIVE LOW.

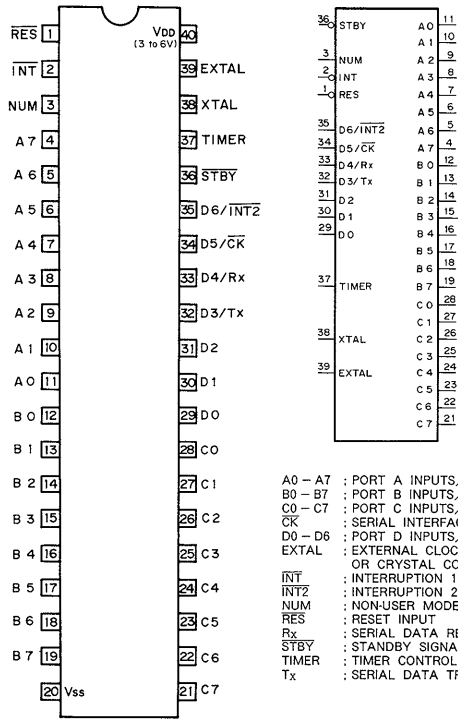


INTERNAL REGISTERS

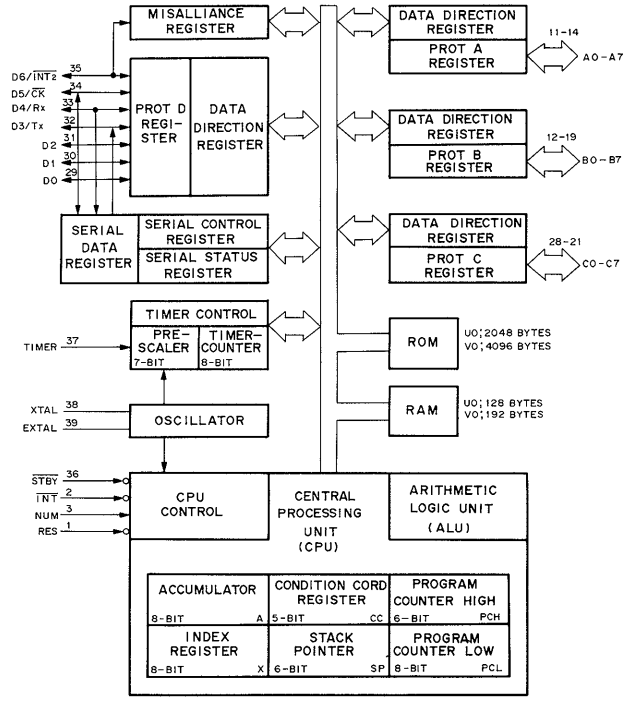
RS0	RS1	SIZE	REGISTER NAME
0	0	8-BIT	PIXEL ADDRESS (WRITE MODE)
1	1	8-BIT	PIXEL ADDRESS (READ MODE)
0	1	18-BIT	COLOR VALUE
1	0	8-BIT	PIXEL MASK

NT108PRO-35VOA99P (NEWTECH)

C-MOS MICROCOMPUTER UNIT
– TOP VIEW –



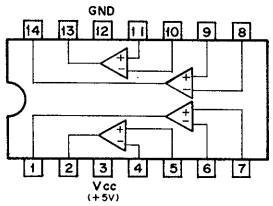
A0 – A7 ; PORT A INPUTS/OUTPUTS
B0 – B7 ; PORT B INPUTS/OUTPUTS
C0 – C7 ; PORT C INPUTS/OUTPUTS
$\overline{\text{CK}}$; SERIAL INTERFACE CLOCK INPUT
D0 – D6 ; PORT D INPUTS/OUTPUTS
EXTAL ; EXTERNAL CLOCK INPUT OR CRYSTAL CONNECTION
$\overline{\text{INT}}$; INTERRUPTION 1 INPUT
$\overline{\text{INT2}}$; INTERRUPTION 2 INPUT
NUM ; NON-USER MODE (FIXED V_{SS} LEVEL)
$\overline{\text{RES}}$; RESET INPUT
R_X ; SERIAL DATA RECEIVE
$\overline{\text{STBY}}$; STANDBY SIGNAL INPUT
TIMER ; TIMER CONTROL INPUT
T_X ; SERIAL DATA TRANSFER



LM339D (SIGNETICS) FLAT PACKAGE

COMPARATOR

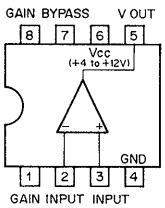
– TOP VIEW –



LM386N (NS)

LOW VOLTAGE AUDIO POWER AMPLIFIER

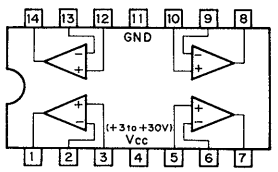
– TOP VIEW –



uPC324C (NEC)

QUAD. OP AMPLIFIER

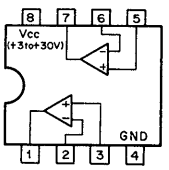
– TOP VIEW –



uPC358C (NEC)

DUAL OPERATIONAL AMPLIFIERS

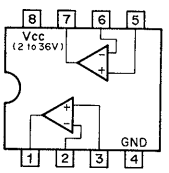
– TOP VIEW –



uPC393C (NEC)

VOLTAGE COMPARATOR

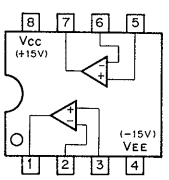
– TOP VIEW –



uPC4558C (NEC)

OPERATIONAL AMPLIFIER

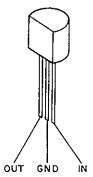
– TOP VIEW –

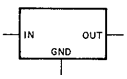


NJM78L ? ?A (JRC)

RC78L ? ?A (RAYTHEON)

POSITIVE VOLTAGE REGULATOR (100mA)



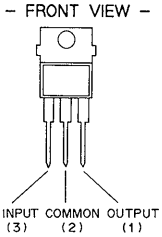


OUTPUT VOLTAGE	NJM78L??A	RC78L??A	uA78L??ACL	uA78L??AWV	uPC78L??J	AN78L??
+2.6V	NJM78L02A	RC78L02A	uA78L02ACL	uA78L26AWV	---------	-------
+4V	---------	-------	---------	---------	-------	AN78L04
+5V	NJM78L05A	RC78L05A	uA78L05ACL	uA78L05AWV	uPC78L05J	AN78L05
+6V	NJM78L06A	RC78L06A	---------	---------	---------	AN78L06
+6.2V	---------	-------	uA78L06ACL	uA78L62AWV	---------	-------
+7V	---------	-------	---------	---------	---------	AN78L07
+8V	NJM78L08A	RC78L08A	uA78L08ACL	---------	uPC78L08J	AN78L08
+8.2V	---------	-------	---------	uA78L82AWV	---------	-------
+9V	NJM78L09A	RC78L09A	uA78L09ACL	uA78L09AWV	---------	AN78L09
+10V	---------	-------	uA78L10ACL	---------	uPC78L10J	AN78L10
+12V	NJM78L12A	RC78L12A	uA78L12ACL	uA78L12AWV	uPC78L12J	AN78L12
+15V	NJM78L15A	RC78L15A	uA78L15ACL	uA78L15AWV	uPC78L15J	AN78L15
+18V	NJM78L18A	RC78L18A	---------	uA78L18AWV	---------	AN78L18
+20V	NJM78L20A	RC78L20A	---------	---------	---------	AN78L20
+24V	NJM78L24A	RC78L24A	---------	uA78L24AWV	---------	AN78L24

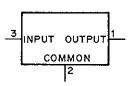
NJM78M ? ?A (JRC)

POSITIVE VOLTAGE REGULATOR (500mA)

– FRONT VIEW –

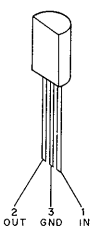


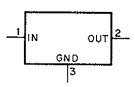
5V NJM78M05A
6V NJM78M06A
8V NJM78M08A
9V NJM78M09A
12V NJM78M12A
15V NJM78M15A
18V NJM78M18A
20V NJM78M20A
24V NJM78M24A



TA78L ? ? ?AP (TOSHIBA)

POSITIVE VOLTAGE REGULATOR (150mA)

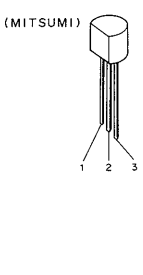




OUTPUT VOLTAGE	???
+5V	005
+6V	006
+7V	007
+7.5V	075
+8V	008
+9V	009
+10V	010
+12V	012
+13.2V	132
+15V	015
+18V	018
+20V	020
+24V	024

PST520 ? (MITSUMI)

SYSTEM RESETTING DEVICE



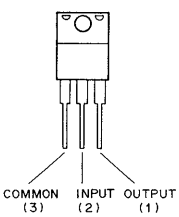
4.5V PST520C
4.4V PST518B
4.2V PST518A/PST520D
3.9V PST520E
3.6V PST520F
3.3V PST520G
3.1V PST520H

REF.; REFERENCE VOLTAGE

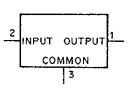
NJM79M ? ?FA (JRC)

NEGATIVE VOLTAGE REGULATOR

– FRONT VIEW –



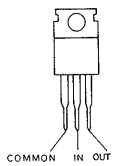
-5V NJM79M05FA
-6V NJM79M06FA
-8V NJM79M08FA
-9V NJM79M09FA
-12V NJM79M12FA
-15V NJM79M15FA
-18V NJM79M18FA
-24V NJM79M24FA

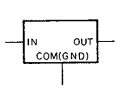


uPC79M ? ?H (NEC)

NEGATIVE VOLTAGE REGULATOR (0.5A)

– SIDE VIEW –



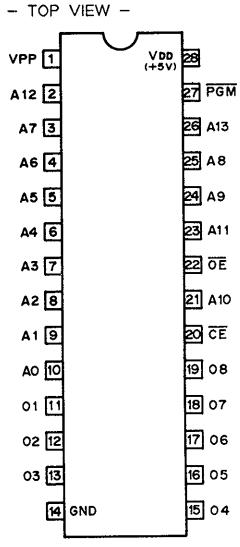


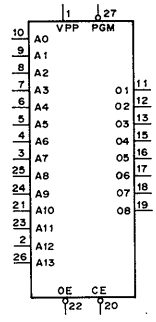
OUTPUT VOLTAGE	uA79M??AUC	FS79??M	AN79M??	uPC79M??H
-5V	uA79M05AUC	FS7905M	AN79M05	uPC79M05H
-6V	uA79M06AUC	-------	AN79M06	---------
-7V	---------	-------	AN79M07	---------
-8V	uA79M08AUC	-------	AN79M08	uPC79M08H
-9V	---------	-------	AN79M09	---------
-10V	---------	-------	AN79M10	---------
-12V	uA79M12AUC	FS7912M	AN79M12	uPC79M12H
-15V	uA79M15AUC	FS7915M	AN79M15	uPC79M15H
-18V	---------	-------	AN79M18	uPC79M18H
-20V	uA79M20AUC	-------	AN79M20	---------
-24V	uA79M24AUC	FS7924M	AN79M24	uPC79M24H

MSM27128AZBRS (OKI) (ACCESS TIME = 150nS)

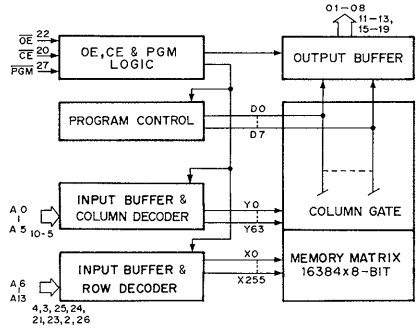
N-MOS 16,384x8 BITS ONE TIME PROM

– TOP VIEW –





A0-13 :ADDRESS INPUT
$\overline{CE}$:CHIP ENABLE
O1-8 :DATA OUTPUT
$\overline{OE}$:OUTPUT ENABLE
$\overline{PGM}$:PROGRAM ENABLE
VPP :PROGRAM POWER SUPPLY

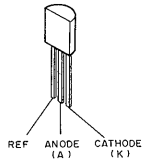


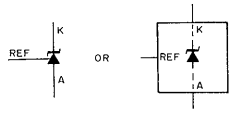
MODE \ TERMINAL	DATA OUTPUT	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Vpp	VDD
READ	DATA OUT	0	0	1	+5V	+5V
STANDBY	HIGH-IMPEDANCE	1	X	X	+5V	+5V
OUTPUT DISABLE	HIGH-IMPEDANCE	0	1	1	+5V	+5V
PROGRAMMING	DATA IN	0	1	0	+12.5V	+6V
PROGRAM VERIFY	DATA OUT	0	0	1	+12.5V	+6V
PROGRAM INHIBIT	HIGH-IMPEDANCE	1	x	X	+12.5V	+6V

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

L5431 (SANYO)

ADJUSTABLE PRECISION SHUNT REGULATOR

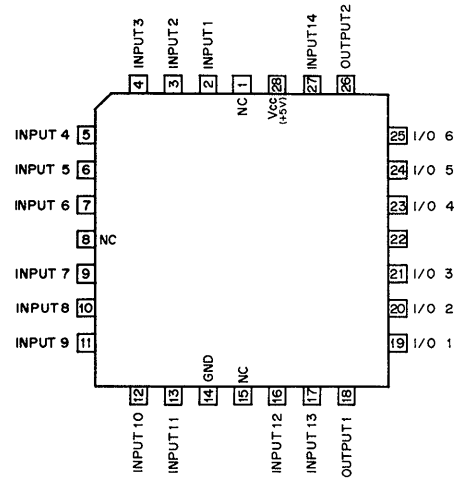


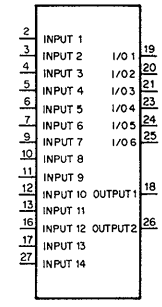


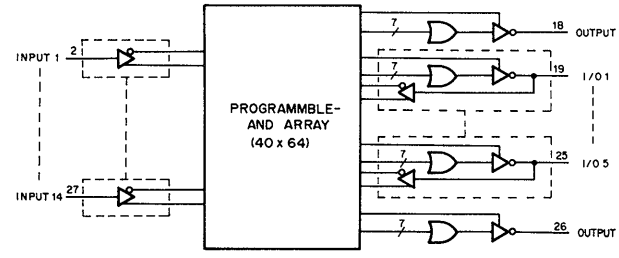
PAL20L8ACNL (MONOLITHIC MEMORIES)

PROGRAMMABLE ARRAY LOGIC (PAL)

– TOP VIEW –



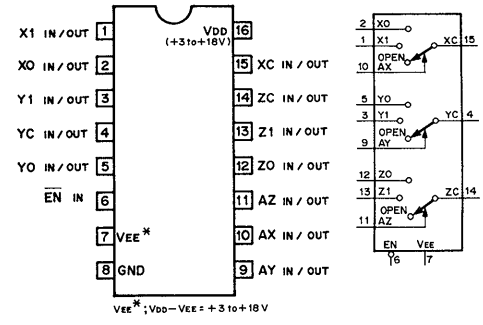




TC4053BP (TOSHIBA)

C-MOS 2-CHANNEL MULTIPLEXER/DEMULTIPLEXER

– TOP VIEW –



VEE* ; VDD – VEE = +3 to +18 V

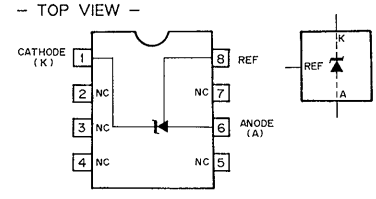
CONT. INPUTS EN	CONT. INPUTS A (X,Y,Z,)	ON CHANNEL
0	0	0
0	1	1
1	X	OPEN

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE.

TL431CPS (TI) FLAT PACKAGE

ADJUSTABLE PRECISION SHUNT REGULATOR

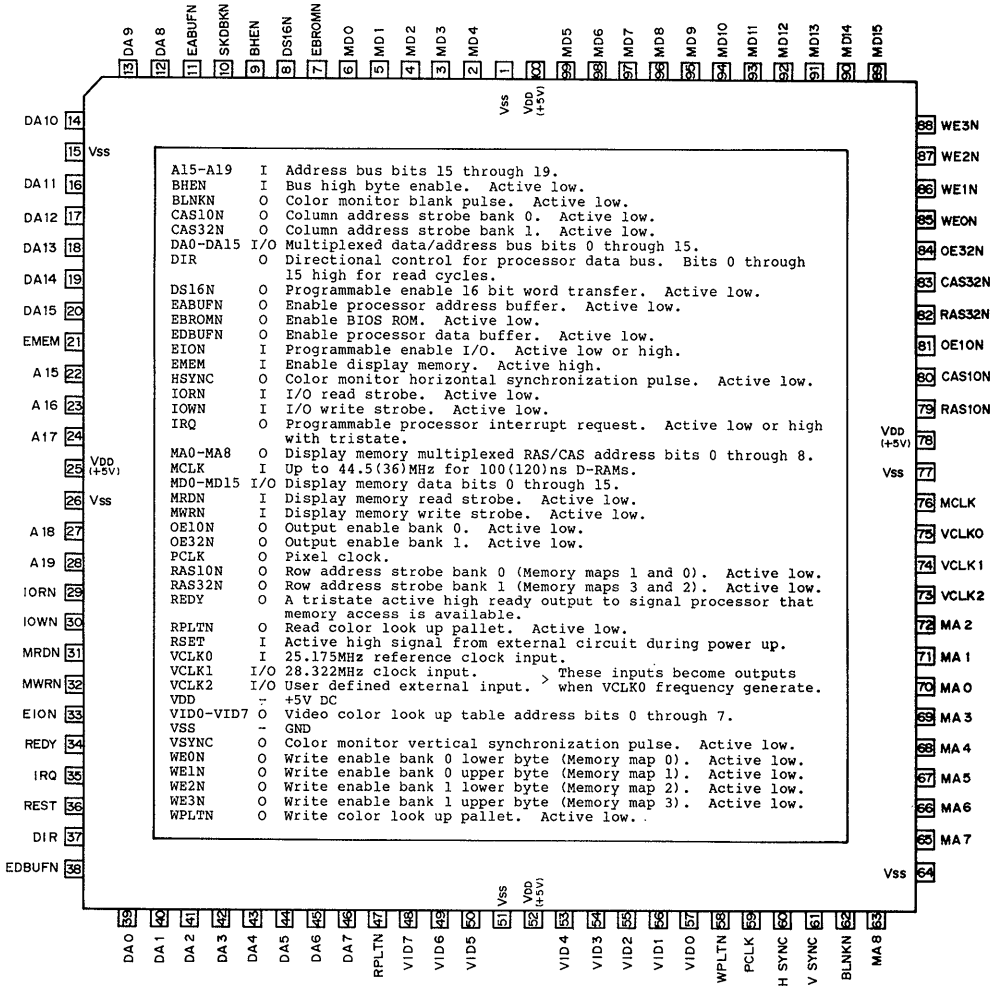
– TOP VIEW –



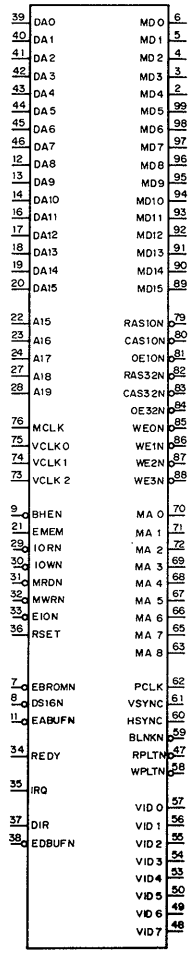
PVGA1A (PARADISE)

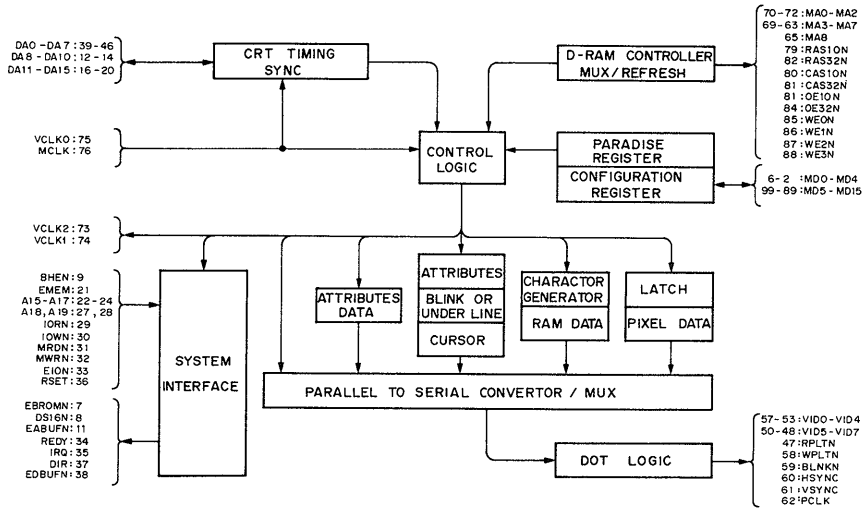
C-MOS VIDEO GRAPHICS ARRAY

– TOP VIEW –

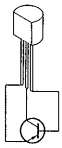


A15-A19	I	Address bus bits 15 through 19.
BHEN	I	Bus high byte enable. Active low.
BLNKN	O	Color monitor blank pulse. Active low.
CAS10N	O	Column address strobe bank 0. Active low.
CAS32N	O	Column address strobe bank 1. Active low.
DA0-DA15	I/O	Multiplexed data/address bus bits 0 through 15.
DIR	O	Directional control for processor data bus. Bits 0 through 15 high for read cycles.
DS16N	O	Programmable enable 16 bit word transfer. Active low.
EABUFN	O	Enable processor address buffer. Active low.
EBROMN	O	Enable BIOS ROM. Active low.
EDBUFN	O	Enable processor data buffer. Active low.
EION	I	Programmable enable I/O. Active low or high.
EMEM	I	Enable display memory. Active high.
HSYNC	O	Color monitor horizontal synchronization pulse. Active low.
IORN	I	I/O read strobe. Active low.
IOWN	I	I/O write strobe. Active low.
IRQ	O	Programmable processor interrupt request. Active low or high with tristate.
MA0-MA8	O	Display memory multiplexed RAS/CAS address bits 0 through 8.
MCLK	I	Up to 44.5(36)MHz for 100(120)ns D-RAMs.
MD0-MD15	I/O	Display memory data bits 0 through 15.
MRDN	I	Display memory read strobe. Active low.
MWRN	I	Display memory write strobe. Active low.
OE10N	O	Output enable bank 0. Active low.
OE32N	O	Output enable bank 1. Active low.
PCLK	O	Pixel clock.
RAS10N	O	Row address strobe bank 0 (Memory maps 1 and 0). Active low.
RAS32N	O	Row address strobe bank 1 (Memory maps 3 and 2). Active low.
REDY	O	A tristate active high ready output to signal processor that memory access is available.
RPLTN	O	Read color look up pallet. Active low.
RSET	I	Active high signal from external circuit during power up.
VCLK0	I	25.175MHz reference clock input.
VCLK1	I/O	28.322MHz clock input. > These inputs become outputs
VCLK2	I/O	User defined external input. > when VCLK0 frequency generate.
VDD	–	+5V DC
VID0-VID7	O	Video color look up table address bits 0 through 7.
VSS	–	GND
VSYNC	O	Color monitor vertical synchronization pulse. Active low.
WE0N	O	Write enable bank 0 lower byte (Memory map 0). Active low.
WE1N	O	Write enable bank 0 upper byte (Memory map 1). Active low.
WE2N	O	Write enable bank 1 lower byte (Memory map 2). Active low.
WE3N	O	Write enable bank 1 upper byte (Memory map 3). Active low.
WPLTN	O	Write color look up pallet. Active low.

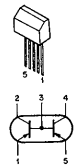




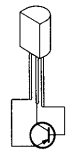
«2SA»



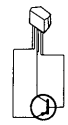
2SA733-K



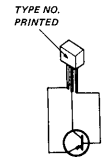
2SA995



2SA1020

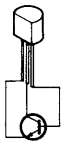


2SA1048

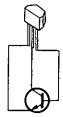


2SA1175F

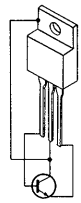
«2SC»



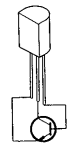
2SC1815



2SC2458



2SC2542



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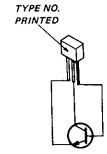

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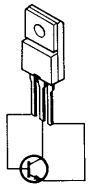
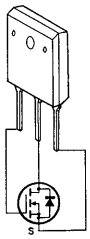
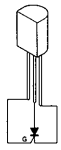


2SC4304

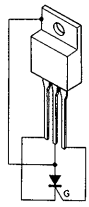
«OTHER»



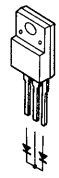
2SK800



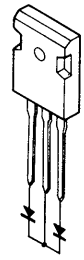
03P2M



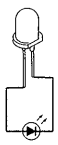
5P4M



F10P20F

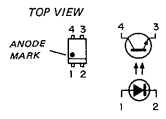


S30SC4M

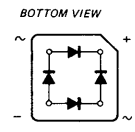


GL-5HY21 ; YELLOW
GL-5HY41 ; YELLOW
GL-5PG21 ; GREEN

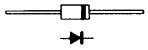
TLG114A ; GREEN
TLUG154 ; GREEN



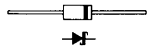
PC817



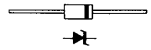
S10WB ? ?



11DF4
11ES ?
1S144
1S1555
1S2473
1SS119
1SS131
1T-22A
DS442
F1-06
S2LA-20



ERA81-004



RD ? ?FB ?
RD ? ?JSB ?

1T33C-01

5-2. PU-59VA BOARD

REF. NO.	TYPE	PIN NO. +5V	PIN NO. GND
IC304	SN74LS125AN	14	7
IC313	D80287-8	9	10,30
IC318	N80286-8	30,62	9,35,60
IC323	P82C201	42,63,84	1,43,64
IC324	SN74LS132N	14	7
IC325	SN74ALS244AN	20	14

CV301;CLOCK ADJUSTMENT

X301;16MHz
X302;14.31818MHz

SMC-3000G(J) ONLY

PU-59(1/4)
1-621-950-11
SMC-3000G(J)
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(UC),(J)
VIW-3020/1(U)

REF. No.	TYPE	PIN No. +5V	PIN No. GND
IC308	74F04PC	14	7
IC309	P82C202	48	1,24
IC322	P82A203	18,52	1,35
IC324	SN74LS132N	14	7

HIGH ADDRESS BUS BUFFER AND PORT B 322

RAM/ROM DECODE I/O CONTROL 309

SA17,SA18 — A17-A20 — CA20 — -MASTER — A20 GATE — CPUHLDA — ALE — -BHE — -DMAEN — SAO — -BRD — -BWR — XD0-XD3 — XD4-XD7 — RESET4 — PCHK — IOCK — REFDET — EN IOC — ERMPCK — SPKR DATA — TIM2 GT — OUT2 — RB304 10K — RB305 10K x 2 — RB304 10K x 4 — RB305 10K x 2 — RB304 10K x 2 — 324

SY BOARD CN102 — SY BOARD CN112 — SY BOARD CN401 — RAM-10 CN401

REF — M/-HG — R328 10K — SEL1 — JP304 — JP305 — HLDA — ALE — UCAS — XMEMR — MDPIN 0 — MDPIN 1 — XBHE — XA0 — XA4 — PPICS — ENAS — Q1WS — X1OR — X1OW — 8042CS

AF16 — RASO — RAS1 — CASO — CAS1 — LCSROM — LMEGCS — MDBEN — PAREN — PAR — SRTDS — SRTAS — SRTRW — NMICS — PORT BRD — PORT BWR — -8042 CS

RAS0 301-31 — RAS1 301-33 — CAS0 301-35 — CAS1 301-37 — -XA0 301-27 — XBHE 301-29 — -XMEMW 301-43

LA17 303-A39 — LA18 303-A38 — LA19 303-A37 — LA20 303-A36 — LA21 303-A35 — LA22 303-A34 — LA23 303-A33 — SA17 303-A14 — SA18 303-A13 — SA19 303-A12 — AEN 303-A11 — BALE 303-B28 — -SBHE 303-A32 — -SMEMR 303-B12 — -SMEMW 303-B11 — -MEMR 303-A40 — -MEMW 303-A41 — -IOR 303-B14 — -IOW 303-B13

RS-232C(COM2) CN304 — (EXT. VIEW) ONLY SMC-3000G(J)

IF-156 — SY BOARD CN112 — 302-C23 RxD-COM2 — 302-C22 CD-COM2 — 302-D25 RI-COM2 — 302-D22 DSR-COM2 — 302-D24 CTS-COM2 — 302-C24 TxD-COM2 — 302-D23 RTS-COM2 — 302-C25 DTR-COM2

RxD 304-2 — CD 304-1 — RI 304-9 — DSR 304-6 — CTS 304-8 — TxD 304-3 — RTS 304-7 — DTR 304-4 — GND 304-5

ONLY SMC-3000G(J) — TH301 — C333 47 16V — C334 0.1

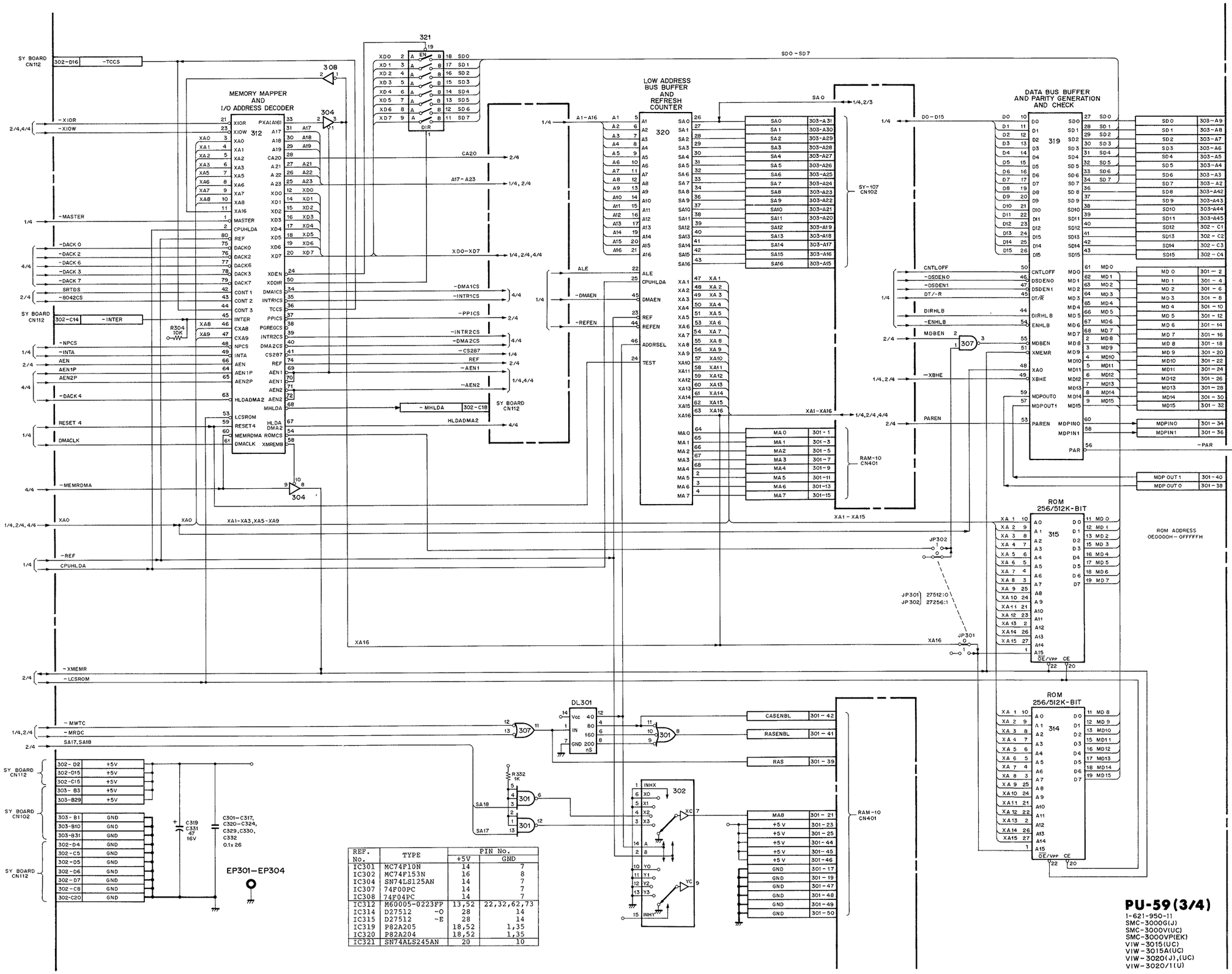
IF-156 — SY BOARD CN112 — 302-C21 KBD CLK — 302-D21 KBD DATA — +5V 305-5 — KB CLK 305-1 — KB DATA 305-2 — NC 305-3 — GND 305-4

KEYBOARD CN305 — (EXT. VIEW) ONLY SMC-3000G(J)

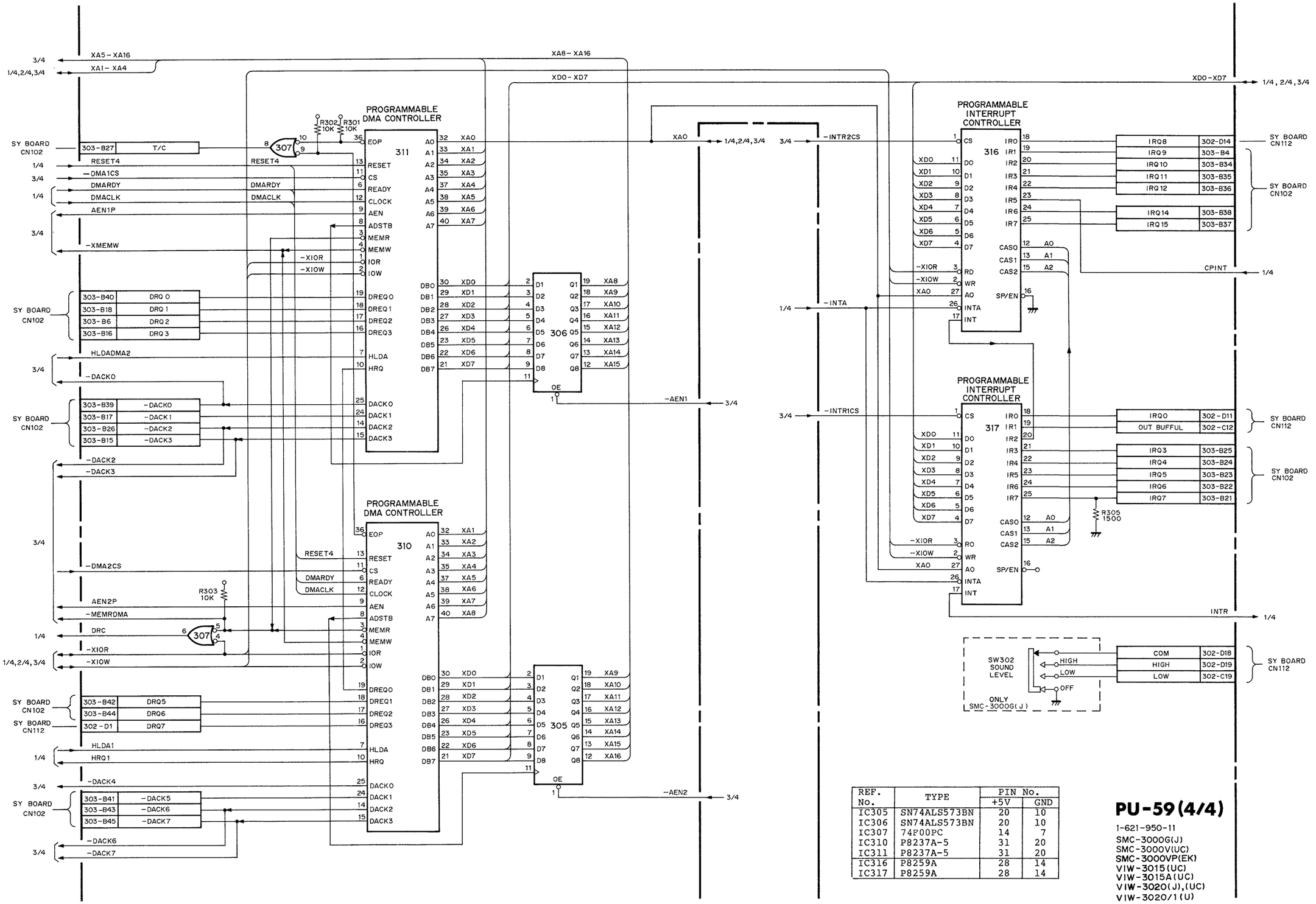
PU-59(2/4)

1-621-950-11

SMC-3000G(J)
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015 (UC)
VIW-3015 A(UC)
VIW-3020(J),(UC)
VIW-3020/1(U)



REF. No.	TYPE	PIN No. +5V	PIN No. GND
IC301	MC74F10N	14	7
IC302	MC74F153N	16	8
IC304	SN74LS125AN	14	7
IC307	74F00PC	14	7
IC308	74F04PC	14	7
IC312	M60005-0223FP	13,52	22,32,62,73
IC314	D27512 -0	28	14
IC315	D27512 -E	28	14
IC319	P82A205	18,52	1,35
IC320	P82A204	18,52	1,35
IC321	SN74ALS245AN	20	10

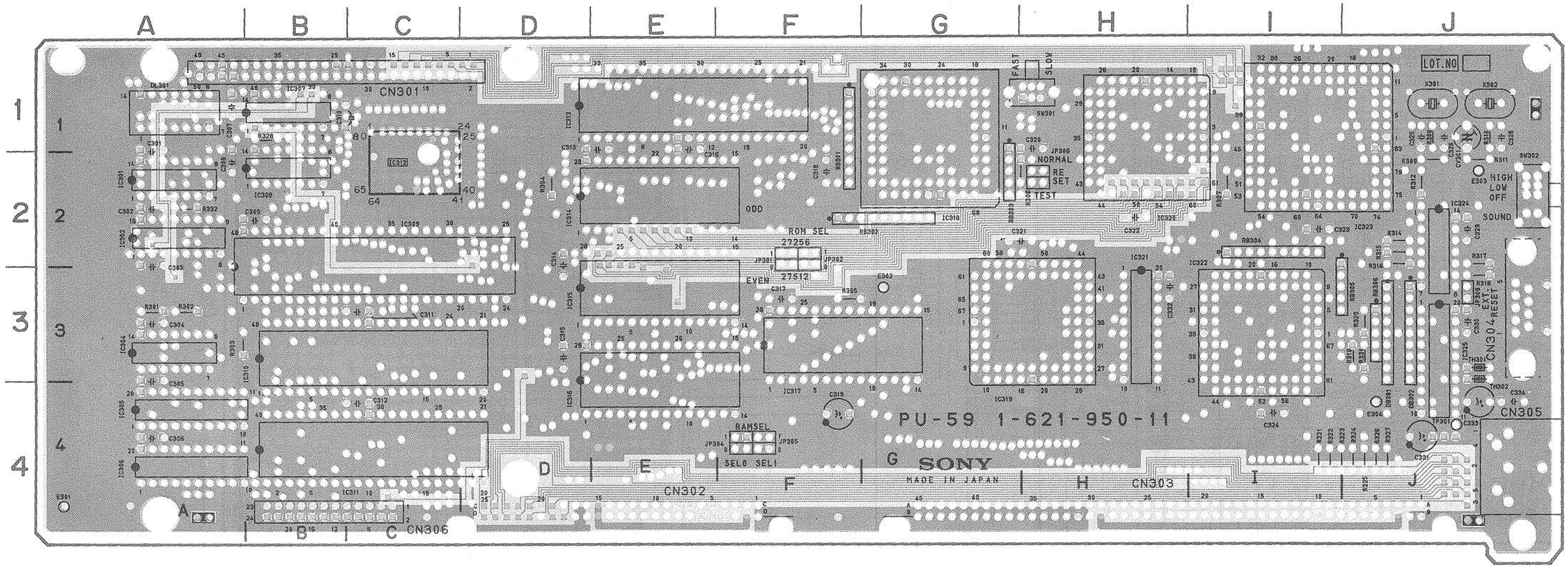


REF. No.	TYPE	PIN No. +5V	PIN No. GND
IC305	SN74ALS573BN	20	10
IC306	SN74ALS573BN	20	10
IC307	74F00PC	14	7
IC310	P8237A-5	31	20
IC311	P8237A-5	31	20
IC316	P8259A	28	14
IC317	P8259A	28	14

PU-59(4/4)

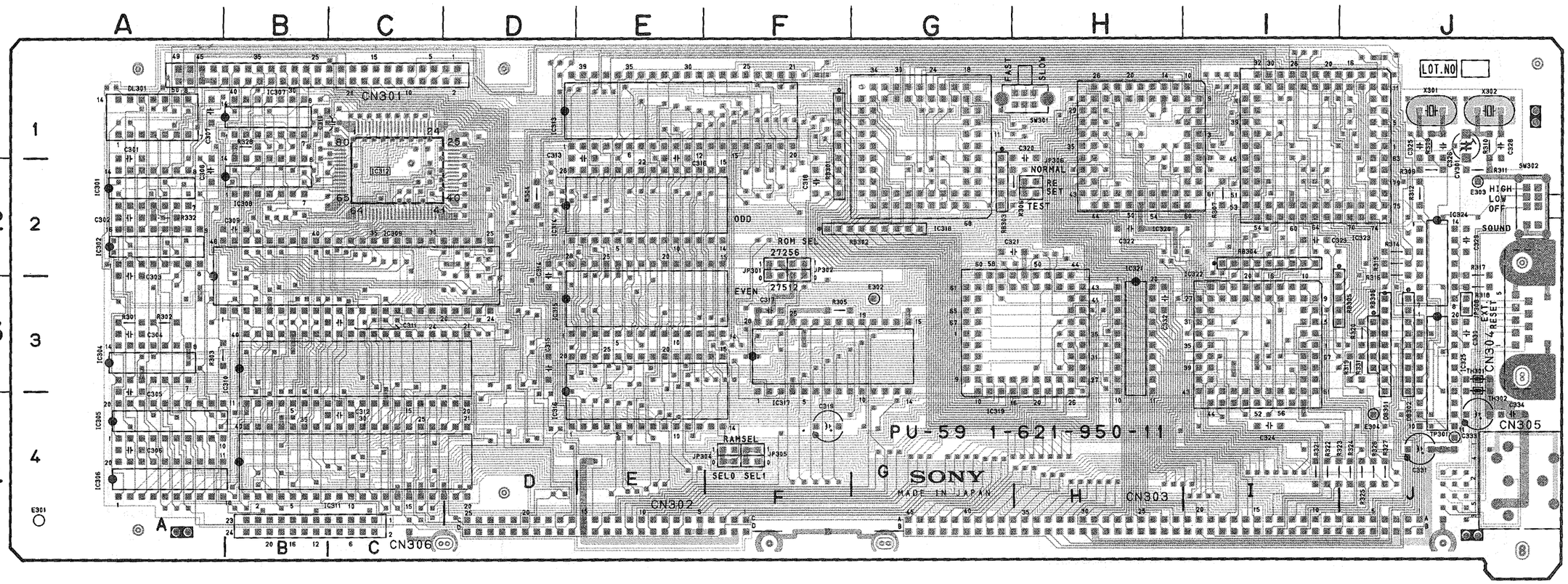
1-621-950-11

SMC-3000G(J)
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J),(UC)
VIW-3020/1(U)



PU-59 – COMPONENT SIDE –

1-621-950-11
SMC-3000G(J)
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)

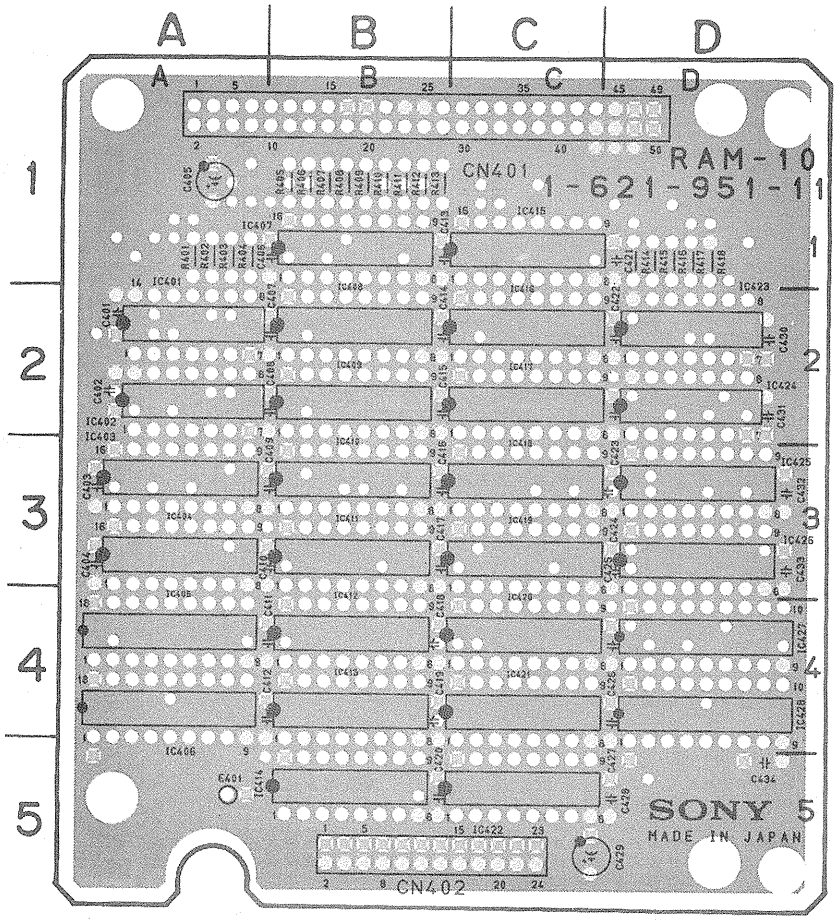


CN301	C - 1	IC301	A - 2	IC321	H - 3	SW301	H - 1
CN302	E - 4	IC302	A - 2	IC322	I - 3	SW302	J - 2
CN303	H - 4	IC304	A - 3	IC323	J - 2		
CN304	J - 3	IC305	A - 4	IC324	J - 2	TH301	J - 3
CN305	J - 4	IC306	A - 4	IC325	J - 3	TH302	J - 4
CN306	C - 4	IC307	B - 1				
		IC308	B - 2	JP301	F - 2	TP301	J - 4
CV301	J - 2	IC309	C - 2	JP302	F - 2		
		IC310	B - 3	JP304	F - 4	X301	J - 1
DB301	J - 4	IC311	B - 4	JP305	F - 4	X302	J - 1
DB302	J - 4	*IC312	C - 2	JP306	H - 2		
		IC313	D - 1	JP308	J - 3	*: SOLDERING SIDE	
DL301	A - 1	IC314	D - 2				
		IC315	D - 3	RB301	F - 2		
E301	A - 4	IC316	D - 4	RB302	G - 2		
E302	G - 3	IC317	F - 4	RB303	G - 2		
E303	J - 2	IC318	G - 2	RB304	I - 2		
E304	J - 4	IC319	G - 4	RB305	J - 3		
		IC320	H - 1	RB306	J - 3		

PU-59 – COMPONENT SIDE –

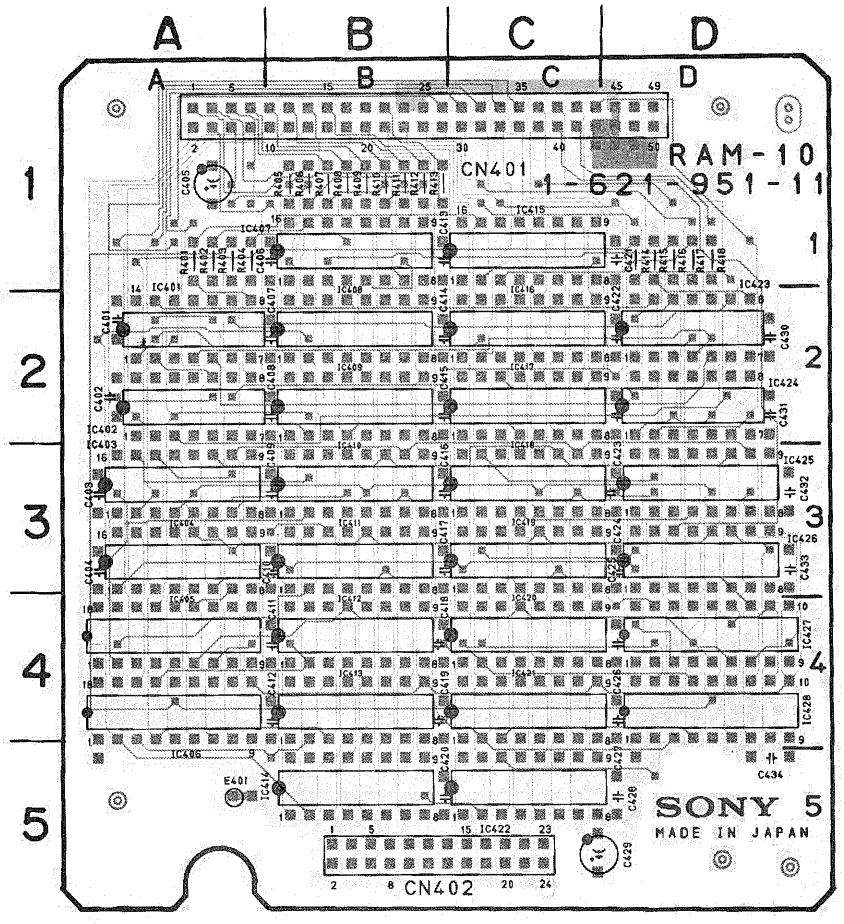
1-621-950-11
SMC-3000G(J)
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)

5-3. RAM-10 BOARD



RAM-10 – COMPONENT SIDE –

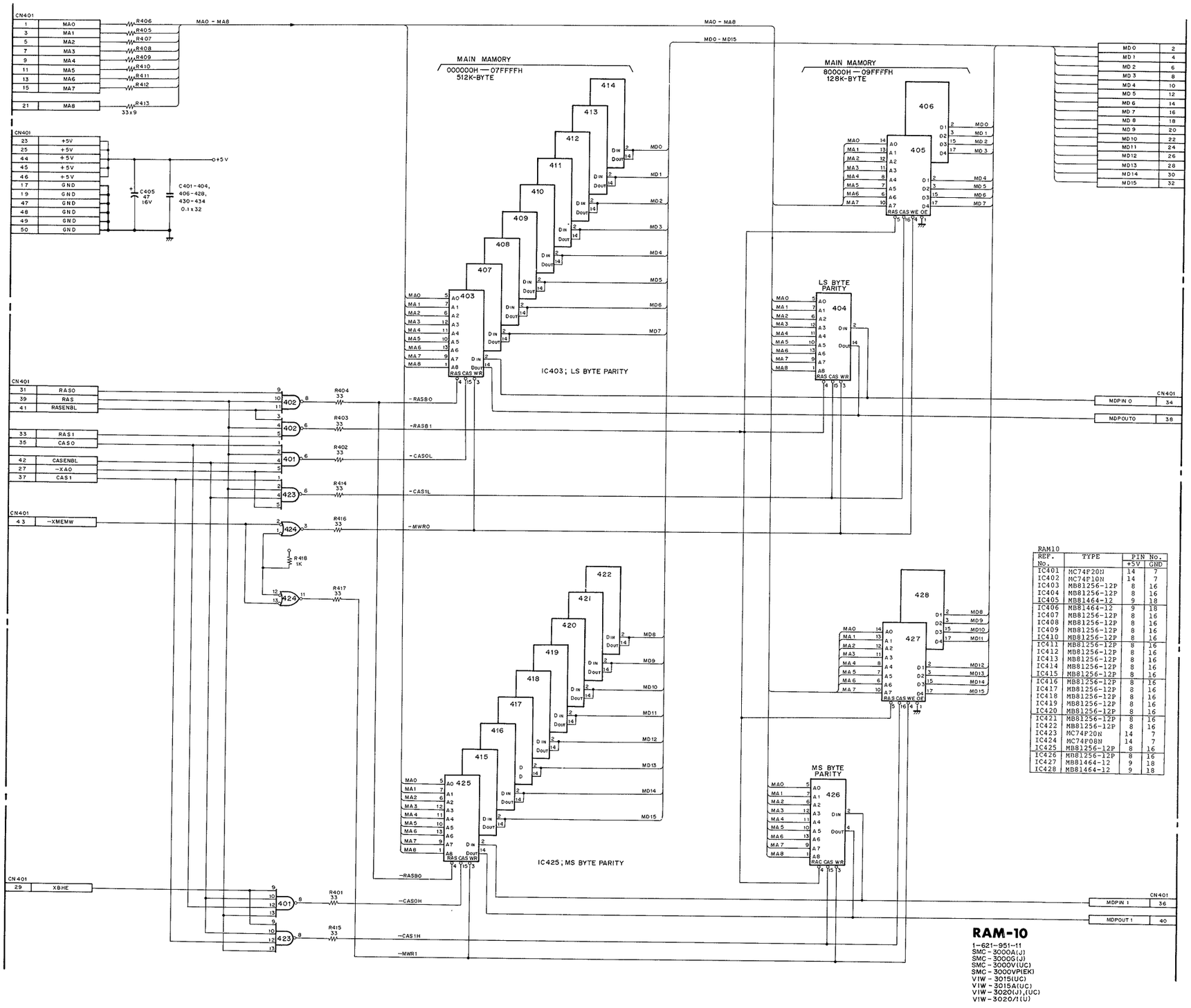
1-621-951-11
SMC-3000A(J)
SMC-3000G(J)
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)



RAM-10 – COMPONENT SIDE –

1-621-951-11
SMC-3000A(J)
SMC-3000G(J)
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)

CN401	C - 1	IC413	B - 4
CN402	B - 5	IC414	B - 5
		IC415	C - 1
E401	A - 5	IC416	C - 2
		IC417	C - 2
IC401	A - 2	IC418	C - 3
IC402	A - 2	IC419	C - 3
IC403	A - 3	IC420	C - 4
IC404	A - 3	IC421	C - 4
IC405	A - 4	IC422	C - 5
IC406	A - 4	IC423	D - 2
IC407	B - 1	IC424	D - 2
IC408	B - 2	IC425	D - 3
IC409	B - 2	IC426	D - 3
IC410	B - 3	IC427	D - 4
IC411	B - 3	IC428	D - 4
IC412	B - 4		



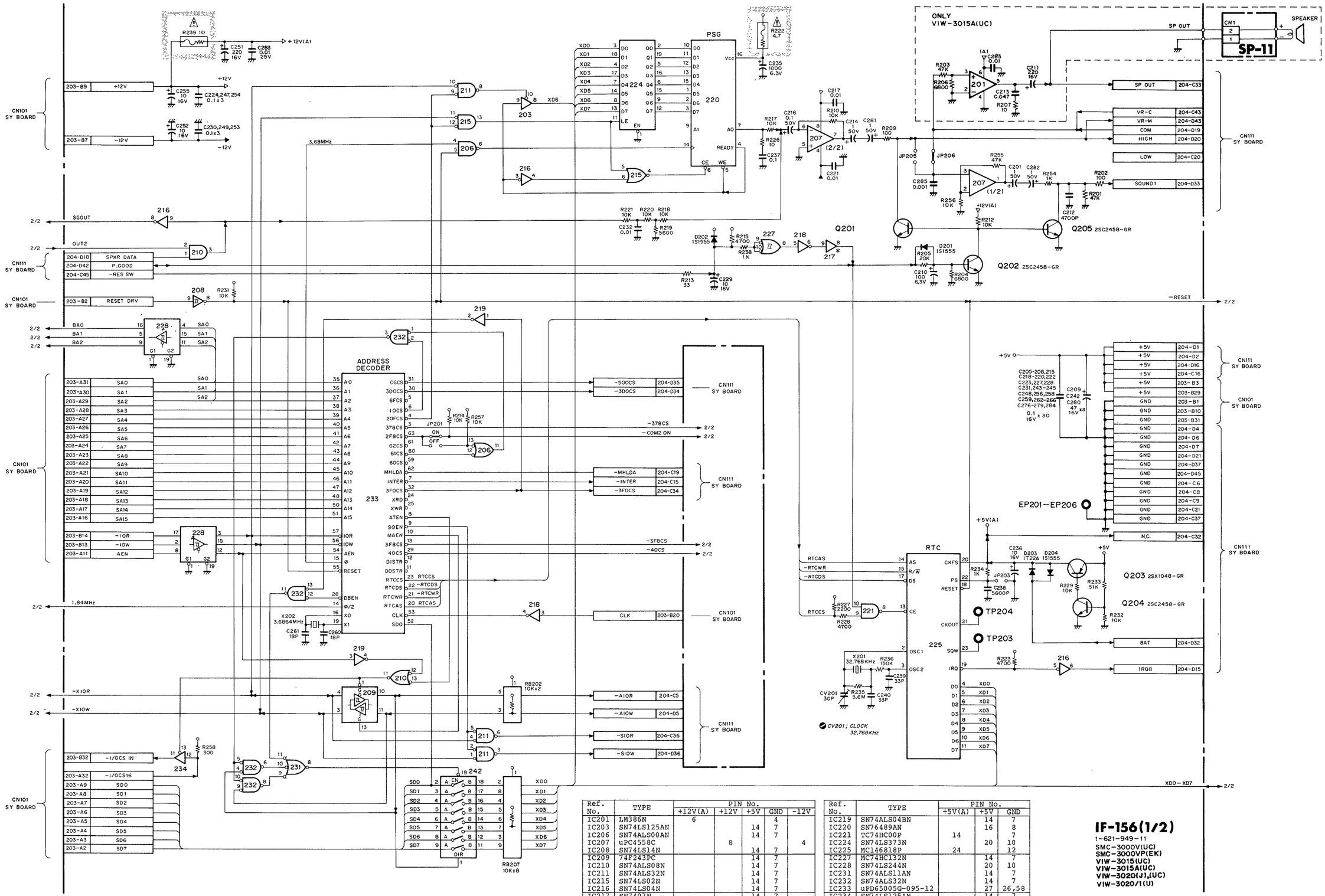
RAM10

REF. No.	TYPE	PIN No. +5V	PIN No. GND
IC401	MC74F20N	14	7
IC402	MC74F10N	14	7
IC403	MB81256-12P	8	16
IC404	MB81256-12P	8	16
IC405	MB81464-12	9	18
IC406	MB81464-12	9	18
IC407	MB81256-12P	8	16
IC408	MB81256-12P	8	16
IC409	MB81256-12P	8	16
IC410	MB81256-12P	8	16
IC411	MB81256-12P	8	16
IC412	MB81256-12P	8	16
IC413	MB81256-12P	8	16
IC414	MB81256-12P	8	16
IC415	MB81256-12P	8	16
IC416	MB81256-12P	8	16
IC417	MB81256-12P	8	16
IC418	MB81256-12P	8	16
IC419	MB81256-12P	8	16
IC420	MB81256-12P	8	16
IC421	MB81256-12P	8	16
IC422	MB81256-12P	8	16
IC423	MC74F20N	14	7
IC424	MC74F08N	14	7
IC425	MB81256-12P	8	16
IC426	MB81256-12P	8	16
IC427	MB81464-12	9	18
IC428	MB81464-12	9	18

RAM-10

1-621-951-11
SMC-3000A(J)
SMC-3000G(J)
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J),(UC)
VIW-3020/1(U)

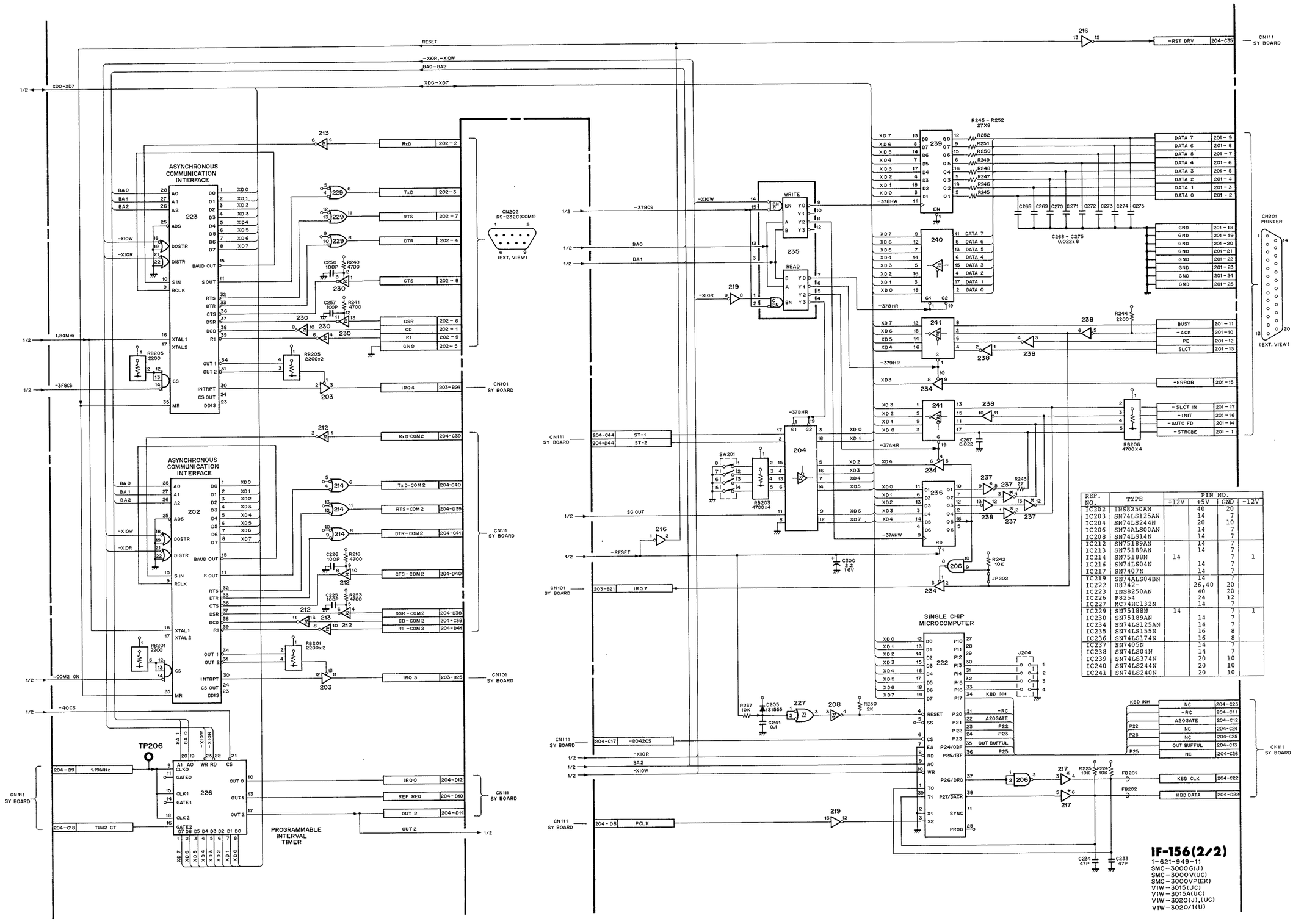
5-4. IF-156VA BOARD



Ref. No.	TYPE	PIN No. +12V(A)	+12V	+5V	GND	-12V
IC201	LM386N	6			4	
IC203	SN74LS125AN			14	7	
IC206	SN74ALS00AN			14	7	
IC207	uPC4558C		8			4
IC208	SN74LS14N			14	7	
IC209	74F243PC			14	7	
IC210	SN74ALS08N			14	7	
IC211	SN74ALS32N			14	7	
IC215	SN74LS02N			14	7	
IC216	SN74LS04N			14	7	
IC217	SN7407N			14	7	
IC218	SN74LS04N			14	7	

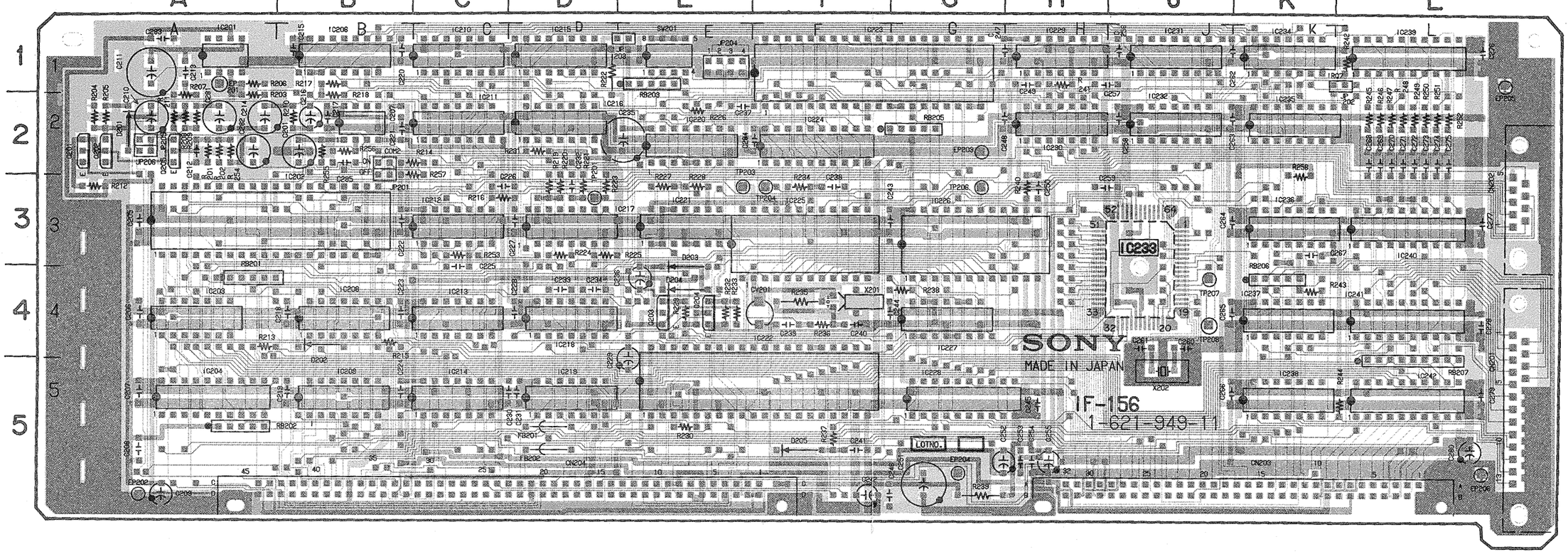
Ref. No.	TYPE	PIN No. +5V(A)	+5V	GND
IC219	SN74ALS04BN		14	7
IC220	SN76489AN		16	8
IC221	TC74HC00P	14		7
IC224	SN74LS373N		20	10
IC225	MC146818P	24		12
IC227	MC74HC132N		14	7
IC228	SN74LS244N		20	10
IC231	SN74ALS11AN		14	7
IC232	SN74ALS32N		14	7
IC233	uPD65005G-095-12		27	26,58
IC234	SN74LS125AN		14	7
IC242	SN74LS245N		20	10

IF-156(1/2)
1-621-949-11
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J),(UC)
VIW-3020/1(U)



REF. NO.	TYPE	PIN NO. +12V	+5V	GND	-12V
IC202	INS8250AN		40	20	
IC203	SN74LS125AN		14	7	
IC204	SN74LS244N		20	10	
IC206	SN74ALS00AN		14	7	
IC208	SN74LS14N		14	7	
IC212	SN75189AN		14	7	
IC213	SN75189AN		14	7	
IC214	SN75188N	14		7	1
IC216	SN74LS04N		14	7	
IC217	SN7407N		14	7	
IC219	SN74ALS04BN		14	7	
IC222	D8742-		26,40	20	
IC223	INS8250AN		40	20	
IC226	P8254		24	12	
IC227	MC74HC132N		14	7	
IC229	SN75188N	14		7	1
IC230	SN75189AN		14	7	
IC234	SN74LS125AN		14	7	
IC235	SN74LS155N		16	8	
IC236	SN74LS174N		16	8	
IC237	SN7405N		14	7	
IC238	SN74LS04N		14	7	
IC239	SN74LS374N		20	10	
IC240	SN74LS244N		20	10	
IC241	SN74LS240N		20	10	

IF-156(2/2)
1-621-949-11
SMC-3000G(J)
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J),(UC)
VIW-3020/1(U)



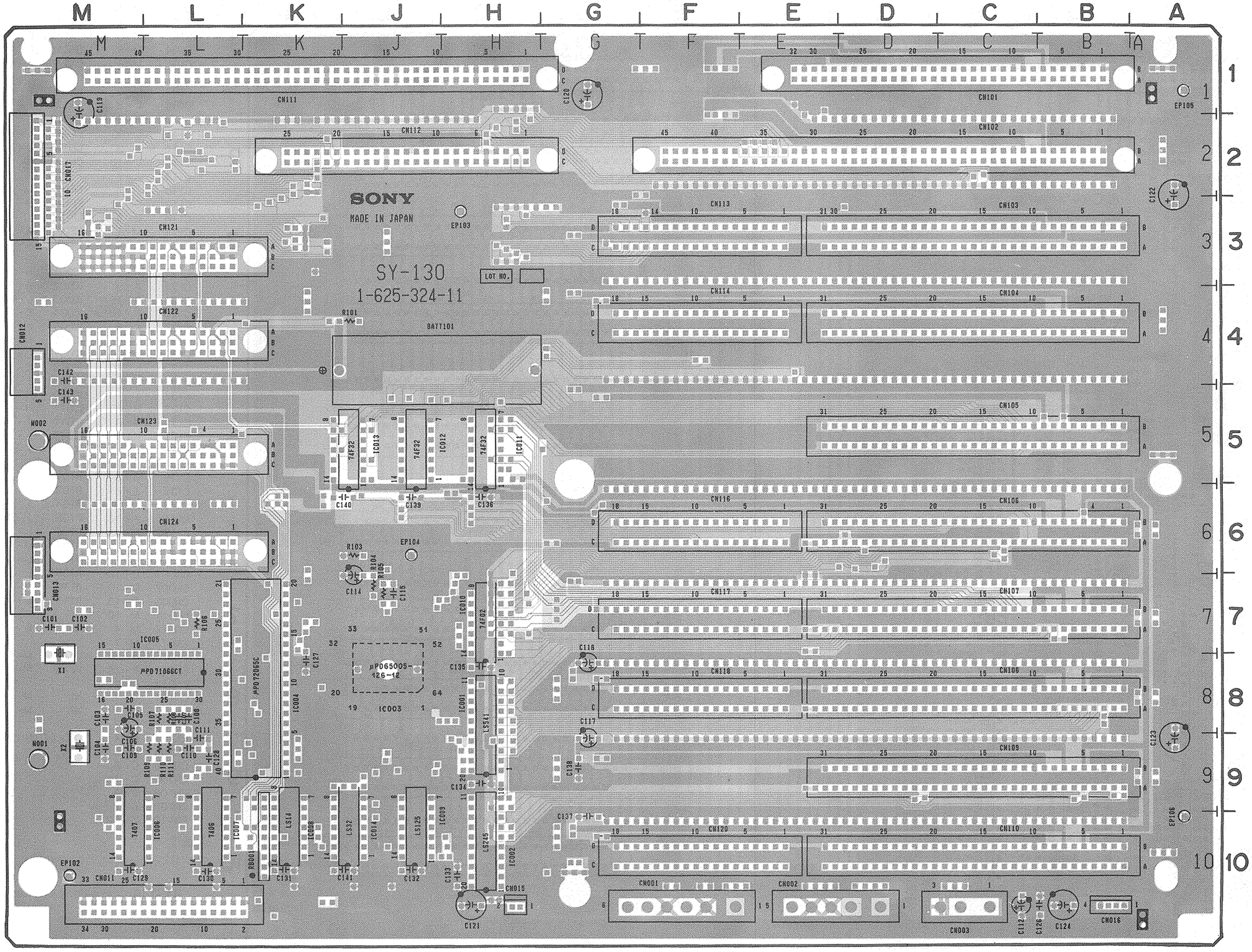
IF-156 – COMPONENT SIDE –

1-621-949-11
SMC-3000G(J)
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)

CN201	L - 5	FB201	D - 5	IC218	D - 4	IC237	K - 4	RB201	A - 4
CN202	L - 3	FB202	D - 5	IC219	D - 5	IC238	K - 5	RB202	A - 5
CN203	K - 5			IC220	E - 2	IC239	L - 1	RB203	E - 1
CN204	D - 5	IC201	A - 1	IC221	E - 3	IC240	L - 3	RB205	G - 2
		IC202	B - 3	IC222	F - 4	IC241	L - 4	RB206	K - 4
CV201	F - 4	IC203	A - 4	IC223	F - 1	IC242	L - 5	RB207	L - 5
		IC204	A - 5	IC224	F - 2				
D201	A - 2	IC206	B - 1	IC225	F - 3	JP201	B - 3	SW201	E - 1
D202	B - 4	IC207	B - 2	IC226	G - 3	JP202	L - 2		
D203	E - 3	IC208	B - 4	IC227	G - 4	JP203	E - 1	TP201	D - 3
D204	E - 4	IC209	B - 5	IC228	G - 5	JP204	E - 1	TP203	E - 3
D205	F - 5	IC210	C - 1	IC229	H - 1	JP205	A - 2	TP204	F - 3
		IC211	C - 2	IC230	H - 2	JP206	A - 2	TP206	G - 3
EP201	A - 1	IC212	C - 3	IC231	J - 1			TP207	J - 4
EP202	A - 5	IC213	C - 4	IC232	J - 2	Q201	A - 2	TP208	J - 4
EP203	G - 2	IC214	C - 5	*IC233	J - 3	Q202	A - 2		
EP204	G - 5	IC215	D - 1	IC234	K - 1	Q203	E - 4	X201	F - 4
EP205	L - 2	IC216	D - 2	IC235	K - 2	Q204	E - 4	X202	J - 5
EP206	L - 5	IC217	D - 3	IC236	K - 3	Q205	A - 2		

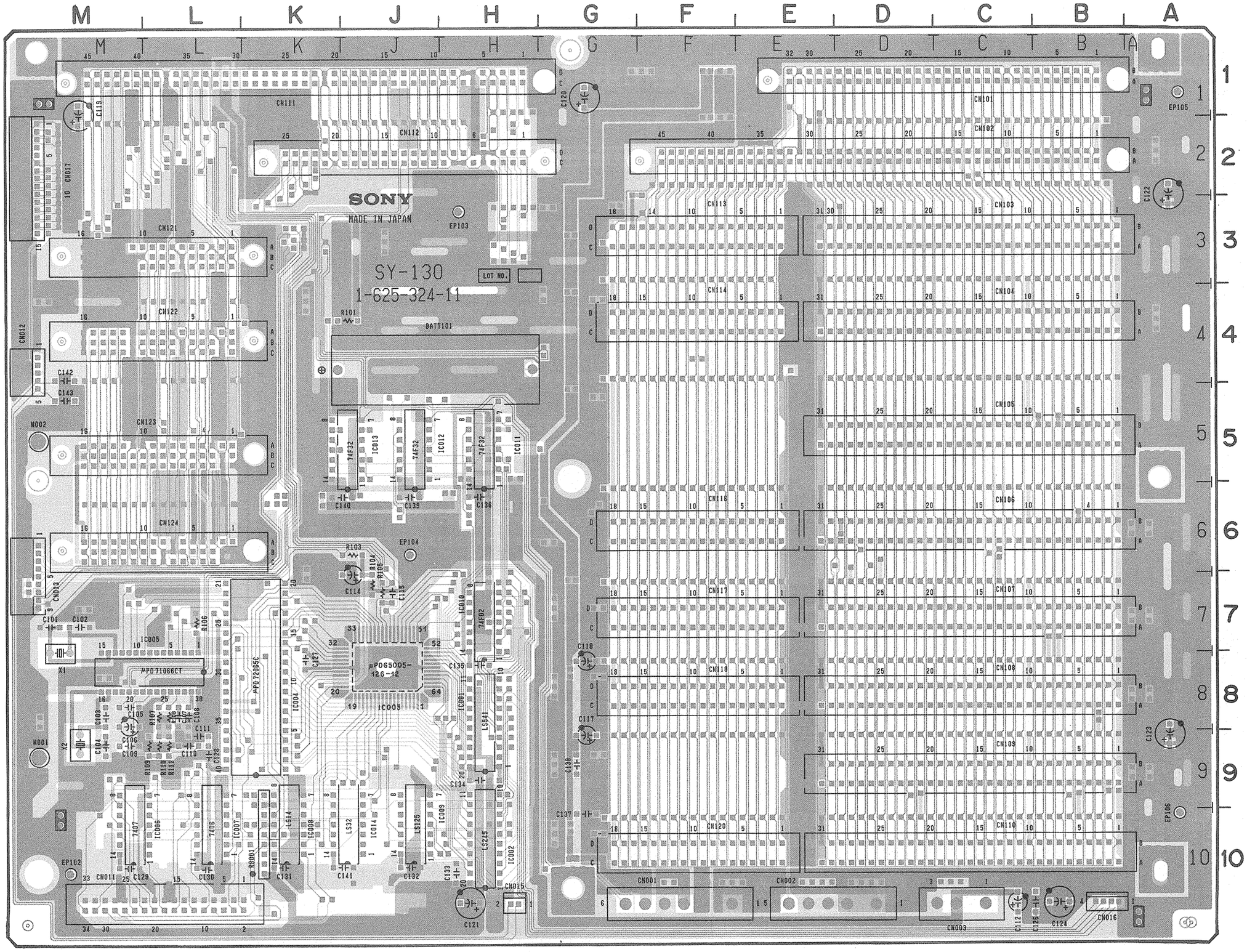
*: SOLDERING SIDE

5-5. SY-130 BOARD



SY-130 – COMPONENT SIDE –

1-625-324-11
SMC-3000VP(EK)
VIW-3015A(UC)



C101	M- 7	CN111	K - 1
C102	M- 7	CN112	J - 2
C103	M- 8	CN113	F - 3
C104	M- 9	CN114	F - 4
C105	M- 8	CN116	F - 6
C106	M- 9	CN117	F - 7
C107	L - 8	CN118	F - 8
C108	L - 8	CN120	F - 10
C109	M- 9	CN121	L - 3
C110	L - 9	CN122	L - 4
C111	L - 9	CN123	L - 5
C112	C - 10	CN124	L - 6
C114	J - 7		
C115	J - 7	EP102	M- 10
C117	G - 8	EP103	H - 3
C118	G - 8	EP104	J - 6
C119	M- 1	EP105	A - 1
C120	G - 1	EP106	A - 10
C121	H - 10		
C122	A - 2	IC001	H - 8
C123	A - 9	IC002	H - 10
C124	B - 10	* IC003	L - 8
C126	B - 10	IC004	K - 8
C127	K - 8	IC005	L - 8
C128	L - 9	IC006	M- 10
C129	M- 10	IC007	L - 10
C130	L - 10	IC008	K - 10
C131	K - 10	IC009	J - 10
C132	J - 10	IC010	H - 7
C133	H - 10	IC011	H - 5
C134	H - 9	IC012	J - 5
C135	H - 8	IC013	J - 5
C136	H - 6	IC014	J - 10
C137	G - 10		
C138	G - 9	R101	J - 4
C139	J - 6	R103	J - 6
C140	J - 6	R104	J - 7
C141	J - 10	R105	J - 7
C142	M- 4	R106	L - 7
C143	M- 5	R107	L - 8
		R108	L - 8
CN001	F - 10	R109	L - 9
CN002	E - 10	R110	L - 9
CN003	C - 10	R111	L - 9
CN011	M- 10		
CN012	M- 4	RB001	K - 10
CN013	M- 7		
CN015	H - 10	W001	M- 9
CN016	B - 10	W002	M- 5
CN017	M- 2		
CN101	C - 1	X1	M- 8
CN102	C - 2	X2	M- 9
CN103	C - 3		
CN104	C - 4	*: SOLDERING SIDE	
CN105	C - 5		
CN106	C - 6		
CN107	C - 7		
CN108	C - 8		
CN109	C - 9		
CN110	C - 10		

SY-130 – COMPONENT SIDE –

1-625-324-11
SMC-3000VP(EK)
VIW-3015A(UC)

MODEL NAME	CP-
SMC-3000VP(EK) S/N 10000s	CP-110 board
SMC-3000VP(EK) S/N 50000s	CP-138 board
VIW-3015A(UC)	CP-110 board

Boards DSC-38, DSC-43V and VS-36 mounted on ONLY SMC-3000VP(EK).

Ref. No.	TYPE	Pin No. +5V	Pin No. GND
IC13	MC74F32N	14	7
IC14	SN74LS32N	14	7

2/2 SUB-FDD

2/2 SUB-C

2/2 SUB-A

CN101 (IF-156/CN203)

A1	(-I/OCHCK)
A2	SD7
A3	SD6
A4	SD5
A5	SD4
A6	SD3
A7	SD2
A8	SD1
A9	SD0
A10	(I/OCHRDY)
A11	AEN
A12	(SA19)
A13	(SA18)
A14	(SA17)
A15	(SA16)
A16	SA15
A17	SA14
A18	SA13
A19	SA12
A20	SA11
A21	SA10
A22	SA9
A23	SA8
A24	SA7
A25	SA6
A26	SA5
A27	SA4
A28	SA3
A29	SA2
A30	SA1
A31	SA0
A32	-I/OCS16

CN102 (PU-59/CN303)

A1	-I/OCHCK
A2	SD7
A3	SD6
A4	SD5
A5	SD4
A6	SD3
A7	SD2
A8	SD1
A9	SD0
A10	I/OCHRDY
A11	AEN
A12	SA19
A13	SA18
A14	SA17
A15	SA16
A16	SA15
A17	SA14
A18	SA13
A19	SA12
A20	SA11
A21	SA10
A22	SA9
A23	SA8
A24	SA7
A25	SA6
A26	SA5
A27	SA4
A28	SA3
A29	SA2
A30	SA1
A31	SA0
A32	-SBHE
A33	LA23
A34	LA22
A35	LA21
A36	LA20
A37	LA19
A38	LA18
A39	LA17
A40	-MEMR
A41	-MEMW
A42	SD8
A43	SD9
A44	SD10
A45	SD11

CN111 (IF-156/CN204)

C1	(IRQ10)
C2	(IRQ11)
C3	(IRQ12)
C4	(IRQ15)
C5	-AIOR
C6	GND
C7	(NC)
C8	GND
C9	GND
C10	(-RES)
C11	-RC
C12	A20 GATE
C13	OUT BUFFUL
C14	(+5V)
C15	-INTER
C16	+5V
C17	-8042CS
C18	TIM2 GT
C19	-MHLDA
C20	(LOW)
C21	GND
C22	KBD CLK
C23	NC
C24	NC
C25	NC
C26	NC
C27	(NC)
C28	(NC)
C29	(NC)
C30	(NC)
C31	(NC)
C32	NC
C33	(SP OUT)
C34	-3F0CS
C35	-RST DRV
C36	-SIOR
C37	GND
C38	CD-COM2
C39	RxD-COM2
C40	TxD-COM2
C41	DTR-COM2
C42	(NC)
C43	VR-C
C44	ST-1
C45	-RES SW

CN112 (PU-59/CN302)

C1	SD12
C2	SD13
C3	SD14
C4	SD15

CN112 (PU-59/CN302)

C5	GND
C6	(NC)
C7	GND
C8	GND
C9	-RES
C10	-RC
C11	A20 GATE
C12	OUT BUFFUL
C13	P.GOOD
C14	-INTER
C15	+5V
C16	-8042CS
C17	TIM2 GT
C18	-MHLDA
C19	(LOW)
C20	GND
C21	(KBD CLK)

CN112 (PU-59/CN302)

C22	(CD-COM2)
C23	(RxD-COM2)
C24	(TxD-COM2)
C25	(DTR-COM2)

CN17 (CP- /W201)

1	GND
2	KBD CLK
3	KBD DATA
4	LP DATA
5	LP SW
6	GND
7	CD
8	DSR
9	RxD
10	RTS
11	TxD
12	CTS
13	DTR
14	RI
15	+5V

2/2 BS-1

8 13 10 9

SOUND1

CN121 (DSC-38/CN403)

A1	-SIOR
A2	-3D0CS
A3	GND
A4	CG/-HG
A5	HD
A6	(FIELD)
A7	GND
A8	B/W
A9	CHR-R
A10	LP DATA
A11	LP SW
A12	GND
A13	GND
A14	GND
A15	GND
A16	GND
B1	GND
B2	GND
B3	DCK
B4	VS
B5	BLANKING
B6	GND
B7	(GDC FIELD)
B8	L ON
B9	CHR-G
B10	GND
B11	GND
B12	GND
B13	GND
B14	GND
B15	GND
B16	GND

CN122 (DSC-43/CN603)

A1	-SIOR
A2	M/-HG
A3	GND
A4	CG/-HG
A5	(NC)
A6	FIELD
A7	GND
A8	(NC)
A9	CHR-R
A10	GND
A11	GND
A12	R1
A13	R2
A14	R3
A15	R4
A16	GND
B1	HREF
B2	GND
B3	DCK
B4	VS
B5	BLANKING
B6	GND
B7	GDC FIELD
B8	(NC)
B9	CHR-G
B10	XPT
B11	GND
B12	G1
B13	G2
B14	G3
B15	G4
B16	GND

CN123 (VS-36/CN121)

A1	(RESERVED)
A2	(RESERVED)
A3	GND
A4	GND
A5	HD
A6	FIELD
A7	SOUND1
A8	(NC)
A9	(RESERVED)
A10	GND
A11	GND
A12	R1
A13	R2
A14	R3
A15	R4
A16	(+12V)
B1	HREF
B2	GND
B3	DCK
B4	VS
B5	BLANKING
B6	GND
B7	GDC FIELD
B8	L ON
B9	(PASS MODE)
B10	XPT
B11	(B.FLAG)
B12	G1
B13	G2
B14	G3
B15	G4
B16	GND

CN124 (NO MOUNTED)

A1	(RESERVED)
A2	(RESERVED)
A3	GND
A4	GND
A5	GND
A6	FIELD
A7	GND
A8	(NC)
A9	(RESERVED)
A10	GND
A11	GND
A12	R1
A13	R2
A14	R3
A15	R4
A16	+12V
B1	GND
B2	GND
B3	DCK
B4	VS
B5	BLANKING
B6	GND
B7	GND
B8	GND
B9	(PASS MODE)
B10	XPT
B11	(B.FLAG)
B12	G1
B13	G2
B14	G3
B15	G4
B16	GND

2/2 SUB-B

CN101 (IF-156/CN203)

B1	GND
B2	RESET DRV
B3	+5V
B4	(IRQ9)
B5	(-5V)
B6	(DRQ2)
B7	(-12V)
B8	(OWS)
B9	+12V
B10	GND
B11	(-SMEMW)
B12	(-SMEMR)
B13	-IOW
B14	-IOR
B15	(-DACK3)
B16	(DRQ3)
B17	(-DACK1)
B18	(DRQ1)
B19	(-REFRESH)
B20	CLK
B21	IRQ7
B22	(IRQ6)
B23	(IRQ5)
B24	IRQ4
B25	IRQ3
B26	(-DACK2)
B27	(T/C)
B28	(BALE)
B29	+5V
B30	(14.318MHz)
B31	GND
B32	-I/OCS IN

CN102 (PU-59/CN303)

B1	GND
B2	RESET DRV
B3	+5V
B4	IRQ9
B5	(-5V)
B6	DRQ2
B7	(-12V)
B8	OWS
B9	(+12V)
B10	GND
B11	-SMEMW
B12	-SMEMR
B13	-IOW
B14	-IOR
B15	-DACK3
B16	DRQ3
B17	-DACK1
B18	DRQ1
B19	-REFRESH
B20	CLK
B21	IRQ7
B22	IRQ6
B23	IRQ5
B24	IRQ4
B25	IRQ3
B26	-DACK2
B27	T/C
B28	BALE
B29	+5V
B30	14.318MHz
B31	GND
B32	-MEMCS16
B33	-I/OCS IN
B34	IRQ10
B35	IRQ11
B36	IRQ12
B37	IRQ15
B38	IRQ14
B39	-DACK0
B40	DRQ0
B41	-DACK5
B42	DRQ5
B43	-DRCK6
B44	DRQ6
B45	-DACK7

CN111 (IF-156/CN204)

D1	+5V
D2	+5V
D3	(-MASTER)
D4	GND
D5	-AIOW
D6	GND
D7	GND
D8	PCLK
D9	1.19MHz
D10	REF REQ
D11	OUT2
D12	IRQ0
D13	(NC)
D14	(+5V)
D15	IRQ8
D16	+5V
D17	(-TCCS)
D18	SPKR DATA
D19	(COM)
D20	(HIGH)
D21	GND
D22	KBD DATA
D23	(NC)
D24	(NC)
D25	(NC)
D26	(NC)
D27	(NC)
D28	(NC)
D29	(NC)
D30	(NC)
D31	(NC)
D32	BAT
D33	SOUND1
D34	-3D0CS
D35	-500CS
D36	-SIOW
D37	GND
D38	DSR-COM2
D39	RTS-COM2
D40	CTS-COM2
D41	RI-COM2
D42	P.GOOD
D43	VR-M
D44	ST-2
D45	GND

CN112 (PU-59/CN302)

D1	DRQ7
D2	+5V
D3	-MASTER
D4	GND

CN112 (PU-59/CN302)

D5	GND
D6	GND
D7	PCLK
D8	1.19MHz
D9	REF REQ
D10	OUT2
D11	IRQ0
D12	(+5V)
D13	(+5V)
D14	IRQ8
D15	+5V
D16	-TCCS
D17	SPKR DATA
D18	(COM)
D19	(HIGH)
D20	M/-HG
D21	(KBD DATA)

R101 680 BAT101 3.6V

CN112 (PU-59/CN302)

D22	(DSR-COM2)
D23	(RTS-COM2)
D24	(CTS-COM2)
D25	(RI-COM2)

CN13 (VR-60/W102)

1	GND
2	VR-C
3	GND
4	VR-M
5	GND
6	ST-1
7	ST-2
8	RESET
9	+5V

2/2 SUB-D

-I/OCS IN

1-6 P.GOOD
2-5 -REMOTE

CN12 (SW-198/W001)

12-1	+5V
12-2	-REMOTE
12-3	GND
12-4	+5V 330Ω
12-5	-HDD LAMP

CN15 (FROM OPTION)

15-1	+5V 330Ω
15-2	-HDD LAMP

+12V C118 47 16V C137 0.1

+5V C119-124 100 x6 16V 0.1 x15 C106 10 16V

C111 C126-136 C139-141 C117 47 16V C138 0.1

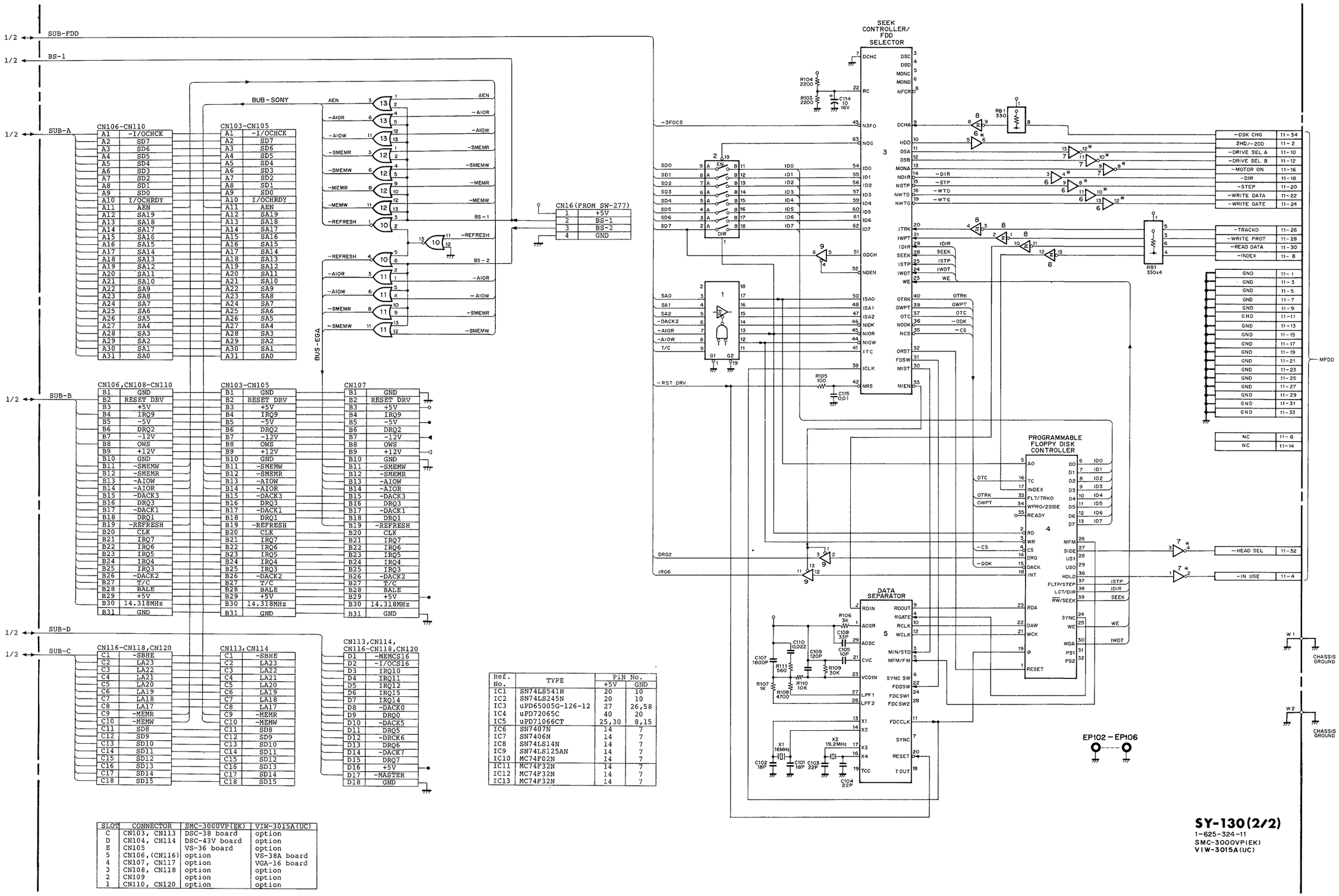
-12V C112 10 16V

-5V

1-3 +12V
1-1 +5V
2-1 +5V
2-2 +5V
1-2 GND
1-4 GND
2-3 GND
2-4 GND
3-3 GND
1-5 -12V
3-1 NC
3-2 -5V

CN1-CN3 (FROM SWITCHING REGULATOR)

SY-130(1/2)
1-625-324-11
SMC-3000VP(EK)
VIW-3015A(UC)

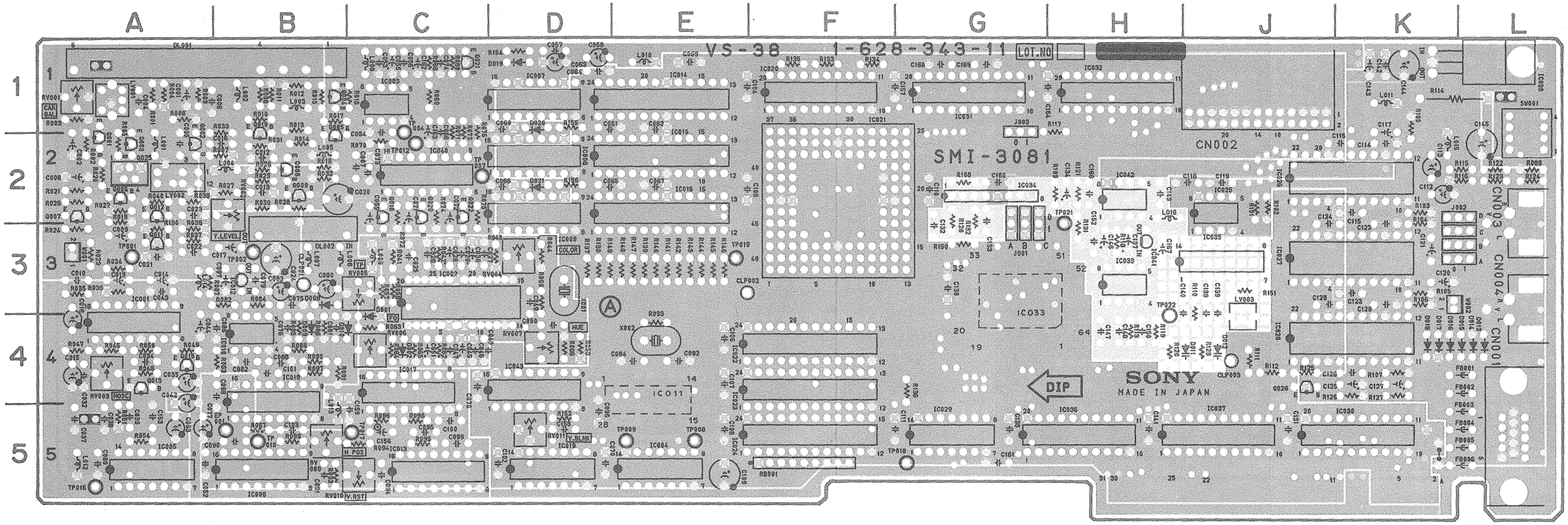


SLOT	CONNECTOR	SMC-3000VP(EK)	VIW-3015A(UC)
C	CN103, CN113	DSC-38 board	option
D	CN104, CN114	DSC-43V board	option
E	CN105	VS-36 board	option
5	CN106,(CN116)	option	VS-38A board
4	CN107, CN117	option	VGA-16 board
3	CN108, CN118	option	option
2	CN109	option	option
1	CN110, CN120	option	option

Ref. No.	TYPE	PiN No. +5V	PiN No. GND
IC1	SN74LS541N	20	10
IC2	SN74LS245N	20	10
IC3	uPD65005G-126-12	27	26,58
IC4	uPD72065C	40	20
IC5	uPD71066CT	25,30	8,15
IC6	SN7407N	14	7
IC7	SN7406N	14	7
IC8	SN74LS14N	14	7
IC9	SN74LS125AN	14	7
IC10	MC74F02N	14	7
IC11	MC74F32N	14	7
IC12	MC74F32N	14	7
IC13	MC74F32N	14	7

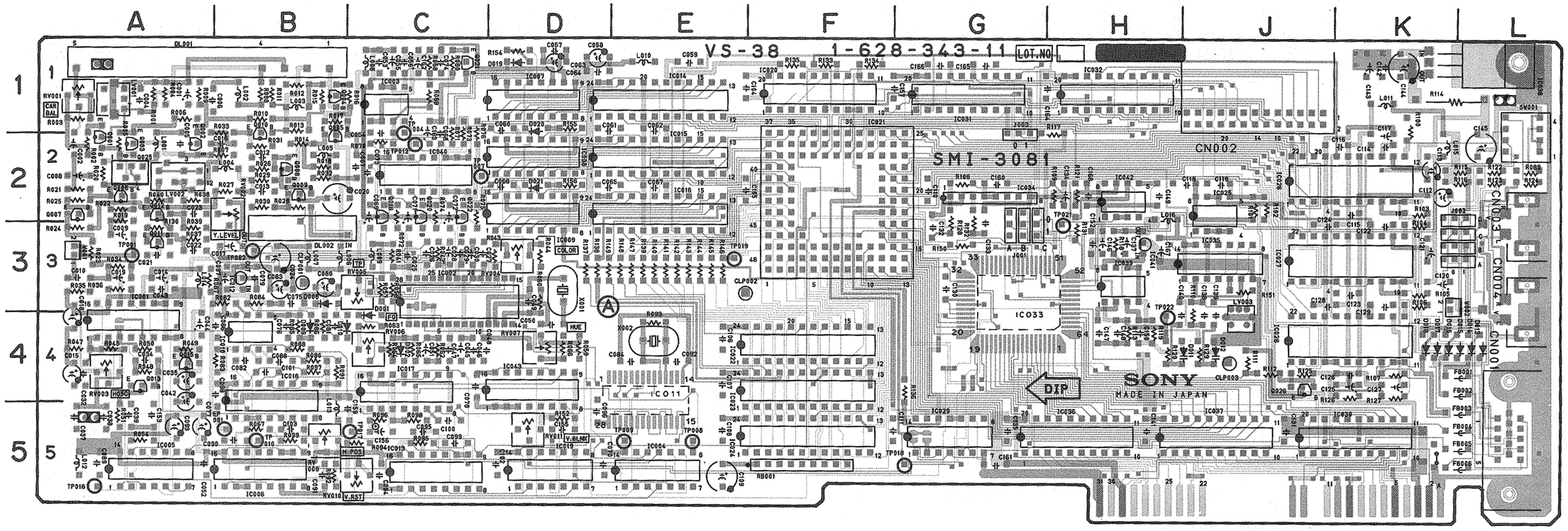
SY-130(2/2)
1-625-324-11
SMC-3000VP(EK)
VIW-3015A(UC)

5-6. VS-38A BOARD



VS-38 – COMPONENT SIDE –

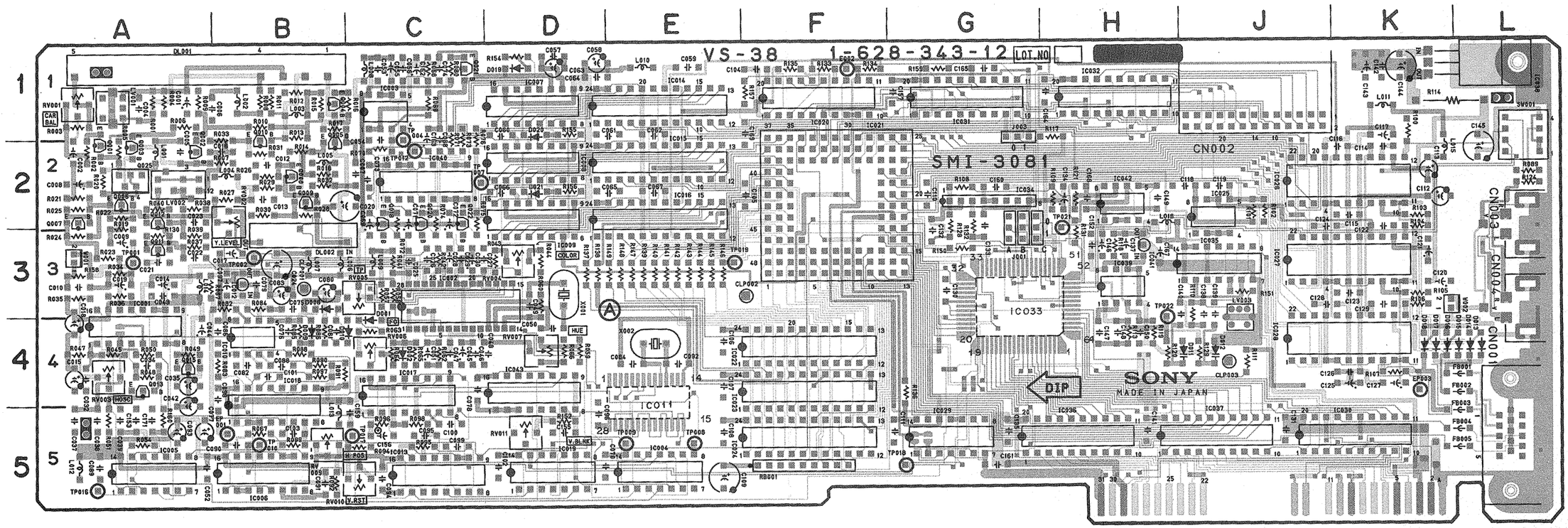
1-628-343-11
SMI-3081/2(UC)
VIW-3015A(UC)



VS-38 – COMPONENT SIDE –

1-628-343-11
SMI-3081/2(UC)
VIW-3015A(UC)

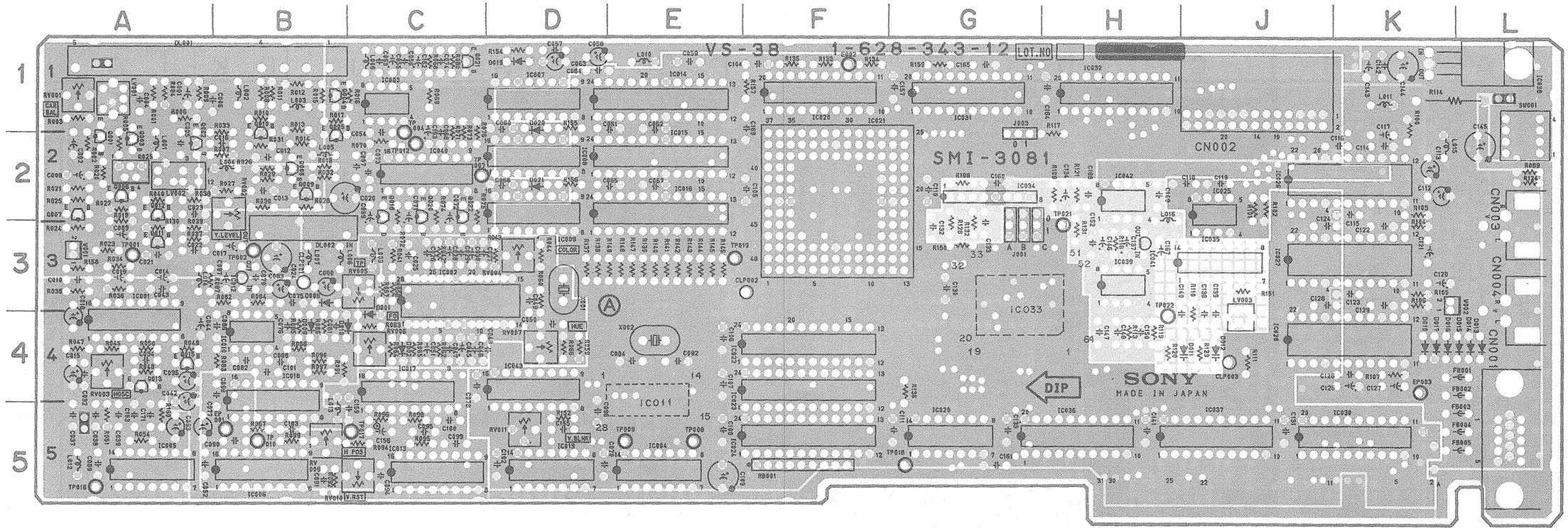
C001	A-1	C044	A-4	C080	B-3	C118	J-2	C157	G-1	EP001	B-5	IC028	J-4	L012	A-5	R006	A-1	R042	C-3	R088	B-4	R124	L-2	RV001	A-1
C002	A-2	C045	C-4	C081	B-4	C119	J-2	C159	C-5			IC029	G-5	L013	B-5	R007	B-2	R043	D-3	R089	L-2	R125	J-4	RV002	B-2
C004	A-1	C046	C-4	C082	B-4	C120	K-3	C160	G-2	FB001	L-4	IC030	K-5	L014	A-3	R008	B-1	R044	D-3	R090	B-4	R126	K-4	RV003	A-4
C005	A-2	C047	C-4	C083	B-3	C121	K-3	C161	G-5	FB002	L-4	IC031	G-1	L015	K-2	R009	A-1	R045	A-4	R091	B-4	R127	K-4	RV004	D-3
C006	B-1	C048	D-4	C084	E-4	C122	K-3	C162	C-1	FB003	L-5	IC032	H-1	L016	H-2	R010	B-1	R047	A-4	R092	B-5	R128	G-2	RV005	C-3
C007	C-2	C049	D-3	C086	B-4	C123	K-3	C163	C-1	FB004	L-5	*IC033	G-3			R011	B-1	R048	A-4	R093	E-4	R129	J-4	RV006	C-4
C008	A-2	C050	D-4	C088	B-4	C124	J-2	C164	H-1	FB005	L-5	IC034	G-2	LV001	A-1	R012	B-1	R049	A-4	R094	C-5	R130	A-3	RV007	D-4
C009	A-3	C051	C-4	C089	A-5	C125	K-4	C165	G-1	FB006	L-5	IC035	J-3	LV002	A-2	R013	B-1	R050	A-4	R095	C-5	R131	H-3	RV009	B-5
C010	A-3	C052	A-5	C090	B-5	C126	K-4	C166	G-1			IC036	H-5	LV003	J-3	R014	B-2	R051	A-5	R096	C-5	R132	G-2	RV010	C-5
C012	B-2	C053	C-1	C091	B-5	C127	K-4	C167	H-3	IC001	A-3	IC037	J-5			R015	B-1	R054	A-5	R097	B-4	R133	F-1	RV011	D-5
C013	B-2	C054	C-2	C092	E-4	C128	J-3	C168	H-2	IC002	C-2	IC038	L-1	Q001	A-2	R016	C-1	R057	C-3	R098	C-5	R134	F-1		
C014	A-3	C055	C-1	C093	A-5	C129	K-3			IC003	C-1	IC039	H-3	Q002	A-2	R017	B-1	R058	C-3	R099	B-5	R135	F-1	SW001	L-1
C015	A-4	C056	C-1	C094	C-5	C130	G-3			IC004	E-5	IC040	C-2	Q003	A-2	R018	B-2	R059	D-4	R100	K-1	R136	G-4		
C016	B-2	C057	D-1	C095	C-5	C131	J-5	CN001	L-4	IC005	A-5	IC041	H-3	Q004	B-1	R019	A-2	R060	D-3	R101	J-2	R137	D-3	TP001	A-3
C017	B-3	C058	D-1	C096	D-5	C132	G-3	CN002	J-2	IC006	B-5	IC042	H-2	Q005	B-1	R020	A-2	R062	C-4	R102	J-2	R138	D-3	TP002	B-3
C018	A-3	C059	E-1	C097	B-3	C133	G-3	CN003	L-2	IC007	D-1	IC043	D-4	Q006	A-2	R021	A-2	R063	C-4	R103	K-2	R139	E-3	TP004	C-1
C019	A-3	C060	D-1	C098	B-4	C134	H-2	CN004	L-3	IC008	D-2			Q007	A-2	R022	A-2	R064	C-4	R104	K-2	R140	E-3	TP007	C-2
C020	C-2	C061	D-1	C099	C-5	C135	G-5			IC009	D-3	J001A	G-3	Q008	B-2	R023	A-3	R065	C-4	R105	K-3	R141	E-3	TP008	E-5
C021	A-3	C062	E-1	C100	C-5	C137	H-3	D001	C-4	IC010	B-4	J001B	G-3	Q009	B-2	R024	A-3	R066	D-4	R106	K-3	R142	E-3	TP009	E-5
C022	A-3	C063	D-1	C101	B-4	C138	J-3	D002	C-4	*IC011	E-4	J001C	G-3	Q010	B-1	R025	A-2	R067	B-5	R107	K-4	R143	E-3	TP010	B-5
C023	A-2	C064	D-1	C102	D-5	C139	J-3	D008	B-3	IC012	B-3	J002A	L-2	Q011	A-3	R026	B-2	R068	C-1	R108	G-2	R144	E-3	TP012	C-2
C024	B-3	C065	E-2	C103	B-5	C140	J-3	D009	B-4	IC013	C-5	J002B	L-2	Q012	A-2	R027	B-2	R069	C-1	R109	H-2	R145	E-3	TP016	A-5
C025	C-3	C066	D-2	C104	F-1	C141	H-5	D010	B-4	IC014	E-1	J002C	L-2	Q013	A-4	R028	B-2	R070	C-2	R110	J-3	R146	E-3	TP017	C-5
C026	C-3	C067	E-2	C105	F-2	C142	K-1	D011	J-4	IC015	E-2	J003	G-1	Q015	A-4	R029	B-2	R071	C-1	R111	J-4	R147	E-3	TP018	G-5
C027	C-3	C068	C-1	C106	E-4	C143	K-1	D012	J-4	IC016	E-2			Q018	C-2	R030	B-2	R072	C-3	R112	J-4	R148	E-3	TP019	E-3
C028	C-3	C069	C-3	C107	E-4	C144	K-1	D013	L-4	IC017	C-4	L001	A-2	Q020	C-2	R031	B-2	R073	C-1	R113	H-4	R149	D-3	TP021	H-2
C029	C-3	C070	E-5	C108	E-5	C145	L-1	D014	L-4	IC018	B-4	L002	B-1	Q021	C-1	R032	B-2	R074	C-2	R114	K-1	R150	G-3	TP022	H-3
C030	C-3	C071	C-3	C109	E-5	C146	H-3	D015	L-4	IC019	D-5	L003	B-1	Q022	C-2	R033	B-1	R075	C-2	R115	L-2	R151	J-3		
C032	A-4	C072	C-3	C110	G-2	C147	H-4	D016	K-4	IC020	F-1	L004	B-2	Q025	A-2	R034	A-3	R076	C-1	R116	L-2	R152	D-5	W001	A-3
C034	A-4	C073	C-2	C111	G-5	C148	H-4	D017	K-4	IC021	F-1	L005	B-2	Q026	J-4	R035	A-3	R080	C-1	R117	H-1	R154	D-1	W002	L-3
C035	A-3	C074	C-1	C112	K-2	C149	H-2	D018	K-4	IC022	F-2	L006	C-3			R036	A-3	R082	B-3	R118	H-3	R155	D-1		
C037	A-5	C075	B-3	C113	K-2	C150	H-4	D019	D-1	IC023	F-2	L007	B-3	R001	A-1	R037	A-3	R083	B-4	R119	H-4	R156	D-2	X001	D-3
C038	A-5	C076	B-4	C114	K-2	C152	H-3	D020	D-1	IC024	F-5	L008	C-1	R002	A-2	R038	A-2	R084	B-3	R120	H-4			X002	E-4
C039	A-5	C077	A-5	C115	K-2	C153	A-5	D021	D-2	IC025	J-2	L009	C-3	R003	A-1	R039	A-2	R085	B-4	R121	L-2	RB001	F-5		
C042	A-4	C078	C-4	C116	K-2	C155	D-5	DL001	A-1	IC026	J-2	L010	E-1	R004	A-1	R040	A-2	R086	B-4	R122	L-2				
C043	A-3	C079	B-3	C117	K-1	C156	C-5	DL002	B-3	IC027	J-3	L011	K-1	R005	A-2	R041	C-3	R087	B-3	R123	L-2	*; SOLDERING SIDE			



VS-38 – COMPONENT SIDE –

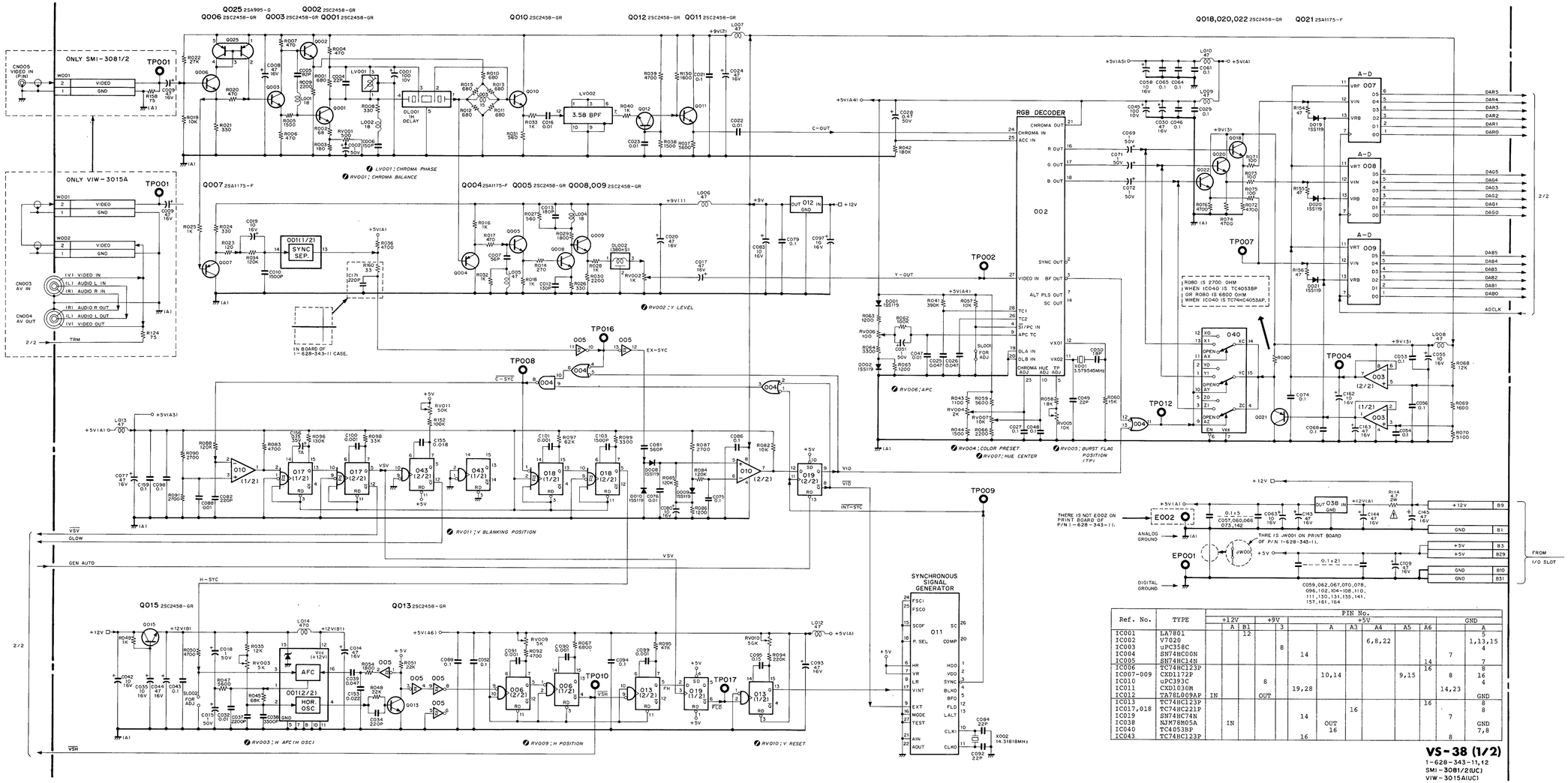
1-628-343-12
SMI-3081/2(UC)
VIW-3015A(UC)

C001	A-1	C044	A-4	C080	B-3	C118	J-2	C157	G-1	DL001	A-1	IC023	F-2	L010	E-1	R001	A-1	R037	A-3	R083	B-4	R128	G-2	RV001	A-1
C002	A-2	C045	C-4	C081	B-4	C119	J-2	C159	C-5	DL002	B-3	IC024	F-5	L011	K-1	R002	A-2	R038	A-2	R084	B-3	R129	J-4	RV002	B-2
C004	A-1	C046	C-4	C082	B-4	C120	K-3	C160	G-2			IC025	J-2	L012	A-5	R003	A-1	R039	A-2	R085	B-4	R130	A-3	RV003	A-4
C005	A-2	C047	C-4	C083	B-3	C121	K-3	C161	G-5	E002	F-1	IC026	J-2	L013	B-5	R004	A-1	R040	A-2	R086	B-4	R131	H-3	RV004	D-3
C006	B-1	C048	D-4	C084	E-4	C122	K-3	C162	C-1			IC027	J-3	L014	A-3	R005	A-2	R041	C-3	R087	B-3	R132	G-2	RV005	C-3
C007	C-2	C049	D-3	C086	B-4	C123	K-3	C163	C-1	EP001	B-5	IC028	J-4	L015	K-2	R006	A-1	R042	C-3	R088	B-4	R133	F-1	RV006	C-4
C008	A-2	C050	D-4	C088	B-4	C124	J-2	C164	H-1	EP003	E-4	IC029	G-5	L016	H-2	R007	B-2	R043	D-3	R089	L-2	R134	F-1	RV007	D-4
C009	A-3	C051	C-4	C089	A-5	C125	K-4	C165	G-1			IC030	K-5			R008	B-1	R044	D-3	R090	B-4	R135	F-1	RV009	B-5
C010	A-3	C052	A-5	C090	B-5	C126	K-4	C167	H-3	FB001	L-4	*IC031	G-1	LV001	A-1	R009	A-1	R045	A-4	R091	B-4	R136	G-4	RV010	C-5
C012	B-2	C053	C-1	C091	B-5	C127	K-4	C168	H-2	FB002	L-4	IC032	H-1	LV002	A-2	R010	B-1	R047	A-4	R092	B-5	R137	D-3	RV011	D-5
C013	B-2	C054	C-2	C092	E-4	C128	J-3	C169	F-1	FB003	L-5	IC033	G-3	LV003	J-3	R011	B-1	R048	A-4	R094	C-5	R138	D-3		
C014	A-3	C055	C-1	C093	A-5	C129	K-3	C171	A-5	FB004	L-5	IC034	G-2			R012	B-1	R049	A-4	R095	C-5	R139	E-3	SW001	L-1
C015	A-4	C056	C-1	C094	C-5	C130	G-3			FB005	L-5	IC035	J-3	Q001	A-2	R013	B-1	R050	A-4	R096	C-5	R140	E-3		
C016	B-2	C057	D-1	C095	C-5	C131	J-5	CN001	L-4			IC036	H-5	Q002	A-2	R014	B-2	R051	A-5	R097	B-4	R141	E-3	TP001	A-3
C017	B-3	C058	D-1	C096	D-5	C132	G-3	CN002	J-2	IC001	A-3	IC037	J-5	Q003	A-2	R015	B-1	R054	A-5	R098	C-5	R142	E-3	TP002	B-3
C018	A-3	C059	E-1	C097	B-3	C133	G-3	CN003	L-2	IC002	C-2	IC038	L-1	Q004	B-1	R016	C-1	R057	C-3	R099	B-5	R143	E-3	TP004	C-1
C019	A-3	C060	D-1	C098	B-4	C134	H-2	CN004	L-3	IC003	C-1	IC039	H-3	Q005	B-1	R017	B-1	R058	C-3	R100	K-1	R144	E-3	TP007	C-2
C020	C-2	C061	D-1	C099	C-5	C135	G-5			IC004	E-5	IC040	C-2	Q006	A-2	R018	B-2	R059	D-4	R101	J-2	R145	E-3	TP008	E-5
C021	A-3	C062	E-1	C100	C-5	C137	H-3	D001	C-4	IC005	A-5	IC041	H-3	Q007	A-2	R019	A-2	R060	D-3	R102	J-2	R146	E-3	TP009	E-5
C022	A-3	C063	D-1	C101	B-4	C138	J-3	D002	C-4	IC006	B-5	IC042	H-2	Q008	B-2	R020	A-2	R062	C-4	R103	K-2	R147	E-3	TP010	B-5
C023	A-2	C064	D-1	C102	D-5	C139	J-3	D008	B-3	IC007	D-1	IC043	D-4	Q009	B-2	R021	A-2	R063	C-4	R104	K-2	R148	E-3	TP012	C-2
C024	B-3	C065	E-2	C103	B-5	C140	J-3	D009	B-4	IC008	D-2			Q010	B-1	R022	A-2	R064	C-4	R105	K-3	R149	D-3	TP016	A-5
C025	C-3	C066	D-2	C104	E-1	C141	H-5	D010	B-4	IC009	D-3	J001A	G-3	Q011	A-3	R023	A-3	R065	C-4	R106	K-3	R150	G-3	TP017	C-5
C026	C-3	C067	E-2	C105	F-2	C142	K-1	D011	J-4	IC010	B-4	J001B	G-3	Q012	A-2	R024	A-3	R066	D-4	R107	K-4	R151	J-3	TP018	G-5
C027	C-3	C068	C-1	C106	E-4	C143	K-1	D012	J-4	*IC011	E-4	J001C	G-3	Q013	A-4	R025	A-2	R067	B-5	R108	G-2	R152	D-5	TP019	E-3
C028	C-3	C069	C-3	C107	E-4	C144	K-1	D013	L-4	IC012	B-3	J003	G-1	Q015	A-4	R026	B-2	R068	C-1	R109	H-2	R154	D-1	TP021	H-2
C029	C-3	C070	E-5	C108	E-5	C145	L-1	D014	L-4	IC013	C-5			Q018	C-2	R027	B-2	R069	C-1	R110	J-3	R155	D-1	TP022	H-3
C030	C-3	C071	C-3	C109	E-5	C146	H-3	D015	L-4	IC014	E-1	L001	A-2	Q020	C-2	R028	B-2	R070	C-2	R111	J-4	R156	D-2		
C032	A-4	C072	C-3	C110	G-2	C147	H-4	D016	K-4	IC015	E-2	L002	B-1	Q021	C-1	R029	B-2	R071	C-1	R113	H-4	R157	F-1	W001	A-3
C034	A-4	C073	C-2	C111	G-5	C148	H-4	D017	K-4	IC016	E-2	L003	B-1	Q022	C-2	R030	B-2	R072	C-3	R114	K-1	R158	A-3	W002	L-3
C035	A-3	C074	C-1	C112	K-2	C149	H-2	D018	K-4	IC017	C-4	L004	B-2	Q025	A-2	R031	B-2	R073	C-1	R117	H-1	R159	G-1		
C037	A-5	C075	B-3	C113	K-2	C150	H-4	D019	D-1	IC018	B-4	L005	B-2			R032	B-2	R074	C-2	R118	H-3	R160	A-5	X001	D-3
C038	A-5	C076	B-4	C114	K-2	C152	H-3	D020	D-1	IC019	D-5	L006	C-3			R033	B-1	R075	C-2	R119	H-4			X002	E-4
C039	A-5	C077	A-5	C115	K-2	C153	A-5	D021	D-1	IC020	F-1	L007	B-3			R034	A-3	R076	C-1	R120	H-4	RB001	F-5		
C042	A-4	C078	C-4	C116	K-2	C155	D-5			IC021	F-1	L008	C-1			R035	A-3	R080	C-1	R121	L-2				
C043	A-3	C079	B-3	C117	K-1	C156	C-5			IC022	F-2	L009	C-3			R036	A-3	R082	B-3	R124	L-2	*; SOLDERLING SIDE			



VS-38 – COMPONENT SIDE –

1-628-343-12
SMI-3081/2(UC)
VIW-3015A(UC)



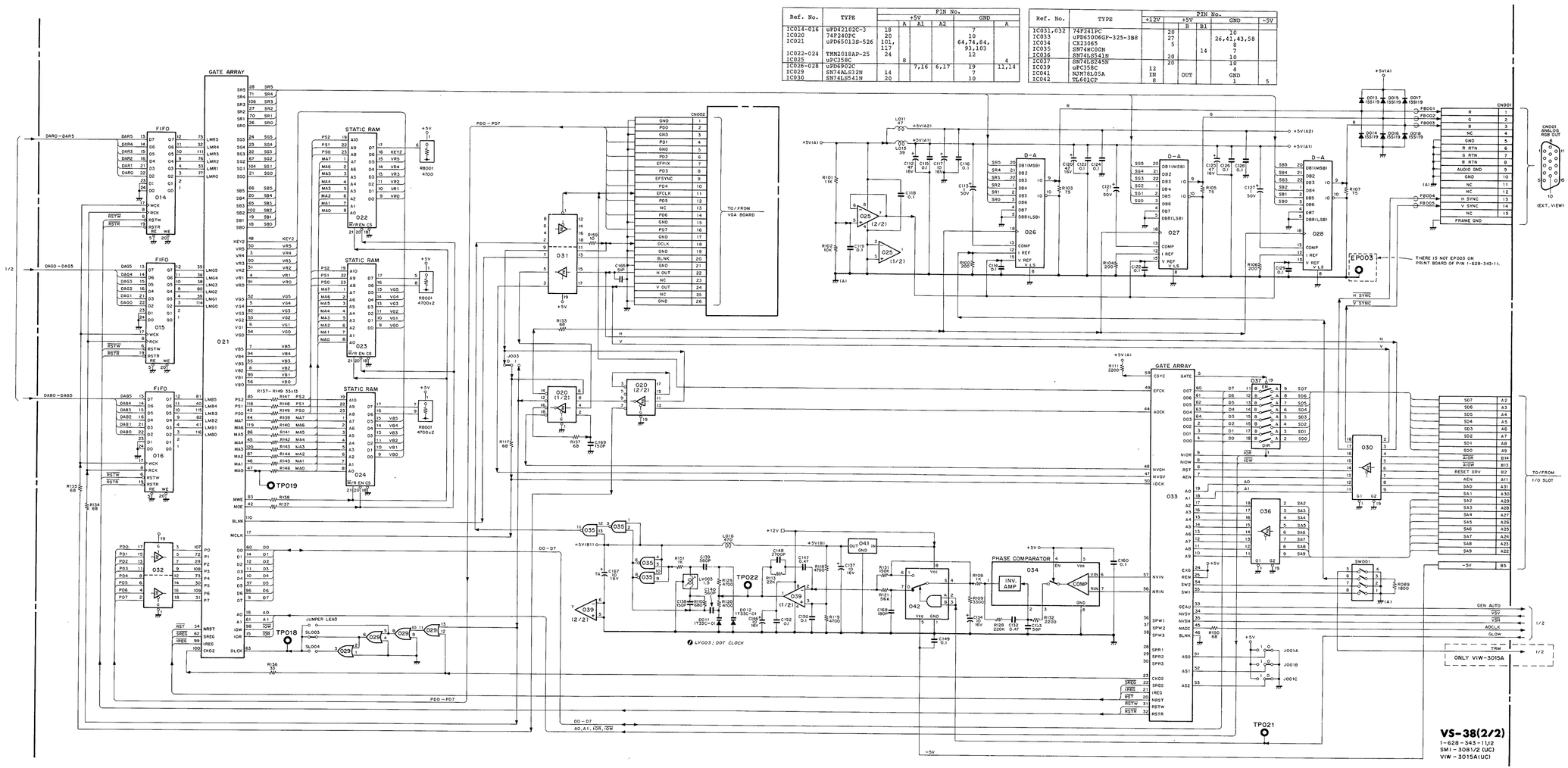
Ref. No.	TYPE	PIN No.											
		+12V		+9V		+5V						GND	
		A	B1		3		A	A3	A4	A5	A6		A
IC001	LA7801		12										5
IC002	V7020								6,8,22				1,13,15
IC003	uPC358C				8								4
IC004	SN74HC00N					14						7	
IC005	SN74HC14N										14		7
IC006	TC74HC123P										16		8
IC007-009	CXD1172P											8	16
IC010	uPC393C				8								4
IC011	CXD1030N						10,14			9,15		14,23	
IC012	TA78L009AP	IN			OUT	19,28							GND
IC013	TC74HC123P										16		8
IC017,018	TC74HC221P							16					8
IC019	SN74HC74N											8	
IC038	NJM78M05A		IN				OUT						GND
IC040	TC4053BP						16						7,8
IC043	TC74HC123P					16						8	

VS-38 (1/2)
1-628-343-11,12
SMI-3081/2(UC)
VIW-3015A(UC)

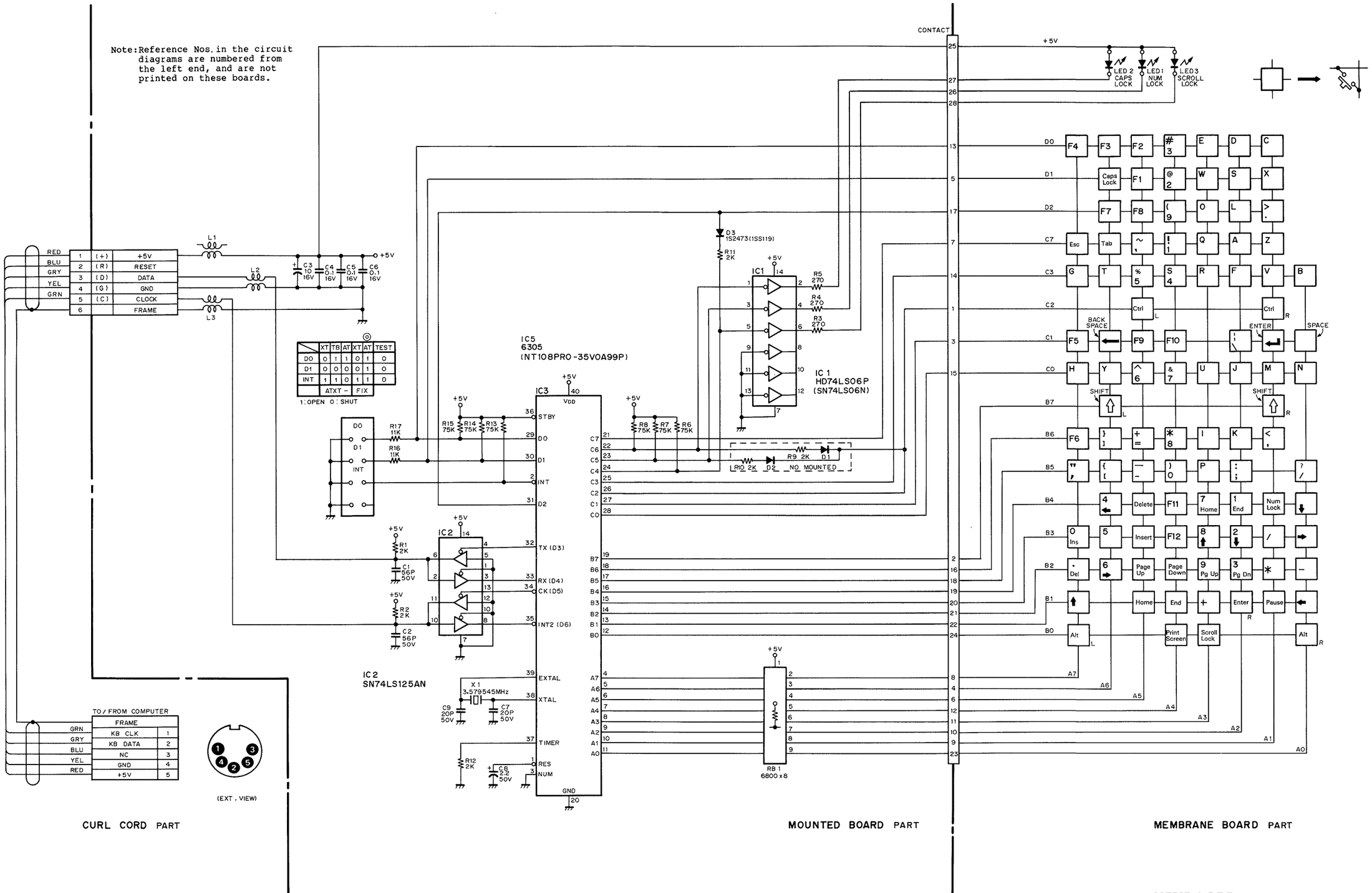
VS-38A(2/2) VS-38A(2/2)

Ref. No.	TYPE	PIN No. +5V	A	A1	A2	GND	A
IC014-016	uPD42102C-3	18				7	
IC020	74F240PC	20				10	
IC021	uPD65013G-526	101, 117				64,74,84, 93,103	
IC022-024	TMM2018AP-25	24				12	
IC025	uPC358C		8				4
IC026-028	uPD6902C			7,16	6,17	19	11,14
IC029	SN74ALS32N	14				7	
IC030	SN74LS541N	20				10	

Ref. No.	TYPE	PIN No. +12V	+5V B	+5V B1	GND	-5V
IC031,032	74F241PC		20		10	
IC033	uPD6506GF-325-3B8		27		26,41,43,58	
IC034	CX23065		1		8	
IC035	SN74HC06N			14	7	
IC036	SN74LS541N		20		10	
IC037	SN74LS245N		20		10	
IC039	uPC358C	12			4	
IC041	NJM78L05A	IN 8		OUT	GND 1	5
IC042	TL601CP					



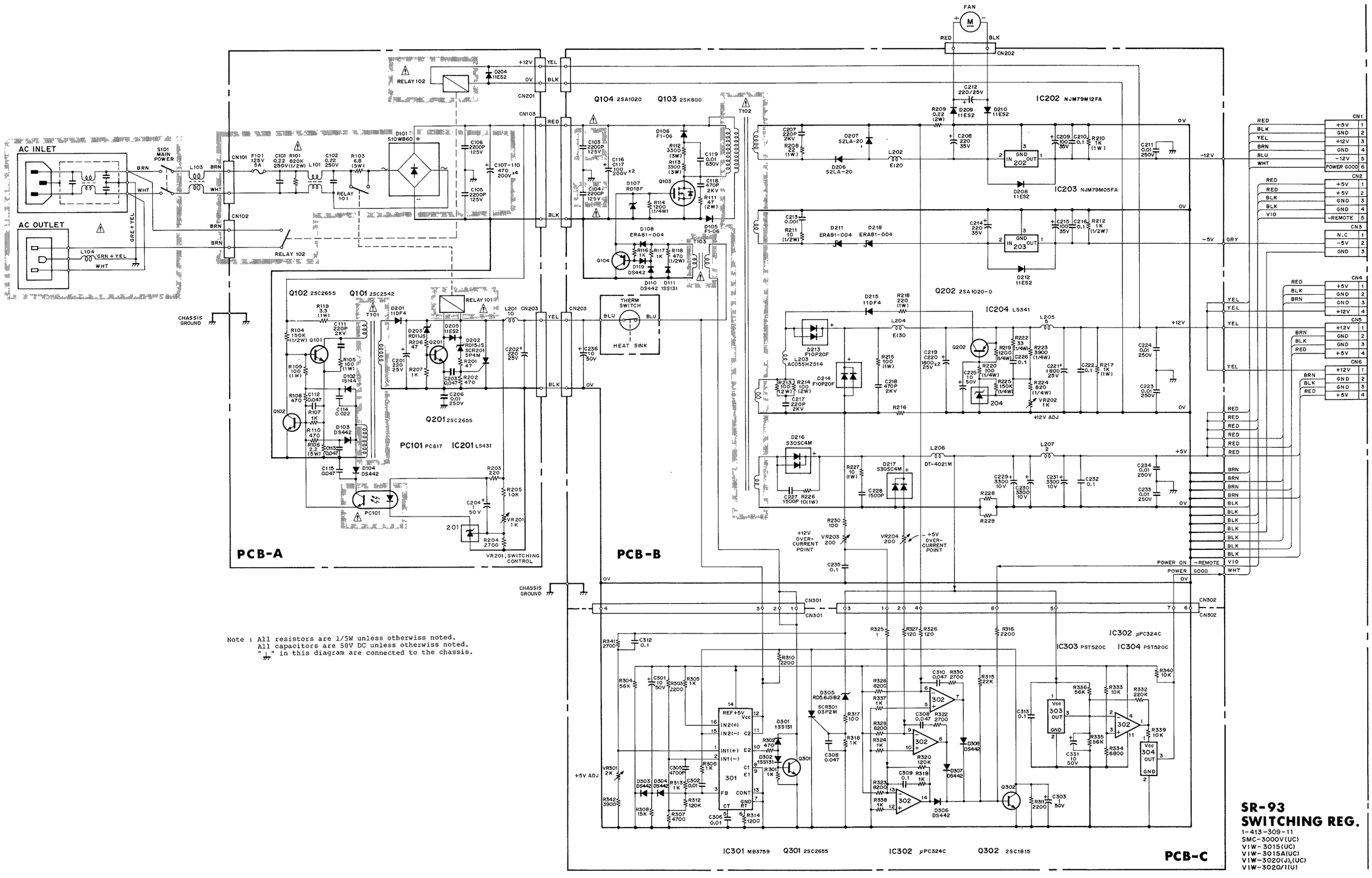
5-7. KEYBOARD



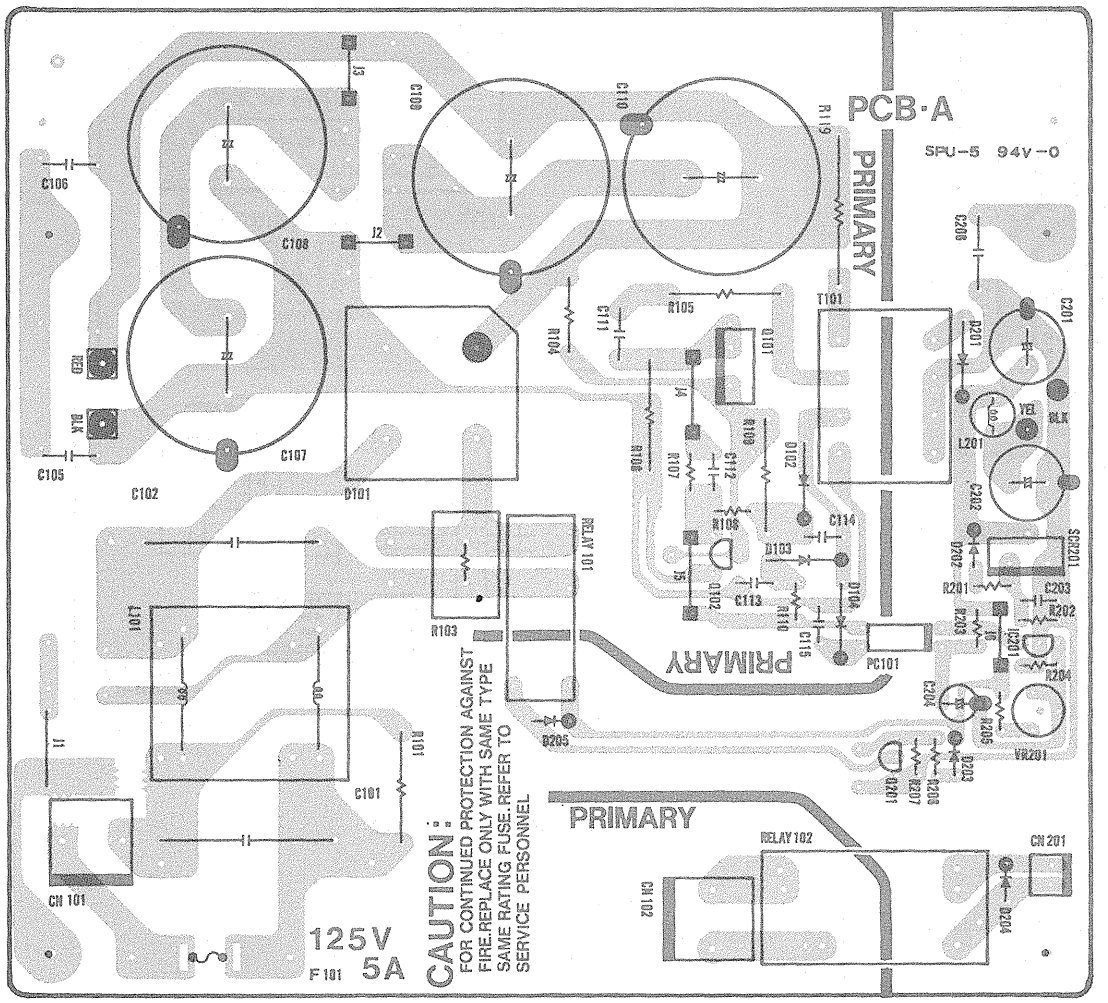
KEYBOARD
1-466-050-11,21
VIW-3015A(UC)
VIW-5000(UC)

SW. REG.	SW. REG.

5-8. SWITCHING REGULATOR

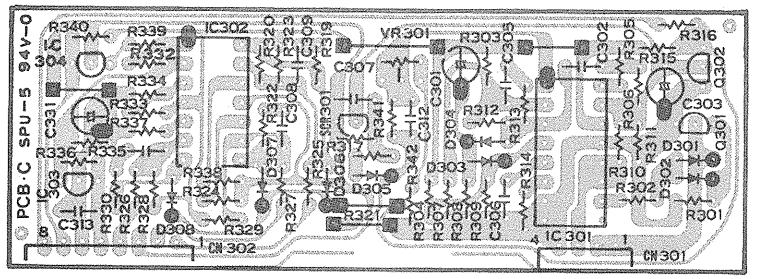


Note : All resistors are 1/5W unless otherwiss noted.
All capacitors are 50V DC unless otherwiss noted.
"⏚" in this diagram are connected to the chassis.



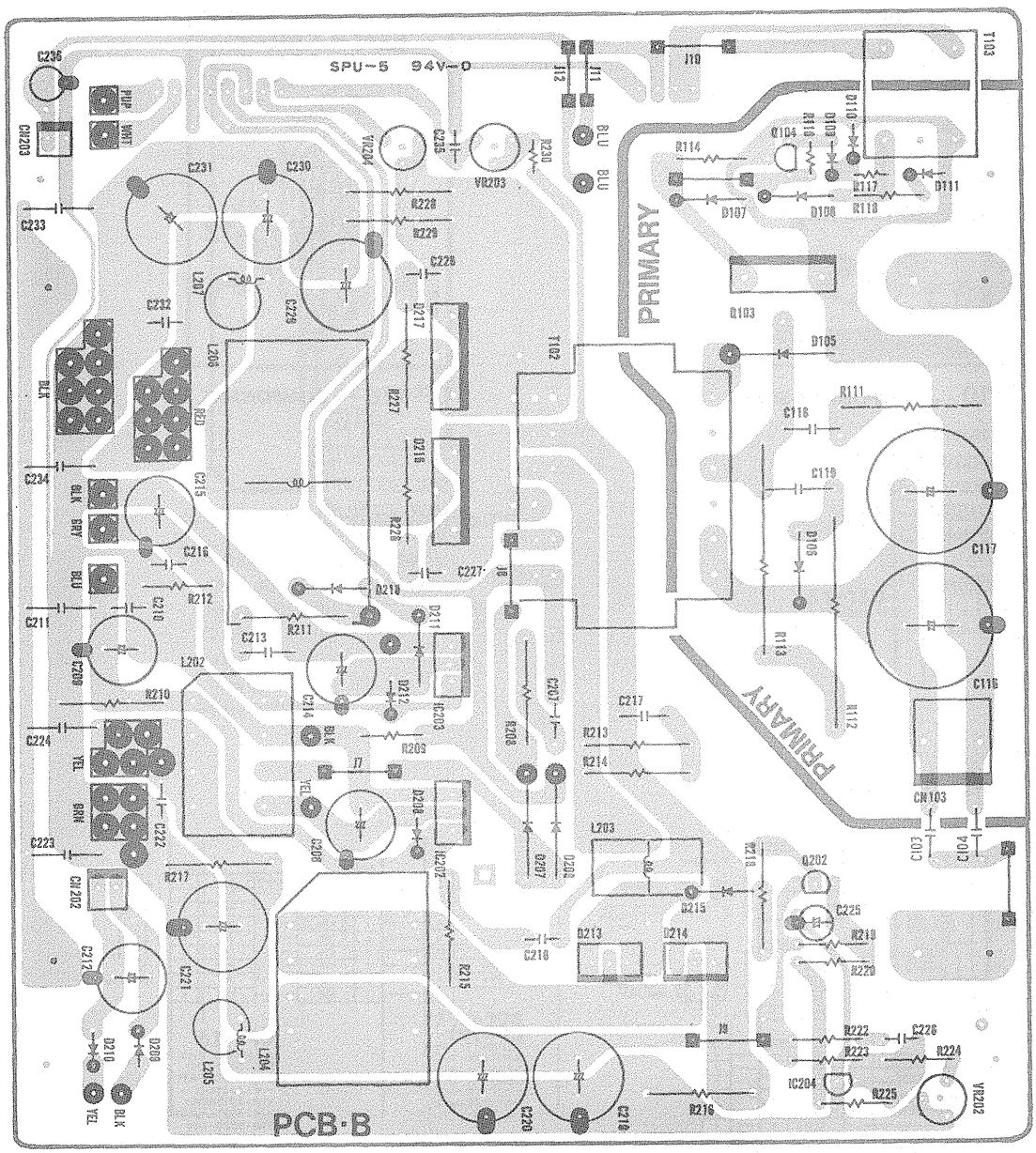
PCB-A – COMPONENT SIDE –

SMC-3000V(UC)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)



PCB-C – COMPONENT SIDE –

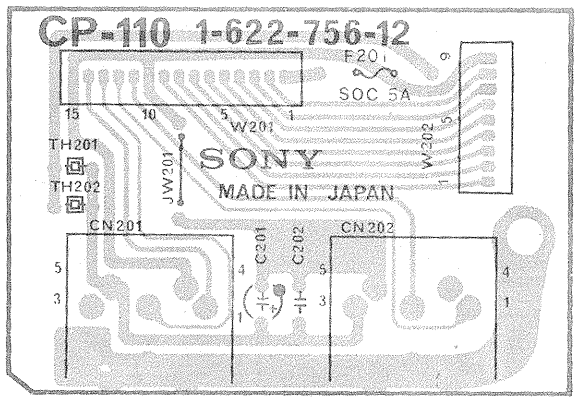
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)



PCB-B – COMPONENT SIDE –

SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)

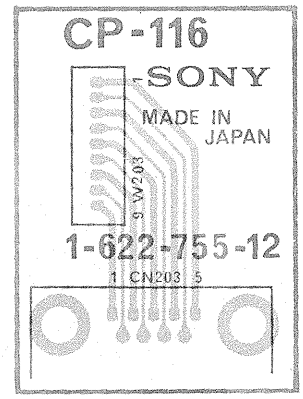
5-9. CP-110 BOARD



CP-110 – COMPONENT SIDE –

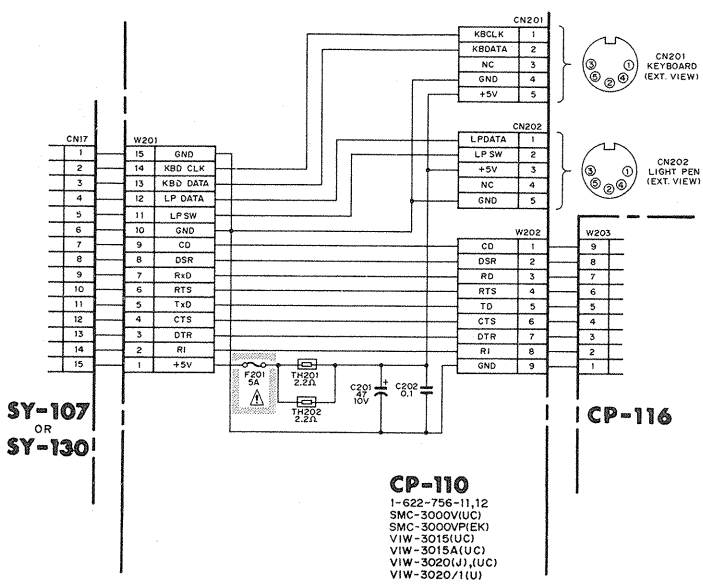
1-622-756-11, 12
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)

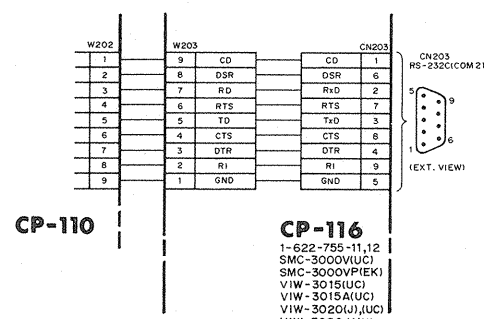
5-10. CP-116 BOARD



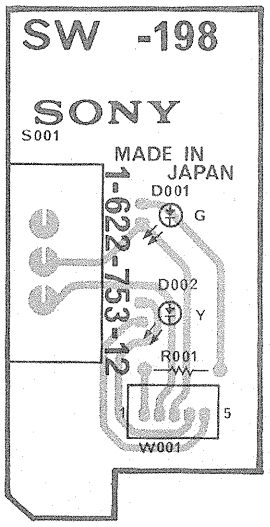
CP-116 – COMPONENT SIDE –

1-622-755-11, 12
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)



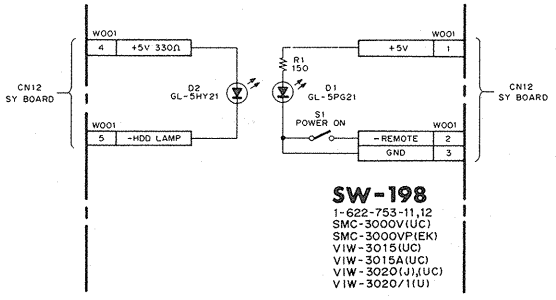


5-11. SW-198 BOARD

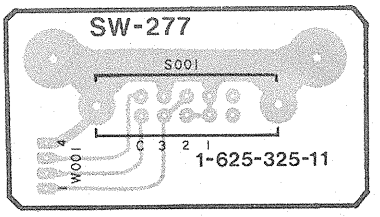


SW-198 – COMPONENT SIDE –

1-622-753-11, 12
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)

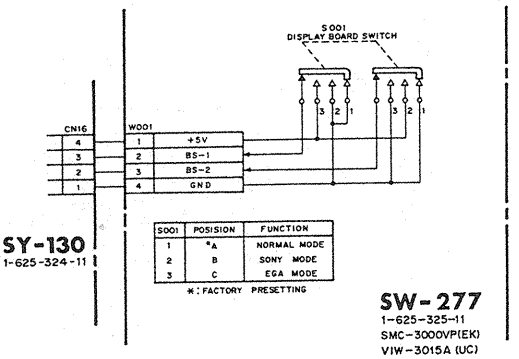


5-12. SW-277 BOARD



SW-277 – SOLDERING SIDE –

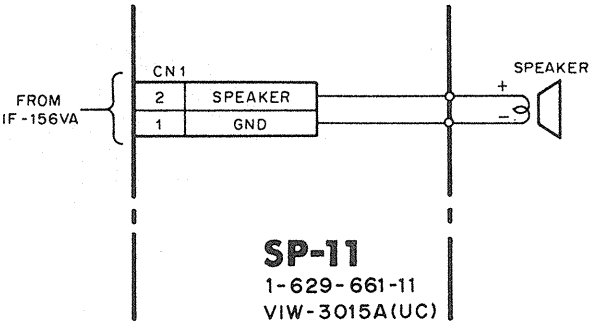
1-625-325-11
SMC-3000VP(EK)
VIW-3015A(UC)



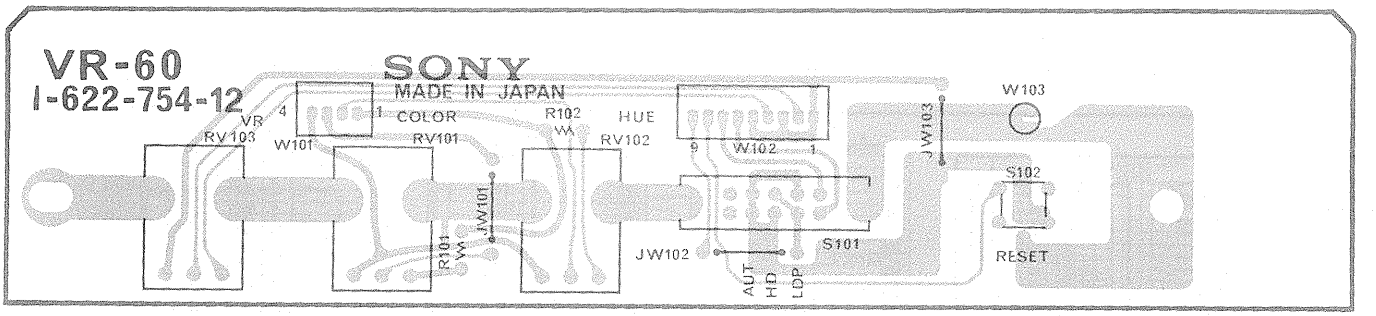
5-13. SP-11 BOARD

SP-11 – COMPONENT SIDE –

1-629-661-11
VIW-3015A(UC)

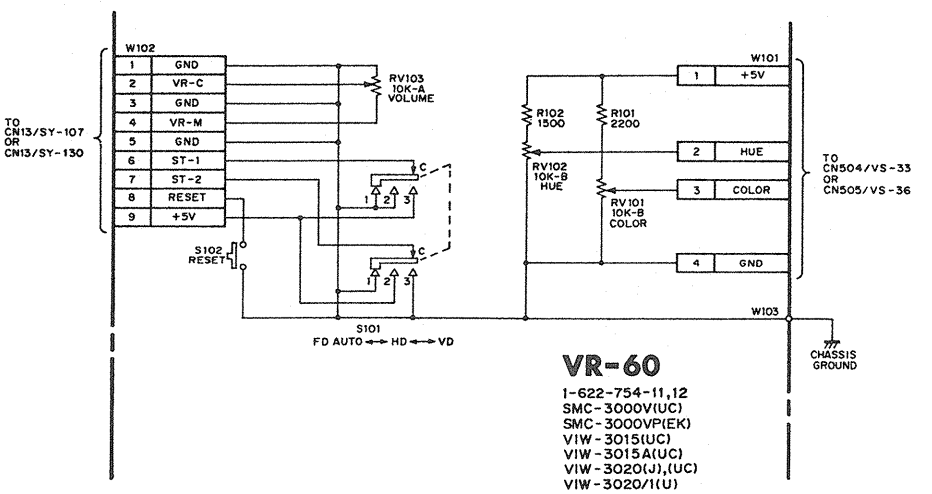


5-14. VR-60 BOARD



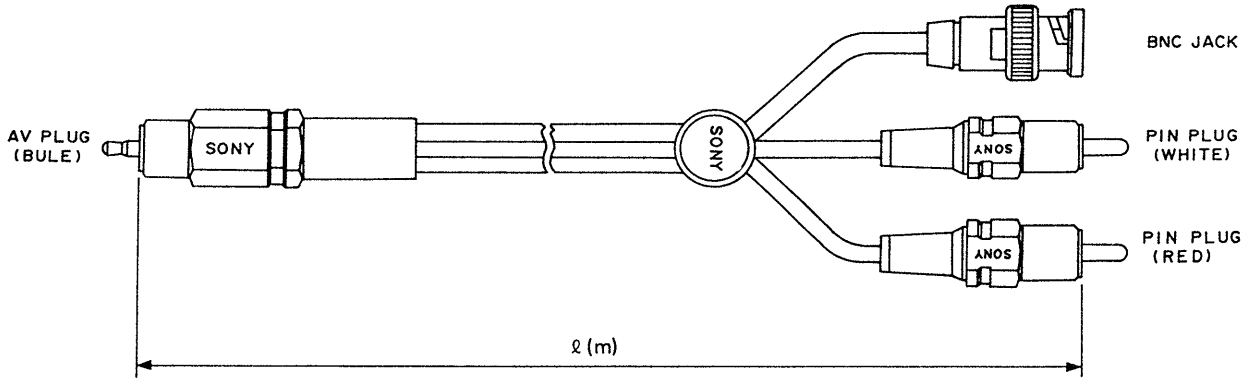
VR-60 – COMPONENT SIDE –

1-622-754-12
SMC-3000V(UC)
SMC-3000VP(EK)
VIW-3015(UC)
VIW-3015A(UC)
VIW-3020(J), (UC)
VIW-3020/1(U)

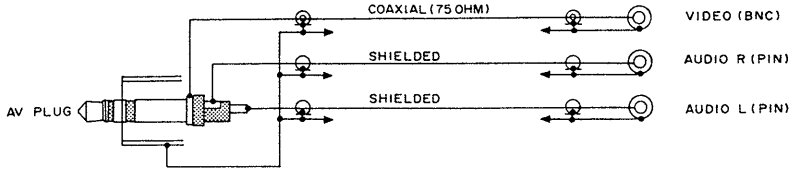


5-15. AV CABLE

OUTSIDE VIEW

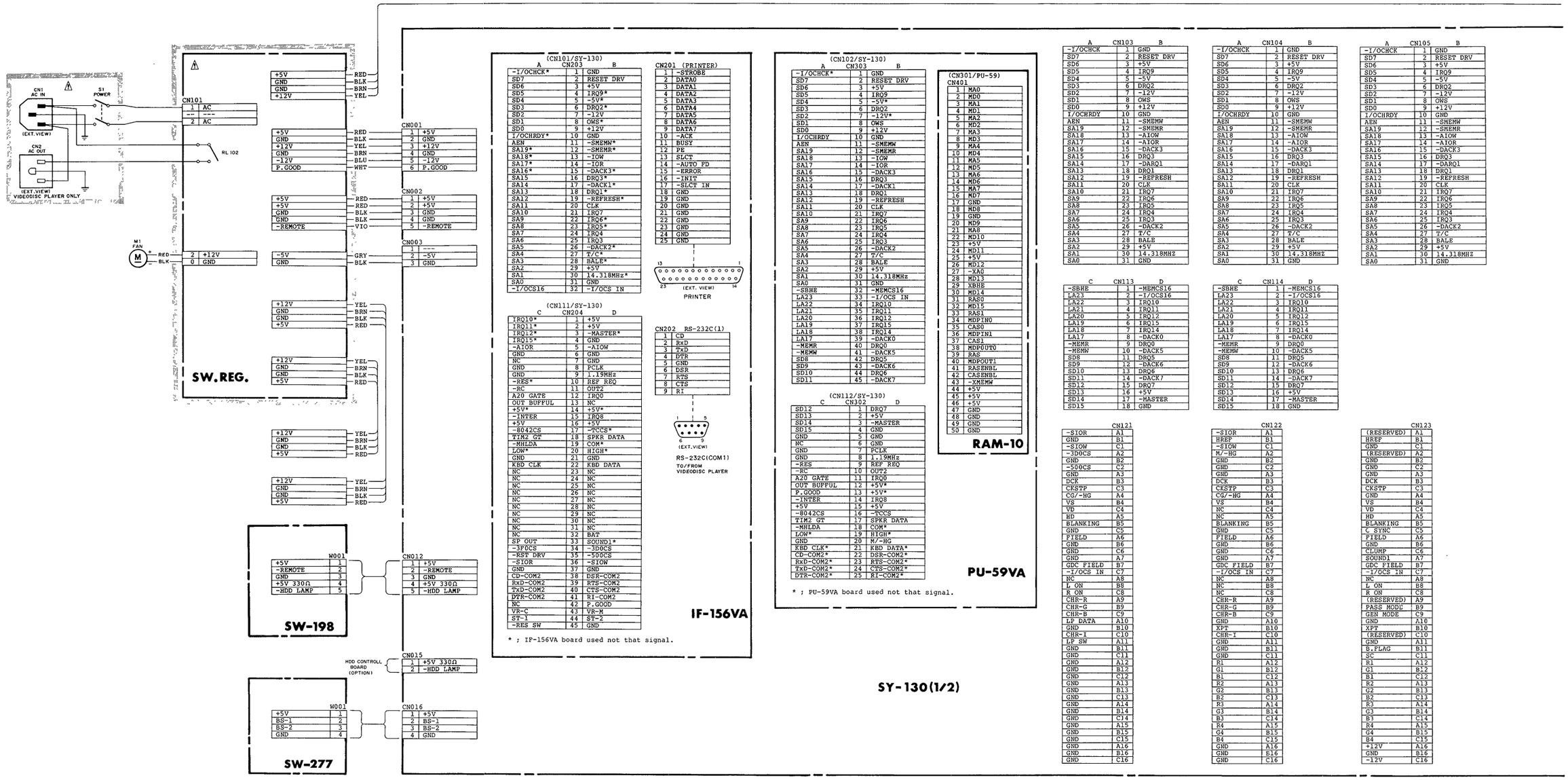


ℓ = 0.58(m) → AV CABLE-S (1-559-870-11)
ℓ = 1.08(m) → AV CABLE-L (1-559-871-11)



AV CABLE
SM I – 3080(E)
VIW – 3015A (UC)

5-16. COMPUTER FRAME



(CN101/SY-130)

A	CN203	B
-I/OCHCK*	1	GND
SD7	2	RESET DRV
SD6	3	+5V
SD5	4	IRQ9*
SD4	5	-5V*
SD3	6	DRQ2*
SD2	7	-12V
SD1	8	OWS*
SD0	9	+12V
I/OCHRDY*	10	GND
AEN	11	-SMEMW*
SA19*	12	-SMEMR*
SA18*	13	-IOW
SA17*	14	-IOR
SA16*	15	-DACK3*
SA15	16	DRQ3*
SA14	17	-DACK1*
SA13	18	DRQ1*
SA12	19	-REFRESH*
SA11	20	CLK
SA10	21	IRQ7
SA9	22	IRQ6*
SA8	23	IRQ5*
SA7	24	IRQ4
SA6	25	IRQ3
SA5	26	-DACK2*
SA4	27	T/C*
SA3	28	BALE*
SA2	29	+5V
SA1	30	14.318MHz*
SA0	31	GND
-I/OCS16	32	-I/OCS IN

(CN111/SY-130)

C	CN204	D
IRQ10*	1	+5V
IRQ11*	2	+5V
IRQ12*	3	-MASTER*
IRQ15*	4	GND
-AIOR	5	-AIOW
GND	6	GND
NC	7	GND
GND	8	PCLK
GND	9	1.19MHz
-RES*	10	REF REQ
-RC	11	OUT2
A20 GATE	12	IRQ0
OUT BUFFUL	13	NC
+5V*	14	+5V*
-INTER	15	IRQ8
+5V	16	+5V
-8042CS	17	-PCCS*
TIM2 GT	18	SPKR DATA
-MHLDA	19	COM*
LOW*	20	HIGH*
GND	21	GND
KBD CLK	22	KBD DATA
NC	23	NC
NC	24	NC
NC	25	NC
NC	26	NC
NC	27	NC
NC	28	NC
NC	29	NC
NC	30	NC
NC	31	NC
NC	32	BAT
SP OUT	33	SOUND1*
-3F0CS	34	-3D0CS
-RST DRV	35	-500CS
-SIOR	36	-SIOW
GND	37	GND
CD-COM2	38	DSR-COM2
RxD-COM2	39	RTS-COM2
TxD-COM2	40	CTS-COM2
DTR-COM2	41	RI-COM2
NC	42	P.GOOD
VR-C	43	VR-M
ST-1	44	ST-2
-RES SW	45	GND

* ; IP-156VA board used not that signal.

IF-156VA

CN201 (PRINTER)

1	-STROBE	
2	DATA0	
3	DATA1	
4	DATA2	
5	DATA3	
6	DATA4	
7	DATA5	
8	DATA6	
9	DATA7	
10	-ACK	
11	BUSY	
12	PE	
13	SLCT	
14	-AUTO FD	
15	-ERROR	
16	-INIT	
17	-SLCT IN	
18	GND	
19	GND	
20	GND	
21	GND	
22	GND	
23	GND	
24	GND	
25	GND	

CN202 RS-232C(1)

1	CD
2	RxD
3	TxD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

(CN102/SY-130)

A	CN303	B
-I/OCHCK*	1	GND
SD7	2	RESET DRV
SD6	3	+5V
SD5	4	IRQ9
SD4	5	-5V*
SD3	6	DRQ2
SD2	7	-12V*
SD1	8	OWS
SD0	9	+12V
I/OCHRDY	10	GND
AEN	11	-SMEMW
SA19	12	-SMEMR
SA18	13	-IOW
SA17	14	-IOR
SA16	15	-DACK3
SA15	16	DRQ3
SA14	17	-DACK1
SA13	18	DRQ1
SA12	19	-REFRESH
SA11	20	CLK
SA10	21	IRQ7
SA9	22	IRQ6
SA8	23	IRQ5
SA7	24	IRQ4
SA6	25	IRQ3
SA5	26	-DACK2
SA4	27	T/C
SA3	28	BALE
SA2	29	+5V
SA1	30	14.318MHz
SA0	31	GND
-SBHE	32	-MEMCS16
LA23	33	-I/OCS IN
LA22	34	IRQ10
LA21	35	IRQ11
LA20	36	IRQ12
LA19	37	IRQ15
LA18	38	IRQ14
LA17	39	-DACK0
-MEMR	40	DRQ0
-MEMW	41	-DACK5
SD8	42	DRQ5
SD9	43	-DACK6
SD10	44	DRQ6
SD11	45	-DACK7

(CN112/SY-130)

C	CN302	D
SD12	1	DRQ7
SD13	2	+5V
SD14	3	-MASTER
SD15	4	GND
GND	5	GND
NC	6	GND
GND	7	PCLK
GND	8	1.19MHz
-RES	9	REF REQ
-RC	10	OUT2
A20 GATE	11	IRQ0
OUT BUFFUL	12	+5V*
P.GOOD	13	+5V*
-INTER	14	IRQ8
+5V	15	+5V
-8042CS	16	-PCCS
TIM2 GT	17	SPKR DATA
-MHLDA	18	COM*
LOW*	19	HIGH*
GND	20	M/-HG
KBD CLK*	21	KBD DATA*
CD-COM2*	22	DSR-COM2*
RxD-COM2*	23	RTS-COM2*
TxD-COM2*	24	CTS-COM2*
DTR-COM2*	25	RI-COM2*

* ; PU-59VA board used not that signal.

PU-59VA

(CN301/PU-59)
CN401

1	MA0	
2	MD0	
3	MA1	
4	MD1	
5	MA2	
6	MD2	
7	MA3	
8	MD3	
9	MA4	
10	MD4	
11	MA5	
12	MD5	
13	MA6	
14	MD6	
15	MA7	
16	MD7	
17	GND	
18	MD8	
19	GND	
20	MD9	
21	MA8	
22	MD10	
23	+5V	
24	MD11	
25	+5V	
26	MD12	
27	-XA0	
28	MD13	
29	XBHE	
30	MD14	
31	RAS0	
32	MD15	
33	RAS1	
34	MDPIN0	
35	CAS0	
36	MDPIN1	
37	CAS1	
38	MDPOUT0	
39	RAS	
40	MDPOUT1	
41	RASENBL	
42	CASENBL	
43	-XMEMW	
44	+5V	
45	+5V	
46	+5V	
47	GND	
48	GND	
49	GND	
50	GND	

RAM-10

SY-130(1/2)

CN103

A		B
-I/OCHCK	1	GND
SD7	2	RESET DRV
SD6	3	+5V
SD5	4	IRQ9
SD4	5	-5V
SD3	6	DRQ2
SD2	7	-12V
SD1	8	OWS
SD0	9	+12V
I/OCHRDY	10	GND
AEN	11	-SMEMW
SA19	12	-SMEMR
SA18	13	-AIOW
SA17	14	-AIOR
SA16	15	-DACK3
SA15	16	DRQ3
SA14	17	-DARQ1
SA13	18	DRQ1
SA12	19	-REFRESH
SA11	20	CLK
SA10	21	IRQ7
SA9	22	IRQ6
SA8	23	IRQ5
SA7	24	IRQ4
SA6	25	IRQ3
SA5	26	-DACK2
SA4	27	T/C
SA3	28	BALE
SA2	29	+5V
SA1	30	14.318MHZ
SA0	31	GND

CN104

A		B
-I/OCHCK	1	GND
SD7	2	RESET DRV
SD6	3	+5V
SD5	4	IRQ9
SD4	5	-5V
SD3	6	DRQ2
SD2	7	-12V
SD1	8	OWS
SD0	9	+12V
I/OCHRDY	10	GND
AEN	11	-SMEMW
SA19	12	-SMEMR
SA18	13	-AIOW
SA17	14	-AIOR
SA16	15	-DACK3
SA15	16	DRQ3
SA14	17	-DARQ1
SA13	18	DRQ1
SA12	19	-REFRESH
SA11	20	CLK
SA10	21	IRQ7
SA9	22	IRQ6
SA8	23	IRQ5
SA7	24	IRQ4
SA6	25	IRQ3
SA5	26	-DACK2
SA4	27	T/C
SA3	28	BALE
SA2	29	+5V
SA1	30	14.318MHZ
SA0	31	GND

CN105

A		B
-I/OCHCK	1	GND
SD7	2	RESET DRV
SD6	3	+5V
SD5	4	IRQ9
SD4	5	-5V
SD3	6	DRQ2
SD2	7	-12V
SD1	8	OWS
SD0	9	+12V
I/OCHRDY	10	GND
AEN	11	-SMEMW
SA19	12	-SMEMR
SA18	13	-AIOW
SA17	14	-AIOR
SA16	15	-DACK3
SA15	16	DRQ3
SA14	17	-DARQ1
SA13	18	DRQ1
SA12	19	-REFRESH
SA11	20	CLK
SA10	21	IRQ7
SA9	22	IRQ6
SA8	23	IRQ5
SA7	24	IRQ4
SA6	25	IRQ3
SA5	26	-DACK2
SA4	27	T/C
SA3	28	BALE
SA2	29	+5V
SA1	30	14.318MHZ
SA0	31	GND

CN113

C		D
-SBHE	1	-MEMCS16
LA23	2	-I/OCS16
LA22	3	IRQ10
LA21	4	IRQ11
LA20	5	IRQ12
LA19	6	IRQ15
LA18	7	IRQ14
LA17	8	-DACK0
-MEMR	9	DRQ0
-MEMW	10	-DACK5
SD8	11	DRQ5
SD9	12	-DACK6
SD10	13	DRQ6
SD11	14	-DACK7
SD12	15	DRQ7
SD13	16	+5V
SD14	17	-MASTER
SD15	18	GND

CN114

C		D
-SBHE	1	-MEMCS16
LA23	2	-I/OCS16
LA22	3	IRQ10
LA21	4	IRQ11
LA20	5	IRQ12
LA19	6	IRQ15
LA18	7	IRQ14
LA17	8	-DACK0
-MEMR	9	DRQ0
-MEMW	10	-DACK5
SD8	11	DRQ5
SD9	12	-DACK6
SD10	13	DRQ6
SD11	14	-DACK7
SD12	15	DRQ7
SD13	16	+5V
SD14	17	-MASTER
SD15	18	GND

CN121

-SIOR	A1
GND	B1
-SIOW	C1
-3D0CS	A2
GND	B2
-500CS	C2
GND	A3
DCK	B3
CKSTP	C3
CG/-HG	A4
VS	B4
VD	C4
HD	A5
BLANKING	B5
GND	C5
FIELD	A6
GND	B6
GND	C6
GND	A7
GDC FIELD	B7
-I/OCS IN	C7
NC	A8
L ON	B8
R ON	C8
CHR-R	A9
CHR-G	B9
CHR-B	C9
LP DATA	A10
GND	B10
CHR-I	C10
LP SW	A11
GND	B11
GND	C11
GND	A12
GND	B12
GND	C12
GND	A13
GND	B13
GND	C13
GND	A14
GND	B14
GND	C14
GND	A15
GND	B15
GND	C15
GND	A16
GND	B16
GND	C16

CN122

-SIOR	A1
HREF	B1
-SIOW	C1
M/-HG	A2
GND	B2
GND	C2
GND	A3
DCK	B3
CKSTP	C3
CG/-HG	A4
VS	B4
NC	C4
NC	A5
BLANKING	B5
GND	C5
FIELD	A6
GND	B6
GND	C6
GND	A7
GDC FIELD	B7
-I/OCS IN	C7
NC	A8
NC	B8
NC	C8
CHR-R	A9
CHR-G	B9
CHR-B	C9
GND	A10
XPT	B10
CHR-I	C10
GND	A11
GND	B11
GND	C11
R1	A12
G1	B12
B1	C12
R2	A13
G2	B13
B2	C13
R3	A14
G3	B14
B3	C14
R4	A15
G4	B15
B4	C15
GND	A16
GND	B16
GND	C16

CN123

(RESERVED)	A1
HREF	B1
GND	C1
(RESERVED)	A2
GND	B2
GND	C2
GND	A3
DCK	B3
CKSTP	C3
GND	A4
VS	B4
VD	C4
HD	A5
BLANKING	B5
C SYNC	C5
FIELD	A6
GND	B6
CLUMP	C6
SOUND1	A7
GDC FIELD	B7
-I/OCS IN	C7
NC	A8
L ON	B8
R ON	C8
(RESERVED)	A9
PASE MODE	B9
GEN MODE	C9
GND	A10
XPT	B10
(RESERVED)	C10
GND	A11
B.FLAG	B11
SC	C11
R1	A12
G1	B12
B1	C12
R2	A13
G2	B13
B2	C13
R3	A14
G3	B14
B3	C14
R4	A15
G4	B15
B4	C15
+12V	A16
GND	B16
-12V	C16

A (CN106/SY-130) B

-I/OCHCK*	1	GND
SD7	2	RESET DRV
SD6	3	+5V
SD5	4	IRQ9*
SD4	5	-5V
SD3	6	DRQ2*
SD2	7	-12V*
SD1	8	OWS*
SD0	9	+12V
I/OCHRDY*	10	GND
AEN	11	-SMEMW*
SA19*	12	-SMEMR*
SA18*	13	-AIOW
SA17*	14	-AIOR
SA16*	15	-DACK3*
SA15*	16	DRQ3*
SA14*	17	-DACK1*
SA13*	18	DRQ1*
SA12*	19	-REFRESH*
SA11*	20	CLK*
SA10*	21	IRQ7*
SA9	22	IRQ6*
SA8	23	IRQ5*
SA7	24	IRQ4*
SA6	25	IRQ3*
SA5	26	-DACK2*
SA4	27	T/C*
SA3	28	BALE*
SA2	29	+5V
SA1	30	14.318MHz*
SA0	31	GND

C (CN116/SY-130) D

-SBHE*	1	-MEMCS16*
LA23*	2	-I/OCS16*
LA22*	3	IRQ10*
LA21*	4	IRQ11*
LA20*	5	IRQ12*
LA19*	6	IRQ15*
LA18*	7	IRQ14*
LA17*	8	-DACK0*
-MEMR*	9	DRQ0*
-MEMW*	10	-DACK5*
SD8*	11	DRQ5*
SD9*	12	-DRCK6*
SD10*	13	DRQ6*
SD11*	14	-DACK7*
SD12*	15	DRQ7*
SD13*	16	+5V*
SD14*	17	-MASTER*
SD15*	18	GND*

ANALOG RGB OUT CN001

R	1
G	2
B	3
NC	4
GND	5
R RTN	6
G RTN	7
B RTN	8
AUDIO GND	9
GND	10
NC	11
NC	12
H SYNC	13
V SYNC	14
NC	15

15 (EXT. VIEW) 9

ANALOG RGB OUT

CN002

GND	1	
PD0	2	
GND	3	
PD1	4	
GND	5	
PD2	6	
EFPIX*	7	
PD3	8	
EFSYNC*	9	
PD4	10	
EFCLK	11	
PD5	12	
NC	13	
PD6	14	
GND	15	
PD7	16	
GND	17	
DCLK	18	
GND	19	
BLNK	20	
GND	21	
H OUT	22	
NC	23	
V OUT	24	
NC	25	
GND	26	

AV INPUT CN003

VIDEO IN	V
AUDIO L IN	L
AUDIO R IN	R
GND	G

AV IN (L, V, R, G)

AV OUTPUT CN004

VIDEO OUT	V
AUDIO L OUT	L
AUDIO R OUT	R
GND	G

AV OUT (L, V, R, G)

*; VS-38A board used not that signal.

VS-38A

PA PB
(A CN107/SY-130 B)

-I/OCHCK*	1	GND
SD7	2	RESET DRV
SD6	3	+5V
SD5	4	IRQ9*
SD4	5	-5V*
SD3	6	DRQ2*
SD2	7	-12V
SD1	8	OWS*
SD0	9	+12V*
I/OCHRDY	10	GND
AEN	11	-SMEMW
SA19	12	-SMEMR
SA18	13	-AIOW
SA17	14	-AIOR
SA16	15	-DACK3*
SA15	16	DRQ3*
SA14	17	-DACK1*
SA13	18	DRQ1*
SA12	19	-REFRESH
SA11	20	CLK*
SA10	21	IRQ7*
SA9	22	IRQ6*
SA8	23	IRQ5*
SA7	24	IRQ4*
SA6	25	IRQ3*
SA5	26	-DACK2*
SA4	27	T/C*
SA3	28	BALE*
SA2	29	+5V
SA1	30	14.318MHz
SA0	31	GND

PC PD
(C CN117/SY-130 D)

-SBHE	1	-MEMCS16
LA23*	2	-I/OCS16*
LA22*	3	IRQ10*
LA21*	4	IRQ11*
LA20*	5	IRQ12*
LA19	6	IRQ15*
LA18	7	IRQ14*
LA17	8	-DACK0*
-MEMR	9	DRQ0*
-MEMW*	10	-DACK5*
SD8	11	DRQ5*
SD9	12	-DRCK6*
SD10	13	DRQ6*
SD11	14	-DACK7*
SD12	15	DRQ7*
SD13	16	+5V
SD14	17	-MASTER*
SD15	18	GND

Z1	GROUND	
Y1	PD0	
Z2	GROUND	
Y2	PD1	
Z3	GROUND	
Y3	PD2	
Z4	SELECT INTERNAL VIDEO	
Y4	PD3	
Z5	SELECT INTERNAL VIDEO	
Y5	PD4	
Z6	SELECT INTERNAL DAC	
Y6	PD5	
Z7	NC	
Y7	PD6	
Z8	GROUND	
Y8	PD7	
Z9	GROUND	
Y9	DAC CLOCK	
Z10	GROUND	
Y10	DAC BLANKING	
Z11	GROUND	
Y11	EXT. HORIZONTAL SYNC	
Z12	NC	
Y12	EXT. VERTICAL SYNC	
Z13	NC	
Y13	GROUND	

ANALOG RGB OUT J1

RED VIDEO	1
GREEN VIDEO	2
BLUE VIDEO	3
MONITOR ID BIT 2*	4
GROUND	5
RED RETURN	6
GREEN RETURN	7
BLUE RETURN	8
KEY*	9
SYNC RETURN	10
MONITOR ID BIT 1*	11
MONITOR ID BIT 0*	12
HORIZONTAL SYNC	13
VERTICAL SYNC	14
NC	15

15 (EXT. VIEW) 9

ANALOG RGB OUT

THIS IS UNABLE TO USE.

*; VGA board used not that signal.

VGA-16

A CN108 B

-I/OCHCK	1	GND
SD7	2	RESET DRV
SD6	3	+5V
SD5	4	IRQ9
SD4	5	-5V
SD3	6	DRQ2
SD2	7	-12V
SD1	8	OWS
SD0	9	+12V
I/OCHRDY	10	GND
AEN	11	-SMEMW
SA19	12	-SMEMR
SA18	13	-AIOW
SA17	14	-AIOR
SA16	15	-DACK3
SA15	16	DRQ3
SA14	17	-DACK1
SA13	18	DRQ1
SA12	19	-REFRESH
SA11	20	CLK
SA10	21	IRQ7
SA9	22	IRQ6
SA8	23	IRQ5
SA7	24	IRQ4
SA6	25	IRQ3
SA5	26	-DACK2
SA4	27	T/C
SA3	28	BALE
SA2	29	+5V
SA1	30	14.318MHz
SA0	31	GND

C CN118 D

-SBHE	1	-MEMCS16
LA23	2	-I/OCS16
LA22	3	IRQ10
LA21	4	IRQ11
LA20	5	IRQ12
LA19	6	IRQ15
LA18	7	IRQ14
LA17	8	-DACK0
-MEMR	9	DRQ0
-MEMW	10	-DACK5
SD8	11	DRQ5
SD9	12	-DRCK6
SD10	13	DRQ6
SD11	14	-DACK7
SD12	15	DRQ7
SD13	16	+5V
SD14	17	-MASTER
SD15	18	GND

A CN109 B

-I/OCHCK	1	GND
SD7	2	RESET DRV
SD6	3	+5V
SD5	4	IRQ9
SD4	5	-5V
SD3	6	DRQ2
SD2	7	-12V
SD1	8	OWS
SD0	9	+12V
I/OCHRDY	10	GND
AEN	11	-SMEMW
SA19	12	-SMEMR
SA18	13	-AIOW
SA17	14	-AIOR
SA16	15	-DACK3
SA15	16	DRQ3
SA14	17	-DACK1
SA13	18	DRQ1
SA12	19	-REFRESH
SA11	20	CLK
SA10	21	IRQ7
SA9	22	IRQ6
SA8	23	IRQ5
SA7	24	IRQ4
SA6	25	IRQ3
SA5	26	-DACK2
SA4	27	T/C
SA3	28	BALE
SA2	29	+5V
SA1	30	14.318MHz
SA0	31	GND

SY-130 (2/2)

A CN110 B

-I/OCHCK	1	GND
SD7	2	RESET DRV
SD6	3	+5V
SD5	4	IRQ9
SD4	5	-5V
SD3	6	DRQ2
SD2	7	-12V
SD1	8	OWS
SD0	9	+12V
I/OCHRDY	10	GND
AEN	11	-SMEMW
SA19	12	-SMEMR
SA18	13	-AIOW
SA17	14	-AIOR
SA16	15	-DACK3
SA15	16	DRQ3
SA14	17	-DACK1
SA13	18	DRQ1
SA12	19	-REFRESH
SA11	20	CLK
SA10	21	IRQ7
SA9	22	IRQ6
SA8	23	IRQ5
SA7	24	IRQ4
SA6	25	IRQ3
SA5	26	-DACK2
SA4	27	T/C
SA3	28	BALE
SA2	29	+5V
SA1	30	14.318MHz
SA0	31	GND

C CN120 D

-SBHE	1	-MEMCS16
LA23	2	-I/OCS16
LA22	3	IRQ10
LA21	4	IRQ11
LA20	5	IRQ12
LA19	6	IRQ15
LA18	7	IRQ14
LA17	8	-DACK0
-MEMR	9	DRQ0
-MEMW	10	-DACK5
SD8	11	DRQ5
SD9	12	-DRCK6
SD10	13	DRQ6
SD11	14	-DACK7
SD12	15	DRQ7
SD13	16	+5V
SD14	17	-MASTER
SD15	18	GND

CN011

---	1
2HD/-2DD	2
GND	3
-INUSE	4
GND	5
---	6
GND	7
-INDEX	8
GND	9
-DRIVE SEL-A	10
GND	11
-DRIVE SEL-B	12
GND	13
---	14
GND	15
-MOTOR ON	16
GND	17
-DIR	18
GND	19
-STEP	20
GND	21
-WRITE DATA	22
GND	23
-WRITE GATE	24
GND	25
-TRACK0	26
GND	27
-WRITE PROT	28
GND	29
-READ DATA	30
GND	31
-HEAD SEL	32
GND	33
-DSK CHG	34

CN1

1	---
2	2HD/-2DD
3	GND
4	-INUSE
5	GND
6	---
7	GND
8	-INDEX
9	GND
10	-DRIVE SEL-A
11	GND
12	-DRIVE SEL-B
13	GND
14	---
15	GND
16	-MOTOR ON
17	GND
18	-DIR
19	GND
20	-STEP
21	GND
22	-WRITE DATA
23	GND
24	-WRITE GATE
25	GND
26	-TRACK0
27	GND
28	-WRITE PROT
29	GND
30	-READ DATA
31	GND
32	-HEAD SEL
33	GND
34	-DSK CHG

CN3

1	+5V
2	GND
3	GND
4	+12V

MFDD

MFDD (OPTION)

1	---
2	2HD/-2DD
3	GND
4	-INUSE
5	GND
6	---
7	GND
8	-INDEX
9	GND
10	-DRIVE SEL-A
11	GND
12	-DRIVE SEL-B
13	GND
14	---
15	GND
16	-MOTOR ON
17	GND
18	-DIR
19	GND
20	-STEP
21	GND
22	-WRITE DATA
23	GND
24	-WRITE GATE
25	GND
26	-TRACK0
27	GND
28	-WRITE PROT
29	GND
30	-READ DATA
31	GND
32	-HEAD SEL
33	GND
34	-DSK CHG

RGB SUPERIMPOSE BOARD (OPTION)

W101

1	GND
2	COLOR
3	HUE
4	+5V

W102

1	GND
2	VR-C
3	GND
4	VR-M
5	GND
6	ST-1
7	ST-2
8	RESET
9	+5V

CN013

GND	1
VR-C	2
GND	3
VR-M	4
GND	5
ST-1	6
ST-2	7
RESET	8
+5V	9

VR-60

CN203 RS-232C(2)

1	CD
2	RxD
3	TxD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

(EXT.VIEW)

RS-232C(COM2)

W203

CD	9
DSR	8
RD	7
RTS	6
TD	5
CTS	4
DTR	3
RI	2
GND	1

CP-116

W201

15	GND
14	KBD CLK
13	KBD DATA
12	LP DATA
11	LP SW
10	GND
9	CD
8	DSR
7	RxD
6	RTS
5	TxD
4	CTS
3	DTR
2	RI
1	+5V

CN017

GND	1
KBD CLK	2
KBD DATA	3
LP DATA	4
LP SW	5
GND	6
CD-COM2	7
DSR-COM2	8
RxD-COM2	9
RTS-COM2	10
TxD-COM2	11
CTS-COM2	12
DTR-COM2	13
RI-COM2	14
+5V	15

KEYBOARD CN201

KB CLK	1
KB DATA	2
NC	3
GND	4
+5V	5

KEYBOARD (EXT. VIEW)

LIGHT PEN CN202

LP DATA	1
LP SW	2
+5V	3
NC	4
GND	5

LIGHT PEN (EXT. VIEW)

W202

CD	1
DSR	2
RD	3
RTS	4
TD	5
CTS	6
DTR	7
RI	8
GND	9

CP-110

FRAME
VIW-3015A(UC)

CHAPTER 6
TROUBLESHOOTING

6-1. OUTLINE

Causes can almost be limited by a trouble condition or its occurrence situation, and by self-diagnosis of the system ROM or diagnosis of the maintenance disk. Each boards checking, however, is needed because it is difficult to restrict causes within a board.

6-1-1. Procedure

＊1. Power supply checking
(SW Reg. power supply line)
↓
＊2. Board condition checking
↓
＊3. Abnormal board checking

＊1. Confirm whether the switching regulator or the power supply line supplying to the respective slots are normal or not. (Refer to section 6-2.)
＊2. Install defective board in the normal unit, and perform a operation checking.

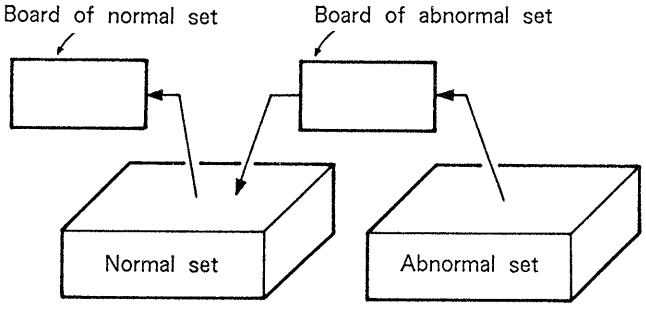


Fig. 6-1.

＊3. Check the corresponding sections following the section 6-3.

6-1-2. Attentions

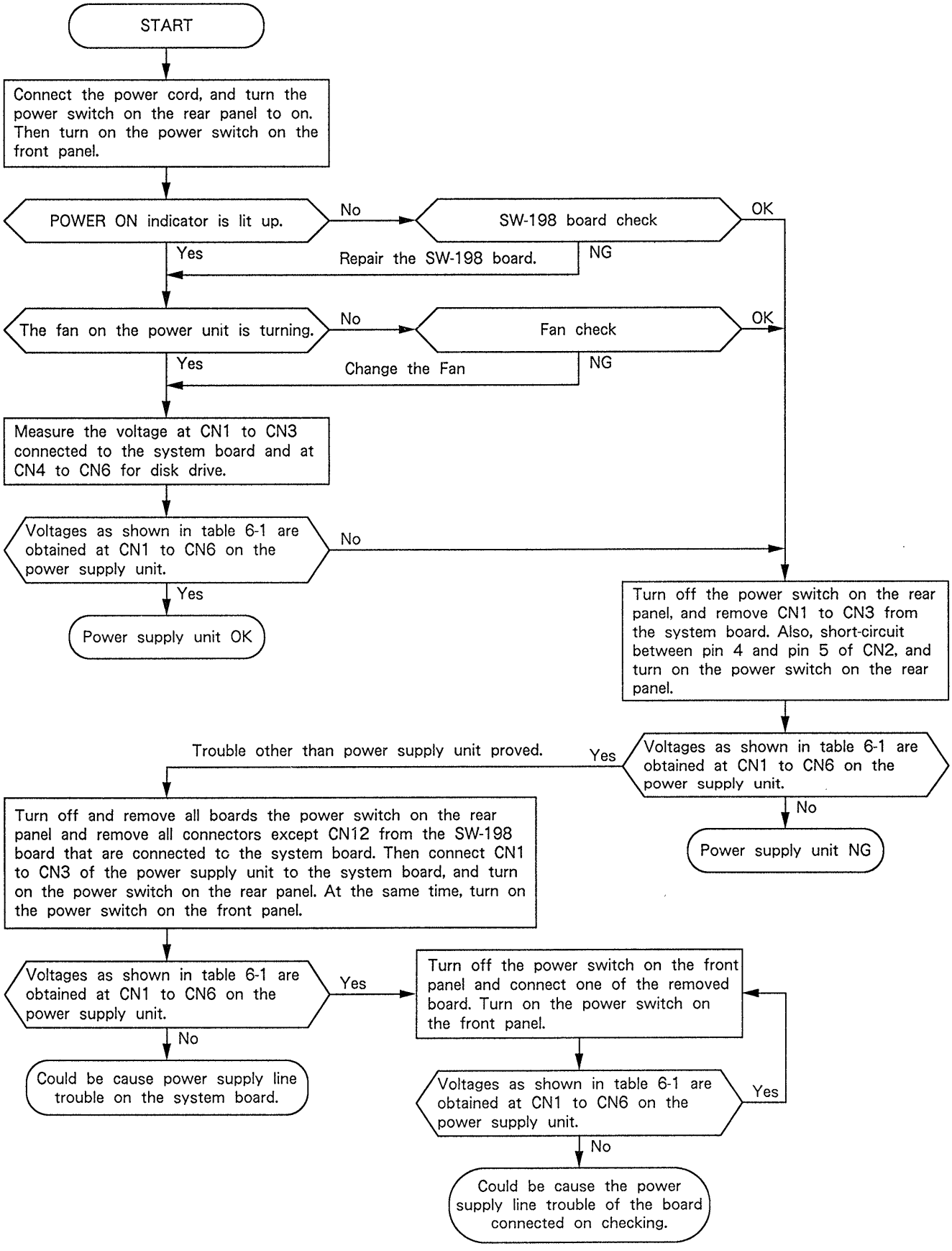
Be sure to check the following items previously ; servicing for maintenance or improvement has been done properly, setting of jumpers or switches has been done correctly, boards or mechanism parts are free from remarkable deformity or damage, pin of sockets or connectors is free from deformity or short-circuit, etc.
Also, as for usage or operation of each devices, refer to the data sheets (data book) or user's manuals released from respective manufacturers. When servicing, refer to circuit diagrams, block diagrams and circuit descriptions.

6-2. POWER SUPPLY UNIT

Check the power supply line around the switching regulator. When the unit does not work, the switching regulator or its feeding lines is considered to be troubled.
Perform the checking in 6-2 page.

Table 6-1

Connector Pin No.	Voltage (V)				
	CN1	CN2	CN3	CN4	CN5, 6
1	+5	+5	—	+5	+12
2	0	+5	−5	0	0
3	+12	0	0	0	0
4	0	0		+12	+5
5	−12	0			
6	+5				


START
Connect the power cord, and turn the power switch on the rear panel to on. Then turn on the power switch on the front panel.
POWER ON indicator is lit up.
No
SW-198 board check
OK
Yes
Repair the SW-198 board.
NG
The fan on the power unit is turning.
No
Fan check
OK
Yes
Change the Fan
NG
Measure the voltage at CN1 to CN3 connected to the system board and at CN4 to CN6 for disk drive.
Voltages as shown in table 6-1 are obtained at CN1 to CN6 on the power supply unit.
No
Yes
Power supply unit OK
Turn off the power switch on the rear panel, and remove CN1 to CN3 from the system board. Also, short-circuit between pin 4 and pin 5 of CN2, and turn on the power switch on the rear panel.
Voltages as shown in table 6-1 are obtained at CN1 to CN6 on the power supply unit.
Yes
Trouble other than power supply unit proved.
No
Power supply unit NG
Turn off and remove all boards the power switch on the rear panel and remove all connectors except CN12 from the SW-198 board that are connected to the system board. Then connect CN1 to CN3 of the power supply unit to the system board, and turn on the power switch on the rear panel. At the same time, turn on the power switch on the front panel.
Voltages as shown in table 6-1 are obtained at CN1 to CN6 on the power supply unit.
Yes
No
Could be cause power supply line trouble on the system board.
Turn off the power switch on the front panel and connect one of the removed board. Turn on the power switch on the front panel.
Voltages as shown in table 6-1 are obtained at CN1 to CN6 on the power supply unit.
Yes
No
Could be cause the power supply line trouble of the board connected on checking.

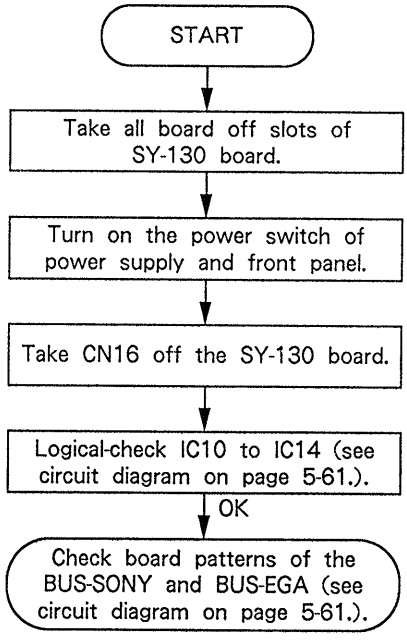
6-3. SY-107V/130 BOARD (SYSTEM BOARD)

6-3-1. Previous Confirmation

Confirm that pins on A and B sides of CN104 to CN110 or pins on C and D sides of CN114 to CN120 are not contacted each other (There are connectors not mounted.). Also, confirm that each jumpers are connected correctly. (Refer to circuit diagrams.)

6-3-2. Display Board Select Circuit

Display system is abnormal caused by the SY-130 board.
Point : IC10 to IC14 are considered to be troubled.
Flow : The following flow.



6-3-3. Floppydisk Control Circuit

6-3-3-1. Representative Trouble

1) When the message of the self-diagnosis error 31H is displayed ;
   Point : When IC4 is reset and no response is obtained, this message is displayed.
   When the self-diagnosis errors 32H and 33H are displayed, IC1 to IC5 are considered to be troubled. And only the message of 31H is displayed, IC4 may be troubled.
   Flow : Section 6-3-3-4.

2) When the message of the self-diagnosis error 32H or 33H is displayed ;
   Point : When both 32H and 33H are displayed, IC3, IC4 and IC6 to IC8 are considered to be troubled . Being displayed either the messages, FDD is to be troubled.
   Flow : Section 6-3-3-3.

3) When the system disk will not start, and the message "Insert the system disk, and press the F1 key" is displayed ;
   Point : The system disk or FDD is considered to be troubled. Also IC3 to IC9 are to be troubled.
   Flow : Section 6-3-3-5.

4) When the system disk will not start, and the message "A sector cannot be found" is displayed ;
   Point : The system disk or FDD is considered to be troubled.
   Flow : Section 6-3-3-6.

5) The write protection error is occurred without the write protection ;
   Point : FDD or the write protection signal system (IC8→IC3→IC4) is considered to be troubled.
   Flow : Section 6-3-3-7.

6) The system board is caused an error, so even the self-diagnosis does not carry out ;
   Point : IC1 and IC2 or IC9 are considered to be troubled.
   Flow : Section 6-3-3-8.

6-3-3-2. Individual Check

On this section, basic operation checkings are performed for each ICs, IC1 to IC5 and IC8, on the system board. IC3 to IC5, however, are checked partially.

1. Prepare normal power supply unit and oscilloscope.
2. Connect CN1 and CN2 of the power supply unit to the system board.
3. Turn on the power switch on the power supply unit.
4. Short-circuit between pins 2 and 3 of CN12 on the system board (see Fig. 6-2.).
5. Check each ICs according to the flowcharts in following pages.

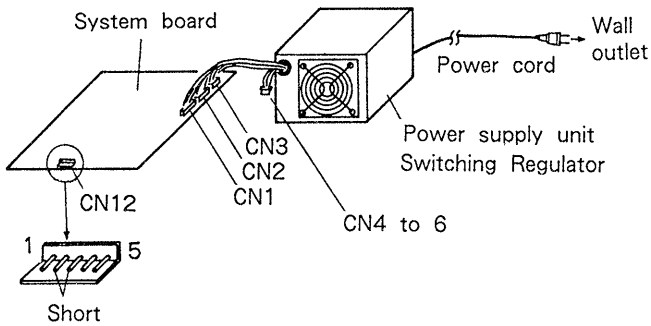
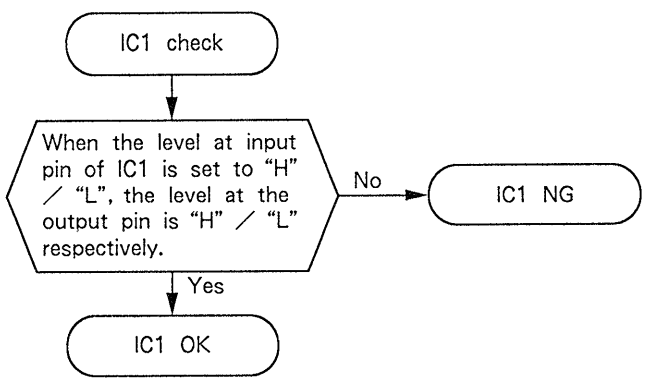
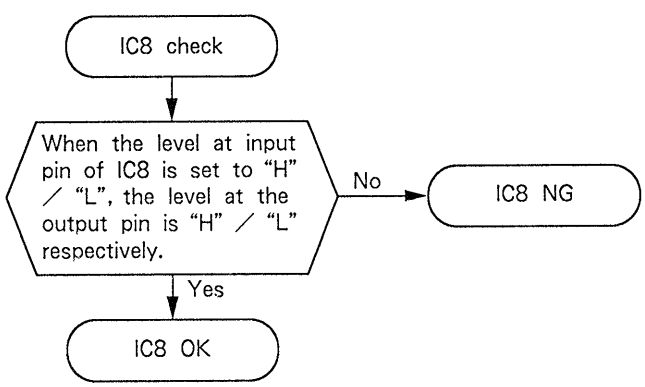
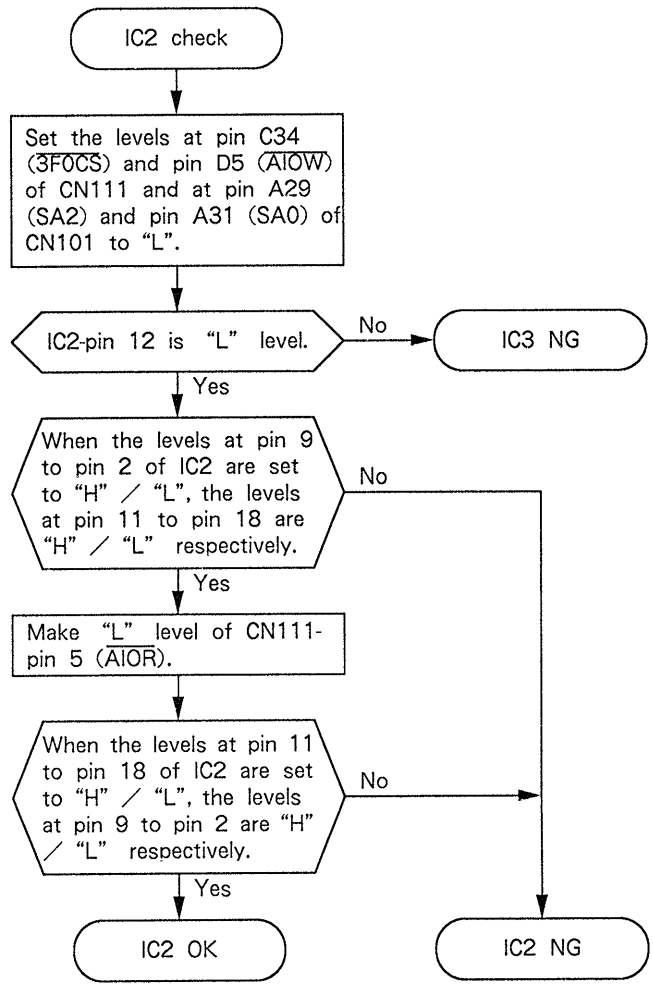
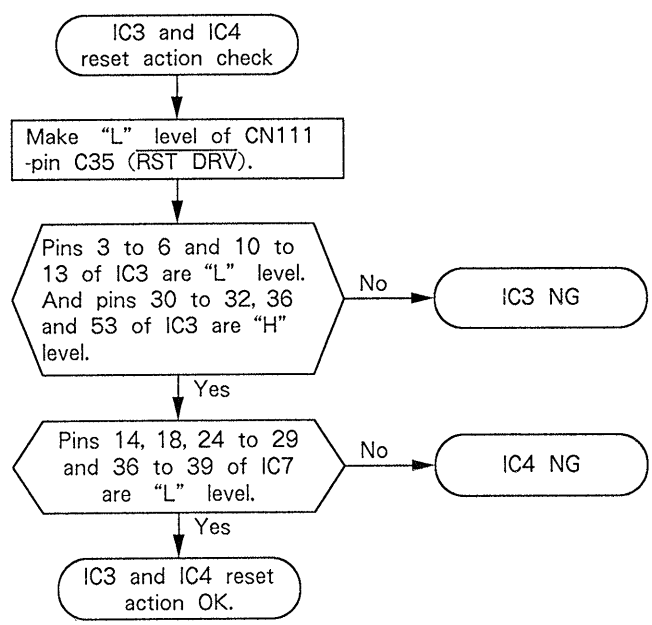


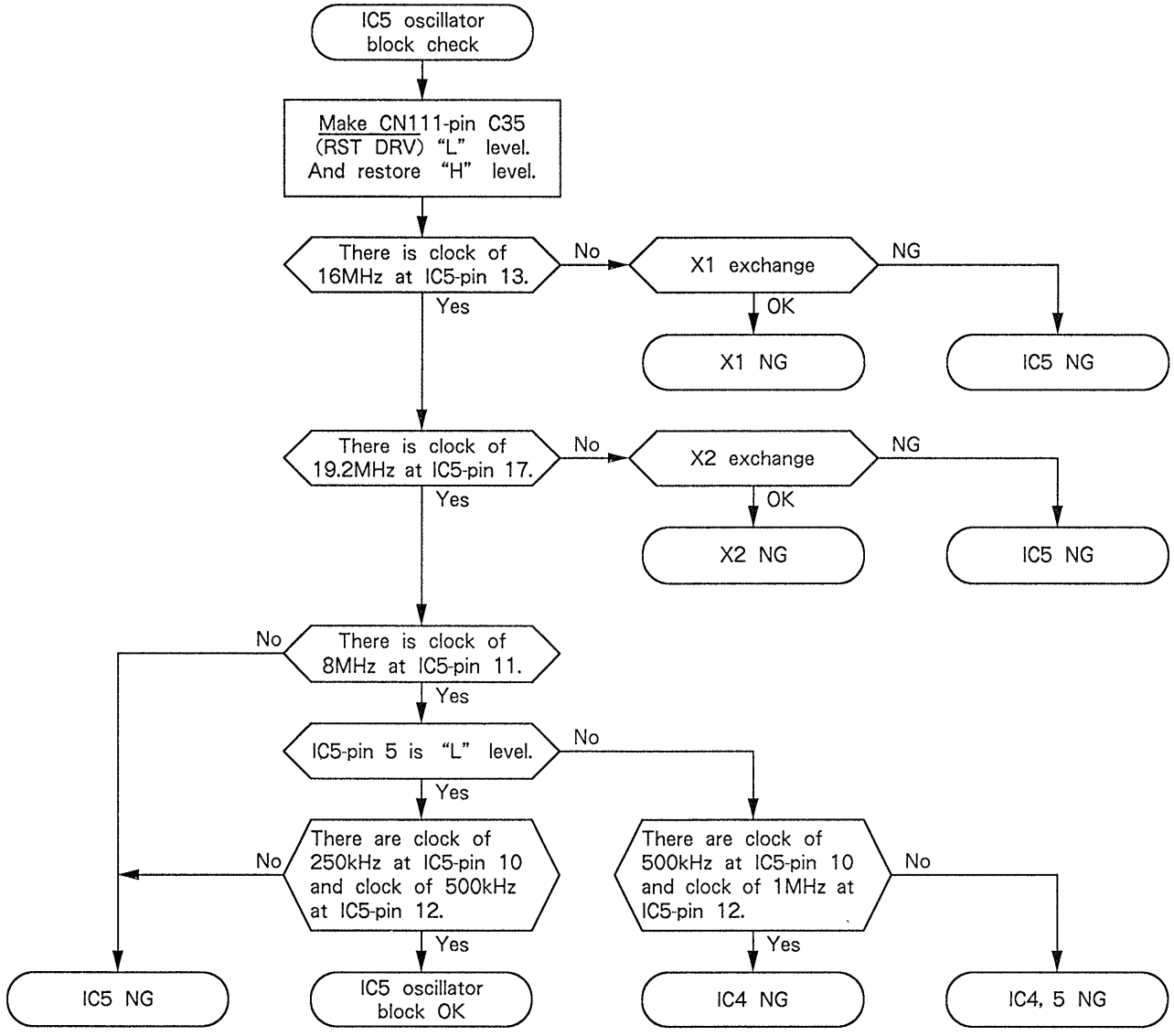
Fig. 6-2.





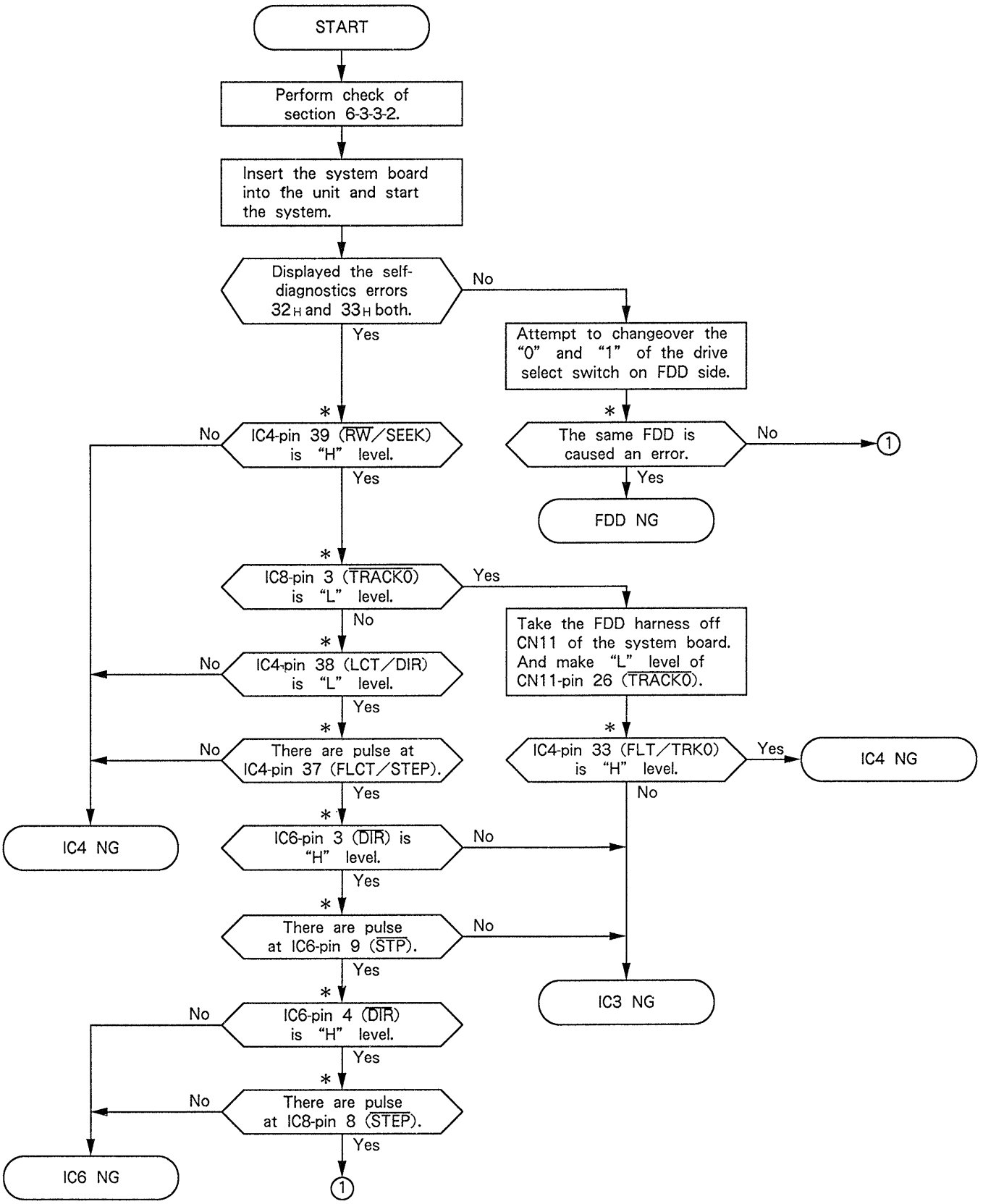


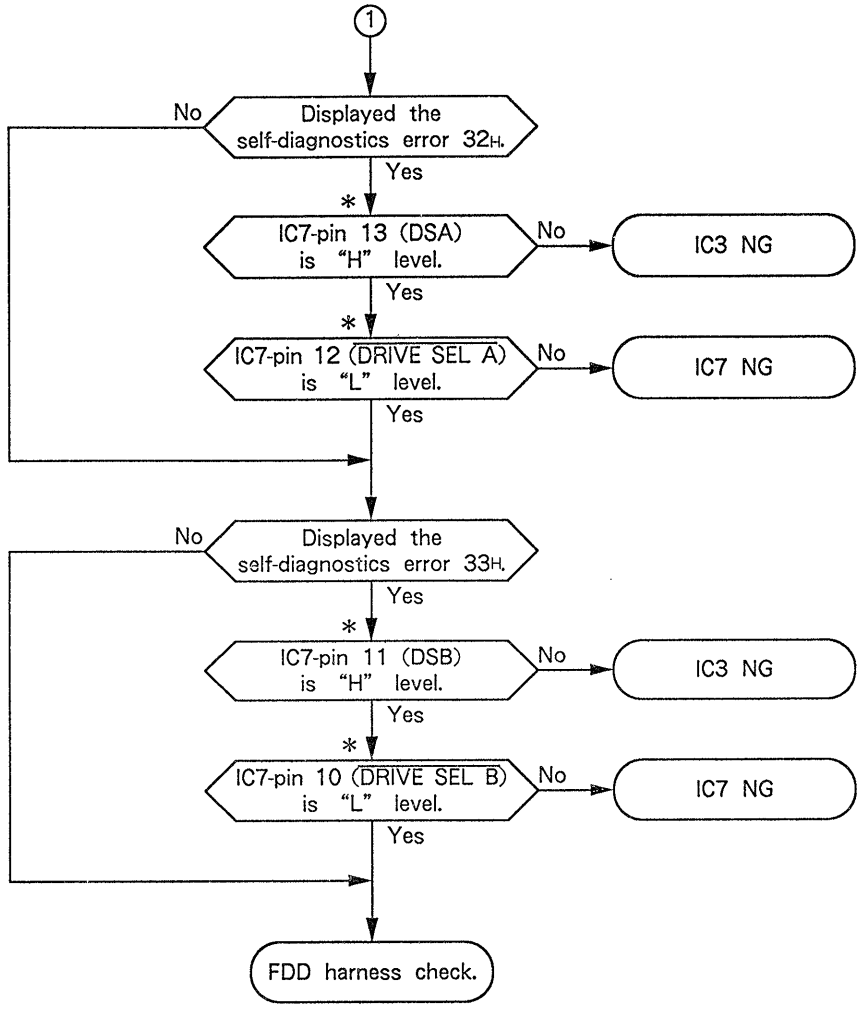



IC5 oscillator block check
Make CN111-pin C35 (RST DRV) "L" level. And restore "H" level.
There is clock of 16MHz at IC5-pin 13.
No
X1 exchange
NG
OK
X1 NG
IC5 NG
Yes
There is clock of 19.2MHz at IC5-pin 17.
No
X2 exchange
NG
OK
X2 NG
IC5 NG
Yes
No
There is clock of 8MHz at IC5-pin 11.
Yes
IC5-pin 5 is "L" level.
No
Yes
There are clock of 250kHz at IC5-pin 10 and clock of 500kHz at IC5-pin 12.
No
There are clock of 500kHz at IC5-pin 10 and clock of 1MHz at IC5-pin 12.
No
Yes
Yes
IC5 NG
IC5 oscillator block OK
IC4 NG
IC4, 5 NG

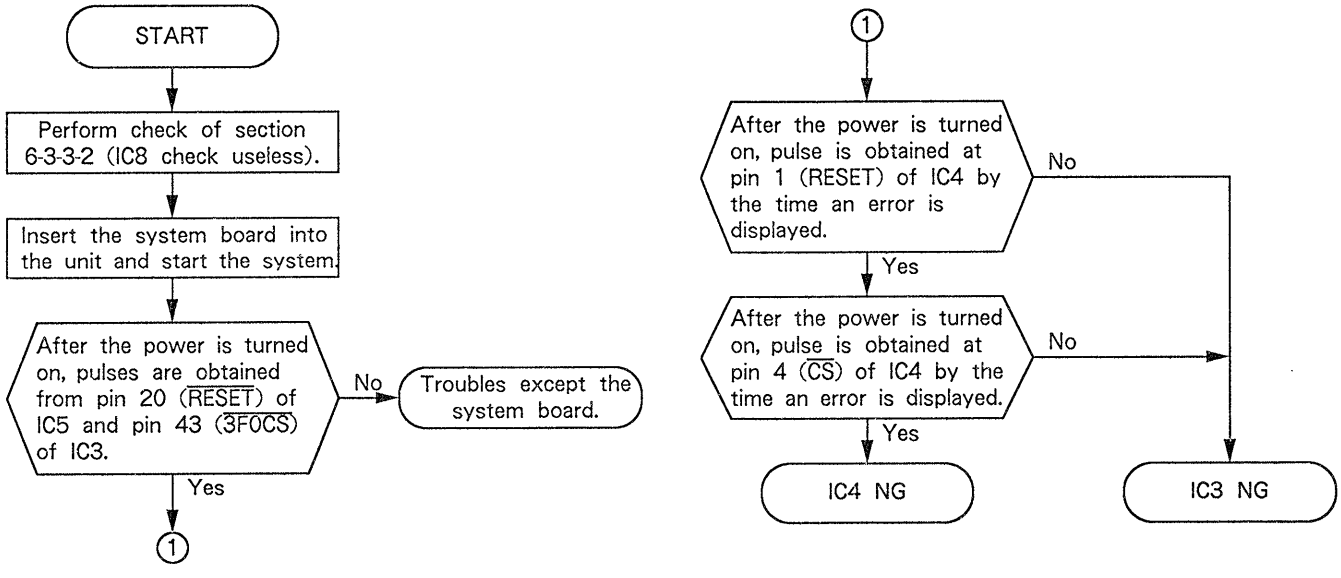
6-3-3-3. Check 1

An asterisk (*) in the flowchart indicates that RESET is entered.



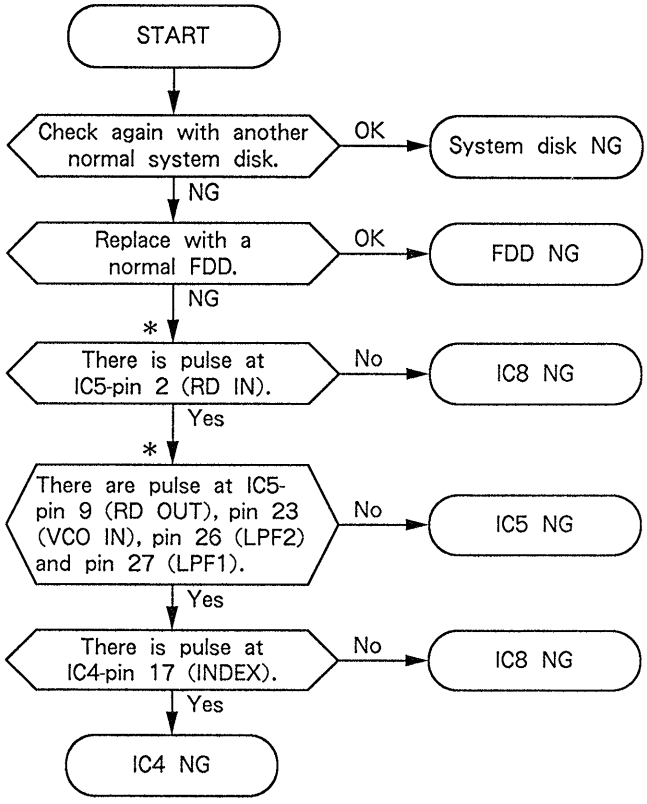

1
No
Displayed the self-diagnostics error 32H.
Yes
*
IC7-pin 13 (DSA) is "H" level.
No
IC3 NG
Yes
*
IC7-pin 12 (DRIVE SEL A) is "L" level.
No
IC7 NG
Yes
No
Displayed the self-diagnostics error 33H.
Yes
*
IC7-pin 11 (DSB) is "H" level.
No
IC3 NG
Yes
*
IC7-pin 10 (DRIVE SEL B) is "L" level.
No
IC7 NG
Yes
FDD harness check.

6-3-3-4. Check 2

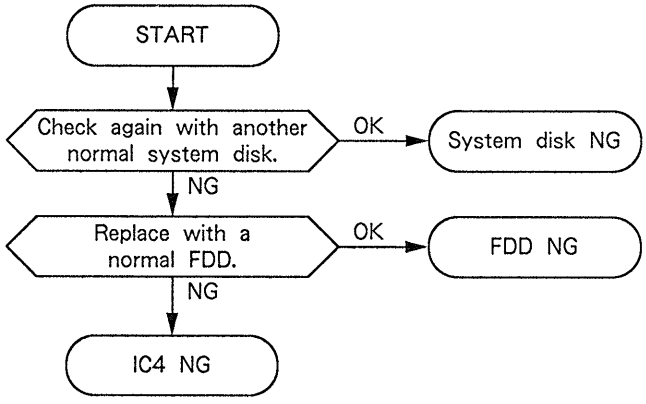

START
Perform check of section 6-3-3-2 (IC8 check useless).
Insert the system board into the unit and start the system.
After the power is turned on, pulses are obtained from pin 20 (RESET) of IC5 and pin 43 (3F0CS) of IC3.
No
Troubles except the system board.
Yes
1
1
After the power is turned on, pulse is obtained at pin 1 (RESET) of IC4 by the time an error is displayed.
No
Yes
After the power is turned on, pulse is obtained at pin 4 (CS) of IC4 by the time an error is displayed.
No
Yes
IC4 NG
IC3 NG

6-3-3-5. Check 3

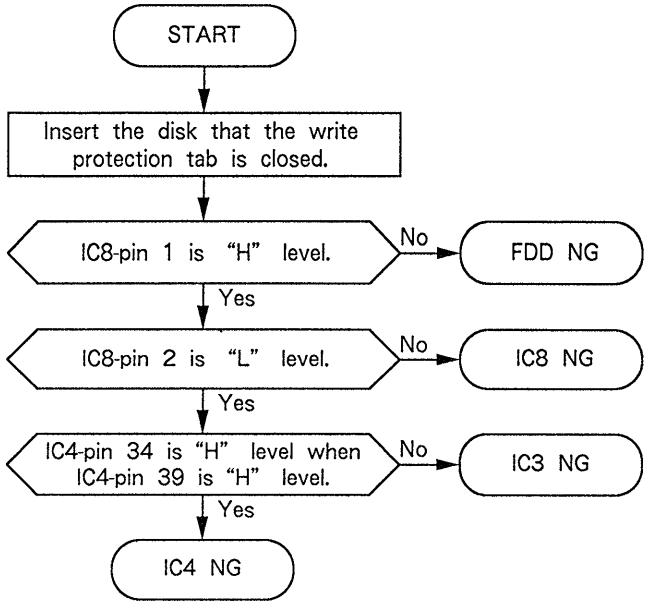
An asterisk (*) in the flowchart indicates that RESET is entered.



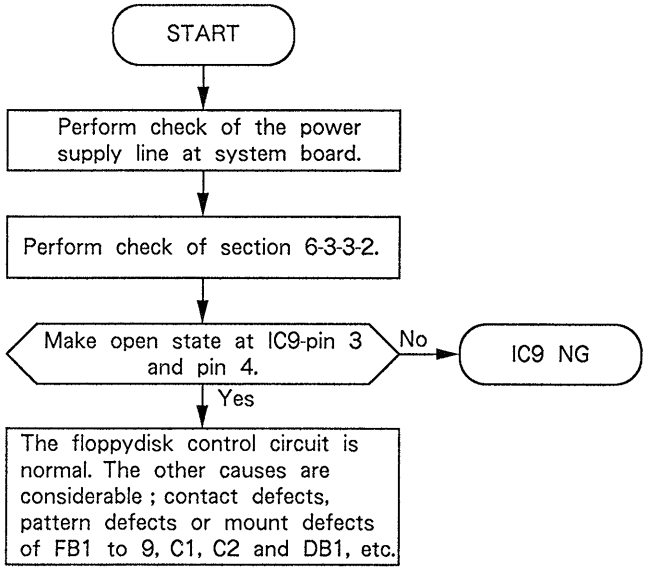
6-3-3-6. Check 4



6-3-3-7. Check 5



6-3-3-8. Check 6



6-4. IF-156V/VA BOARD (INTERFACE BOARD)

6-4-1. Previous Confirmation

Confirm that the connector pins of CN203 and CN204 are not bent, that the keyboard controller (IC222) is correctly mounted in the socket, that the I/O device switch (SW201) and jumpers are set properly, and that there is no problems with the interface connectors, cable and connected equipment.
The interface connector of the RS-232C (2) is located on the front panel.
The controls for adjusting the volume of the PSG, etc., are also located on the front panel.

6-4-2. Representative Trouble

1) When the system will not start ;
   Point : The computer has halted due to a malfunction of IC222, RTC (IC225), the address decoder (IC233), or peripheral circuitry. The system will not start due to bus interface malfunctions.
   Flow : Section 6-4-2-1.

2) When the keyboard related abnormality ;
2-1) When the massage of the self-diagnosis error 06H is displayed ;
   Point : Probable malfunction in the keyboard or IC222.
2-2) When the keyboard can not operate without an error indication.
   Point : Probable causes include a malfunction in the keyboard, malfunction of IC222 or peripheral circuitry, improper setting of the I/O device switch, or malfunction in peripheral circuitry.
   Flow : Section 6-4-2-2.
Note :Computer may also be halted due to IC222 malfunction.

3) When the RTC is abnormal ;
3-1) When the massage of the self-diagnosis error 03H is displayed ;
   Point : Confirm that the backup battery on the system board is defective. This error is indicated when the computer has not been used for an extended period of time or when this interface board is removed from the slot.
   If there is no battery malfunction, a probable cause is a malfunction of the RTC or charging circuit.
3-2) When the massage of the self-diagnosis error 13H is displayed ;
   Point : Probable malfunction in RTC or X201, etc.
   Flow : Section 6-4-2-3.
Note : Computer may also be halted due to RTC malfunction.

4) When the serial interface is abnormal ;
4-1) When NG (no good) is displayed by diagnosis of the maintenance disk ;
   Point : Probable malfunction in the interface controllers (IC202 or IC223) or IC203.
4-2) When the massage of the self-diagnosis error 05H or 15H is displayed ;
   Point : Probable malfunction in the interface controllers (IC202 or IC223) or the address decoder (IC233).
4-3) There is actual communication trouble although there are none of the above problems.
   Point : It is highly probable that the driver/receiver ICs of the serial interface are malfunctioning. Using another unit, confirm that the equipment on the other side operates properly and that the connection method is correct.
   Flow : Section 6-4-2-5.

5) When the printer interface is abnormal ;
5-1) When NG (no good) is displayed by diagnosis of the maintenance disk, or the massage of the self-diagnosis error 04H is displayed ;
   Point :
5-2) When the action of the printer is abnormal ;
   Point : Malfunction related to the I/O decoder (IC235) or IC206,234,236-238,241 printer interface. Confirm that the printer and that the connection method is correct.
   Flow : Section 6-4-2-6.

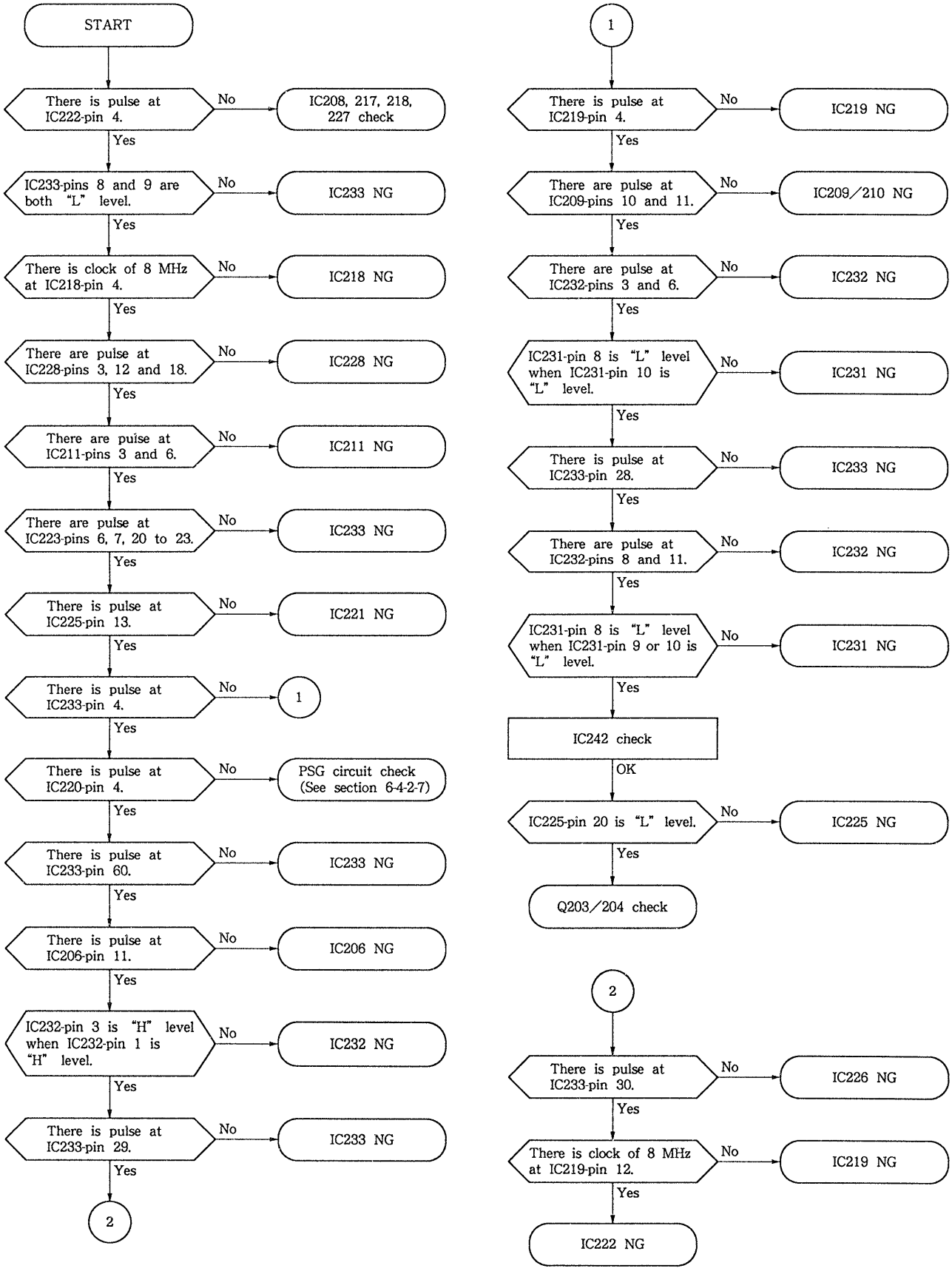
6) When beep or sound of the PSG is abnormal ;
   Point : When both the PSG sound and beeps are abnormal, it is probable that the malfunction is in the audio amplifier or muting circuit. If only the beeps are abnormal, the malfunction is probably in IC210 or the timer (IC226). If only the PSG sound is abnormal, the malfunction is probably in the PSG, peripheral circuitry, or the address decoder (IC233).
   Flow : Section 6-4-2-7.

7) Screen is not displayed when the causes in the interface board.
   Point : Probable malfunction in the IC211 or IC233.
   Flow : Section 6-4-2-4.

8) Floppydisk drive does not operate when the causes in the interface board.
   This trouble is the same as paragraph 7.

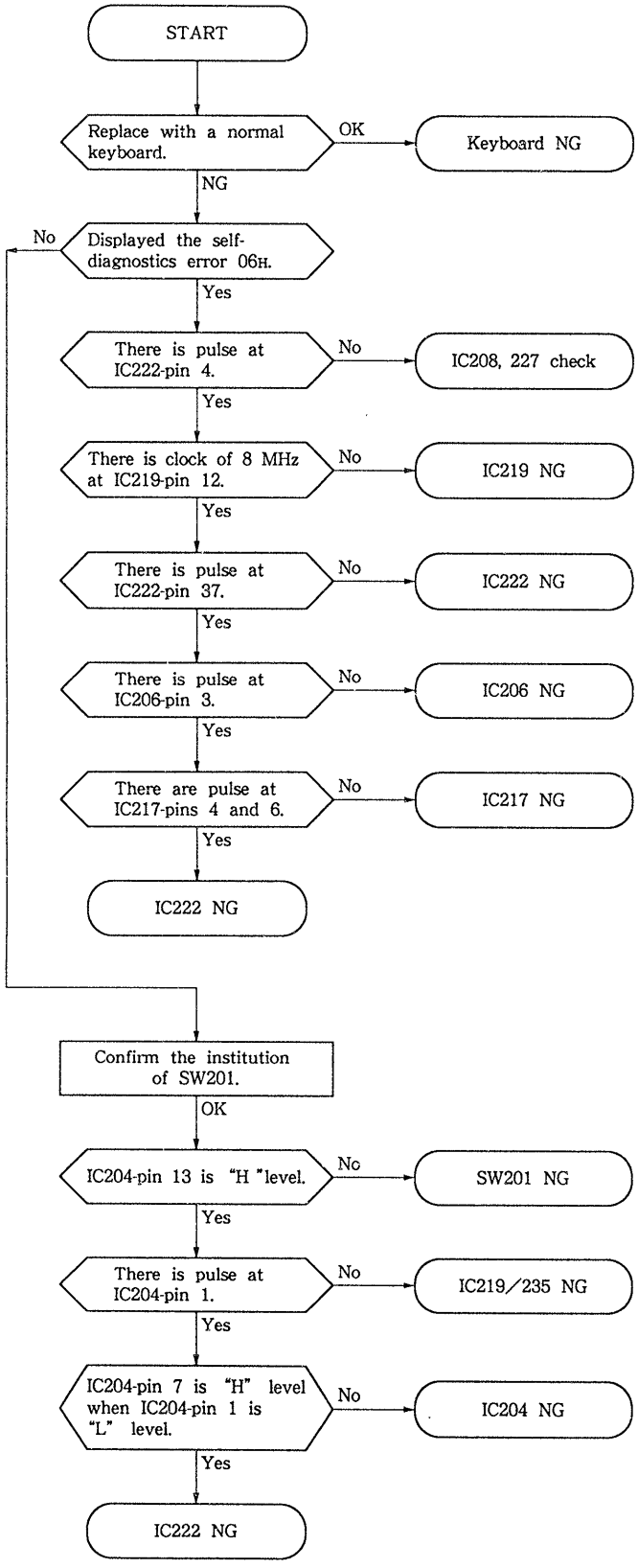
6-4-2-1. When the system will not start

Observation of the various signals is mode after applying a RESET.



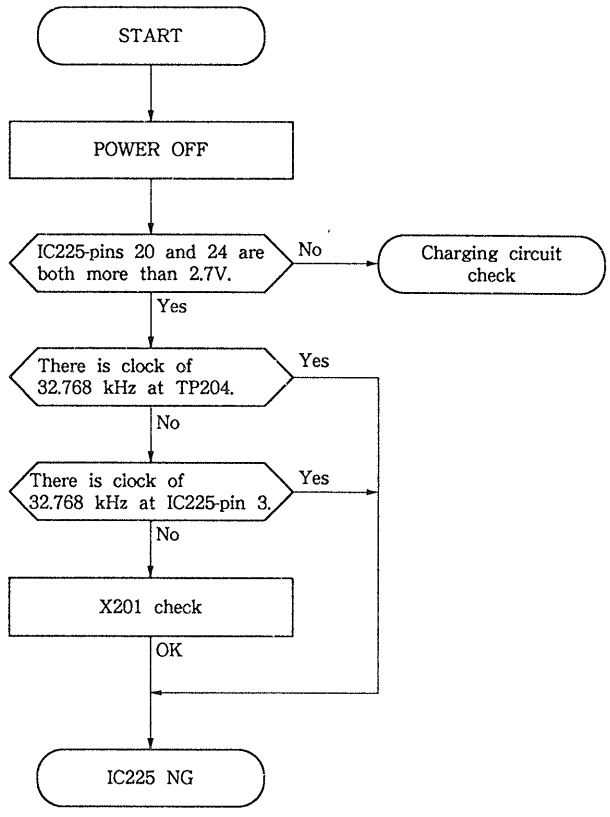
6-4-2-2. When the keyboard is abnormal

Observation of the various signals is mode after applying a RESET.



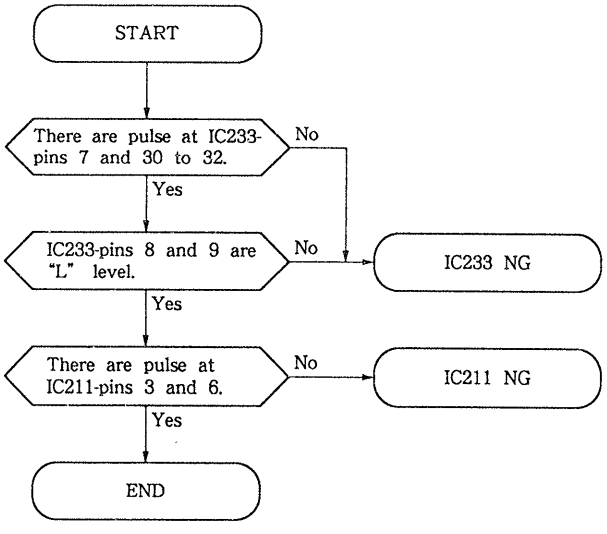
6-4-2-3. When the RTC is abnormal

Observation of the various signals is mode after applying a RESET.



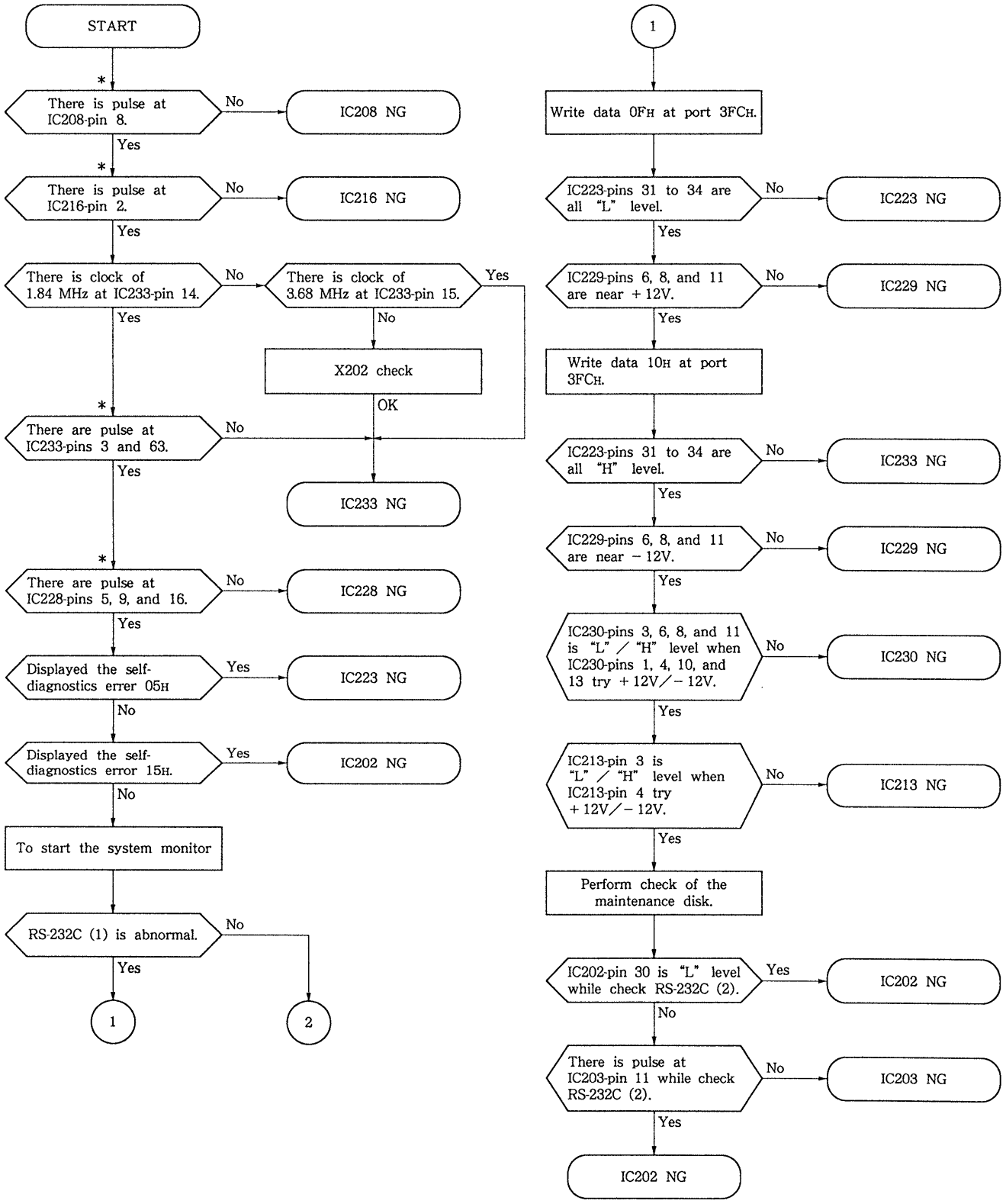
6-4-2-4. Check of the address decoder IC233

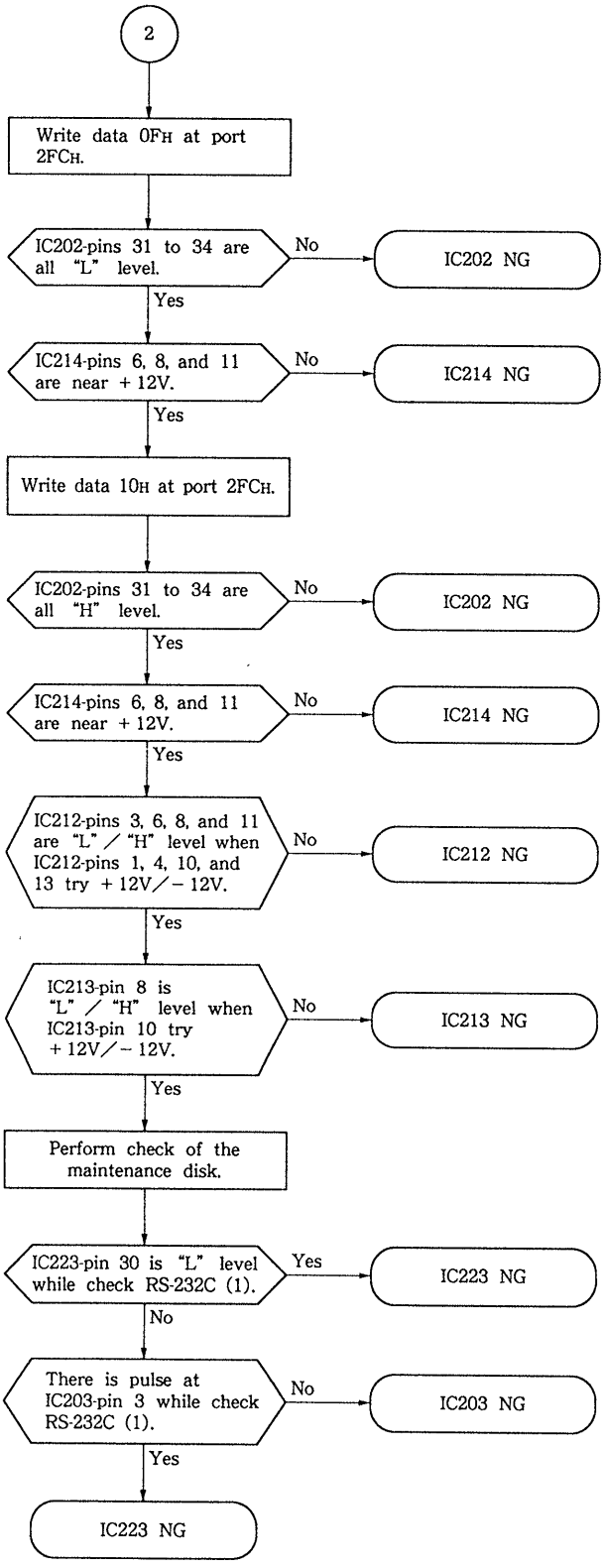
Observation of the various signals is mode after applying a RESET.



6-4-2-5. When the serial interface is abnormal

An asterisk (*) in the flowchart indicates that the RESET is entered.





6-4-2-6. When the printer interface is abnormal

An asterisk (*) in the flowchart indicates that the RESET is entered.

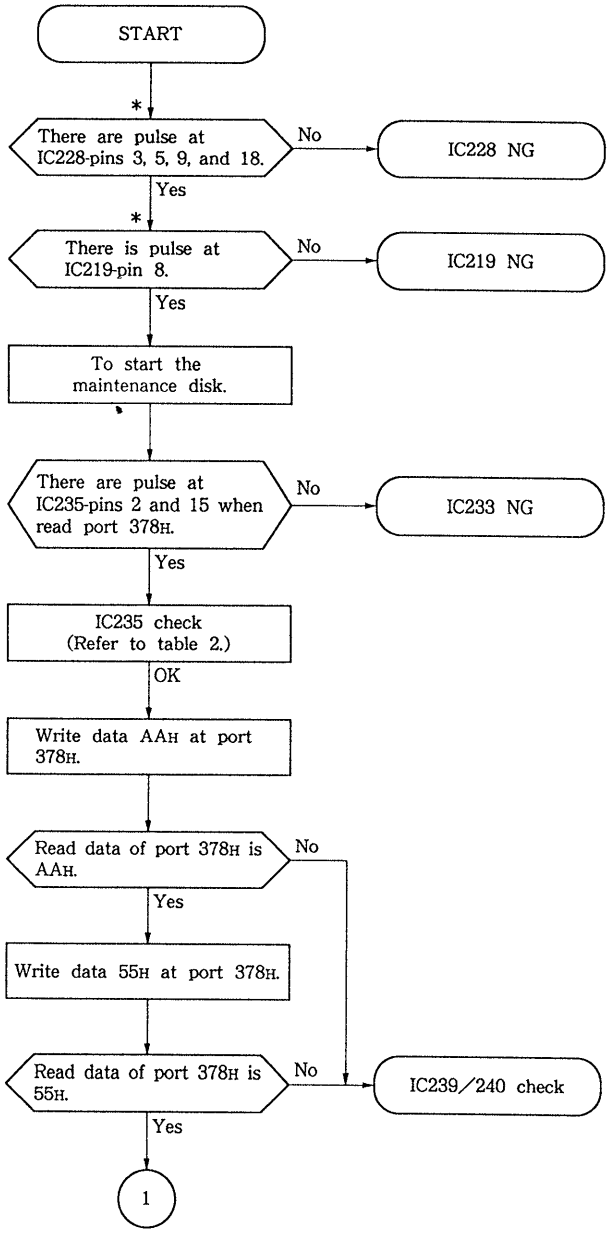
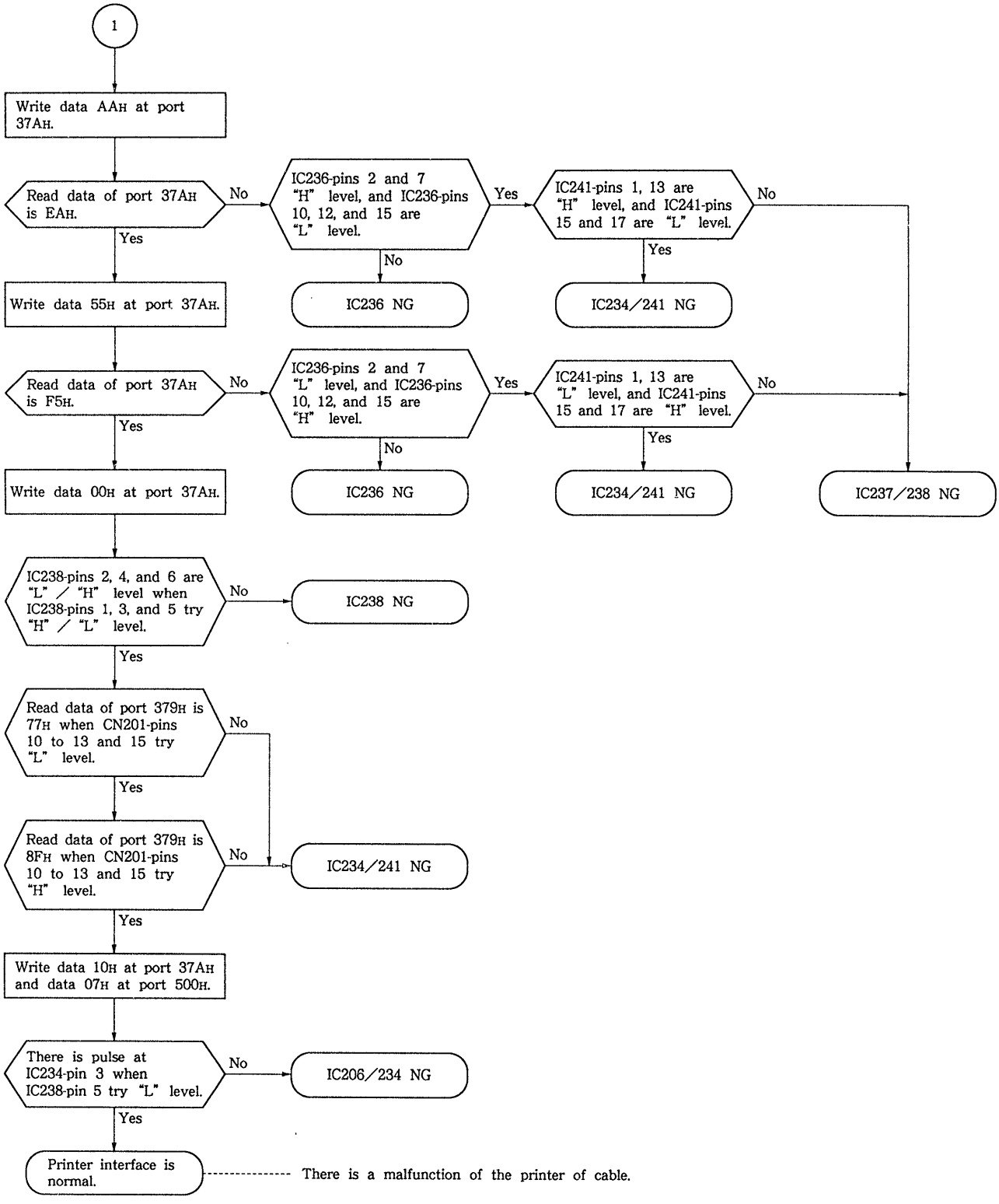


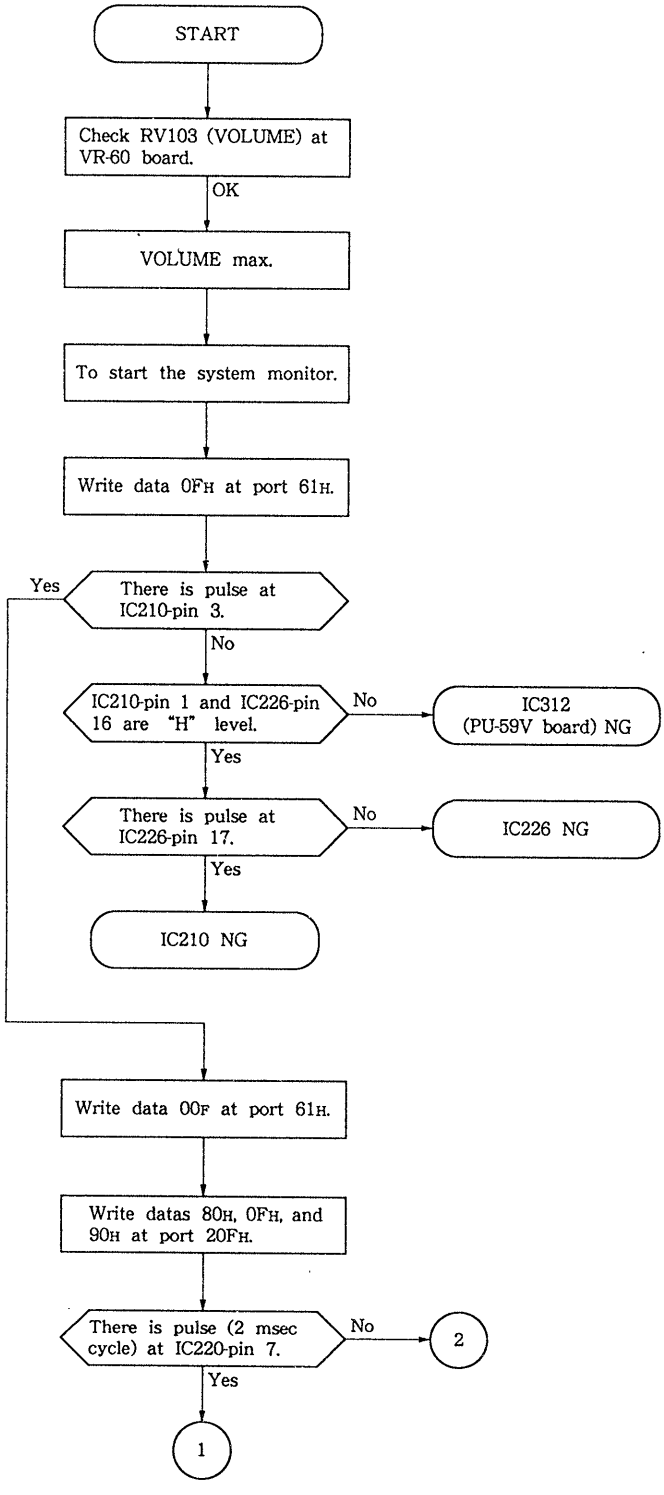
Table 2

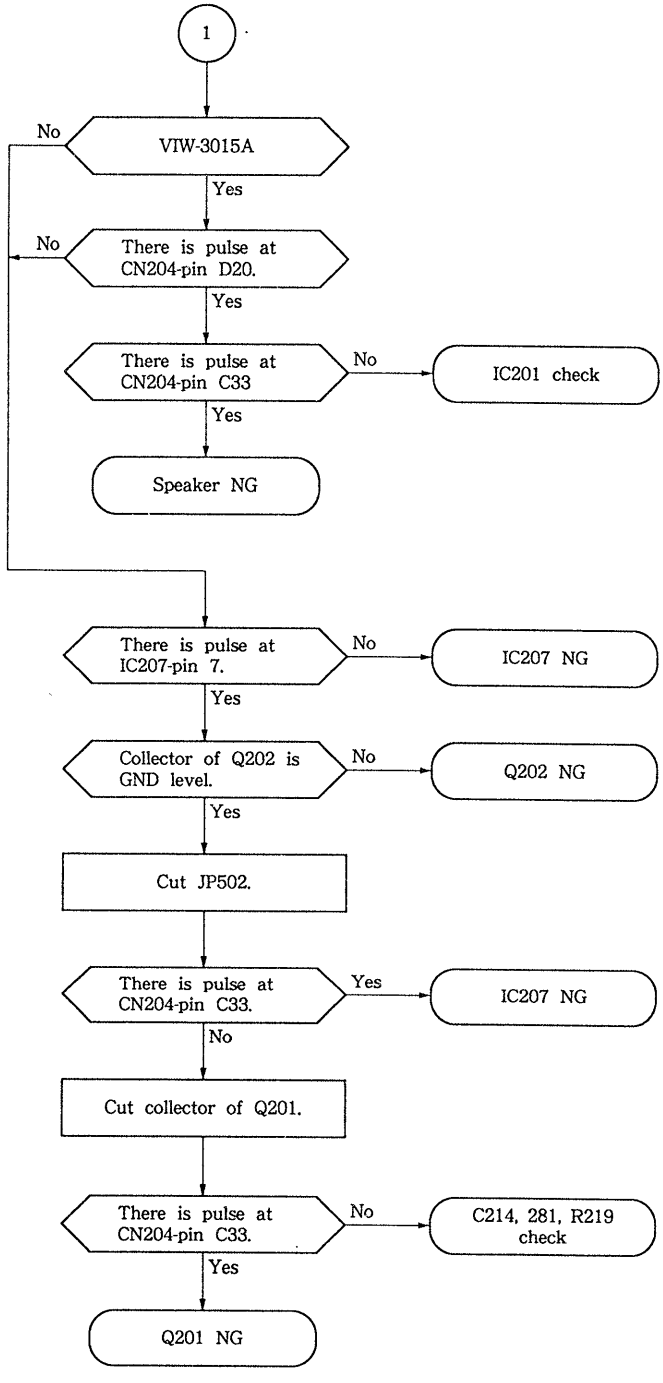
Port	R/W	Output of decode signal pulse
378H	Read	Pin 7 of IC235.
	Write	Pin 9 of IC235.
379H	Read	Pin 6 of IC235.
	Write	Pin 10 of IC235.
37AH	Read	Pin 5 of IC235.
	Write	Pin 11 of IC235.
37BH	Read	Pin 4 of IC235.
	Write	Pin 12 of IC235.

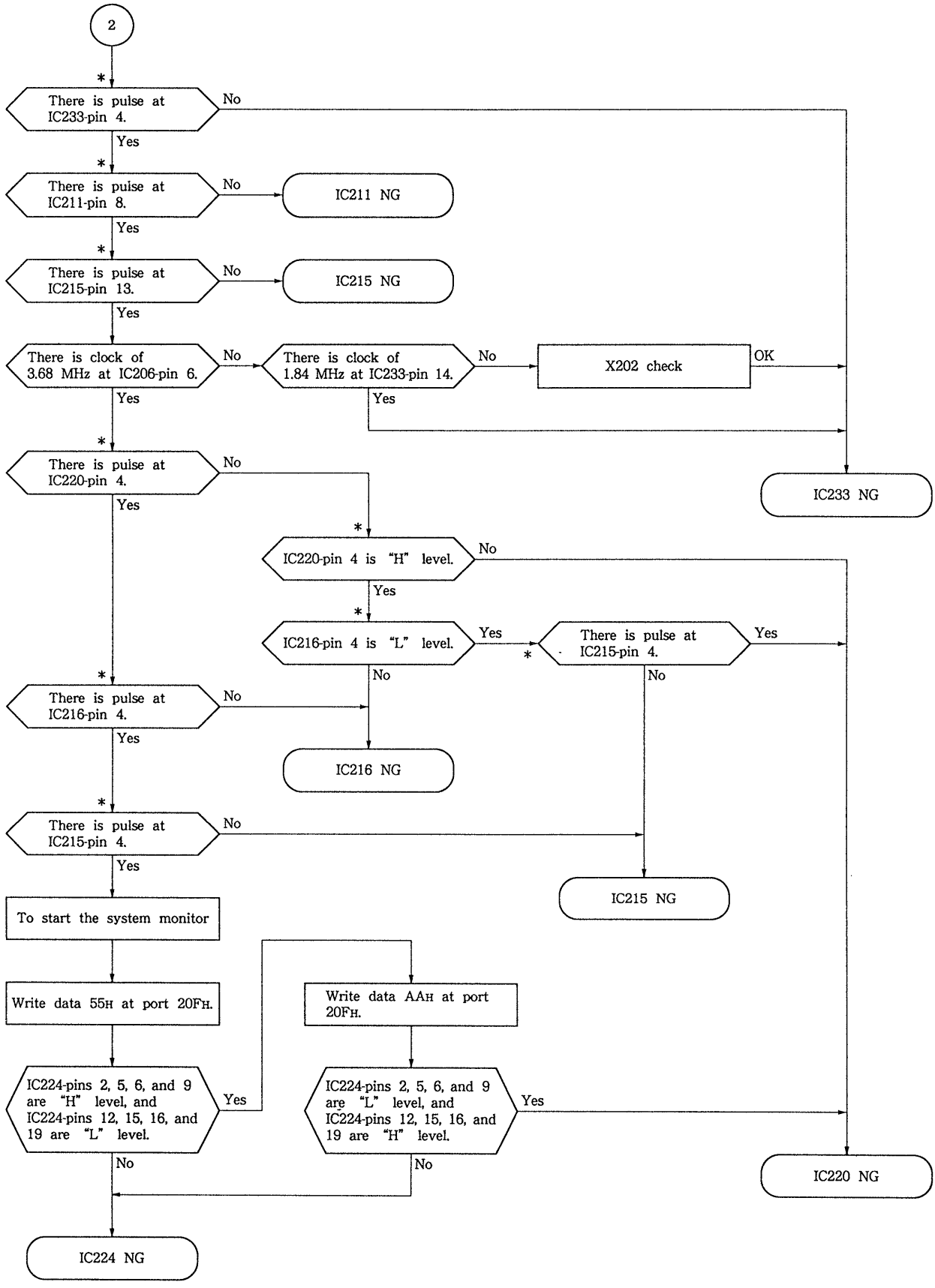

1
Write data AAH at port 37AH.
Read data of port 37AH is EAH.
No
IC236-pins 2 and 7 "H" level, and IC236-pins 10, 12, and 15 are "L" level.
Yes
IC241-pins 1, 13 are "H" level, and IC241-pins 15 and 17 are "L" level.
No
Yes
No
Yes
Write data 55H at port 37AH.
IC236 NG
IC234/241 NG
Read data of port 37AH is F5H.
No
IC236-pins 2 and 7 "L" level, and IC236-pins 10, 12, and 15 are "H" level.
Yes
IC241-pins 1, 13 are "L" level, and IC241-pins 15 and 17 are "H" level.
No
Yes
No
Yes
Write data 00H at port 37AH.
IC236 NG
IC234/241 NG
IC237/238 NG
IC238-pins 2, 4, and 6 are "L" / "H" level when IC238-pins 1, 3, and 5 try "H" / "L" level.
No
IC238 NG
Yes
Read data of port 379H is 77H when CN201-pins 10 to 13 and 15 try "L" level.
No
Yes
Read data of port 379H is 8FH when CN201-pins 10 to 13 and 15 try "H" level.
No
IC234/241 NG
Yes
Write data 10H at port 37AH and data 07H at port 500H.
There is pulse at IC234-pin 3 when IC238-pin 5 try "L" level.
No
IC206/234 NG
Yes
Printer interface is normal.
There is a malfunction of the printer of cable.

6-4-2-7. When the beeps or PSG sound is abnormal

An asterisk (*) in the flowchart indicates that the RESET is entered.






2
There is pulse at IC233-pin 4.
No
Yes
There is pulse at IC211-pin 8.
No
IC211 NG
Yes
There is pulse at IC215-pin 13.
No
IC215 NG
Yes
There is clock of 3.68 MHz at IC206-pin 6.
No
There is clock of 1.84 MHz at IC233-pin 14.
No
X202 check
OK
Yes
Yes
IC233 NG
There is pulse at IC220-pin 4.
No
Yes
IC220-pin 4 is "H" level.
No
Yes
IC216-pin 4 is "L" level.
Yes
There is pulse at IC215-pin 4.
Yes
No
No
There is pulse at IC216-pin 4.
No
Yes
IC216 NG
There is pulse at IC215-pin 4.
No
Yes
IC215 NG
To start the system monitor
Write data 55H at port 20FH.
Write data AAH at port 20FH.
IC224-pins 2, 5, 6, and 9 are "H" level, and IC224-pins 12, 15, 16, and 19 are "L" level.
Yes
IC224-pins 2, 5, 6, and 9 are "L" level, and IC224-pins 12, 15, 16, and 19 are "H" level.
Yes
No
No
IC220 NG
IC224 NG

6-5. PU-59V BOARD (CPU MAIN BOARD)

6-5-1. Previous Confirmation

Check to be sure that connector pins CN302, CN303 are not bent, that the IC corresponding to the socket is properly inserted, that it is properly connected with the RAM-10 board, and also that a proper step has been taken to keep up the proper function.
When checking PU-59V board (VIW-3015A), don't remove it from SMC-3000V. This is because PU-59V board check is executed by detecting a presence of a malfunction of CG (DSC-38) board and HG (DSC-43V) board.

6-5-2. Representative Trouble

1) When the system will not start ;

1-1) When the message of the self-diagnosis error are displayed.
Point : Confirm just what error message has been displayed as a result of a check by referring to Chapter 7 (See Chapter 6-10 in SMC-3000V service manual). But care should be taken as an error message might be displayed for some other reason or other.
Flow : Section 6-5-2-1.

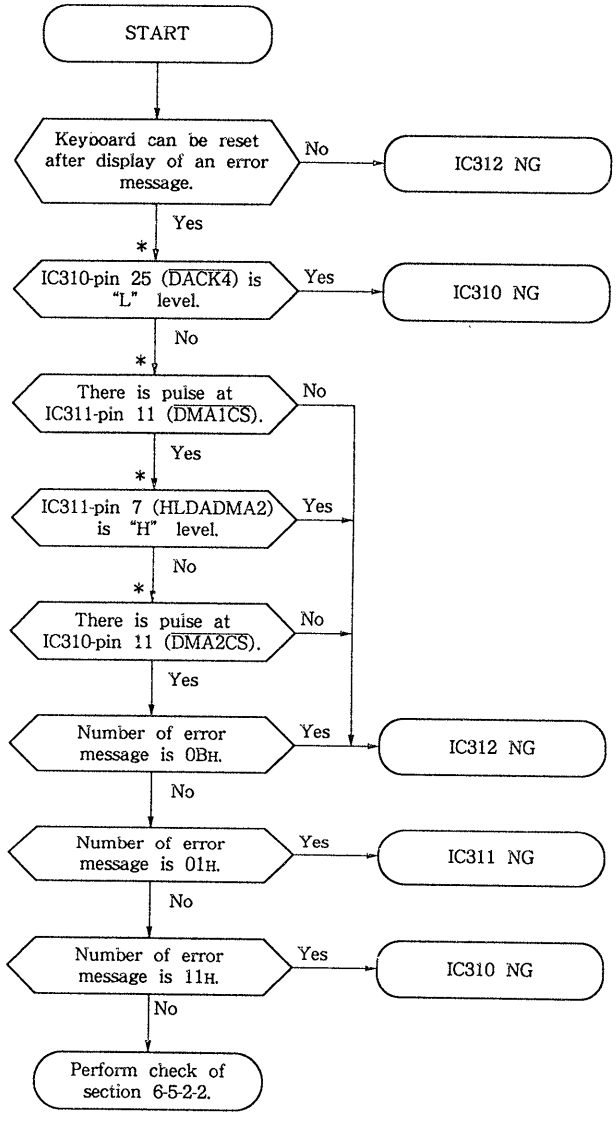
1-2) When the message of the self-diagnosis error is not displayed.
Point : Entire PU-59V board.
Flow : Section 6-5-2-2.

2) When the message of the self-diagnosis error are displayed.
Point : The same as 1-1). Also, such an error message is accompanied by other unusual symptom on the display screen in many cases. It is therefore suspected that memory bank with the RAM on CG and HG might not have been properly made. Also, if the board has an expansion RAM, it is often not possible to correctly judge the RAM size.
Flow : Section 6-5-2-3.

3) No error message of the self-diagnosis is displayed, but DMA does not normally operate.
Point : No error message is displayed because the interface between the DMA controller and the CPU is normal. Therefore, a trouble elsewhere is suspected (that is, a trouble with the DMA controller itself, or with the clock, IC307, etc.)
Flow : Section 6-5-2-4.

6-5-2-1. When the system will not start (When the message of the self-diagnosis error are displayed) ;

Normally, this applies to a case where an error message 01H, 0BH, or 11H has been displayed.
An asterisk (*) in the flowchart indicates that the RESET is entered.



6-5-2-2. When the system will not start

(When the message of the self-diagnosis error is not displayed) ;

An asterisk (*) in the flowchart indicates that the RESET is entered.

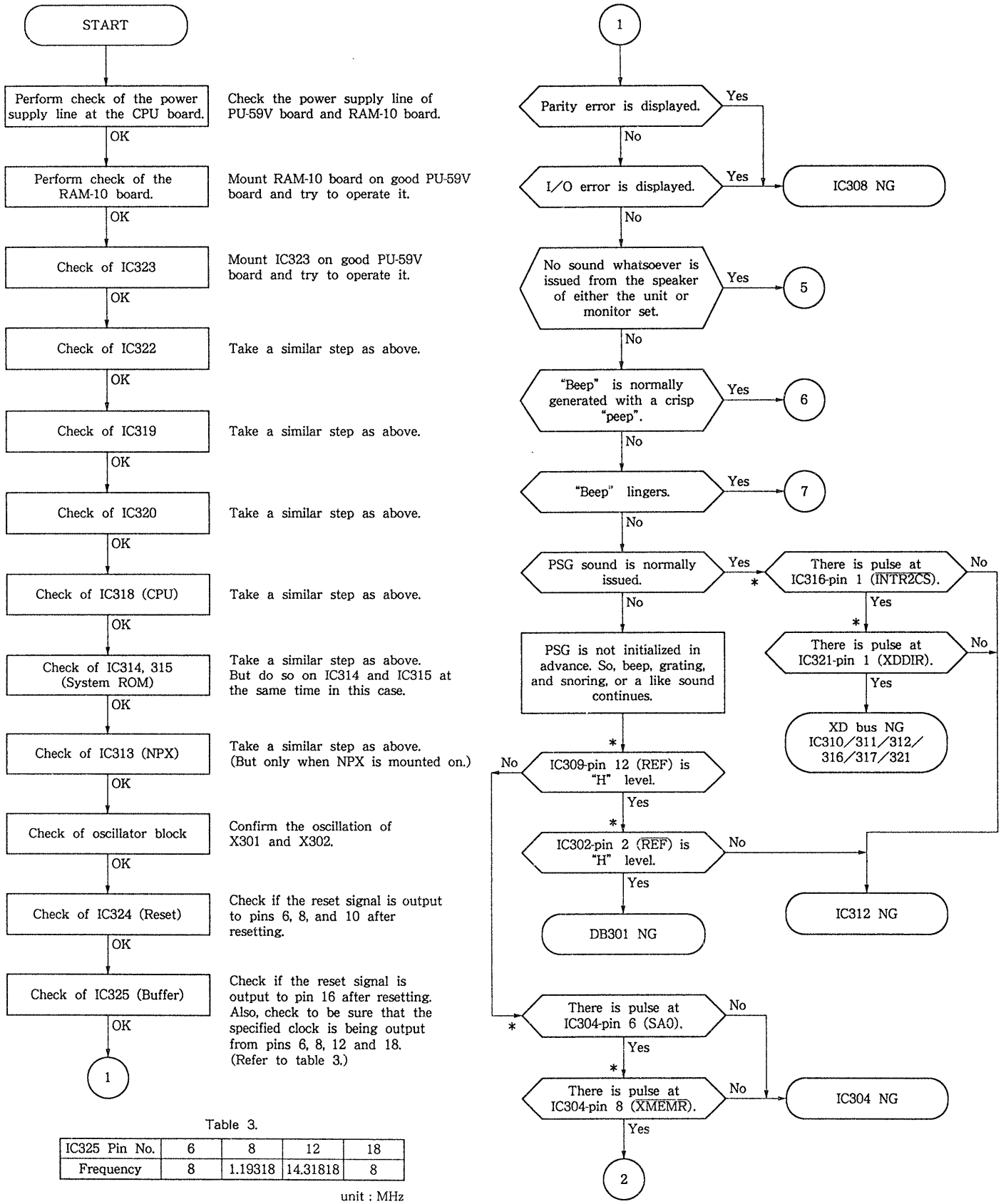
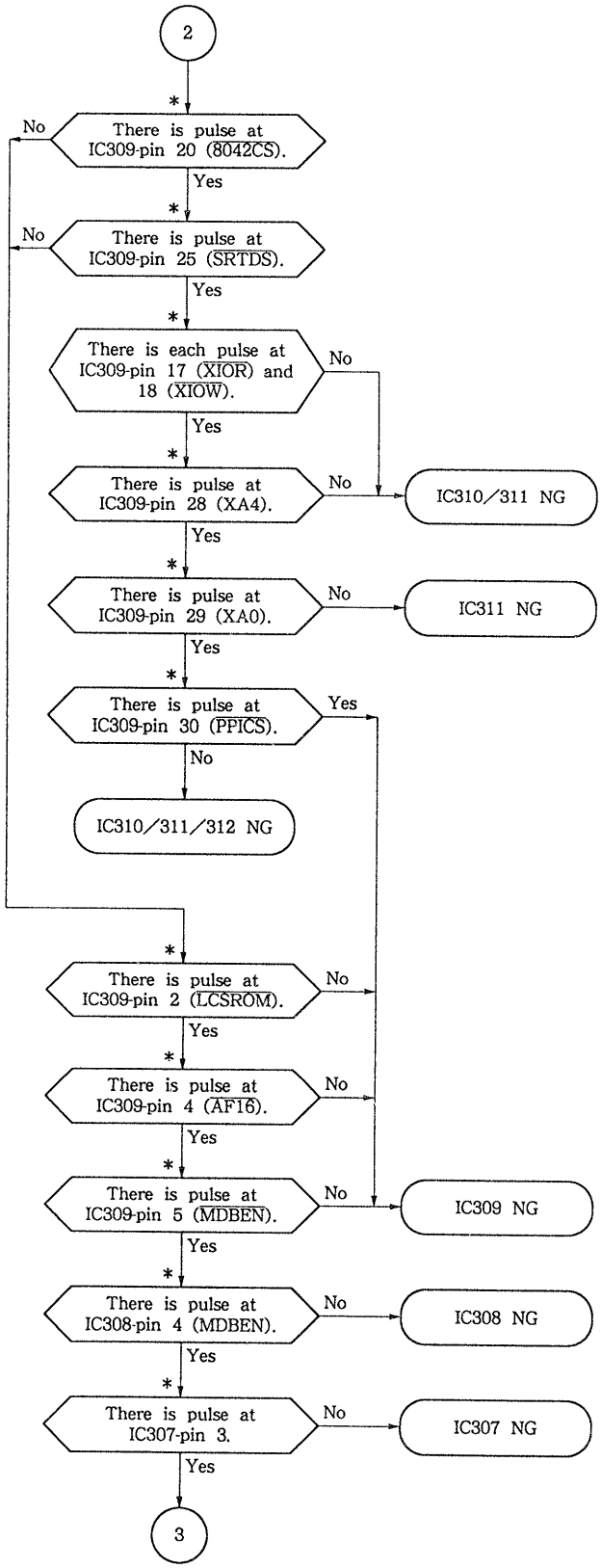
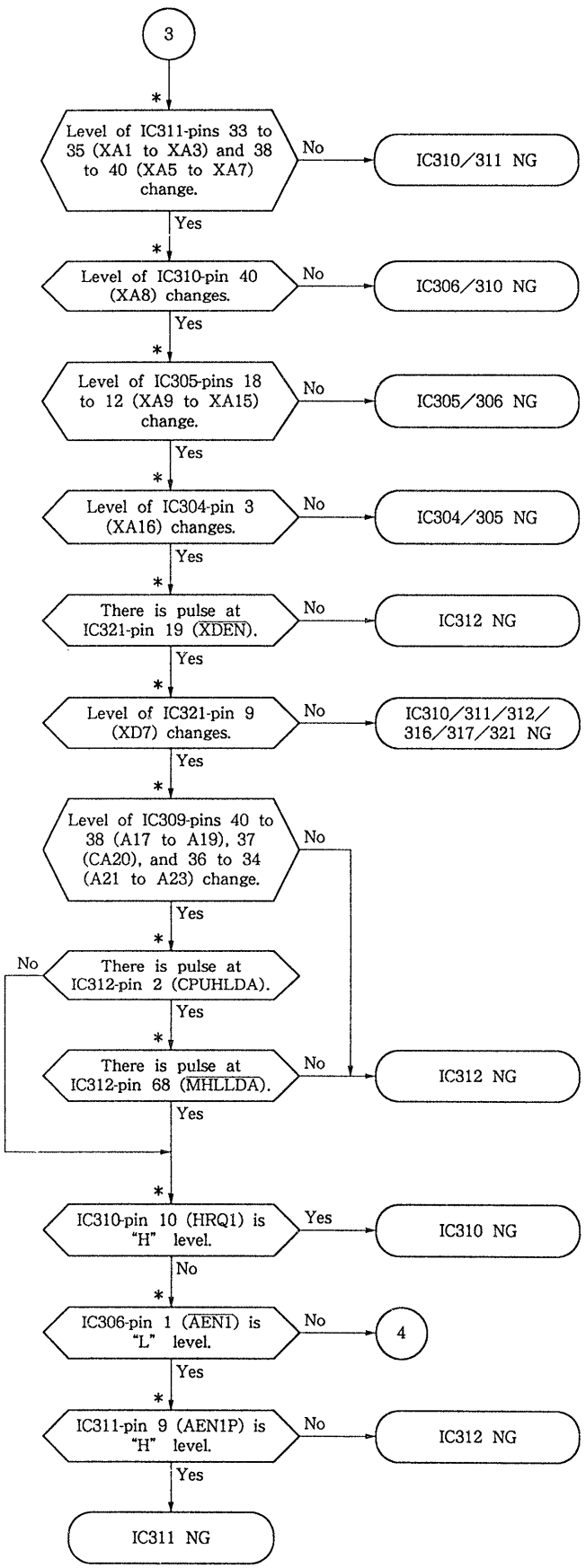


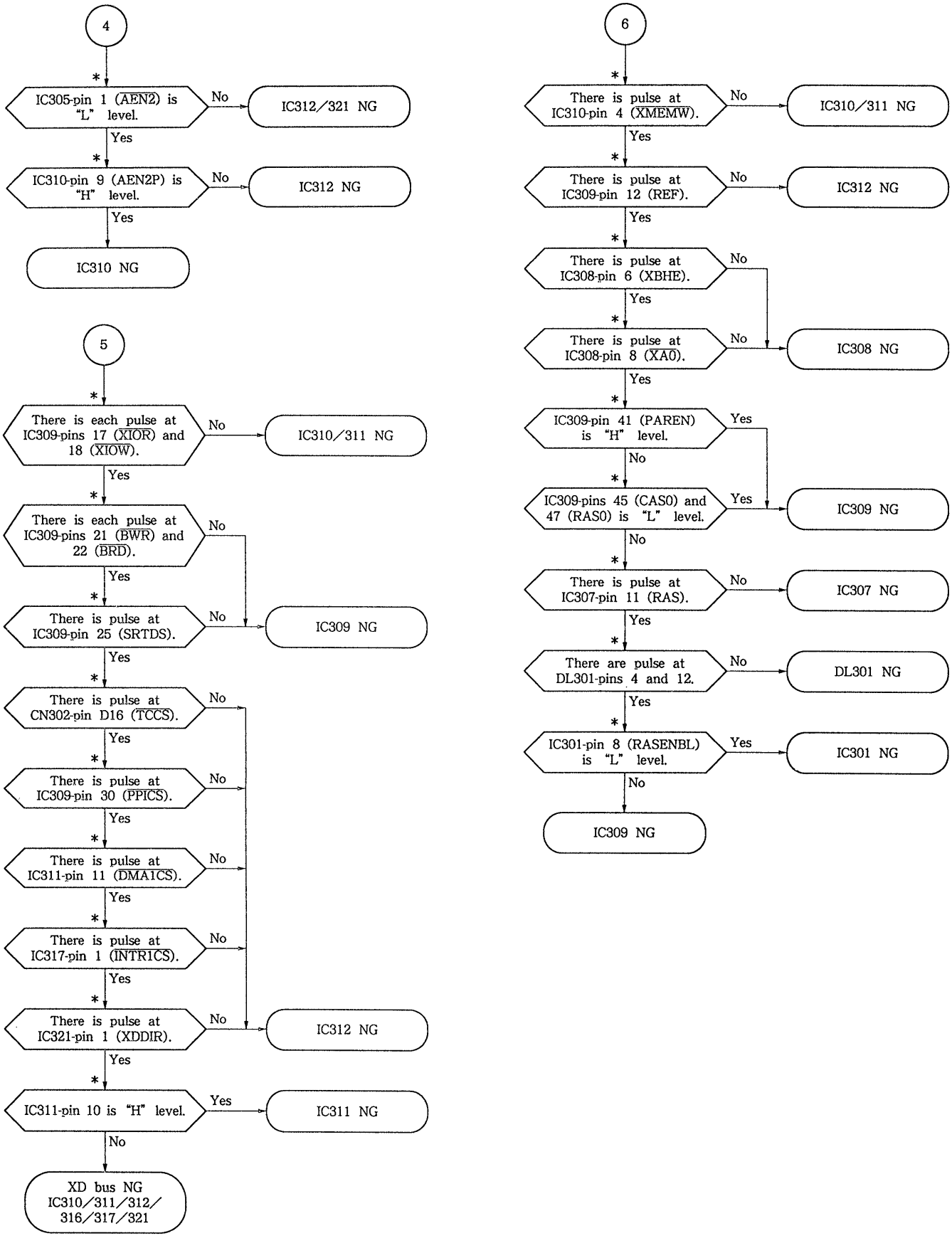
Table 3.

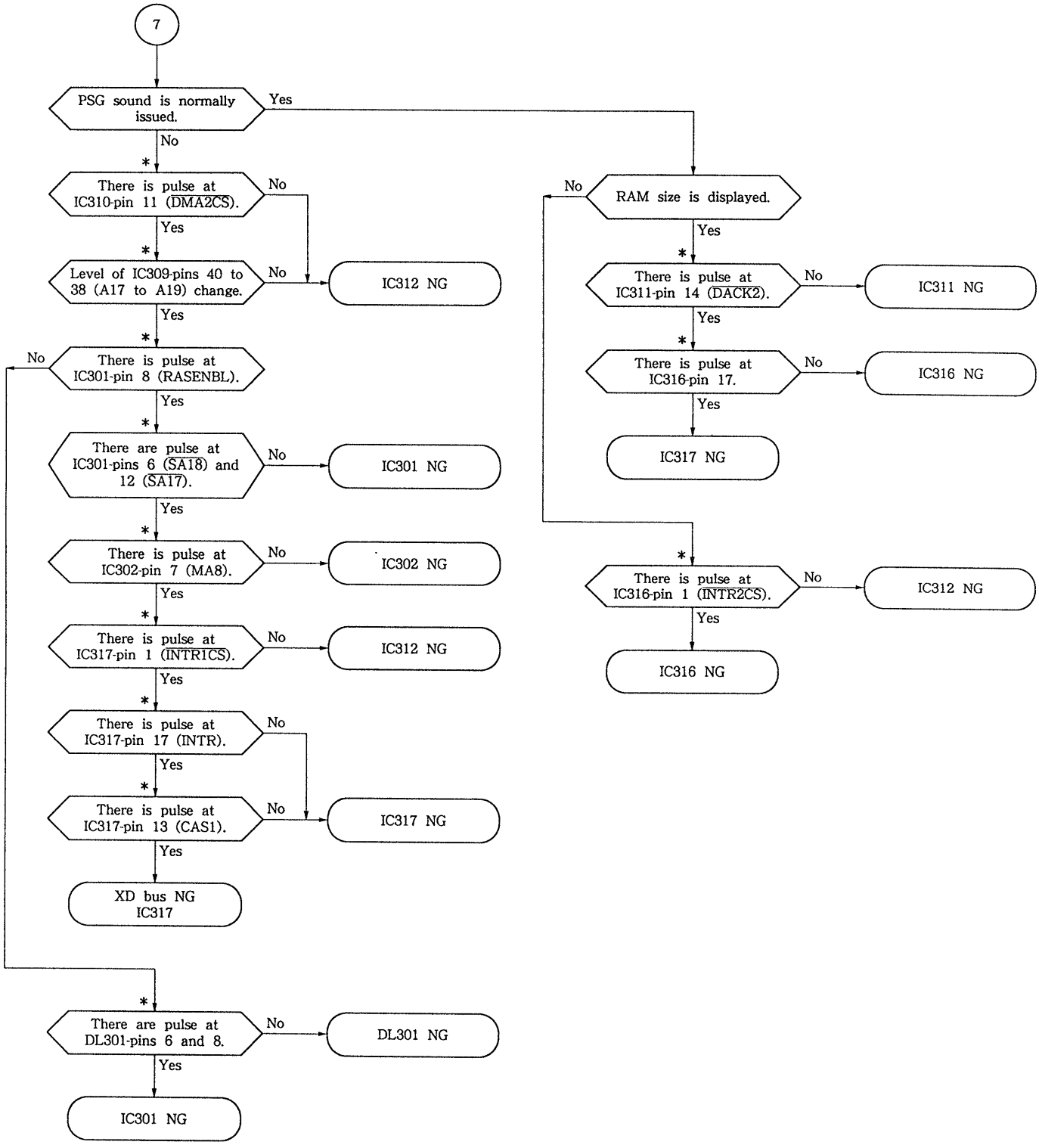
IC325 Pin No.	6	8	12	18
Frequency	8	1.19318	14.31818	8

unit : MHz


2
There is pulse at IC309-pin 20 (8042CS).
No
Yes
There is pulse at IC309-pin 25 (SRTDS).
No
Yes
There is each pulse at IC309-pin 17 (XIOR) and 18 (XIOW).
No
Yes
There is pulse at IC309-pin 28 (XA4).
No
IC310/311 NG
Yes
There is pulse at IC309-pin 29 (XA0).
No
IC311 NG
Yes
There is pulse at IC309-pin 30 (PPICS).
Yes
No
IC310/311/312 NG
There is pulse at IC309-pin 2 (LCSROM).
No
Yes
There is pulse at IC309-pin 4 (AF16).
No
Yes
There is pulse at IC309-pin 5 (MDBEN).
No
IC309 NG
Yes
There is pulse at IC308-pin 4 (MDBEN).
No
IC308 NG
Yes
There is pulse at IC307-pin 3.
No
IC307 NG
Yes
3

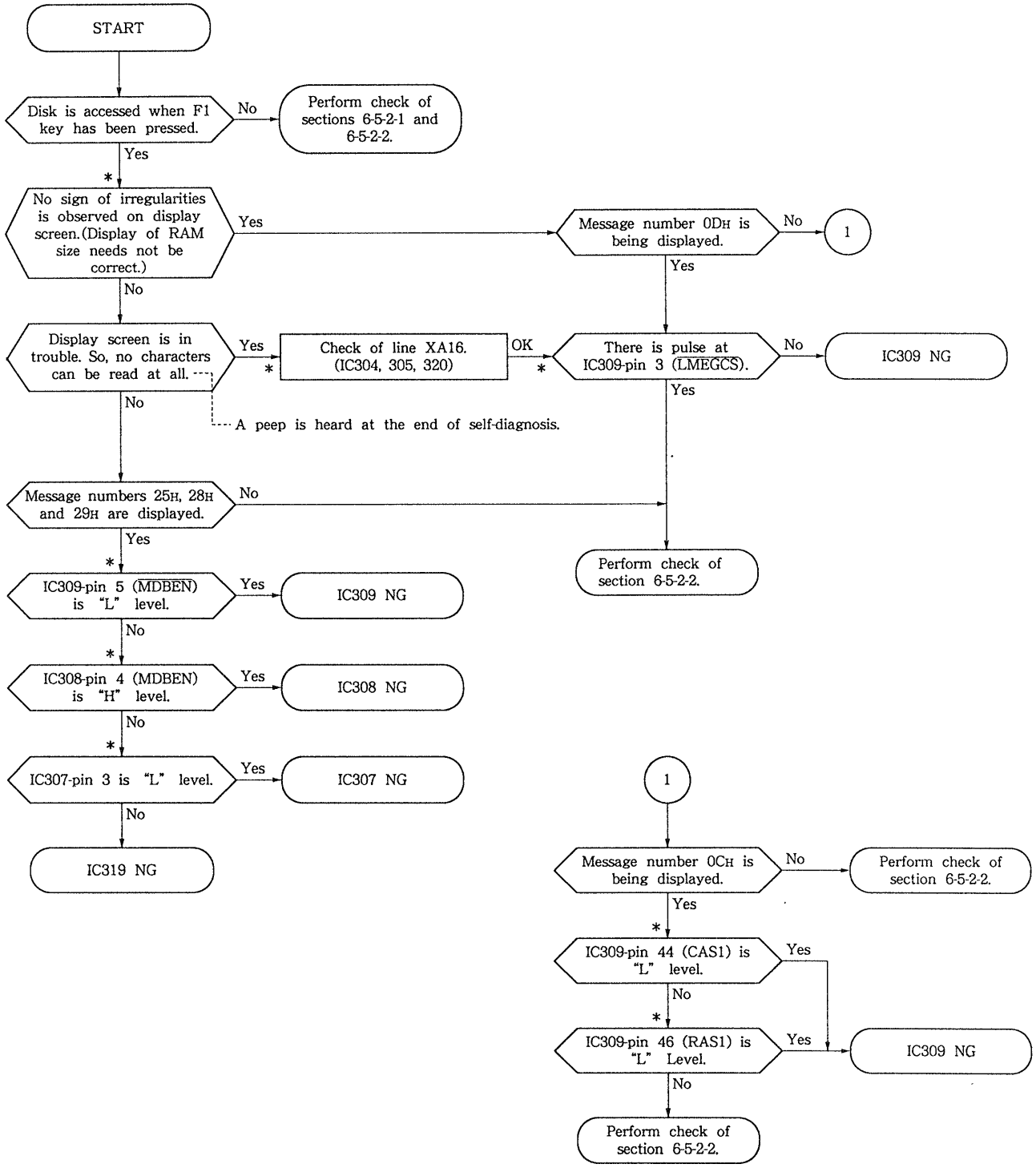

3
Level of IC311-pins 33 to 35 (XA1 to XA3) and 38 to 40 (XA5 to XA7) change.
No
IC310/311 NG
Yes
Level of IC310-pin 40 (XA8) changes.
No
IC306/310 NG
Yes
Level of IC305-pins 18 to 12 (XA9 to XA15) change.
No
IC305/306 NG
Yes
Level of IC304-pin 3 (XA16) changes.
No
IC304/305 NG
Yes
There is pulse at IC321-pin 19 (XDEN).
No
IC312 NG
Yes
Level of IC321-pin 9 (XD7) changes.
No
IC310/311/312/316/317/321 NG
Yes
Level of IC309-pins 40 to 38 (A17 to A19), 37 (CA20), and 36 to 34 (A21 to A23) change.
No
Yes
No
There is pulse at IC312-pin 2 (CPUHLDA).
Yes
There is pulse at IC312-pin 68 (MHLLDA).
No
IC312 NG
Yes
IC310-pin 10 (HRQ1) is "H" level.
Yes
IC310 NG
No
IC306-pin 1 (AEN1) is "L" level.
No
4
Yes
IC311-pin 9 (AEN1P) is "H" level.
No
IC312 NG
Yes
IC311 NG


4
IC305-pin 1 (AEN2) is "L" level.
No
IC312/321 NG
Yes
IC310-pin 9 (AEN2P) is "H" level.
No
IC312 NG
Yes
IC310 NG
5
There is each pulse at IC309-pins 17 (XIOR) and 18 (XIOW).
No
IC310/311 NG
Yes
There is each pulse at IC309-pins 21 (BWR) and 22 (BRD).
No
Yes
There is pulse at IC309-pin 25 (SRTDS).
No
IC309 NG
Yes
There is pulse at CN302-pin D16 (TCCS).
No
Yes
There is pulse at IC309-pin 30 (PPICS).
No
Yes
There is pulse at IC311-pin 11 (DMA1CS).
No
Yes
There is pulse at IC317-pin 1 (INTR1CS).
No
Yes
There is pulse at IC321-pin 1 (XDDIR).
No
IC312 NG
Yes
IC311-pin 10 is "H" level.
Yes
IC311 NG
No
XD bus NG
IC310/311/312/316/317/321
6
There is pulse at IC310-pin 4 (XMEMW).
No
IC310/311 NG
Yes
There is pulse at IC309-pin 12 (REF).
No
IC312 NG
Yes
There is pulse at IC308-pin 6 (XBHE).
No
Yes
There is pulse at IC308-pin 8 (XA0).
No
IC308 NG
Yes
IC309-pin 41 (PAREN) is "H" level.
Yes
No
IC309-pins 45 (CAS0) and 47 (RAS0) is "L" level.
Yes
IC309 NG
No
There is pulse at IC307-pin 11 (RAS).
No
IC307 NG
Yes
There are pulse at DL301-pins 4 and 12.
No
DL301 NG
Yes
IC301-pin 8 (RASENBL) is "L" level.
Yes
IC301 NG
No
IC309 NG


7
PSG sound is normally issued.
Yes
No
*
There is pulse at IC310-pin 11 (DMA2CS).
No
Yes
*
Level of IC309-pins 40 to 38 (A17 to A19) change.
No
IC312 NG
Yes
*
No
There is pulse at IC301-pin 8 (RASENBL).
Yes
*
There are pulse at IC301-pins 6 (SA18) and 12 (SA17).
No
IC301 NG
Yes
*
There is pulse at IC302-pin 7 (MA8).
No
IC302 NG
Yes
*
There is pulse at IC317-pin 1 (INTR1CS).
No
IC312 NG
Yes
*
There is pulse at IC317-pin 17 (INTR).
No
Yes
*
There is pulse at IC317-pin 13 (CAS1).
No
IC317 NG
Yes
XD bus NG IC317
*
There are pulse at DL301-pins 6 and 8.
No
DL301 NG
Yes
IC301 NG
No
RAM size is displayed.
Yes
*
There is pulse at IC311-pin 14 (DACK2).
No
IC311 NG
Yes
*
There is pulse at IC316-pin 17.
No
IC316 NG
Yes
IC317 NG
*
There is pulse at IC316-pin 1 (INTR2CS).
No
IC312 NG
Yes
IC316 NG

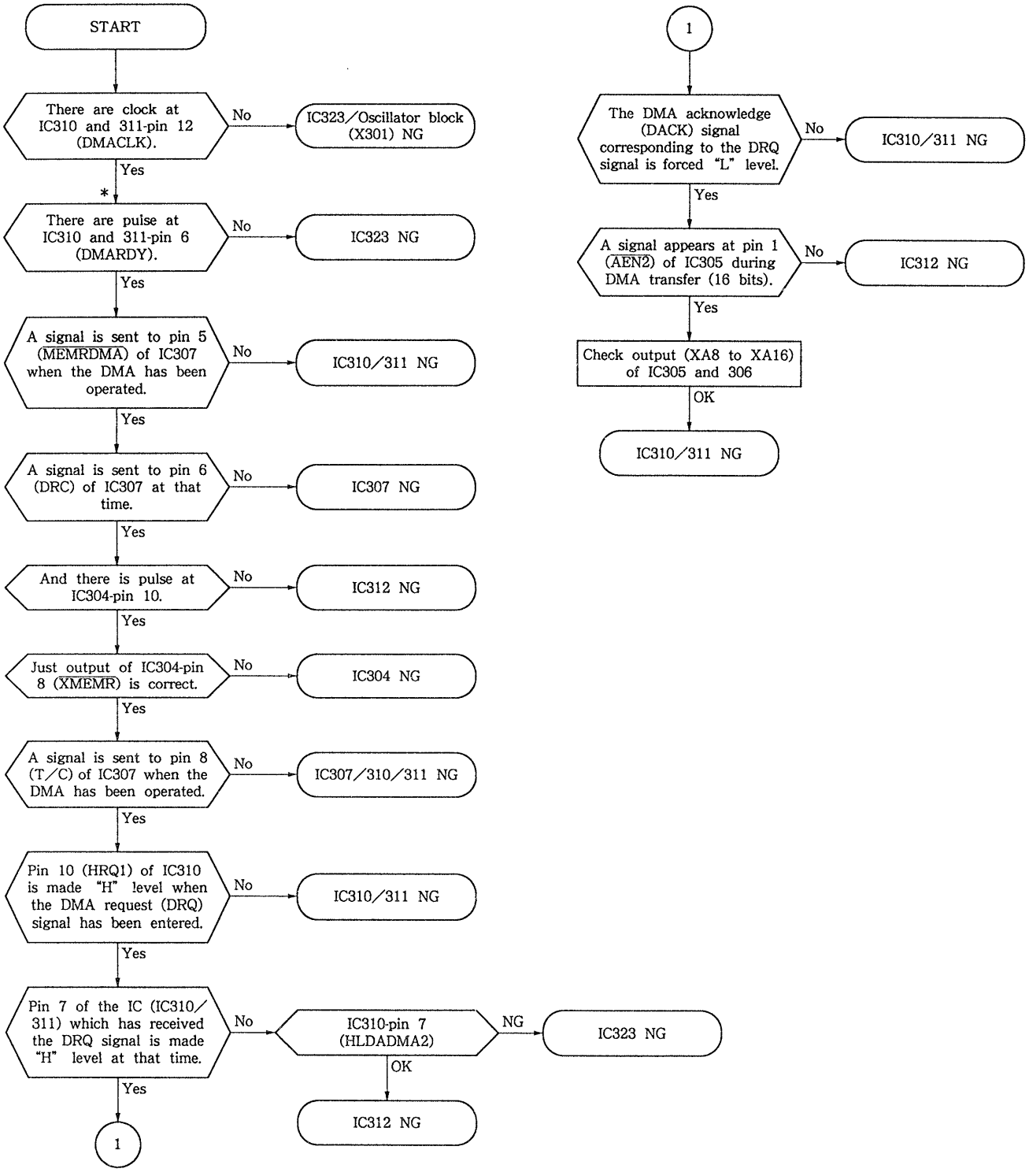
6-5-2-3. When the message of the self-diagnosis error are displayed ;

An asterisk (*) in the flowchart indicates that the RESET is entered.



6-5-2-4. When DMA does not normally operate.

An asterisk (*) in the flowchart indicates that the RESET is entered.

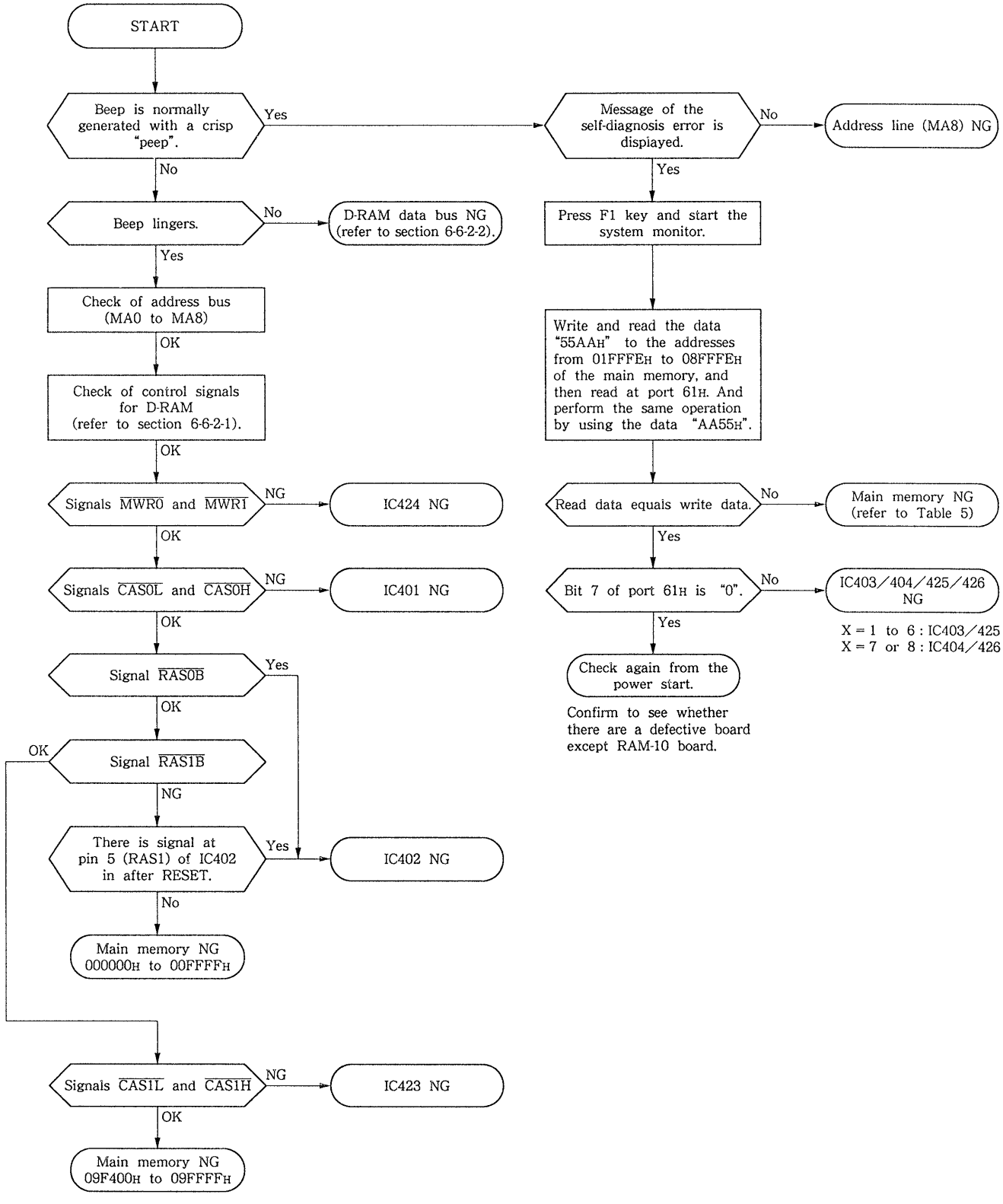


6-6. RAM-10 BOARD

6-6-1. Previous Confirmation

Confirm that the PU-59V board is normal or use proper one, check the RAM-10 board.

6-6-2. Troubleshooting of RAM-10 Board

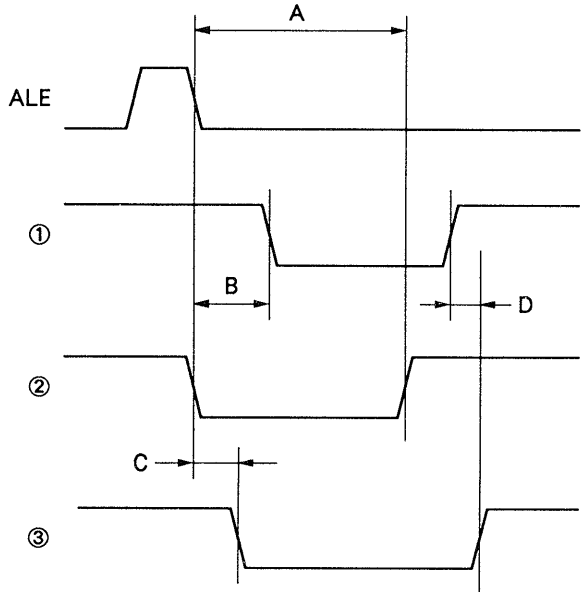


6-6-2-1. Check of control signals for D-RAM

Confirm the following signals by using ALE signal (pin 14 of IC309) as the trigger (sloop : ↑).

Table 4

Control signal name for D-RAMs.	Wave form No.
$\overline{CAS0L}$ (Pin 6 of IC401) $\overline{CAS0H}$ (Pin 8 of IC401) $\overline{CAS1L}$ (Pin 6 of IC423) $\overline{CAS1H}$ (Pin 8 of IC423)	①
$\overline{RAS0B}$ (Pin 8 of IC402) $\overline{RAS1B}$ (Pin 6 of IC402)	②
$\overline{MWR0}$ (Pin 3 of IC424) $\overline{MWR1}$ (Pin 11 of IC424)	③



A = 375 (∗ 300) nsec
B = 80nsec
C = 25 (MAX) nsec
D = 21 (MAX) nsec

Fig. 6-3.

6-6-2-2. Check of data bus

Take the RAM-10 board out from the unit and apply a power voltage to the RAM-10 board, and confirm to see whether the D-RAM data lines are high impedance condition.

- Apply a +5V to pin 25 of CN401.
- Connect pin 17 of CN401 to ground.
- Set pin 39 (RAS) of CN401 to ground.
- Apply a +5V to pin 43 of CN401 ($\overline{XMEMW}$).
- Confirm that all D-RAM control signals (refer to Table 4 of section 6-6-2-1.) are "H" level.
- Confirm that the D-RAM data lines are high impedance condition.

Table 5

Bit No.	Signal name	D-RAM	
Bit0	MD0	Pin 14 of IC414	Pin 2 of IC406
Bit1	MD1	Pin 14 of IC413	Pin 3 of IC406
Bit2	MD2	Pin 14 of IC412	Pin 15 of IC406
Bit3	MD3	Pin 14 of IC411	Pin 17 of IC406
Bit4	MD4	Pin 14 of IC410	Pin 2 of IC405
Bit5	MD5	Pin 14 of IC409	Pin 3 of IC405
Bit6	MD6	Pin 14 of IC408	Pin 15 of IC405
Bit7	MD7	Pin 14 of IC407	Pin 17 of IC405
Bit8	MD8	Pin 14 of IC422	Pin 2 of IC428
Bit9	MD9	Pin 14 of IC421	Pin 3 of IC428
Bit10	MD10	Pin 14 of IC420	Pin 15 of IC428
Bit11	MD11	Pin 14 of IC419	Pin 17 of IC428
Bit12	MD12	Pin 14 of IC418	Pin 2 of IC427
Bit13	MD13	Pin 14 of IC417	Pin 3 of IC427
Bit14	MD14	Pin 14 of IC416	Pin 15 of IC427
Bit15	MD15	Pin 14 of IC415	Pin 17 of IC427
	MDPOUT0	Pin 14 of IC403	Pin 14 of IC404
	MDPOUT1	Pin 14 of IC425	Pin 14 of IC426
Addresses		000000H to 07FFFFH	080000H to 09FFFFH

CHAPTER 8
ADJUSTMENT

There is a LDP-1500-type videodisc player mounted on the VIW-3015A. Disconnect it as explained in Chapter 2 before adjustment.

8-1. TOOLS LIST

In general, adjustment of this unit requires the following equipments :

1. Checker VIW-3015A
2. Monitor (CPD-1302 etc.) and Monitor cable
3. SMW-3001B (MS-DOS)
4. Accessories floppydisk and AV cable
5. Frequency counter
6. Oscilloscope (refer to section 8-4-1-2)
7. EIA color-bar signal generator (refer to section 8-4-1-3)
8. IF-156 extension board : P/N J-6093-380-A
9. PU-59 extension board : P/N J-6093-540-A
10. Two extension boards : P/N J-6093-490-A 2 sets
11. Screwdrivers for adjustment
12. Soldering iron and solder

8-2. IF-156VA BOARD

8-2-1. Preparation

Insert the IF-156 extension board (J-6093-380-A) into a slot A for the IF-156VA board, and the IF-156VA board to adjust into this extension board.
Have to exact connect, because, to prevent troubles.
Power ON, the computer and frequency counter.

8-2-2. RTC Clock Adjustment

Measuring equipment : Frequency counter
Measuring point : TP204
Specification : 32,768 ± 0.1Hz
Adjustment : CV201

8-3. PU-59VA BOARD

8-3-1. Preparation

Insert the PU-59 extension board (J-6093-540-A) into a slot B for the PU-59VA board, and the PU-59VA board to adjust into this extension board.
Have to exact connect, because, to prevent troubles.
Power ON, the computer and frequency counter.

8-3-2. System Clock Adjustment

Measuring equipment : Frequency counter
Measuring point : TP301
Specification : 14,318,180 ± 100Hz
Adjustment : CV301

8-4. VS-38A BOARD

8-4-1. Preparations

8-4-1-1. Installing

1. Referring to Section 2-1-4 (① through ③), remove the VS-38A board from slot 5 and insert the extension board (J-6093-490-1) in its place.

2. Referring to Section 2-1-4 (④ and ⑤), remove the VGA-16 board from slot 4 and insert the extension board (J-6093-490-1) in its place.

3. Attach the VS-38A board and the VGA-16 board to the extension boards.

4. Attach the cable (referring to ① of section 2-1-4) to the VS-38A board and the VGA-16 board.

5. Attach the AV cable to CN004 (AV IN) of the VS-38A board.

8-4-1-2. About Oscilloscope

An oscilloscope capable of following three or more waveforms (or two, if it has an external trigger input terminal) and provided with a TV sync (field, line) separator is required for adjustment of the VS-38A board.

- Band width limit
  This function restraints high-frequency components to make the waveform easier to observe. However, adjustment is also possible without this function.

- TV-LINE and TV-FLD
  Shows the TV sync separator trigger mode.

8-4-1-3. About Video signal

EIA standard color-bar signal (NTSC, setup 0%, white level 100%, 1Vp-p) is used as the video signal for the adjustment. While adjust the VS-38A board, must always give this signal to the VS-38A board.

8-4-1-4. Initial setting

DISP. BOARD switch is C side.
STARTING DEV switch is FD.AUTO side.
Refer to section 1-2-3.

- VGA-16 Board
  - SW1 ····· Only No.4 ON
  - W1 ····· Connected
  - W2 ····· Connected, below
- VS-38A Board
  - J001 ····· All 0 side
  - J003 ····· 0 side
  - SL001 ····· Short by the solder
  - SL002 ····· Short by the solder
  - SL003 ····· Short by the solder
  - SL004 ····· Open
  - SW001 ····· Only No.3 OFF

8-4-2. Run System

Operation 1 : Power on, the computer and monitor. Also, the oscilloscope and signal generator.
Operation 2 : Insert system disk (SMW-3001B) of MS-DOS in drive A.
Operation 3 : Make display the prompt "A>". Refer to the user's guide of MS-DOS.
Operation 4 : Take the system disk out of drive A.
Operation 5 : Insert accessory floppydisk on VIW-3015A.
Key operation 1 : INT10EX [RETURN]
Key operation 2 : VMODE SUP : S [RETURN]
Key operation 3 : VMODE MOD : 12 [RETURN]

8-4-3. H AFC Adjustment

Confirmation 1 : Applied the solder on the pattern jumper SL002.
Measuring equipment : Oscilloscope
Vertical mode : CHOP
Trigger channel : ch-1
Trigger slope : Up edge
Trigger coupling : AC
Measuring point ch-1 : TP010 (coupling : DC)
Measuring point ch-2 : TP008 (coupling : DC)

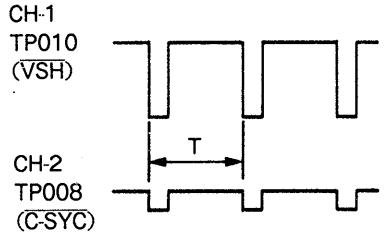


Fig. 8-4-3. TP008, TP010

Specification : T = 63.5 ± 0.5 μsec
Adjustment : RV003
Adjust the RV003 so that waveform of ch-1 drifts slowest.

Note : Set oscilloscope to 0.2V/DIV and 20 μsec/DIV.

Operation 1 : Power off, the computer
Operation 2 : Remove the solder from the pattern jumper SL002.
Operation 3 : Power on, the computer
Operation 4 : Run system (refer to section 8-4-2)
Confirmation 2 : Monitor screen and waveform of ch-1 are stable.

8-4-4. APC Adjustment

Operation 1 : Power off, the computer
Operation 2 : Remove the solder from the pattern jumper SL001.
Operation 3 : Power on, the computer
Operation 4 : Run system (refer to section 8-4-2)
Measuring equipment : Monitor

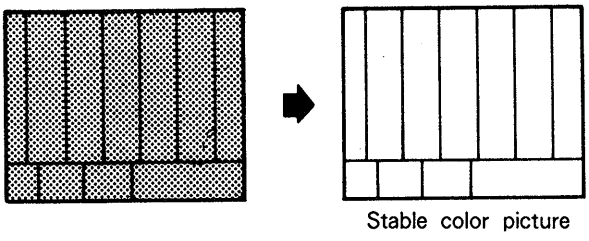


Fig. 8-4-4. Monitor screen

Specification : Color-sync is stable. See Fig. 8-4-4.
Adjustment : RV006

Operation 5 : Power off, the computer
Operation 6 : Apply the solder on the pattern jumper SL001.
Operation 7 : Power on, the computer
Operation 8 : Run system (refer to section 8-4-2)
Confirmation : Color-sync is stable. See Fig. 8-4-4.

8-4-5. Output RGB Level Adjustment

Measuring equipment : Oscilloscope
Vertical mode : ALT
Trigger channel : ch-3
Trigger slope : Up edge
Trigger coupling : AC
Measuring point ch-1 : TP004 (coupling : DC)
Measuring point ch-2 : TP007 (coupling : DC)
Measuring point ch-3 : TP008
Operation : Overlap GND-level of ch-1 and ch-2 on the oscilloscope screen.

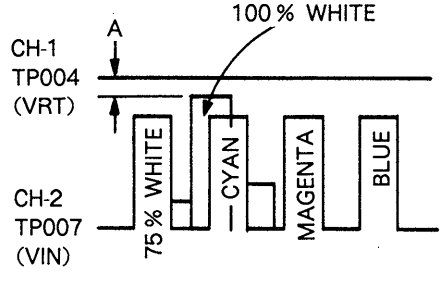


Fig. 8-4-5. TP004, TP007

Specification : A = 35 ± 5mV
Adjustment : RV002

Note : Set oscilloscope to 50mV/DIV and 20 μsec/DIV.

8-4-6. Carrier Leak Level Adjustment

Measuring equipment : Oscilloscope
Vertical mode : ch-1
Trigger channel : ch-2
Trigger slope : Up edge
Trigger coupling : AC
Measuring point ch-1 : TP002 (coupling : AC)
Measuring point ch-2 : TP008 (coupling : AC)

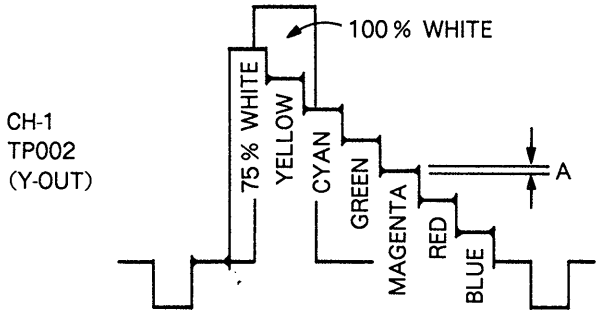


Fig. 8-4-6. TP002

Specification : A ≦ 10mVp-p
Adjustment : RV001, LV001 (alternately adjust)

Note : Set oscilloscope to 2mV/DIV and 20 μsec/DIV adjust with the level of the magenta color bar.

8-4-7. Burst Flag Position Adjustment

Measuring equipment : Oscilloscope
Vertical mode : ALT
Trigger channel : ch-2
Trigger slope : Up edge
Trigger coupling : AC
Measuring point ch-1 : TP002 (coupling : AC)
Measuring point ch-2 : TP012 (coupling : AC)

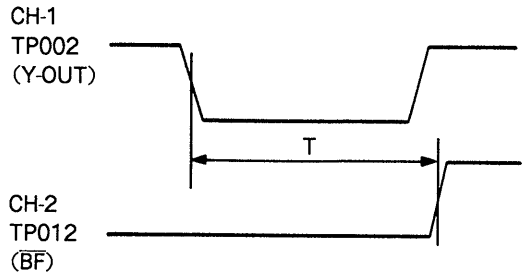


Fig. 8-4-7. TP002, TP012

Specification : T = 5.3 ± 0.05 μsec
Adjustment : RV005

Note : Set oscilloscope to 1 μsec/DIV, 10mV/DIV at ch-1, and 0.5mV/DIV at ch-2.

8-4-8. Hue and Color Adjustment

Measuring equipment : Oscilloscope
Vertical mode : ch-1
Trigger channel : ch-2
Trigger slope : Up edge
Trigger coupling : TV-LINE
Measuring point ch-1 : TP007 (coupling : AC)
Measuring point ch-2 : TP010 (coupling : DC)

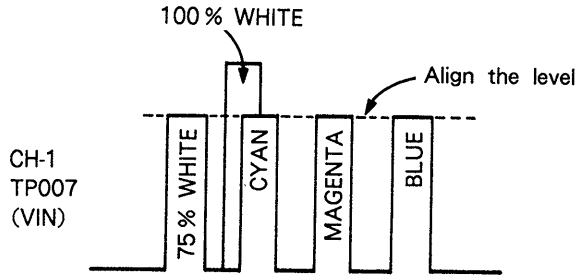


Fig. 8-4-8. TP007

Specification : Refer to Fig. 8-4-8.
Adjustment : RV004, RV007 (alternately adjust)

Note : Set oscilloscope to 20mV/DIV and 20 μsec/DIV.

8-4-9. VCO Adjustment

Measuring equipment : Oscilloscope
Vertical mode : ch-1
Trigger channel : ch-1
Trigger slope : Up edge
Trigger coupling : AC
Measuring point ch-1 : TP022 (coupling : DC)

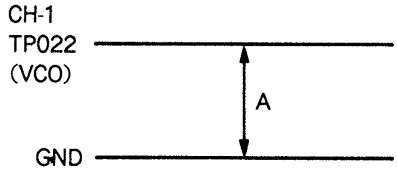


Fig. 8-4-9. TP022

Specification : A = 3.0 ± 0.2V
Adjustment : LV003

8-4-10. Vertical Reset Timing Adjustment

Key operation : Cursor down key, twice
Measuring equipment : Oscilloscope
  Vertical mode : CHOP
  Trigger channel : ch-3
  Trigger slope : Up edge
  Trigger coupling : TV-FLD
Measuring point ch-1 : TP009 (coupling : DC)
Measuring point ch-2 : TP016 (coupling : DC)
Measuring point ch-3 : TP017

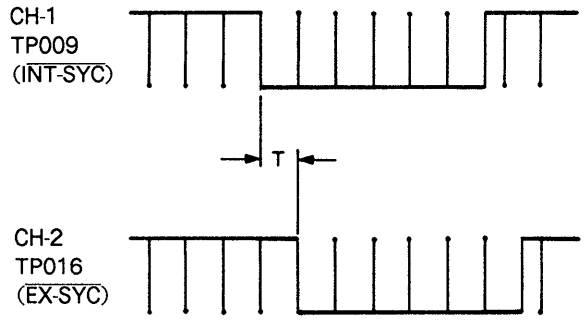


Fig. 8-4-10. TP009, TP016

Specification : T = ± 0.5H
Adjustment : RV010

Note : Set oscilloscope to 50 µsec/DIV.

8-4-11. H Position Adjustment

Measuring equipment : Oscilloscope
  Vertical mode : ALT, Band width limit (20MHz)
  Trigger channel : ch-2
  Trigger slope : Down edge
  Trigger coupling : DC
Measuring point ch-1 : TP002 (coupling : AC)
Measuring point ch-2 : TP010 (coupling : DC)

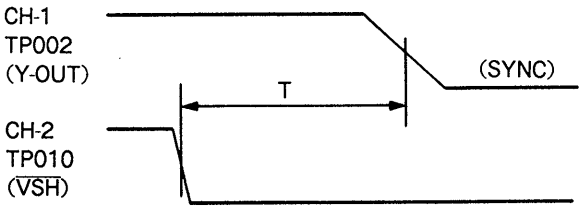


Fig. 8-4-11. TP002, TP010

Specification : T = 700 ± 20nsec
Adjustment : RV009

Note : Set oscilloscope to 20nsec/DIV, 0.1V/DIV at ch-1, and 2V/DIV at ch-2.

8-4-12. Vertical Blanking Adjustment

Measuring equipment : Oscilloscope
  Vertical mode : ch-1
  Trigger channel : ch-1
  Trigger slope : Up edge
  Trigger coupling : DC
Measuring point ch-1 : TP021 (coupling : DC)

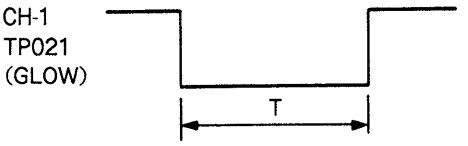


Fig. 8-4-12. TP021

Specification : T = 965 ± 20 µsec
Adjustment : RV011

8-4-13. Setting in After Adjustment

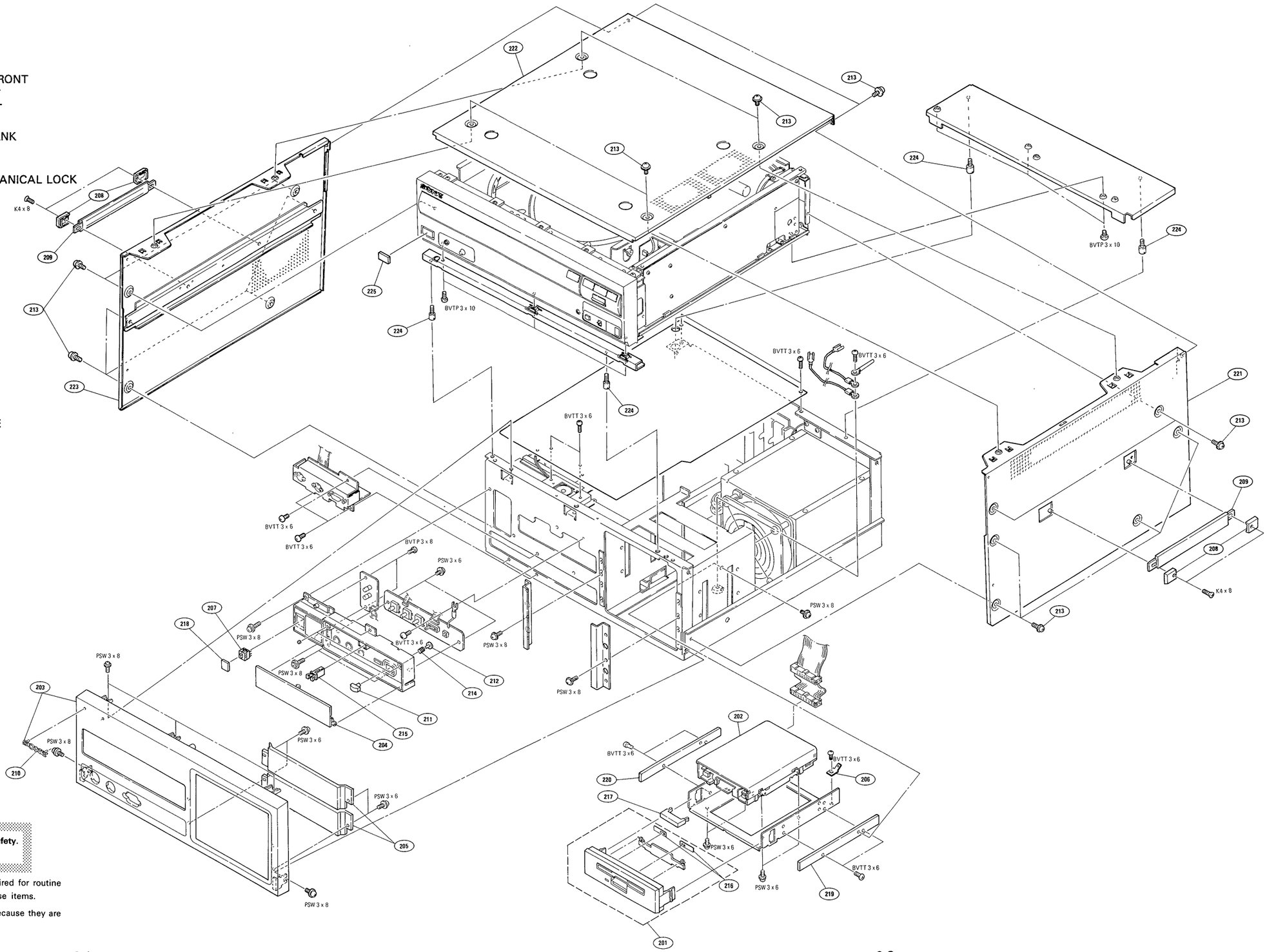
- VGA-16 Board
  SW1 ····· Only No.4 ON
  W1 ····· Connected
  W2 ····· Connected, below
- VS-38A Board
  J001 ····· All 0 side
  J003 ····· 0 side
  SL001 ····· Short by the solder
  SL002 ····· Open
  SL003 ····· Short by the solder
  SL004 ····· Open
  SW001 ····· All ON side

CHAPTER 9
RIPAIR PARTS AND FIXTURES

9-1. MECHANICAL PARTS LIST

9-1-1. Cover Block

No.	Parts No.	Description
201	*A-8040-766-A	PANEL (FD) ASSY, FRONT
202	*A-8040-839-B	MFD-73W-51D ASSY
203	*A-8041-031-A	PANEL ASSY, FRONT
204	X-4611-238-1	DOOR ASSY
205	X-4611-239-1	PANEL ASSY,FD BLANK
206	*1-535-445-11	TERMINAL, FASTEN
207	1-571-091-21	SWITCH, KEY MECHANICAL LOCK
208	*2-253-306-21	TABLE, HANDLE
209	3-419-372-01	HANDLE
210	*3-566-707-21	EMBLEM, SONY
211	3-668-007-02	PUSH BUTTON (5x9)
212	3-668-009-02	PIN, PUSH BUTTON
213	3-675-598-00	SCREW, CASE
214	4-309-349-00	SPRING, COIL
215	4-374-714-01	CATCH, PUSH
216	4-609-222-01	SPRING
217	*4-609-223-31	BUTTON, EJECT
218	*4-612-202-11	BUTTON, PUSH
219	*4-612-293-01	RAIL (RIGHT), FH
220	*4-612-294-01	RAIL (LEFT), FH
221	4-613-022-02	PANEL (RIGHT), SIDE
222	*4-613-024-01	PANEL, TOP
223	4-613-025-01	PANEL (LEFT), SIDE
224	*4-613-061-01	SCREW, VIEW-3015
225	*4-613-834-01	COVER (1500), SW

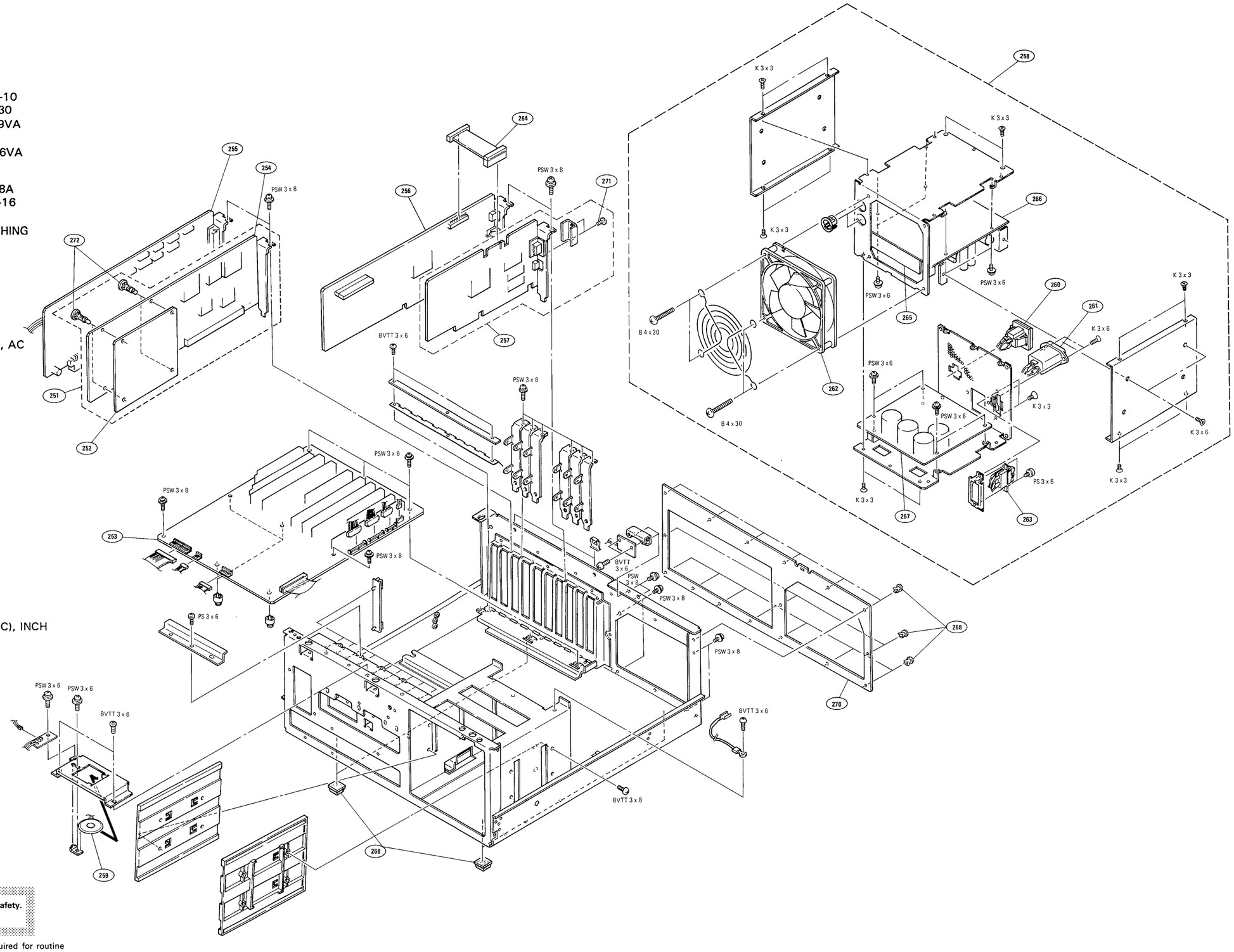


NOTE:

1. **The shaded and ⚠ -marked components are critical to safety. Replace only with same components as specified.**
2. Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.
3. Item with no part number and/or description are not stocked because they are seldom required for routine service.

9-1-2. Computer Chassis Block

No.	Parts No.	Description
251	*A-8041-028-A	PU-59VA ASSY
252	*A-8051-327-A	MOUNTED CB, RAM-10
253	*A-8051-384-A	MOUNTED CB, SY-130
254	*A-8051-442-A	MOUNTED CB, PU-59VA
⚠255	*A-8051-487-A	MOUNTED CB, IF-156VA
256	*A-8051-488-A	MOUNTED CB, VS-38A
257	*A-8080-400-A	MOUNTED CB, VGA-16
⚠258	*1-413-309-11	REGULATOR, SWITCHING (SR-93)
259	1-503-221-00	SPEAKER
⚠260	1-526-986-11	OUTLET, AC
⚠261	1-526-987-11	INLET (WITH FILTER), AC
262	1-541-337-21	FAN
⚠263	1-571-230-11	SWITCH, POWER
264	1-574-371-11	CABLE
⚠265	1-623-761-11	PC BOARD, C
⚠266	1-623-762-11	PC BOARD, B
⚠267	1-623-763-11	PC BOARD, A
268	4-609-442-01	RIVET (U), NYLON
269	4-611-214-01	FOOT, RUBBER
270	*4-612-295-41	COVER, REAR
271	4-615-071-01	SCREW (No.4-40UNC), INCH
272	4-912-181-01	SUPPORT, PC



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9-1-3. Keyboard Block

No.	Parts No.	Description
1		KEYTOP(C4C100) '(SINGLE QUOTES)
2		KEYTOP(C4C100) 1
3		KEYTOP(C4C100) 2
4		KEYTOP(C4C100) 3
5		KEYTOP(C4C100) 4
6		KEYTOP(C4C100) 5
7		KEYTOP(C4C100) 6
8		KEYTOP(C4C100) 7
9		KEYTOP(C4C100) 8
10		KEYTOP(C4C100) 9
11		KEYTOP(C4C100) 0
12		KEYTOP(C4C100) −
13		KEYTOP(C4C100) =
14		KEYTOP(C4C100) \ (BACK SLASH)
15		KEYTOP(C4C100) ←(BACK SPACE)
16		KEYTOP(C4C150) Tab
17		KEYTOP(C4C100) Q
18		KEYTOP(C4C100) W
19		KEYTOP(C4C100) E
20		KEYTOP(C4C100) R
21		KEYTOP(C4C100) T
22		KEYTOP(C4C100) Y
23		KEYTOP(C4C100) U
34		KEYTOP(C4C100) I
25		KEYTOP(C4C100) O
26		KEYTOP(C4C100) P
27		KEYTOP(C4C100) [
28		KEYTOP(C4C100)]
29		KEYTOP(C4CJ175) Caps Lock
30		KEYTOP(C4C100) A
31		KEYTOP(C4C100) S
32		KEYTOP(C4C100) D
33		KEYTOP(C4CH100) F
34		KEYTOP(C4C100) G
35		KEYTOP(C4C100) H
36		KEYTOP(C4CH100) J
37		KEYTOP(C4C100) K
38		KEYTOP(C4C100) L
39		KEYTOP(C4C100) ; (SEMICOLON)
40		KEYTOP(C4C100) '(APOSTROPHE)
41		KEYTOP(C4CCG225) Enter
42		KEYTOP(C4C225) Shift
43		KEYTOP(C4C100) Z
44		KEYTOP(C4C100) X
45		KEYTOP(C4C100) C
46		KEYTOP(C4C100) V
47		KEYTOP(C4C100) B
48		KEYTOP(C4C100) N
49		KEYTOP(C4C100) M
50		KEYTOP(C4C100) , (COMMA)
51		KEYTOP(C4C100) . (PERIOD)
52		KEYTOP(C4C100) / (SLASH)
53		KEYTOP(C4C275) Shift
54		KEYTOP(C4C150) Ctrl
55		KEYTOP(C4C150) Alt
56		KEYTOP(C5CMG700A) (SPACE)
57		KEYTOP(C4C150) Alt
58		KEYTOP(C4C150) Ctrl
59		KEYTOP(C4C100) Insert
60		KEYTOP(C4C100) Home
61		KEYTOP(C4C100) Page Up
62		KEYTOP(C4C100) Delete
63		KEYTOP(C4C100) End
64		KEYTOP(C4C100) Page Down
65		KEYTOP(C4C100) ↑(CURSOR UP)
66		KEYTOP(C4C100) ←(CURSOR LEFT)
67		KEYTOP(C4C100) →(CURSOR DOWN)
68		KEYTOP(C4C100) ↓(CURSOR RIGHT)
69		KEYTOP(C4C100) Num Lock
70		KEYTOP(C4C100) / (SLASH)
71		KEYTOP(C4C100) *(ASTRISK)
72		KEYTOP(C4C100) −
73		KEYTOP(C4C100) 7
74		KEYTOP(C4C100) 8
75		KEYTOP(C4C100) 9
76		KEYTOP(C4CCG100) +
77		KEYTOP(C4C100) 4
78		KEYTOP(C4CH100) 5
79		KEYTOP(C4C100) 6
80		KEYTOP(C4C100) 1
81		KEYTOP(C4C100) 2
82		KEYTOP(C4C100) 3
83		KEYTOP(C4CCG100) Enter
84		KEYTOP(C4C200) 0
85		KEYTOP(C4C100) .
86		KEYTOP(C4C100) Esc
87		KEYTOP(C4C100) F1
88		KEYTOP(C4C100) F2
89		KEYTOP(C4C100) F3
90		KEYTOP(C4C100) F4
91		KEYTOP(C4C100) F5
92		KEYTOP(C4C100) F6
93		KEYTOP(C4C100) F7
94		KEYTOP(C4C100) F8
95		KEYTOP(C4C100) F9
96		KEYTOP(C4C100) F10
97		KEYTOP(C4C100) F11
98		KEYTOP(C4C100) F12
99		KEYTOP(C4C100) Print Screen
100		KEYTOP(C4C100) Scroll Lock
101		KEYTOP(C4C100) Pause

No.	Parts No.	Description
150		CASE, LOWER
151		CASE, UPPER
152		FOOT
153		FOOT, RUBER
154		LALEL, LED
155		COAD, CURL
156		LED-R ASSY
157		CONTACT ASSY
158		CONTACT ASSY, for SPACE KEY
159		CLICK RUBER
160		CLICK RUBER, for SPACE KEY
161		SPRING, COIL
162		LINK
163		LINK
164		LINK
165		LINK
166		MEMBRANE BOARD
167		SCREW, 2×6
168		SCREW, 3×10
170	*1-466-050-11	KEYBOARD ASSY

NOTE:

1. **The shaded and ⚠ -marked components are critical to safety. Replace only with same components as specified.**
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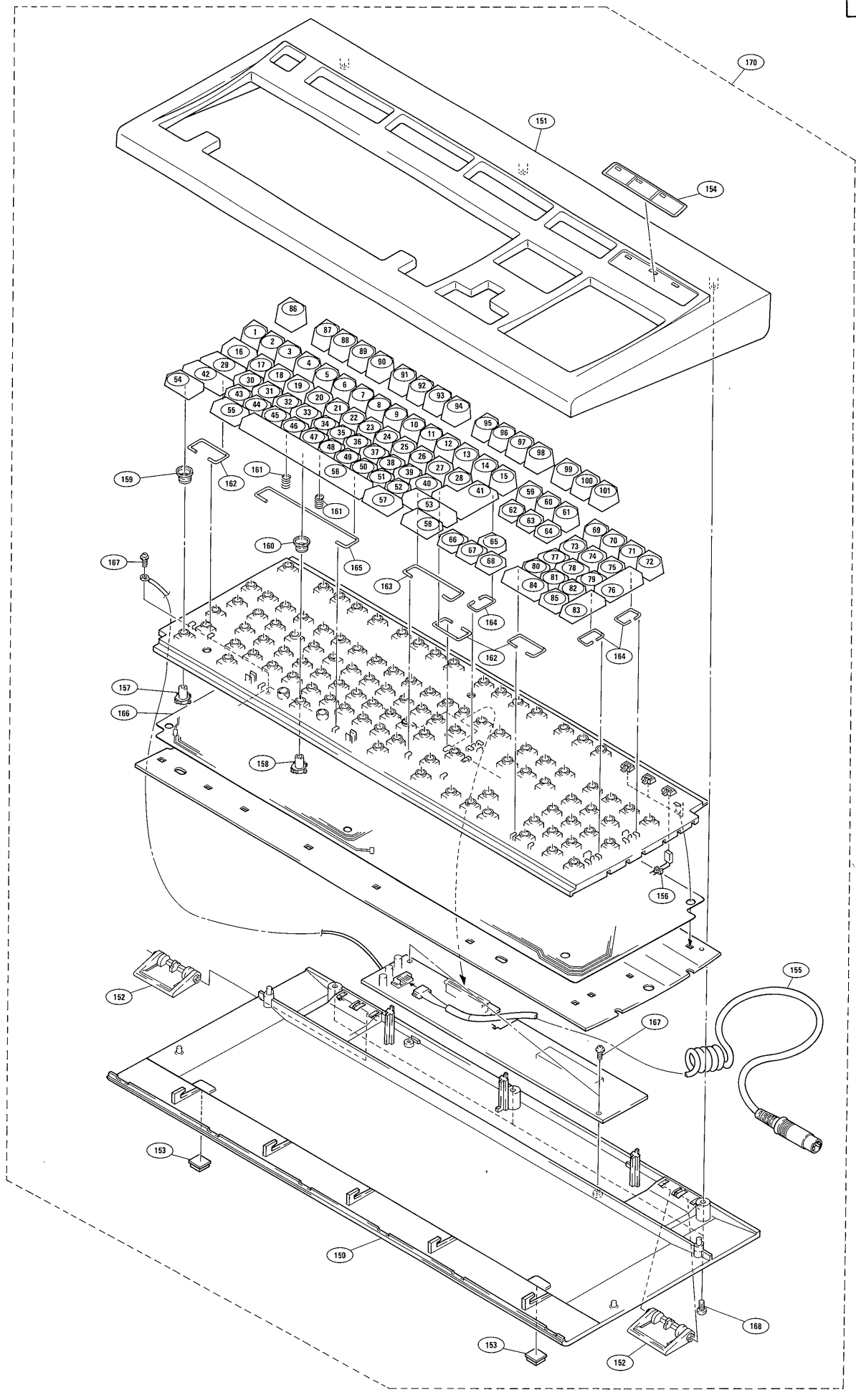
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9-2. ELECTRICAL PARTS LIST

9-2-1. CP-110 Board

Ref.No.	Parts No.	Description
	* 1-622-756-11	PRINTED CB, CP-110
C201	1-123-306-00	ELECT 47 20% 10V
C202	1-162-851-11	CERAMIC 0.1 20% 16V
CN201,202	1-563-496-12	DIN 5P
⚠F201	1-532-783-21	MICRO (SECONDARY)
TH201,202	1-202-850-00	THERMISTOR (POSITIVE)
W201	* 1-939-256-11	HARNESS (SY-CP)
W202	* 1-939-257-11	HARNESS (CP-CP)

9-2-2. CP-116 Board

Ref.No.	Parts No.	Description
	* 1-622-755-11	PRINTED CB, CP-116
CN203	1-506-959-11	D-SUB (MOUNT TYPE) 9P

9-2-3. IF156VA Board

Ref.No.	Parts No.	Description
⚠	* A-8051-487-A	MOUNTED CB, IF-156VA
	* 1-526-972-11	SOCKET, IC 40P (IC222)
C201	1-123-380-00	ELECT 1 20% 50V
C205-208	1-162-851-11	CERAMIC 0.1 20% 16V
C209	1-123-332-00	ELECT 47 20% 16V
C210	1-126-101-11	ELECT 100 20% 6.3V
C211	1-123-321-00	ELECT 220 20% 16V
C212	1-161-047-00	CERAMIC 0.0047 10% 25V
C213	1-161-021-11	CERAMIC 0.047 10% 25V
C214	1-123-380-00	ELECT 1 20% 50V
C215	1-162-851-11	CERAMIC 0.1 20% 16V
C216	1-124-463-00	ELECT 0.1 20% 50V
C217	1-161-051-00	CERAMIC 0.01 10% 25V
C218-220	1-162-851-11	CERAMIC 0.1 20% 16V
C221	1-161-051-00	CERAMIC 0.01 10% 25V
C222-224	1-162-851-11	CERAMIC 0.1 20% 16V
C255,226	1-102-973-00	CERAMIC 100pF 5% 50V
C227,228	1-162-851-11	CERAMIC 0.1 20% 16V
C229	1-123-356-00	ELECT 10 20% 16V
C230,231	1-162-851-11	CERAMIC 0.1 20% 16V
C232	1-161-051-00	CERAMIC 0.01 10% 25V
C233, 234	1-101-880-00	CERAMIC 47pF 5% 50V
C235	1-124-471-00	ELECT 1000 20% 6.3V
C236	1-123-356-00	ELECT 10 20% 16V
C237	1-162-851-11	CERAMIC 0.1 20% 16V
C238	1-161-048-00	CERAMIC 0.0056 10% 25V
C239,240	1-102-963-00	CERAMIC 33pF 5% 50V
C241	1-162-851-11	CERAMIC 0.1 20% 16V
C242	1-123-332-00	ELECT 47 20% 16V
C243-245, 247-249	1-162-851-11	CERAMIC 0.1 20% 16V
C250	1-102-973-00	CERAMIC 100pF 5% 50V
C251	1-123-321-00	ELECT 220 20% 16V
C252	1-123-356-00	ELECT 10 20% 16V
C253,C254	1-162-851-11	CERAMIC 0.1 20% 16V
C255	1-123-356-00	ELECT 10 20% 16V
C256	1-162-851-11	CERAMIC 0.1 20% 16V
C257	1-102-973-00	CERAMIC 100pF 5% 50V
C258,259	1-162-851-11	CERAMIC 0.1 20% 16V
C260,261	1-102-953-00	CERAMIC 18pF 5% 50V
C262-266	1-162-851-11	CERAMIC 0.1 20% 16V
C267-275	1-161-055-00	CERAMIC 0.022 10% 25V
C276-279	1-162-851-11	CERAMIC 0.1 20% 16V

NOTE:

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Ref.No.	Parts No.	Description
C280	1-123-332-00	ELECT 47 20% 16V
C281,282	1-123-380-00	ELECT 1 20% 50V
C283	1-161-051-00	CERAMIC 0.01 10% 25V
C284	1-162-851-11	CERAMIC 0.1 20% 16V
C285	1-102-074-00	CERAMIC 0.001 10% 50V
C300	1-123-381-00	ELECT 2.2 20% 50V
CN201	1-563-142-11	D-SUB (MOUNT TYPE) 25P
CN202	1-506-959-11	D-SUB (MOUNT TYPE) 9P
CN203	*1-566-580-11	MULTI 64P
CN204	1-563-456-11	MULTI 90P
CV201	1-141-245-00	TRIMMER, CERAMIC
D201,202	8-719-911-19	1SS119
D203	8-719-422-21	1T22A
D204,205	8-719-911-19	1SS119
FB201,202	1-543-236-11	BEAD, FERRITE
IC201	8-759-903-86	LM386N
IC202	8-759-918-68	INS8250AN
IC203	8-759-901-25	SN74LS125AN
IC204	8-759-902-44	SN74LS244N
IC206	8-759-904-18	SN74ALS00AN
IC207	8-759-145-58	μPC4558C
IC208	8-759-900-14	SN74LS14N
IC209	8-759-917-71	74F243PC
IC210	8-759-904-26	SN74ALS08N
IC211	8-759-904-38	SN74ALS32N
IC212,213	8-759-951-89	SN75189AN
IC214	8-759-951-88	SN75188N
IC215	8-759-900-02	SN74LS02N
IC216	8-759-900-04	SN74LS04N
IC217	8-759-974-07	SN7407N
IC218	8-759-900-04	SN74LS04N
IC219	8-759-946-64	SN74ALS04BN
IC220	8-759-909-59	SN76489AN
IC221	8-759-202-11	TC74HC00P
IC222	8-759-781-93	D8742-IF156K0002
IC223	8-759-918-68	INS8250AN
IC224	8-759-903-73	SN74LS373N
IC225	8-759-012-88	MC146818P
IC226	8-759-940-95	P8254
IC227	8-759-001-00	MC74HC132N

Ref.No.	Parts No.	Description
IC228	8-759-908-71	SN74ALS244AN
IC229	8-759-951-88	SN75188N
IC230	8-759-951-89	SN75189AN
IC231	8-759-945-78	SN74ALS11AN
IC232	8-759-904-38	SN74ALS32N
IC233	8-759-112-60	μPD65005G-095-12
IC234	8-759-901-25	SN74LS125AN
IC235	8-759-901-55	SN74LS155N
IC236	8-759-901-74	SN74LS174N
IC237	8-759-974-05	SN7405N
IC238	8-759-900-04	SN74LS04N
IC239	8-759-903-74	SN74LS374N
IC240	8-759-902-44	SN74LS244N
IC241	8-759-902-40	SN74LS240N
IC242	8-759-912-21	SN74ALS245AN
JP201R	1-562-579-21	RECEPTACLE, CONNECTOR
JP201P	*1-564-952-21	PIN, CONNECTOR 4P
Q201,202	8-729-119-78	2SC2785
Q203	8-729-204-83	2SA1048-GR
Q204,205	8-729-119-78	2SC2785
R201	1-249-437-11	CARBON 47K 5% 1/4W
R202	1-249-405-11	CARBON 100 5% 1/4W
R203	1-249-437-11	CARBON 47K 5% 1/4W
R204	1-249-427-11	CARBON 6.8K 5% 1/4W
R205	1-247-862-11	CARBON 20K 5% 1/4W
R206	1-249-427-11	CARBON 6.8K 5% 1/4W
R207	1-249-393-11	CARBON 10 5% 1/4W
R209	1-249-405-11	CARBON 100 5% 1/4W
R210,212	1-249-429-11	CARBON 10K 5% 1/4W
R213	1-249-399-11	CARBON 33 5% 1/4W
R214	1-249-429-11	CARBON 10K 5% 1/4W
R215,216	1-249-425-11	CARBON 4.7K 5% 1/4W
R217,218	1-249-429-11	CARBON 10K 5% 1/4W
R219	1-249-426-11	CARBON 5.6K 5% 1/4W
R220,221	1-249-429-11	CARBON 10K 5% 1/4W
⚠R222	1-212-849-00	FUSIBLE 4.7 5% 1/4W
R223	1-249-425-11	CARBON 4.7K 5% 1/4W
R224,225	1-249-429-11	CARBON 10K 5% 1/4W
R226	1-249-393-11	CARBON 10 5% 1/4W
R227	1-249-421-11	CARBON 2.2K 5% 1/4W

NOTE:

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   Replace only with same components as specified.

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Ref.No.	Parts No.	Description
R228	1-249-425-11	CARBON 4.7K 5% 1/4W
R229	1-249-429-11	CARBON 10K 5% 1/4W
R230	1-247-838-00	CARBON 2K 5% 1/4W
R231,232	1-249-429-11	CARBON 10K 5% 1/4W
R233	1-247-872-11	CARBON 51K 5% 1/4W
R234	1-249-417-11	CARBON 1K 5% 1/4W
R235	1-202-473-00	SOLID 5.6M 20% 1/4W
R236	1-247-883-00	CARBON 150K 5% 1/4W
R237	1-249-429-11	CARBON 10K 5% 1/4W
R238	1-249-417-11	CARBON 1K 5% 1/4W
⚠R239	1-212-857-00	FUSIBLE 10 5% 1/4W
R240,241	1-249-425-11	CARBON 4.7K 5% 1/4W
R242	1-249-429-11	CARBON 10K 5% 1/4W
R243	1-249-398-11	CARBON 27 5% 1/4W
R244	1-249-421-11	CARBON 2.2K 5% 1/4W
R245-252	1-249-398-11	CARBON 27 5% 1/4W
R253	1-249-425-11	CARBON 4.7K 5% 1/4W
R254	1-249-417-11	CARBON 1K 5% 1/4W
R255	1-249-437-11	CARBON 47K 5% 1/4W
R256,257	1-249-429-11	CARBON 10K 5% 1/4W
R258	1-247-818-11	CARBON 300 5% 1/4W
RB201	1-235-351-11	BLOCK 2.2Kx4
RB202	1-235-355-11	BLOCK 10Kx4
RB203	1-235-353-11	BLOCK 4.7Kx4
RB205	1-235-351-11	BLOCK 2.2Kx4
RB206	1-235-353-11	BLOCK 4.7Kx4
RB207	1-235-195-00	BLOCK 10Kx8
SW201	1-571-020-21	DIP
X201	1-567-098-00	VIBRATOR, CRYSTAL
X202	1-567-883-11	VIBRATOR, CRYSTAL

Ref.No.	Parts No.	Description

9-2-4. Keyboard

	1-101-884-00	CAP, CERAMIC 56pF 5% 50V
	1-102-985-00	CAP, CERAMIC 20pF 5% 50V
	1-123-356-00	CAP, ELECT 10 20% 16V
	1-123-381-00	CAP, ELECT 2.2 20% 50V
	1-162-851-11	CAP, CERAMIC 0.1 20% 16V
	1-235-335-11	RES, BLOCK 6.8K×8
	1-247-705-11	RES, CARBON 270 5% 1/4W
	1-247-138-00	RES, CARBON 2K 5% 1/4W
	1-247-156-00	RES, CARBON 11K 5% 1/4W
	1-247-176-00	RES, CARBON 75K 5% 1/4W
*	1-564-521-11	PLUG, CONNECTOR 6P
	1-567-505-11	VIBRATOR, CRYSTAL
	8-719-911-19	DIODE 1SS119
	8-759-901-12	IC SN74LS125AN
	8-759-914-03	IC SN74LS06N

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Ref.No.	Parts No.	Description
9-2-5. PU-59VA Board		
	A-8041-029-A	PU-59VA ROM ASSY (IC314, 315)
	* A-8051-442-A	MOUNTED CB, PU-59VA
	1-526-962-11	SOCKET, IC 68P (IC318,319,320,322)
	1-526-963-11	SOCKET, IC 84P (IC323)
	* 1-526-971-11	SOCKET, IC 28P (IC314,315)
	* 1-526-972-11	SOCKET, IC 40P (IC313)
	* 1-564-952-21	PIN, CONNECTOR 8P
C301-317	1-162-179-11	CERAMIC 0.1 25V
C318	1-161-021-11	CERAMIC 0.047 10% 25V
C319	1-123-332-00	ELECT 47 20% 16V
C320-324	1-162-179-11	CERAMIC 0.1 25V
C325	1-102-961-00	CERAMIC 27pF 5% 50V
C326	1-102-960-00	CERAMIC 24pF 5% 50V
C328	1-102-963-00	CERAMIC 33pF 5% 50V
C329, 330	1-162-179-11	CERAMIC 0.1 25V
C331	1-123-332-00	ELECT 47 20% 16V
C332	1-162-179-11	CERAMIC 0.1 25V
CN301	* 1-506-950-11	PIN, 50P
CN302	* 1-566-579-11	MULTI 50P
CN303	1-563-456-11	MULTI 90P
CV301	1-141-245-00	TRIMMER, CERAMIC
DL301	1-415-571-11	DELAY LINE, PULSE
IC301	8-759-904-82	74F10PC
IC302	8-759-002-00	MC74F153N
IC304	8-759-901-25	SN74LS125AN
IC305,306	8-759-946-37	SN74ALS573BN
IC307	8-759-904-79	74F00PC
IC308	8-759-904-80	74F04PC
IC309	8-759-931-97	P82C202
IC310,311	8-759-940-97	P8237A-5
IC312	8-759-604-53	M60005-0223FP
IC316,317	8-759-940-93	P8259A

Ref.No.	Parts No.	Description
IC318	8-759-948-56	N80286-8
IC319	8-759-932-01	P82A205
IC320	8-759-931-99	P82A204
IC321	8-759-912-21	SN74ALS245AN
IC322	8-759-931-98	P82A203
IC323	8-759-931-96	P82C201
IC324	8-759-901-32	SN74LS132N
IC325	8-759-908-71	SN74ALS244AN
R301-304	1-249-429-11	CARBON 10K 5% 1/4W
R305	1-249-419-11	CARBON 1.5K 5% 1/4W
R306,307	1-249-429-11	CARBON 10K 5% 1/4W
R308	1-247-903-00	CARBON 1M 5% 1/4W
R309	1-249-412-11	CARBON 390 5% 1/4W
R310	1-247-903-00	CARBON 1M 5% 1/4W
R311	1-249-412-11	CARBON 390 5% 1/4W
R312	1-249-429-11	CARBON 10K 5% 1/4W
R314	1-249-418-11	CARBON 1.2K 5% 1/4W
R315-318	1-249-429-11	CARBON 10K 5% 1/4W
R319	1-249-417-11	CARBON 1K 5% 1/4W
R320	1-249-425-11	CARBON 4.7K 5% 1/4W
R321-327	1-249-393-11	CARBON 10 5% 1/4W
R328	1-249-429-11	CARBON 10K 5% 1/4W
R331	1-249-419-11	CARBON 1.5K 5% 1/4W
R332	1-249-417-11	CARBON 1K 5% 1/4W
RB301,302	1-235-195-00	BLOCK 10Kx8
RB303	1-235-355-11	BLOCK 10Kx4
RB304	1-235-195-00	BLOCK 10Kx8
RB305	1-235-355-11	BLOCK 10Kx4
RB306	1-235-452-11	BLOCK 330x4
SW301	1-554-222-00	SLIDE
X301	1-567-881-11	VIBRATOR, CRYSTAL
X302	1-567-878-11	VIBRATOR, CRYSTAL

9-2-5-1. PU-59VA ROM ASSY

IC314	8-759-781-94	D27512J-PU59V40E03
IC315	8-759-781-95	D27512J-PU59V40003

NOTE:

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9-2-6. RAM-10 Board

Ref.No.	Parts No.	Description
	*A-8051-327-A	MOUNTED CB, RAM-10
C401-404	1-162-179-11	CERAMIC 0.1 25V
C405	1-124-589-11	ELECT 47 20% 16V
C406-428,430-434	1-162-179-11	CERAMIC 0.1 25V
CN401	*1-563-441-11	HOUSING, 50P
IC401	8-759-001-87	MC74F20N
IC402	8-759-904-82	74F10PC
IC403,404	8-759-303-05	HM50256P-12
IC405,406	8-759-922-42	MB81464-12
IC407-422	8-759-303-05	HM50256P-12
IC423	8-759-001-87	MC74F20N
IC424	8-759-904-81	74F08PC
IC425,426	8-759-303-05	HM50256P-12
IC427,428	8-759-922-42	MB81464-12
R401-417	1-249-399-11	CARBON 33 5% 1/4W
R418	1-249-417-11	CARBON 1K 5% 1/4W

9-2-7. SP-11 Board

Ref.No.	Parts No.	Description
	*1-629-661-11	PRINTED CB, SP-11
CN1	*1-506-481-11	PIN, 2P

9-2-8. SW-198 Board

Ref.No.	Parts No.	Description
	*1-622-753-11	PRINTED CB, SW-198
D001	8-719-811-44	TLG114A
D002	8-719-941-46	GL-5HY41
R001	1-247-702-11	CARBON 150 5% 1/4W
W001	*1-939-253-11	HARNESS (SW-SY)

9-2-9. SW-277 Board

Ref.No.	Parts No.	Description
	*1-625-325-11	PRINTED CB, SW-277
S001	1-554-482-00	SLIDE
W001	*1-940-371-11	HARNESS (BUS-SW)

9-2-10. SY-130 Board

Ref.No.	Parts No.	Description
	*A-8051-384-A	MOUNTED CB, SY-130
	*3-646-222-00	GUIDE, SLIDE
BAT101	1-528-202-11	BATTERY, NICKEL CADMIUM
C101,102	1-102-953-00	CERAMIC 18pF 5% 50V
C103,104	1-102-959-00	CERAMIC 22pF 5% 50V
C105	1-102-947-00	CERAMIC 10pF 0.5PF 50V
C106	1-123-356-00	ELECT 10 20% 16V
C107	1-130-474-00	MYLAR 0.0018 5% 50V

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Ref.No.	Parts No.	Description
C108	1-102-963-00	CERAMIC 33pF 5% 50V
C109	1-102-816-00	CERAMIC 120pF 5% 50V
C110	1-130-487-00	MYLAR 0.022 5% 50V
C111	1-161-485-00	CERAMIC 0.1 50V
C112,114	1-123-356-00	ELECT 10 20% 16V
C115	1-161-051-00	CERAMIC 0.01 10% 25V
C117,118	1-123-332-00	ELECT 47 20% 16V
C119-122	1-123-333-00	ELECT 100 20% 16V
C123	1-124-584-00	ELECT 100 20% 10V
C124	1-123-333-00	ELECT 100 20% 16V
C126-141	1-161-485-00	CERAMIC 0.1 50V
CN001	*1-564-423-11	HEADER, SPRING (POWER) 6P
CN002	1-564-422-11	HEADER, SPRING (POWER) 5P
CN003	*1-564-420-11	HEADER, SPRING (POWER) 3P
CN011	1-939-258-11	HARNESS, FDD
CN012	*1-506-484-11	PIN, 5P
CN013	*1-506-488-11	PIN, 9P
CN015	*1-506-467-11	PIN, 2P
CN016	*1-506-469-11	PIN, 4P
CN017	*1-506-494-11	PIN, 15P
CN101	*1-566-582-11	RECEPTACLE, MULTI 64P
CN102	1-563-460-11	RECEPTACLE, MULTI 90P
CN103,104	1-563-427-11	SOCKET
CN105	1-563-422-11	SOCKET 62P
CN106-108	1-563-427-11	SOCKET
CN109	1-563-422-11	SOCKET 62P
CN110	1-563-427-11	SOCKET
CN111	1-563-460-11	RECEPTACLE, MULTI 90P
CN112	*1-566-581-11	RECEPTACLE, MULTI 50P
CN121-123	1-563-335-11	HOUSING, (DIP) 48P
IC001	8-759-902-92	SN74LS541N
IC002	8-759-902-45	SN74LS245N
IC003	8-759-113-37	μPD65005G-126-12
IC004	8-759-109-87	μPD72065C
IC005	8-759-113-40	μPD71066CT
IC006	8-759-974-07	SN7407N
IC007	8-759-974-06	SN7406N
IC008	8-759-900-14	SN74LS14N
IC009	8-759-901-25	SN74LS125AN
IC010	8-759-915-41	74F02PC
IC011-013	8-759-904-83	74F32PC
IC014	8-759-900-32	SN74LS32N

Ref.No.	Parts No.	Description
R101	1-249-415-11	CARBON 680 5% 1/4W
R103,104	1-249-421-11	CARBON 2.2K 5% 1/4W
R105	1-249-405-11	CARBON 100 5% 1/4W
R106	1-247-842-11	CARBON 3K 5% 1/4W
R107	1-249-417-11	CARBON 1K 5% 1/4W
R108	1-249-425-11	CARBON 4.7K 5% 1/4W
R109	1-247-866-11	CARBON 30K 5% 1/4W
R110	1-249-429-11	CARBON 10K 5% 1/4W
R111	1-249-414-11	CARBON 560 5% 1/4W
RB001	1-231-399-00	BLOCK 330x8
X001	1-567-881-11	VIBRATOR, CRYSTAL
X002	1-567-880-11	VIBRATOR, CRYSTAL

9-2-11. VGA-16 Board

	*A-8041-400-A	MOUNTED CB, VGA-16

9-2-12. VR-60 Board

	*1-622-754-11	PRINTED CB, VR-60
R101	1-249-421-11	CARBON 2.2K 5% 1/4W
R102	1-249-419-11	CARBON 1.5K 5% 1/4W
RV101,102	1-237-725-11	VAR, CARBON 10K
RV103	1-237-726-11	VAR, CARBON 10K
S101	1-554-482-21	SLIDE
S102	1-554-174-00	KEY
W101	*1-939-254-11	HARNESS (VR-VS)
W102	*1-939-255-11	HARNESS (VR-SY)

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9-2-13. VS-38A Board

Ref.No.	Parts No.	Description
⚠	*A-8051-488-A	MOUNTED CB, VS-38A
	*1-564-948-11	PIN, CONNECTOR 3P
	*1-943-013-11	HARNESS (VIDEO)
C001	1-124-584-00	ELECT 100 20% 10V
C002	1-124-438-00	ELECT 1 20% 50V
C004	1-102-959-00	CERAMIC 22pF 5% 50V
C005	1-102-971-00	CERAMIC 82pF 5% 50V
C006	1-101-361-00	CERAMIC 150pF 5% 50V
C007	1-101-884-00	CERAMIC 56pF 5% 50V
C008,009	1-124-589-11	ELECT 47 20% 16V
C010	1-161-374-11	CERAMIC 0.0015 20% 16V
C012	1-101-081-00	CERAMIC 130pF 5% 50V
C013	1-102-976-00	CERAMIC 180pF 5% 50V
C014	1-124-589-11	ELECT 47 20% 16V
C015	1-124-438-00	ELECT 1 20% 50V
C016	1-161-379-00	CERAMIC 0.01 20% 16V
C017	1-124-589-11	ELECT 47 20% 16V
C018	1-124-438-00	ELECT 1 20% 50V
C019	1-126-157-11	ELECT 10 20% 16V
C020	1-124-589-11	ELECT 47 20% 16V
C021	1-164-159-11	CERAMIC 0.1 50V
C022,023	1-161-379-00	CERAMIC 0.01 20% 16V
C024	1-124-589-11	ELECT 47 20% 16V
C025,026	1-136-161-00	FILM 0.047 5% 50V
C027	1-164-159-11	CERAMIC 0.1 50V
C028	1-124-465-00	ELECT 0.47 20% 50V
C029	1-164-159-11	CERAMIC 0.1 50V
C030	1-124-589-11	ELECT 47 20% 16V
C032	1-161-379-00	CERAMIC 0.01 20% 16V
C034	1-162-286-31	CERAMIC 220pF 10% 50V
C035	1-126-157-11	ELECT 10 20% 16V
C037	1-130-728-00	FILM 0.0022 5% 50V
C038	1-108-798-11	MYLAR 0.0033 5% 50V
C039	1-136-161-00	FILM 0.047 5% 50V
C042	1-126-157-11	ELECT 10 20% 16V
C043	1-164-159-11	CERAMIC 0.1 50V
C044	1-124-589-11	ELECT 47 20% 16V
C045	1-124-584-00	ELECT 100 20% 10V
C046	1-164-159-11	CERAMIC 0.1 50V
C047	1-161-379-00	CERAMIC 0.01 20% 16V
C048	1-164-159-11	CERAMIC 0.1 50V
C049	1-162-207-31	CERAMIC 22pF 5% 50V
C050	1-162-205-31	CERAMIC 18pF 5% 50V
C051	1-124-438-00	ELECT 1 20% 50V
C052-054	1-164-159-11	CERAMIC 0.1 50V
C055	1-126-157-11	ELECT 10 20% 16V
C056,057	1-164-159-11	CERAMIC 0.1 50V
C058	1-126-157-11	ELECT 10 20% 16V
C059-062	1-164-159-11	CERAMIC 0.1 50V
C063	1-126-157-11	ELECT 10 20% 16V
C064-068	1-164-159-11	CERAMIC 0.1 50V
C069	1-124-438-00	ELECT 1 20% 50V
C070	1-164-159-11	CERAMIC 0.1 50V
C071,072	1-124-438-00	ELECT 1 20% 50V
C073-075	1-164-159-11	CERAMIC 0.1 50V
C076	1-161-379-00	CERAMIC 0.01 20% 16V
C077	1-124-589-11	ELECT 47 20% 16V
C078,079	1-164-159-11	CERAMIC 0.1 50V
C080	1-126-157-11	ELECT 10 20% 16V
C081	1-162-291-31	CERAMIC 560pF 10% 50V
C082	1-162-286-31	CERAMIC 220pF 10% 50V
C083	1-126-157-11	ELECT 10 20% 16V
C084	1-162-207-31	CERAMIC 22pF 5% 50V
C086	1-164-159-11	CERAMIC 0.1 50V
C088	1-161-379-00	CERAMIC 0.01 20% 16V
C089	1-164-159-11	CERAMIC 0.1 50V
C090	1-162-294-31	CERAMIC 0.001 10% 50V
C091	1-130-471-00	MYLAR 0.001 5% 50V
C092	1-162-207-31	CERAMIC 22pF 5% 50V
C093	1-124-589-11	ELECT 47 20% 16V
C094	1-164-159-11	CERAMIC 0.1 50V
C095	1-136-167-00	FILM 0.15 5% 50V
C096	1-164-159-11	CERAMIC 0.1 50V
C097	1-126-157-11	ELECT 10 20% 16V
C098	1-164-159-11	CERAMIC 0.1 50V
C099,100	1-162-294-31	CERAMIC 0.001 10% 50V
C101	1-130-471-00	MYLAR 0.001 5% 50V
C102	1-164-159-11	CERAMIC 0.1 50V
C103	1-161-374-11	CERAMIC 0.0015 20% 16V
C104-108	1-164-159-11	CERAMIC 0.1 50V
C109	1-124-589-11	ELECT 47 20% 16V
C110,111	1-164-159-11	CERAMIC 0.1 50V
C112	1-124-589-11	ELECT 47 20% 16V
C113	1-124-438-00	ELECT 1 20% 50V
C114-116	1-164-159-11	CERAMIC 0.1 50V
C117	1-126-157-11	ELECT 10 20% 16V
C118,119	1-164-159-11	CERAMIC 0.1 50V
C120	1-124-589-11	ELECT 47 20% 16V
C121	1-124-438-00	ELECT 1 20% 50V
C122-124	1-164-159-11	CERAMIC 0.1 50V
C125	1-124-589-11	ELECT 47 20% 16V
C126	1-164-159-11	CERAMIC 0.1 50V
C127	1-124-438-00	ELECT 1 20% 50V

NOTE:

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   Replace only with same components as specified.

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Ref.No.	Parts No.	Description
C128-131	1-164-159-11	CERAMIC 0.1 50V
C132	1-136-173-00	FILM 0.47 5% 50V
C133	1-162-217-31	CERAMIC 56pF 5% 50V
C134	1-126-157-11	ELECT 10 20% 16V
C135	1-164-159-11	CERAMIC 0.1 50V
C137	1-126-157-11	ELECT 10 20% 16V
C138	1-101-361-00	CERAMIC 150pF 5% 50V
C139,140	1-162-291-31	CERAMIC 560pF 10% 50V
C141,142	1-164-159-11	CERAMIC 0.1 50V
C143-145	1-124-589-11	ELECT 47 20% 16V
C146	1-126-157-11	ELECT 10 20% 16V
C147	1-136-173-00	FILM 0.47 5% 50V
C148	1-130-476-00	MYLAR 0.0027 5% 50V
C149,150	1-164-159-11	CERAMIC 0.1 50V
C152	1-164-159-11	CERAMIC 0.1 50V
C153	1-136-157-00	FILM 0.022 5% 50V
C155	1-136-156-00	FILM 0.018 5% 50V
C156	1-131-342-00	TANTALUM 0.15 10% 35V
C157	1-164-159-11	CERAMIC 0.1 50V
C159-161	1-164-159-11	CERAMIC 0.1 50V
C162	1-126-157-11	ELECT 10 20% 16V
C163	1-124-589-11	ELECT 47 20% 16V
C164	1-164-159-11	CERAMIC 0.1 50V
C165	1-101-882-00	CERAMIC 51pF 5% 50V
C167	1-131-365-00	TANTALUM 10 10% 16V
C168	1-162-285-31	CERAMIC 180pF 10% 50V
C169	1-101-361-00	CERAMIC 150pF 5% 50V
C171	1-162-286-31	CERAMIC 220pF 10% 50V
CN001	1-568-126-11	D-SUB 15P
CN002	* 1-561-029-00	26P
CN003,004	1-507-940-21	JACK, AV
D001,002	8-719-911-19	1SS119
D008-010	8-719-911-19	1SS119
D011,012	8-713-300-88	1T33C-01
D013-021	8-719-911-19	1SS119
DL001	1-415-356-11	DELAY LINE, 1H
DL002	1-415-251-00	DELAY LINE
FB001-005	1-410-396-41	FERRITE BEAD INDUCTOR 0.45

Ref.No.	Parts No.	Description
IC001	8-759-800-11	LA7801
IC002	8-752-030-75	V7020
IC003	8-759-135-80	μPC358C
IC004	8-759-202-11	TC74HC00P
IC005	8-759-916-20	SN74HC14N
IC006	8-759-202-86	TC74HC123P
IC007-009	8-752-328-69	CXD1172P
IC010	8-759-103-93	μPC393C
IC011	8-752-321-16	CXD1030M
IC012	8-759-278-09	TA78L009AP
IC013	8-759-202-86	TC74HC123P
IC014-016	8-759-144-70	μPD42102C-3
IC017,018	8-759-203-08	TC74HC221P
IC019	8-759-916-29	SN74HC74N
IC020	8-759-901-44	74F240PC
IC021	8-759-143-59	μPD65013S-526
IC022-024	8-759-231-68	TMM2018AP-25
IC025	8-759-135-80	μPC358C
IC026-028	8-759-143-58	μPD6902C
IC029	8-759-904-38	SN74ALS32N
IC030	8-759-902-92	SN74LS541N
IC031,032	8-759-917-70	74F241PC
IC033	8-759-143-57	μPD65006GF-325-3B8
IC034	8-759-918-71	CX23065
IC035	8-759-234-07	TC74AC00P
IC036	8-759-902-92	SN74LS541N
IC037	8-759-902-45	SN74LS245N
IC038	8-759-700-11	NJM78M05A
IC039	8-759-135-80	μPC358C
IC040	8-759-231-66	TC74HC4053AP
IC041	8-759-982-21	RC78L05A
IC042	8-759-906-01	TL601CP
IC043	8-759-202-86	TC74HC123P
L001,002	1-410-473-11	18
L003	1-408-411-00	15
L004	1-410-473-11	18
L005-013	1-408-417-00	47
L014	1-408-429-00	470
L015	1-410-670-31	39
L016	1-408-429-00	470
LV001	1-408-513-00	COIL (VARIABLE)
LV002	1-235-161-00	FILTER, BAND PASS
LV003	1-459-940-11	COIL (VARIABLE)

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Ref.No.	Parts No.	Description
Q001-003	8-729-119-78	2SC2785
Q004	8-729-173-38	2SA733-K
Q005,006	8-729-119-78	2SC2785
Q007	8-729-173-38	2SA733-K
Q008-013	8-729-119-78	2SC2785
Q015,018	8-729-119-78	2SC2785
Q020	8-729-119-78	2SC2785
Q021	8-729-173-38	2SA733-K
Q022	8-729-119-78	2SC2785
Q025	8-729-699-51	2SA995
R001	1-249-415-11	CARBON 680 5% 1/4W
R002	1-249-403-11	CARBON 68 5% 1/4W
R003	1-249-408-11	CARBON 180 5% 1/4W
R004	1-249-413-11	CARBON 470 5% 1/4W
R005	1-249-419-11	CARBON 1.5K 5% 1/4W
R006,007	1-249-413-11	CARBON 470 5% 1/4W
R008	1-249-411-11	CARBON 330 5% 1/4W
R009	1-249-421-11	CARBON 2.2K 5% 1/4W
R010-013	1-249-415-11	CARBON 680 5% 1/4W
R014	1-249-410-11	CARBON 270 5% 1/4W
R015	1-249-415-11	CARBON 680 5% 1/4W
R016	1-249-417-11	CARBON 1K 5% 1/4W
R017	1-249-413-11	CARBON 470 5% 1/4W
R018	1-249-417-11	CARBON 1K 5% 1/4W
R019	1-249-429-11	CARBON 10K 5% 1/4W
R020	1-249-413-11	CARBON 470 5% 1/4W
R021	1-249-411-11	CARBON 330 5% 1/4W
R022	1-249-434-11	CARBON 27K 5% 1/4W
R023	1-249-406-11	CARBON 120 5% 1/4W
R024	1-249-411-11	CARBON 330 5% 1/4W
R025	1-249-417-11	CARBON 1K 5% 1/4W
R026	1-249-411-11	CARBON 330 5% 1/4W
R027	1-249-414-11	CARBON 560 5% 1/4W
R028	1-249-417-11	CARBON 1K 5% 1/4W
R029	1-249-420-11	CARBON 1.8K 5% 1/4W
R030	1-249-421-11	CARBON 2.2K 5% 1/4W
R031	1-249-414-11	CARBON 560 5% 1/4W
R032,033	1-249-417-11	CARBON 1K 5% 1/4W
R034	1-247-881-00	CARBON 120K 5% 1/4W
R035	1-249-430-11	CARBON 12K 5% 1/4W
R036	1-249-425-11	CARBON 4.7K 5% 1/4W
R037	1-249-426-11	CARBON 5.6K 5% 1/4W
R038	1-249-419-11	CARBON 1.5K 5% 1/4W
R039	1-249-425-11	CARBON 4.7K 5% 1/4W
R040	1-249-417-11	CARBON 1K 5% 1/4W

Ref.No.	Parts No.	Description
R041	1-247-893-11	CARBON 390K 5% 1/4W
R042	1-247-885-00	CARBON 180K 5% 1/4W
R043	1-247-832-11	CARBON 1.1K 5% 1/4W
R044	1-249-419-11	CARBON 1.5K 5% 1/4W
R045	1-249-439-11	CARBON 68K 5% 1/4W
R047	1-249-426-11	CARBON 5.6K 5% 1/4W
R048	1-249-433-11	CARBON 22K 5% 1/4W
R049	1-249-417-11	CARBON 1K 5% 1/4W
R050	1-249-425-11	CARBON 4.7K 5% 1/4W
R051	1-249-433-11	CARBON 22K 5% 1/4W
R054	1-249-420-11	CARBON 1.8K 5% 1/4W
R057	1-249-429-11	CARBON 10K 5% 1/4W
R058	1-249-432-11	CARBON 18K 5% 1/4W
R059	1-249-426-11	CARBON 5.6K 5% 1/4W
R060	1-249-431-11	CARBON 15K 5% 1/4W
R062	1-249-441-11	CARBON 100K 5% 1/4W
R063	1-249-418-11	CARBON 1.2K 5% 1/4W
R064	1-249-423-11	CARBON 3.3K 5% 1/4W
R065	1-249-418-11	CARBON 1.2K 5% 1/4W
R066	1-249-421-11	CARBON 2.2K 5% 1/4W
R067	1-249-427-11	CARBON 6.8K 5% 1/4W
R068	1-215-447-00	METAL 12K 1% 1/6W
R069	1-215-426-00	METAL 1.6K 1% 1/6W
R070	1-215-438-00	METAL 5.1K 1% 1/6W
R071	1-249-405-11	CARBON 100 5% 1/4W
R072	1-249-425-11	CARBON 4.7K 5% 1/4W
R073	1-249-405-11	CARBON 100 5% 1/4W
R074	1-249-425-11	CARBON 4.7K 5% 1/4W
R075	1-249-405-11	CARBON 100 5% 1/4W
R076	1-249-425-11	CARBON 4.7K 5% 1/4W
R080	1-249-422-11	CARBON 2.7K 5% 1/4W (IC040; TC4053BP)
	1-247-844-11	CARBON 3.6K 5% 1/4W (IC040; TC74HC4053AP)
R082	1-249-429-11	CARBON 10K 5% 1/4W
R083	1-249-425-11	CARBON 4.7K 5% 1/4W
R084,085	1-247-881-00	CARBON 120K 5% 1/4W
R086	1-249-418-11	CARBON 1.2K 5% 1/4W
R087	1-249-422-11	CARBON 2.7K 5% 1/4W
R088	1-247-881-00	CARBON 120K 5% 1/4W
R089	1-215-427-00	METAL 1.8K 1% 1/6W
R090,091	1-249-422-11	CARBON 2.7K 5% 1/4W
R092	1-249-425-11	CARBON 4.7K 5% 1/4W
R094	1-247-887-00	CARBON 220K 5% 1/4W
R095	1-249-437-11	CARBON 47K 5% 1/4W
R096	1-247-882-11	CARBON 130K 5% 1/4W
R097	1-215-464-00	METAL 62K 1% 1/6W
R098	1-249-435-11	CARBON 33K 5% 1/4W

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Ref.No.	Parts No.	Description
R099	1-249-423-11	CARBON 3.3K 5% 1/4W
R100	1-215-404-81	METAL 200 1% 1/6W
R101	1-215-446-00	METAL 11K 1% 1/6W
R102	1-215-445-00	METAL 10K 1% 1/6W
R103	1-215-394-00	METAL 75 1% 1/6W
R104	1-215-404-81	METAL 200 1% 1/6W
R105	1-215-394-00	METAL 75 1% 1/6W
R106	1-215-404-81	METAL 200 1% 1/6W
R107	1-215-394-00	METAL 75 1% 1/6W
R108	1-249-417-11	CARBON 1K 5% 1/4W
R109	1-249-423-11	CARBON 3.3K 5% 1/4W
R110	1-249-415-11	CARBON 680 5% 1/4W
R111	1-249-421-11	CARBON 2.2K 5% 1/4W
R113	1-249-433-11	CARBON 22K 5% 1/4W
⚠R114	1-216-377-11	METAL OXIDE 4.7 5% 2W
R117	1-249-403-11	CARBON 68 5% 1/4W
R118-120	1-249-425-11	CARBON 4.7K 5% 1/4W
R121	1-249-438-11	CARBON 56K 5% 1/4W
R124	1-215-394-00	METAL 75 1% 1/6W
R128	1-247-887-00	CARBON 220K 5% 1/4W
R129	1-249-425-11	CARBON 4.7K 5% 1/4W
R130	1-247-836-11	CARBON 1.6K 5% 1/4W
R131	1-247-883-00	CARBON 150K 5% 1/4W
R132	1-249-421-11	CARBON 2.2K 5% 1/4W
R133-135	1-249-403-11	CARBON 68 5% 1/4W
R136-149	1-249-399-11	CARBON 33 5% 1/4W
R150	1-249-403-11	CARBON 68 5% 1/4W
R151	1-249-417-11	CARBON 1K 5% 1/4W
R152	1-249-441-11	CARBON 100K 5% 1/4W
R154-156	1-249-401-11	CARBON 47 5% 1/4W
R157	1-249-403-11	CARBON 68 5% 1/4W
R159	1-249-393-11	CARBON 10 5% 1/4W
R160	1-249-399-11	CARBON 33 5% 1/4W
RB001	1-235-194-00	BLOCK 4.7Kx8
RV001	1-237-514-21	ADJUSTMENT, CERMET 500
RV002	1-237-515-21	ADJUSTMENT, CERMET 1K
RV003	1-237-517-21	ADJUSTMENT, CERMET 5K
RV004	1-237-516-21	ADJUSTMENT, CERMET 2K
RV005	1-237-518-21	ADJUSTMENT, CERMET 10K
RV006	1-237-512-21	ADJUSTMENT, CERMET 100
RV007	1-237-518-21	ADJUSTMENT, CERMET 10K
RV009	1-237-517-21	ADJUSTMENT, CERMET 5K
RV010,011	1-237-520-21	ADJUSTMENT, CERMET 50K

Ref.No.	Parts No.	Description
SW001	1-571-788-11	DIP
X001	1-577-292-11	VIBRATOR, CRYSTAL
X002	1-567-878-11	VIBRATOR, CRYSTAL

9-2-14. Switching Regulator

⚠	*1-413-309-11	REGULATOR, SWITCHING (SR-93)
⚠	*1-526-986-11	OUTLET, AC
⚠	*1-526-987-11	INLET (WITH FILTER)
	1-541-337-21	FAN
⚠	1-623-761-11	PC BOARD, C
⚠	1-623-762-11	PC BOARD, B
⚠	1-623-763-11	PC BOARD, A
⚠F101	1-532-988-11	FUSE 5A
⚠R103	1-217-779-11	FUSE 6.8 5% 1W
⚠RL101	1-515-673-11	RELAY (VG-24TM)
⚠RL102	1-515-674-11	RELAY (VS-12MB-NR)
⚠SW1	1-570-743-11	POWER

9-2-15. Computer Frame

1-503-221-00	SPEAKER
1-574-371-11	CABLE (VS-VGA)

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Ref.No.	Parts No.	Description

9-3. ACCESSORIES AND PACKING MATERIAL

⚠	1-551-812-00	CORD, POWER (WITH SHIELD)
	1-559-341-11	CORD, CONNECTION (RS-232C CROSS CABLE)
	1-559-871-11	CORD, CONNECTION (AV CABLE)
*	3-769-308-21	MANUAL, INSTRUCTION (LDP-1500)
*	3-786-527-21	MANUAL, INSTRUCTION (VIW-3015A)

9-4. FIXTURES

*	J-6093-380-A	EXTENSION BOARD, IF-156
*	J-6093-490-A	EXTENSION BOARD ASSY
*	J-6093-540-A	EXTENSION BOARD, PU-59
*	J-6093-570-A	IC EXTRACTION TOOL, 68
*	J-6093-580-A	IC EXTRACTION TOOL, 84
*	J-6200-200-A	KEYTOP EXTRACTION TOOL

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VIW-3015A(UC)
9-975-688-01

Sony Corporation

Printed in Japan
1989.3 09

VIW-3015A

SONY
SERVICE MANUAL

SUPPLEMENT-1

File this supplement with the service manual.

This supplement-1 is added THEORY OF OPERATION (VS-38A BOARD, SWITCHING REGULATOR, KEYBOARD), ADJUSTMENT.

Sony VIEW System

SONY

TABLE OF CONTENTS

3. THEORY OF OPERATION

8. ADJUSTMENT

3-5. VS-38A BOARD

3-5-1. Outline

The VS-38A board allows the RGB superimposition of computer graphics images produced by the VGA-16 board onto video images.

The circuit description of the analog system is in Section 3-5-4 to 3-5-13. The circuit description of the digital system is in Section 3-5-14.

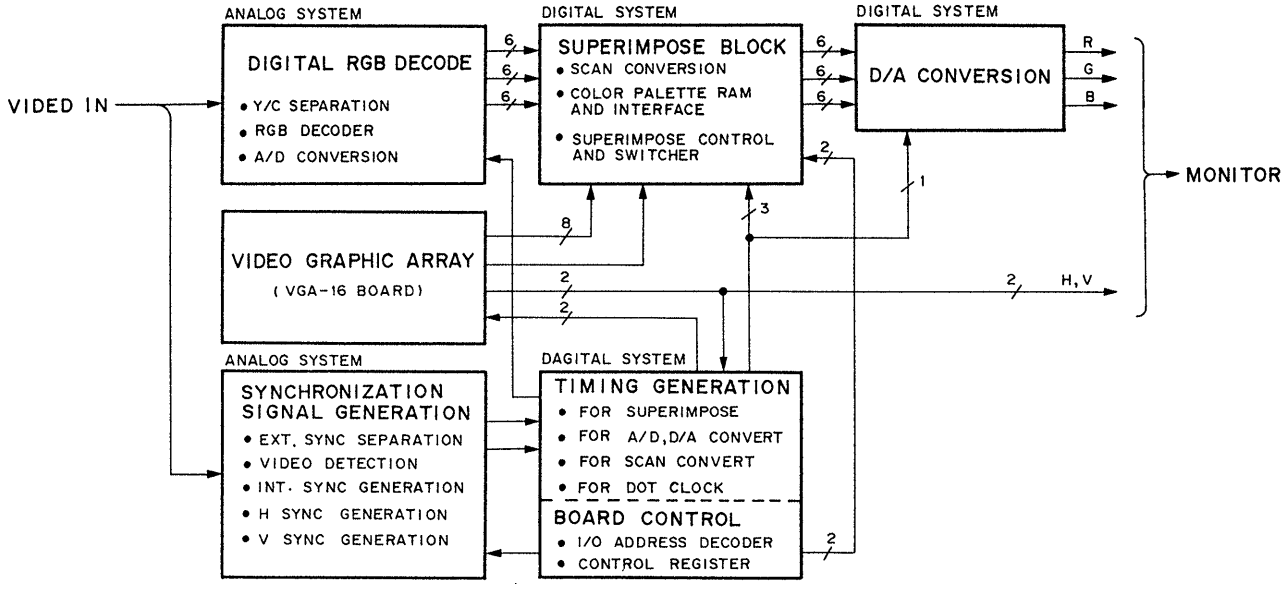


Fig. 3-5-1 High Scan Superimposer Outline

3-5-2. Video System

After passing through the video amplifier, the input video signal (NTSC) is separated into Y (luminance) and C (chrominance) signals on the Y/C separation section. These Y and C signals are input to the RGB decoder IC002 (V7020) which generates red (R), green (G) and blue (B) analog color signals.

Each of these R, G and B signals is converted into a 6-bit digital signal (V_{RGB}) by Analog-to-Digital Converters IC007, IC008 and IC009 (CXD1172). The conversion rate is the frequency which is generated by halving the dot clock frequency (pixel clock transmitted from the VGA-16 board) in IC201.

The V_{RGB} signal is scan-converted by line memories IC014, IC015 and IC016 (μPD42102) into a signal with the same format as a computer graphics image. In this process, the V_{RGB} signal is written into the line memory at a frequency half the dot clock frequency, while it is read out at the dot clock frequency. In this way, the same line is read twice in succession, and the signal is converted into a signal with a 1-field, 525-line raster and an f_H of 31.5 kHz.

When this signal is replaced with the computer graphics signal by the selector incorporated in the gate array IC021 (μPD65013S-526), superimposition is possible.

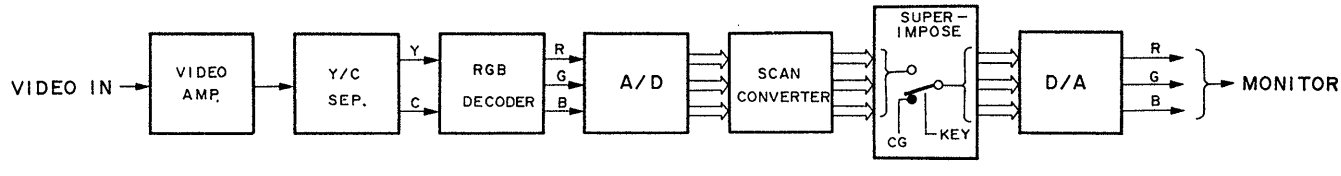


Fig. 3-5-2 Video System

3-5-3. Computer Graphics System

The 8-bit signal (PD0 to PD7) transmitted from the VGA-16 board is the address signal (pixel address data) for the color palette RAM IC022, IC023 and IC024 (TMM2018AP), and the color palette RAM consists of a 6-bit (18 bits in all) × 256 memory for each of the R, G and B signals.
The 8-bit pixel address is used to specify and read the required data from the 18-bit color data (stored previously) so that the data with up to 256 colors can be detected.

When this data is switched with the RGB signal from the video by the selector incorporated in the gate array IC021 (μ PD65013S-526), superimposition is possible.
The output (each 6-bit in RGB) from this selector is converted to analog RGB signals by digital-to-analog converters IC026, IC027 and IC028 (μPD6902C), then output to the monitor.

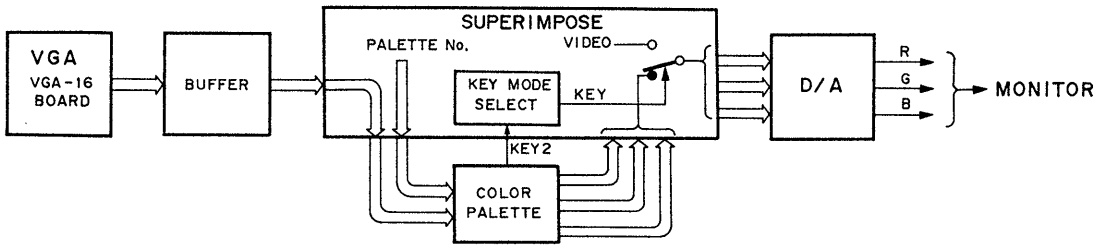


Fig. 3-5-3 Computer Graphics System

3-5-4. Video Amplifier

The input video signal is amplified by approx. 4.7 dB in Q006 and Q025, and then supplied to the Y/C separator circuit in which the signal is separated into Y (luminance) and C (chrominance) signals. The amplified signal is also applied to the external sync separator circuit.

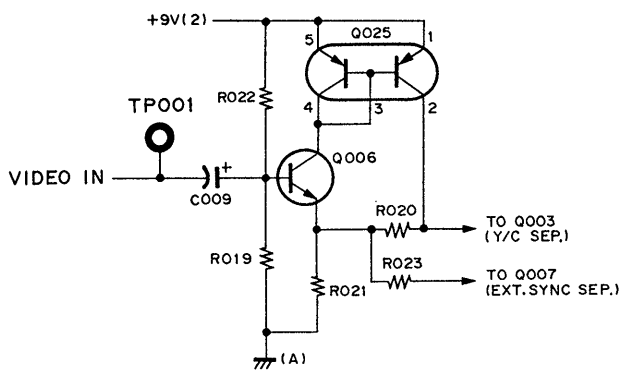


Fig. 3-5-4 Video Amplifer

3-5-5. Y/C Separation

Y (luminance) /C (chrominance) separation is performed by the comb filter using a 1H delay line (DL001). Q003 is the buffer for the driver.
See Fig. 3-5-5-1 of page 3-29.
The phase of the lower frequencies of the signal input to DL001 is compensated by trap circuit 1 (C005, L001) and trap circuit 2 (R008, L002, C006). The phase and amplitude of the signal passing through DL001 and those of the signal input to the bridge circuit directly are adjusted by LV001 (for phase) and RV001 (for amplitude) so that they are matched.
The Y signal and the C signals are separated in the bridge circuit (consisting of R011 to R013, R015 and L003).
See Fig. 3-5-5-2 of page 3-29.
After this, the C signal is passed through the 3.58 MHz band-pass filter and amplified in Q012, then input to RGB decoder IC002 (V7020) via buffer Q011. The Y signal is applied to the low-pass filter (consisting of C007, L005 and R032) to be compensated so that the response in the frequency range between 0 and 4.2 MHz becomes flat, then it is passed through the peaking circuit (consisting of L004, C012, C013, R026, R027, R029 and Q008), and applied to a 380 nsec delay line (DL002) then input to IC002.
The level of the Y signal is adjusted by RV002 before it is input to IC002.

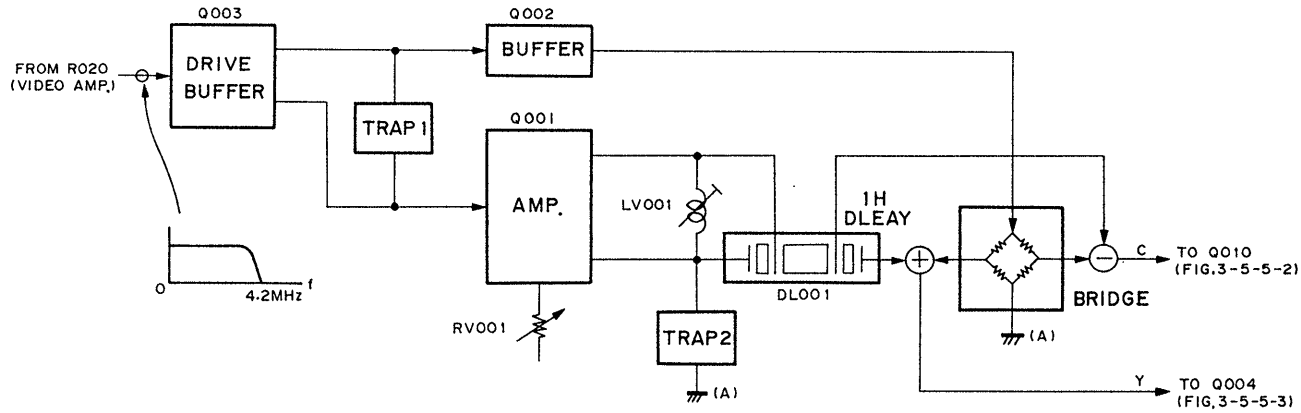


Fig. 3-5-5-1 Y/C Separation

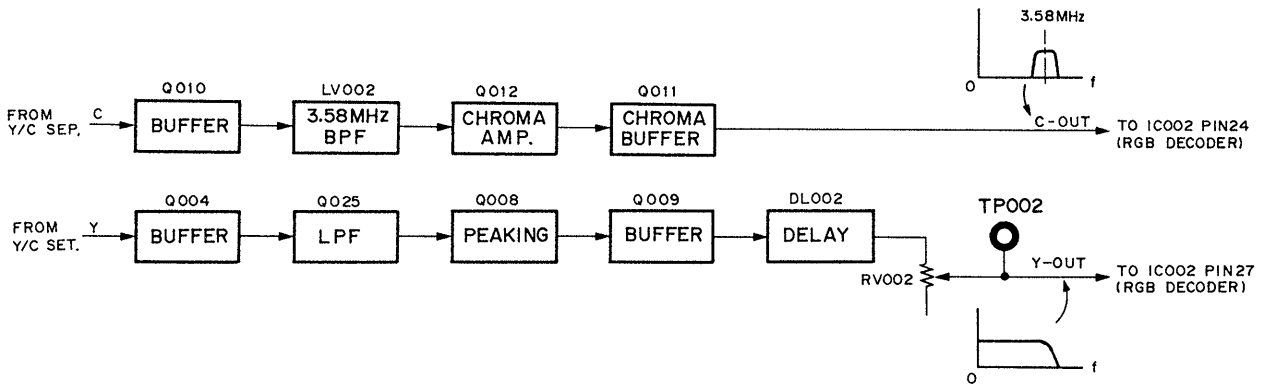


Fig. 3-5-5-2 Chrominance (C) Signal Out (upper) and Luminance (Y) Signal Out (lower)

3-5-6. RGB Decoding

The Y signal and the C signal are input to the RGB decoder IC002 (V7020) in which the input signals are converted into R, G and B signals to be output.
The color subcarrier signal used as the reference signal is generated by phase-locking the 3.58 MHz clock frequency generated by X001 with the color burst signal of the C signal.
The color of the signal is adjusted by RV004, the burst flag position is adjusted by RV005, the automatic picture color (APC) is adjusted by RV006, and the hue is adjusted by RV007.

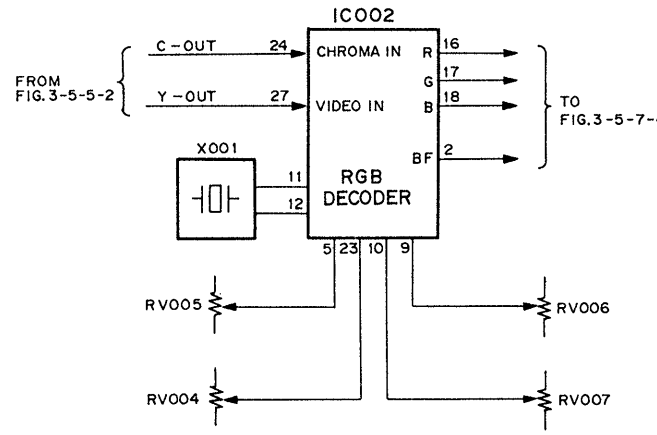


Fig. 3-5-6 RGB Decoder

3-5-7. A/D Conversion

3-5-7-1. Reference input voltage

The reference input voltages for the A/D converters (IC007, IC008 and IC009) are produced by resistance dividing by R068, R069 and R070, and VRT and VRB are passed through IC003 (μPC358) before being input to the A/D converters.

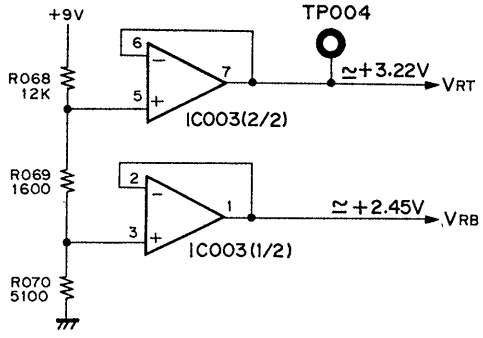


Fig. 3-5-7-1 Reference Top/Bottom Voltage

3-5-7-2. Clamping

The R, G and B analog color signals output from the RGB decoder IC002 (V7020) are clamped by the potential of VRB + VBE (Q021) during the burst period. The $\overline{BF}$ output is used as the signal indicating the burst period. When there is no external video input, the VID signal goes low to cltamp the signal in the same way.

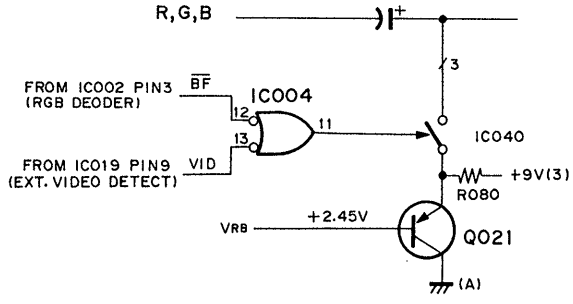


Fig. 3-5-7-2 R/G/B Clamping

3-5-7-3. Low-luminance parts compensation

If the video image is displayed on the monitor of a computer, the whole screen will be dark when compared with the picture on a video monitor. To compensate for this on the VS-38A board, resistors and diodes are inserted serially between VIN and VRB of each A/D converter. In this way, high-voltage (high-luminance) parts of the R, G and B signals are compressed so that the levels of low-voltage (low-luminance) parts are relatively higher.

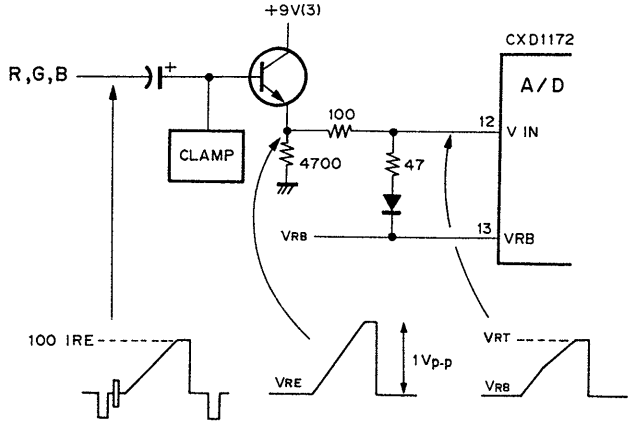


Fig. 3-5-7-3 Low-luminance Parts Compensation

3-5-7-4. A/D conversion

Each of R, G and B signals input to the A/D converter is digitized into 6-bit (64-gradation) signals between voltages VRT and VRB, then output.

CXD1172 is used as the A/D converter.

3-5-8. External Sync Separation

Separation of the external sync signal is performed by circuitry in IC001 (LA7801). Q007 is the buffer for the driver.
The duty level of sync separation is approximately the ratio of R034 to R024. Time constant circuit consisting of R034 and C019 is provided to absorb the DC potential difference between IC001 and the input video signal.
The separated sync signal is output from pin 13 of IC001 and inverted by IC005 (74HC14) to be used as the $\overline{\text{EX-SYC}}$ (TP016) signal.

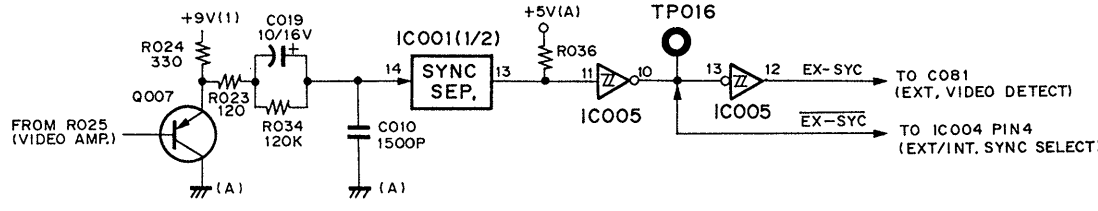


Fig. 3-5-8 External Video Sync Separation

3-5-9. External Video Signal Detection

In the Auto-GENLOCK mode, the sync system on the VS-38A board alternates between external sync and internal sync depending on whether an external video input signal is present or not.
The detection of the external video signal is performed using the EX-SYC signal which is generated by inverting the $\overline{\text{EX-SYC}}$ (TP016) signal by IC005 (74HC14).
The detection circuit consists of the rectifier circuit (C076, C081, D008, D010) and the comparator circuit.
The EX-SYC signal which is the external composite sync signal is smoothed by the rectifier circuit and input to pin 5 of the comparator IC010 (2/2) (μPC393). As opposed to this, the voltage of approx. 1.97V divided by R084, R086, D009, etc. is input to pin 6 of IC010 (2/2).
The detection sensitivity is determined by C076, and D009 is provided to prevent the potential of both signals input to IC010 (2/2) becoming equal when an external video signal is not input.
The comparison output signal is output from pin 7 of IC010 (2/2) and input to IC019 (2/2) (74HC74) to be latched.
The output signal $\overline{\text{INT-SYC}}$ (TP009) from the sync generator IC011 (CXD1030) provided for internal sync is used as the clock frequency for latching.
The VID signal and its inverted output $\overline{\text{VID}}$ signal is output from IC019 (2/2) as the external/internal sync selection signal.

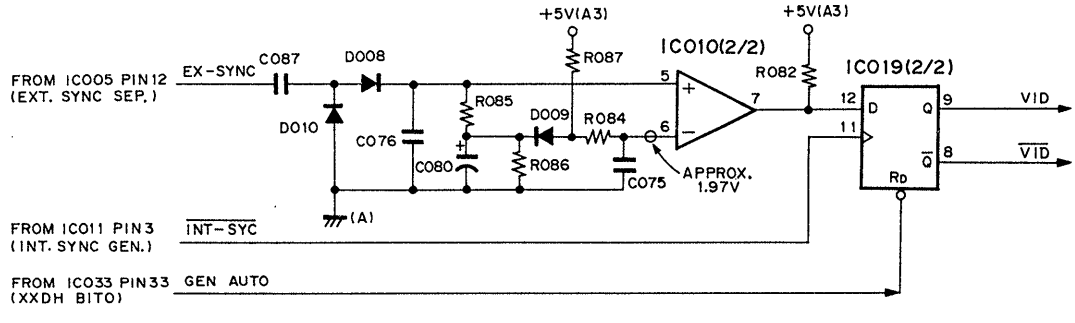


Fig. 3-5-9 External Video Signal Detection

3-5-10. External/Internal Sync Selection

Selection of the synchronization mode on the VS-38A board between external and internal sync is performed by IC004 (74HC00). In the Auto-GENLOCK mode, mode selection is done by the VID signal and $\overline{\text{VID}}$ signal from the external video signal detection section. In the Internal-GENLOCK mode, the GEN AUTO signal goes low to set the output of IC019 (2/2) in the external video signal detection section to the reset status (the VID signal is fixed at low and the $\overline{\text{VID}}$ signal is fixed at high), so that the sync mode is fixed to internal synchronization.

The $\overline{\text{C-SYC}}$ (TP008) signals switched by IC004 are as shown in the following table.

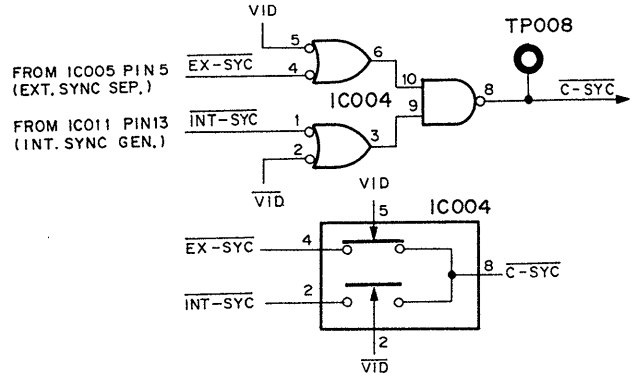


Fig. 3-5-10 EXT/INT Sync Selection

GENLOCK mode	GEN AUTO signal	$\overline{\text{VID}}$ signal	VID signal	$\overline{\text{C-SYC}}$ output
Auto-GENLOCK	"1"	"0"	"1"	$\overline{\text{EX-SYC}}$ signal
	"1"	"1"	"0"	$\overline{\text{INT-SYC}}$ signal
Internal-GENLOCK	"0"	"1"	"0"	

"1" ; High level
"0" ; Low level

3-5-11. Vertical Sync Signal Detection

In this section, the vertical sync period is detected from the $\overline{\text{C-SYC}}$ (TP008) signal to generate the $\overline{\text{VSV}}$ vertical sync signal and its inverted output, the VSV signal.
The $\overline{\text{C-SYC}}$ signal is passed through the integrating circuit (C082, R088), and its voltage is compared with the threshold voltage of approx. 2.5V.
The threshold voltage is voltage-divided at R090 and R091. The voltage is compared in IC010 (1/2) (μPC393).
The IC010 (1/2) output (V sync signal) is masked by the monostable multivibrator IC017 (1/2) (74HC221) during approx. 1 field period (approx. 13 msec.). The VSV signal and the $\overline{\text{VSV}}$ signal having the pulse width of approx. 28 μsec are output from IC017 (2/2).

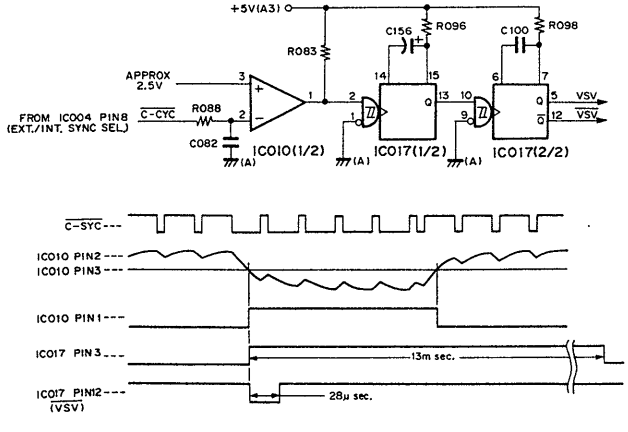


Fig. 3-5-11 Vertical Sync Signal Detection and Genetation

3-5-12. Horizontal Sync Signal Generation

In this section, the equalizing pulse with a period of 1/2H is removed from the $\overline{\text{C-SYC}}$ (TP008) signal. The resultant signal is input to the horizontal sync AFC (Auto Frequency Control) circuit to generate the stable horizontal sync signal $\overline{\text{VSH}}$ (TP010) signal.
In this way, even if the horizontal sync signal in the external video signal is lost, it is interpolated by the period which is equalized by the horizontal sync signal immediately before.

See Fig. 3-5-12 of page 3-33.
The equalizing pulse within the $\overline{\text{C-SYC}}$ signal is removed by the monostable multivibrator IC018 (74HC221). This signal (H-SYC) is input to the HAFC circuit in IC001 (LA7801) and is used to control the oscillating frequency of the HOSC circuit in IC001. This oscillating frequency is optimized by RV003 and PLL circuits are used in the HOSC and the HAFC circuits to stabilize the oscillation frequency.
The output from the horizontal sync AFC circuit is waveform-shaped by IC005 (74HC14), then applied to the monostable multivibrator IC006 (74HC123), in which the relative positions of the computer graphics image and the external video image in the horizontal direction are adjusted (RV009). The pulse width of the $\overline{\text{VSH}}$ signal is approx. 4.6 μsec.

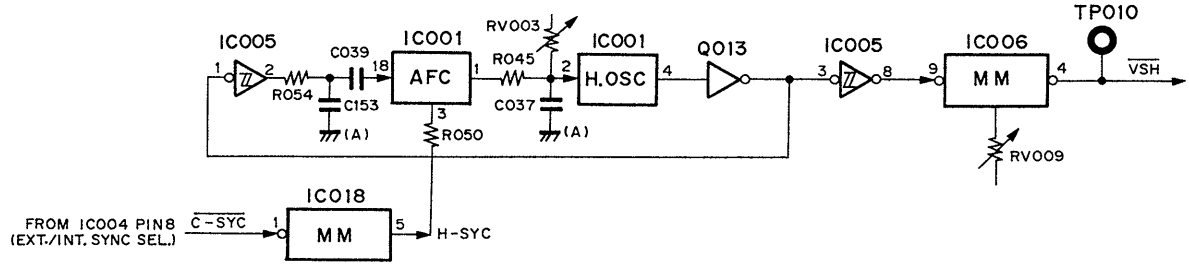


Fig. 3-5-12 Horizontal Sync Signal Generation

3-5-13. Internal Sync Signal Generation

Sync generator IC011 (CXD1030) generates the pseudo composite sync signal for the internal sync mode.
The local oscillator X002 generates 14.3 MHz clock, and it is output as the INT-SYC (TP009) signal from IC011.
IC011 outputs this INT-SYC signal continuously regardless of the setting of the external or internal sync mode. However, if an external video signal is present, generation of the INT-SYC signal will be initialized whenever the first field of the external video signal starts.
Whether this external video signal is present or not is transmitted by the VID signal which is output from the external video signal detection block. The detection of the first field is performed using the VSH (TP010) signal which is output from the horizontal sync signal generation block, and the VSV signal which is output from the vertical sync signal generation block.

See Fig. 3-5-13.
The pulse width of the VSH signal is widened to approx. 33 µsec by the monostable multivibrator IC013 (2/2) (74HC123) to generate the FH signal. This FH signal is clocked with the VSV signal at IC019 (1/2) (74HC74) so that the FLD (TP017) signal which is the first field detection signal is output.
The FLD signal is applied to IC013 (1/2) so as to generate the V-reset signal for IC011. RV010 changes the pulse width of the V-reset signal (to approx. 16.5 msec.) to adjust the timing of initialization of the INT-SYC signal. RV010 also adjusts the phase of the INT-SYC signal so that it matches the phase of the EXT-SYC signal.

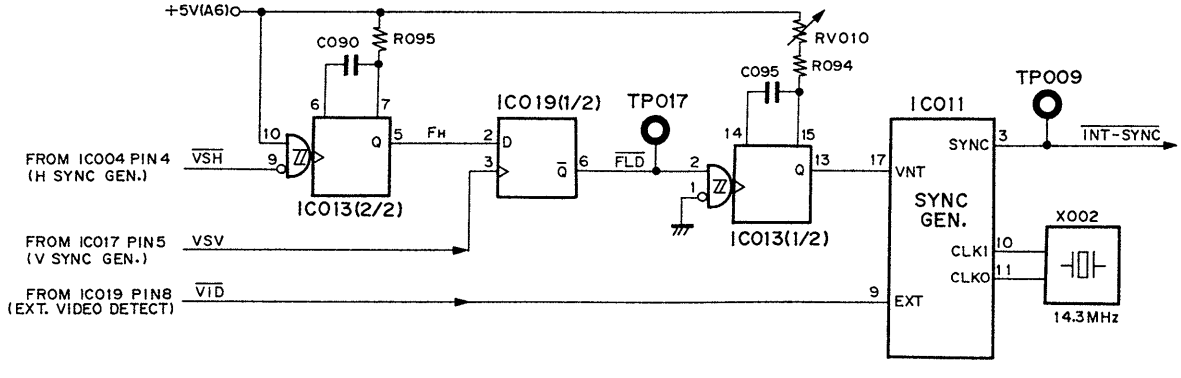


Fig. 3-5-13 Internal Sync Signal Generation

In the internal sync mode, initialization of the INT-SYC signal mentioned above is not performed. Because of this, if the external video signal is present in the Internal-GENLOCK mode, the phase of the EX-SYC signal does not coincide with that of the C-SYC signal.
In this case, the video image will be muted by software so that non-synchronized video images are not displayed. (Using application software, it is processed so that the video image is normally muted in the Internal-GENLOCK mode.)

3-5-14. Filter Gain Select Signal Generation

The GLOW (gain low) signal is created from the VSV signal by IC043 (2/2). The position (width) of this signal is adjusted by RV011 (low for approximately 965 µsec).
The GLOW signal is used for selecting the LPF gain of the dot clock PLL circuit.

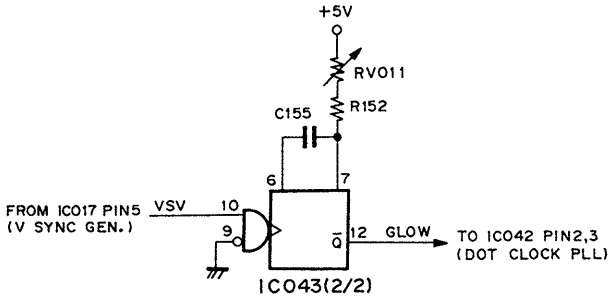


Fig. 3-5-14. GLOW Signal Generation

3-5-15. Gate Array IC021

3-5-15-1. Outline of IC021

IC021 is a gate array (µPD65013S-526) designed for use as a superimposer for VGA (Video Graphic Array).
The main functions of the µPD65013S - 526 are superimposion and color palette control.

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	31	P7	61	A1	91	VR0
2	NC	32	LMR4	62	SREG	92	VG3
3	VR4	33	LMR1	63	DLCK	93	GND
4	VR1	34	NRST	64	GND	94	VB4
5	VG4	35	LMG5	65	SB3	95	VB1
6	VG1	36	LMG4	66	SB5	96	D6
7	VB5	37	NC	67	SG2	97	NC
8	VB2	38	LMG3	68	NC	98	IOW
9	D7	39	LMG1	69	NC	99	IREG
10	D4	40	LMB4	70	SR1	100	CKD2
11	D3	41	LMB1	71	SR4	101	Vcc
12	D2	42	MOE	72	P1	102	SB2
13	NC	43	PS0	73	P4	103	GND
14	D1	44	MA7	74	GND	104	SG1
15	IOR	45	MA4	75	LMR5	105	NC
16	A0	46	MA1	76	LMR2	106	SR3
17	MCLK	47	MA0	77	LMR0	107	P0
18	SB0	48	KEY2	78	NC	108	P3
19	SB1	49	NC	79	NC	109	P6
20	SB4	50	VR5	80	LMG2	110	BLNK
21	SG0	51	VR2	81	LMB5	111	LMR3
22	SG3	52	VG5	82	LMB2	112	NC
23	SG4	53	VG2	83	MWE	113	NC
24	SG5	54	VG0	84	GND	114	LMG0
25	NC	55	VB3	85	PS2	115	LMB3
26	SR0	56	VB0	86	MA5	116	LMB0
27	SR2	57	D5	87	MA2	117	Vcc
28	SR5	58	NC	88	NC	118	PS1
29	P2	59	NC	89	NC	119	MA6
30	P5	60	D0	90	VR3	120	MA3

As for pin assignment, refer to Fig. 3-5-15-8 (3-37 page).

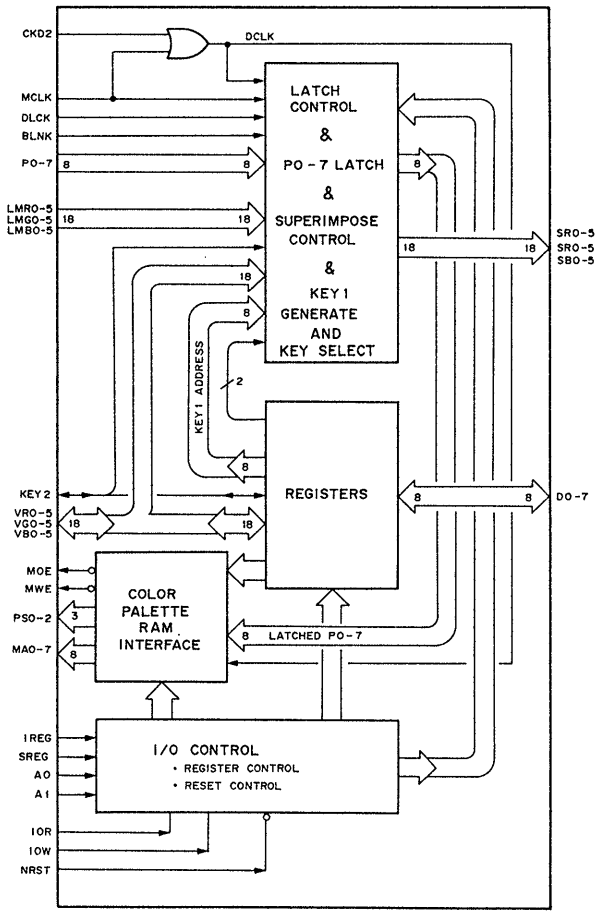


Fig. 3-5-15-1. µPD65013S-526 Block Diagram

3-5-15-2. Terminal functions

Refer to Section 3-5-15-1. for the pin numbers.

- P0 to P7 ····· Palette address inputs
  Input terminals for the palette address output from the VGA-16 board.
- BLNK ····· Blanking input
  Input terminal for BLNK signal output from VGA-16 board. Blanking of both video image and computer graphics image when low.
- MCLK ····· Master clock input
  Input terminal for master clock used within µPD65013S-526. The input frequency varies between 25.7 MHz and 32.3 MHz according to the display mode.
- CKD2 ····· Clock divide by two
  Input terminal for signal used to generate dot clock used within µPD65013S-526. Low level is input for the horizontal 640-dot display mode. A clock with a frequency 1/2 of MCLK is input for the horizontal 320-dot mode.
- MA0 to MA7 ····· Memory address outputs
  Address output terminals for external color palette RAM
- PS0 to PS2 ····· Palette select signal outputs
  Output terminal for signal used to designate one of eight palette areas.

Terminal functions (Cont.)

- VR0 to VR5 ····· Video R data inputs/outputs
  Input/output terminals for color palette R data
- VG0 to VG5 ····· Video G data inputs/outputs
  Input/output terminals for color palette G data
- VB0 to VB5 ····· Video B data inputs/outputs
  Input/output terminals for color palette B data
- KEY2 ····· Input/output
  Terminal for reading/writing key bit together with color palette R data
- LMR0 to LMR5 ····· Video R data inputs from line memory
  Input terminal for video R data adjusted to interlace by line memory.
- LMG0 to LMG5 ····· Video G data inputs from line memory
  Input terminal for video G data adjusted to interlace by line memory.
- LMB0 to LMB5 ····· Video B data inputs from line memory
  Input terminal for video B data adjusted to interlace by line memory.
- DLCK ····· Data latch clock input
  Clock input terminal for latching of data from color palette. Timing of externally generated dot clock is measured and input.
- SR0 to SR5 ····· Superimposition R data outputs
  Output terminals for R data after superimposing of video image and computer graphics image.
- SG0 to SG5 ····· Superimposition G data outputs
  Output terminals for G data after superimposing of video image and computer graphics image.
- SB0 to SB5 ····· Superimposition B data outputs
  Output terminals for B data after superimposing of video image and computer graphics image.
- MWE ····· Memory write enable output
  Output terminal for color palette RAM write control signal. Write when low.
- MOE ····· Memory output enable output
  Output terminal for color palette RAM output enable signal. Enabled when low.
- D0 to D7 ····· Data bus inputs/outputs
  Input/output terminals for reading/writing data to internal ports.
- IOW ····· I/O write strobe input
  Write signal input terminal for internal port registers. Write when low.
- IOR ····· I/O read strobe input
  Read signal input terminal for internal ports. Read when low.
- A0, A1 ····· I/O address line inputs
- IREG ····· IBM registers enable signal input
- SREG ····· Sony registers enable signal input
  A0, A1, IREG, and SREG are select signal input terminals for the internal ports. Refer to Section 3-5-15-5.
- NRST ····· Reset input
  Reset applied when low.
- Vcc ····· + 5V DC input
- GND ····· Connected ground
- NC ····· No connection

3-5-15-3. Flow of display data

The computer graphics data input (P0 to P7) is latched by DCLK, and is output through the address selector as the color palette RAM address signal after masking by the mask register.

The palette RAM data (VR0 to VR5, VG0 to VG5, VB0 to VB5, and KEY2) accessed by that address are latched by DLCK and DCLK, superimposed with the external video image by the selector, latched again, and output to the D/A convertor (as SR0 to SR5, SG0 to SG5, and SB0 to SB5). On the other hand, after the data inputs (LMR0 to LMR5, LMG0 to LMG5, and LMB0 to LMB5) for the external video image are latched by MCLK, they are input to the selector, superimposed, and output to the D/A convertor.

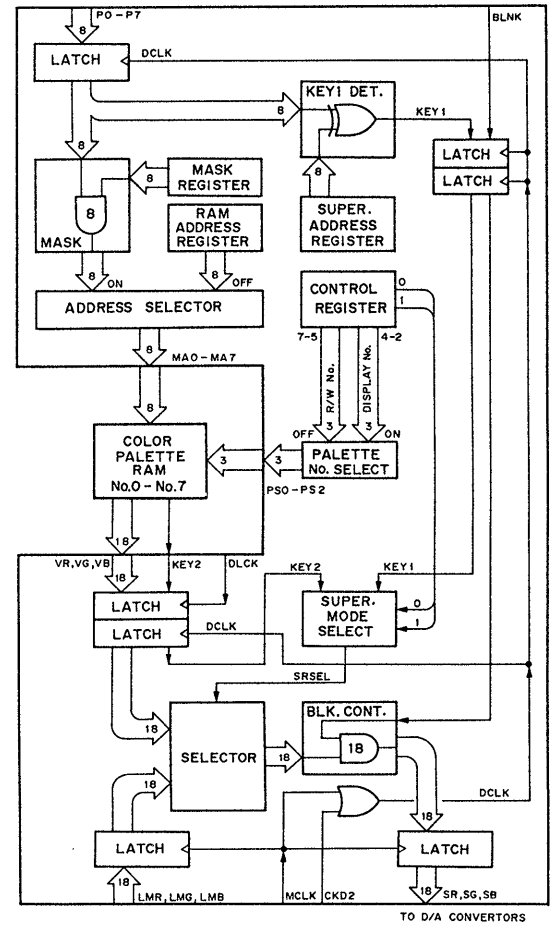


Fig. 3-5-15-3. Display Condition

3-5-15-4. Superimposition

There are two superimposition methods available.

KEY 1 : Superimposition by palette address

In this method, there is superimposition with the external video image when the value written to the super. address port matches the pixel address data (latch output for P0 to P7).

The only transparent color is single color indicated by the super. address port (refer to Section 3-5-15-5).

KEY 2 : Superimposition by key bit

In this superimposition method, the key bit indicating whether the data from the color palette RAM is itself a transparent color is added as a single bit at the beginning.

A maximum of 256 transparent colors can be designated by adding key bits to all palette data. The key bit is assigned to bit 6 when R data is written to the color palette RAM.

See Fig. 3-5-15-3.

Superimposition is performed by SRSEL signal. This SRSEL signal is selected among 4 state, High level, Low level, KEY 1 and KEY 2, by the Super. mode selector.

This selector is switched by the control register superimpose control bits (0 and 1).

Bit 1	Bit 0	Function
"0"	"0"	Display only computer graphics.
"0"	"1"	Performs superimposition by palette address.
"1"	"0"	Performs superimposition by key bit in the color (red) data.
"1"	"1"	Display only the external video picture.

3-5-15-5. Internal ports

The μPD65013S-526 is equipped with the following internal ports.

- Palette write address port (R/W) ···· 8 bits

  This port can not be read from the VS-38A board.

  When data are written in the color palette RAM, addresses corresponding to the color Nos. are designated by this port. The RAM address counter is set to the address value written in this port.

- Palette data (IBM) port (R/W) ····· 6 bits

  This port can not be read from the VS-38A board.

  This port is used to read/write color palette RAM data. Data from this port are always written in the palette No. 0 area, and cannot be written in palette No. 1 to 7 areas. On the other hand, data in the palette No. designated by the control register is selected when reading.

  Palette data are read/written consecutively in the order of R, G and B. The address corresponding to the color No. is written in the palette read address port or the palette write address port before reading or writing, respectively.

- Mask register port (R/W) ····· 8 bits

  This port can not be read from the VS-38A board.

  Pixel address data from the VGA-16 board are masked in 1-bit units.

  "0" ·····Mask

  "1" ·····Enable

  If bit n of the mask register is set to "0", bit n of the pixel address data is masked, and bit n of the address output (8 bits) to the color palette RAM is fixed to "0". When performing 256-color display, all mask register bits are set to "1".

- Palette read address port (R/W) ····· 8 bits

  This port can not be read from the VS-38A board.

  An address corresponding to the color No. is designated by this port when reading color palette RAM data.

  The RAM address counter is set to the address value written in this port.

- Status register port (R) ····· 2 bits

  This port can not be read from the VS-38A board.

  This port shows whether the color palette RAM is presently in the read or write cycle.

  Bit 1 Bit 0

  "0" "0"·····Write cycle

  "1" "1"·····Read cycle

- Control register port (W) ····· 8 bits

  This port designates superimpose control and palette No. of the color palette RAM.

  Bits 1 and 0·····Superimpose control bits (refer to Section 3-5-15-4)

  Bits 4, 3, 2·····Designate the palette No. for display, selecting among the 8 values from "000" to "111".

  Bits 7, 6, 5·····Designate the palette No. for read/write, selecting among the 8 values from "000" to "111".

- Board control port (W) ····· 1 bit

  This port mutes monitor output.

  Bit 1

  "1"·····Monitor display disabled

  "0"·····Monitor display enabled

- Superimpose address port (R/W) ···· 8 bits

  When performing palette address superimposition, the address is written in this port.

  Superimposition is executed when the value in this port equals the pixel address data from the VGA-16 board.

• Palette data (SONY) port ····· 6 bits
(7 bits for red color only)

This port is used for data read/write operations with the color palette RAM, likewise the palette data (IBM) port.

It differs from the palette data (IBM) port in that key data is added to bit 7 of R data, and that color palette Nos. can be designated from the control register port for write as well as for read operations.

The above internal ports are selected as shown in the following table. A0, A1, IREG and SREG are select signal input terminals for the internal ports.

IREG	SREG	A1	A0	R/W	Ports
0	1	0	0	* R/W	Palette write address
0	1	0	1	* R/W	Palette data (IBM)
0	1	1	0	* R/W	Mask register
0	1	1	1	W	Palette read address
0	1	1	1	* R	Status register
1	0	0	0	W	Control register
1	0	0	1	W	Board control
1	0	1	0	* R/W	Superimpose address
1	0	1	1	* R/W	Palette data (SONY)

* Can not be read from the VS-38A board.

3-5-15-6. Color palette RAM interface

Read/write operations with the color palette RAM are performed after the corresponding color palette address is written into the RAM address register. This register works also as an address counter. When R, G and B data are read /written into the data register after the address is written to RAM address register, the RAM address register count is automatically incremented by 1. The color palette RAM has eight 256-color areas.

Palettes used for display and for read/write operations are designated among these eight by the control register (refer to Section 3-5-15-5).

The color palette RAM write enable and output enable signals are also generated at μPD65013S-526 from DCLK. Switching between color palette RAM addresses (color address and palette No.) for display and for CPU access is performed on the basis of DCLK.

3-5-15-7. Dot clock within μPD65013S-526

Two clock pulses are input to μPD65013S-526. The VS-38A board internal dot clock is input from the MCLK terminal. This pulse is delayed, a logical sum is performed between it and the CKD2 signal, and the resulting signal is input from the DLCK terminal.

Furthermore, DCLK is obtained by performing a logical sum inside μPD65013S-526 between the dot clock input to the MCLK terminal and CKD2.

DCLK and DLCK are mutually out of phase (see Fig. 3-5-15-7). The CKD2 signal delivers a clock pulse equivalent to one-half of MCLK in the 320-horizontal-dot mode, and remains at low level in the 640-horizontal-dot mode.

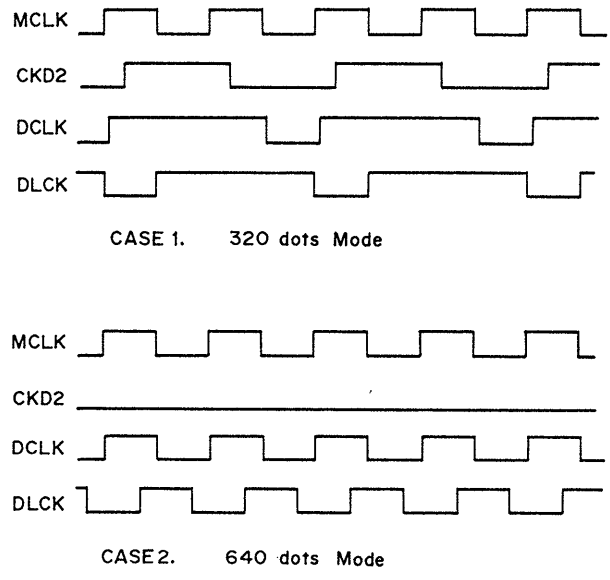


Fig. 3-5-15-7. Dot Clock

3-5-15-8. External view

Fig. 3-5-15-8 shows the pin assignment viewed from the bottom of the μPD65013S-526. This gate array is the package of PPGA (Plastic Pin Grid Array) of 120-pin. IND. terminal is used for prevention against accidental imposition.

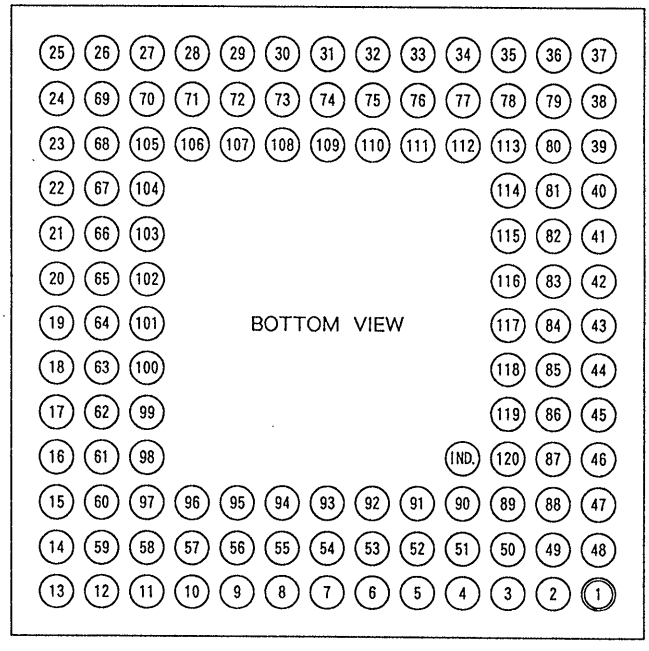


Fig. 3-5-15-8. Pin Assignment

3-5-16. Gate Array IC033

3-5-16-1. Outline of IC033

IC033 is a gate array (μPD65006GF-325-3B8) designed for use as a superimposer for VGA.
It is shaped as a 64-pin flat package.

μPD65006GF-325-3B8 Functions

- I/O address decoder
- Superimpose control register
- Composite sync generation
- Board status registers
- Clock generator for line memories and A/D converters
- Genlock controller

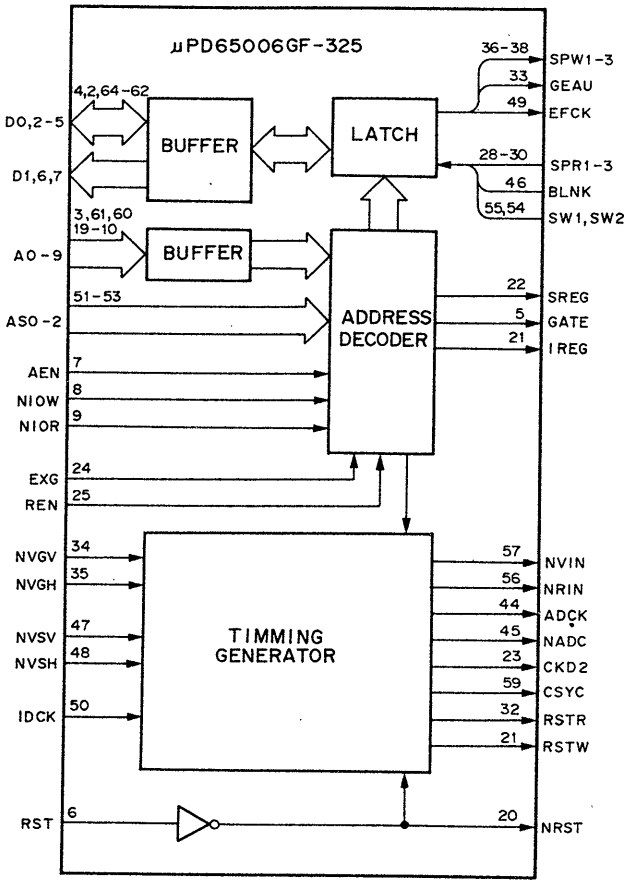


Fig. 3-5-16-1. μPD65006GF-325-3B8 Block Diagram

3-5-16-2. Terminal functions

Pin's Name

No.	Name	No.	Name	No.	Name	No.	Name
1	NC	17	A2	33	GEAU	49	EFCK
2	D02	18	A1	34	NVSV	50	IDCK
3	D01	19	A0	35	NVSH	51	AS0
4	D00	20	NRST	36	SPW1	52	AS1
5	GATE	21	IREG	37	SPW2	53	AS2
6	RST	22	SREG	38	SPW3	54	SW2
7	AEN	23	CKD2	39	NC	55	SW1
8	NIOW	24	EXG	40	NC	56	NRIN
9	NIOR	25	REN	41	GND	57	NVIN
10	A9	26	GND	42	NC	58	GND
11	A8	27	VDD	43	GND	59	CSYC
12	A7	28	SPR1	44	ADCK	60	D07
13	A6	29	SPR2	45	NADC	61	D06
14	A5	30	SPR3	46	BLNK	62	D05
15	A4	31	RSTW	47	NVGV	63	D04
16	A3	32	RSTR	48	NVGH	64	D03

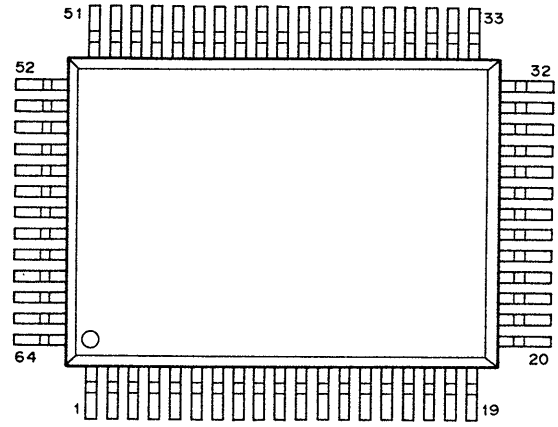


Fig. 3-5-16-2. μPD65006GF-325-3B8 Ext. View

- A0 to A9 ····· I/O address line inputs
- D00 to D07 ···· Data bus line inputs/outputs
- NIOR ····· I/O read strobe input
  Active low.
- NIOW ····· I/O write strobe input
  Active low.
- AEN ····· Address bus enable input
  Active high.
- RST····· Reset input
  Reset applied when high.
- GATE ····· Data bus gate signal output
  Active low.
- NRST ····· Reset output
  Inverted RST (pin 6).

Terminal function (Cont.)

- IREG ····· IBM registers enable signal output
  This signal inputs to IREG (pin 99) of the gate array IC021 (μPD65013S-526).
- SREG ····· Sony registers enable signal output
  This signal inputs to SREG (pin 62) of the gate array IC021.
- CKD2 ····· Clock divide by two, output
  This signal uses to generate dot clock used within IC021.
  Low level is output for the horizontal 640-dot display mode.
  A clock with a frequency 1/2 of IDCK (pin 50) is output for the horizontal 320-dot display mode. Refer to Section 3-5-16-3.
- EXG ····· External GATE control signal input
  Fixed high level. When EXG is low level, disable GATE (pin 5).
- REN ····· I/O read enable signal input
  Active high, fixed high level. When REN is low level, can not be read from the Sony registers within the gate array IC021.
- SPR1 ····· Spear read terminal 1
  Can be read from bit 3 of port ××CH. Unused terminal in this board.
- SPR2 ····· Spear read terminal 2
  Can be read from bit 4 of port ××CH. Unused terminal in this board.
- SPR3 ····· Spear read terminal 3
  Can be read from bit 5 of port ××CH. Unused terminal in this board.
- SPW1 ····· Spear write terminal 1
  Can be write from bit 3 of port ××H. Unused terminal in this board.
- SPW2 ····· Spear write terminal 2
  Can be write from bit 4 of port ××DH. Unused terminal in this board.
- SPW3 ····· Spear write terminal 3
  Can be write from bit 5 of port ××DH. Unused terminal in this board.
- RSTR ····· Reset read signal outputs for line memories
  This signal inputs to the reset read (pin 19) of the line memories IC014 to IC016 (each μPD42102).
- RSTW ····· Reset write signal outputs for line memories
  This signal inputs to the reset write (pin 6) of the line memories IC014 to IC016.
- GEAU ····· Indication output of genlock-auto mode
  Can be write from bit 0 of port ××DH, GEAU is inverse that bit.
  GEAU indicate the genlock mode, low level (that bit set "1") is genlock-internal mode, high level (that bit set "0") is genlock-auto mode.
- NVSV ····· V sync input from video
  Vertical sync from video signal. Negative pulse input.
- NVSH ····· H sync input from video
  Horizontal sync from video signal. Negative pulse input.
- NVGV ····· V sync input from VGA board
  Vertical sync from the VGA-16 board. Negative pulse input.
- NVGH ····· H sync input from VGA board
  Horizontal sync (delayed by IC020) from the VGA-16 board.
  Negative pulse input.
- ADCK ····· A/D conversion clock output
  This clock uses as the write clock (pin 17) of the line memories IC014 to IC016 in this board.
- NADC ····· A/D conversion clock output
  Inverse output of ADCK (pin 44). Inputs to pin 7 of the A/D converters IC008 to IC009 (each CXD1172).
- BLNK ····· Blanking signal input
  Input positive pulse. Can be read from bit 2 of port ×× CH.
- EFCK ····· External feature clock enable signal output
  EFCK is the signal for supplying an external clock to the VGA-16 board.
- IDCK ····· In-board dot clock input
- AS0 to AS2 ···· I/O ports select inputs
  These are terminals for selecting I/O addresses of Sony registers among following values ; 25×H, 26×H, 28×H, 29×H, 2A×H, 33×H, 34×H and 35×H.
  These terminals are connected to J001, which decides the I/O addresses. Refer to the Section 3-5-16-3.
- SW1 ····· Switch input 1
  Be connected with SW001,s sw1 (pin 8). Can be read from bit 0 of port ××CH. Unused its switch in this board.
- SW2 ····· Switch input 2
  Be connected with SW001's sw2 (pin 7). Can be read from bit 1 of port ××CH. Unused its switch in this board.
- NRIN ····· output for reference-in of phase detector
  This signal inputs to RIN (pin 7) of the phase comparator IC034 (CX23065).
- NVIN ····· Output for variance-in of phase detector
  This signal inputs to VIN (pin 6) of the phase comparator IC034.
- CSYC ····· Composite sync output
  Open drain output. Negative pulse output.

3-6. SWITCHING REGULATOR

3-6-1. Outline

The switching regulator of this unit consists of three circuit boards ··· A board, B board and C board ··· and it is divided into the following blocks :

(1) Primary side
   a. Primary voltage and rectifier circuit, contained in A board
   b. Switching oscillator circuit for standby use, contained in A board
   c. Main switching circuit, contained in B board

(2) Secondary side
   a. Power-on circuit, contained in C board
   b. Switching control circuit, contained in C board
   c. + 5V, + 12V, − 12V and − 5V rectifier circuit, contained in B board
   d. POWER GOOD circuit, contained in C board
   e. Excessive-current and overvoltage detector circuit, contained in C board

   The following describes the functions of the main circuits.

3-6-2. Switching Circuit for Standby Use

When the Main Power Switch located at the rear of the unit is turned on, the AC power is rectified by D101 and the switching circuit for standby use is thereby activated. This switching circuit consists of Q101 and Q102 and T101, and it generates approximately 150 kHz rectangular waves. The secondary side of T101 rectifies this rectangular wave to output + 12V (EVER 12V). When EVER 12V is supplied to C board, the circuit is put into a standby state.

3-6-3. Main Switching Circuit

Comprised of T103, Q103 and T102, this circuit is driven by 85 kHz rectangular waves which are output by IC301 (MB3759) mounted on C board.

3-6-4. POWER ON Circuit

When the Main Power Switch is turned on and the Power Switch on the front panel of the unit is pushed, all the power of the unit turns on. As the + 12V line rises, RELAY 102 turns on, letting the AC power be supplied to AC OUTLET. When the Power Switch on the front panel of the unit is turned on, the POWER ON ($\overline{\text{REMOTE}}$) line is grounded. Thereby Q302 on C board triggers switching-start to IC301.

3-6-5. Switching Control Circuit

IC301 in C board generates 85 kHz rectangular waves. If the + 5V voltage fluctuates, the DC voltage on the secondary side is controlled by controlling the width of these rectangular waves.

3-6-6. P.G. (POWER GOOD) Circuit

This circuit consists of two regulators ··· IC302 (1/4) (μPC324C) and IC303 (PST520C) and IC304 (PST520C). P.G. is output at 100 to 500 msec after the + 5V voltage rises.
P.G. serves as a reset signal for the system controller on the PU-59V board and a sound mute signal on the IF-156V board.

3-6-7. Overcurrent Detector Circuit

By detecting changes of voltage in the detection resistor on the ground side of the − 12V, + 12V and + 5V lines with IC302. Overcurrent point of + 5V is adjusted by VR204. Overcurrent point of + 12V is adjusted by VR203.

3-6-8. Control of + 12V Overvoltage

+ 12V is output after being rectified by D213. As + 12V rises high, a current flows in the L203 saturable reactor through Q202 and D215, thereby controlling the output voltage.

3-6-9. Protection of + 5V Overvoltage

If the + 5V line rises above + 5.8V, D305 (5.6V Zener) and thyristor SCR301 (03P2M) are turned on. As result, the output of the main switching is stopped.

3-7. KEYBOARD

3-7-1. Outline

Main features are as follows :

- Communications system
  A bidirectional, clock-synchronized serial communication. Refer to Section 3-7-2.

- Key code
  Sends a make code when the key is pushed and a break code when the key is released. Three sorts of codes are transmitted. Refer to Section 3-7-3.

- Keyboard buffer
  The keyboard comes with a 16 keys capacity FIFO (First In First Out) buffer to keep data until the system becomes ready to receive it. When the 17th data is generated, an overrun code is input to the 17th place of the buffer. If any key is pushed further, it is ignored.

- Repeat function
  If any key is held pushed, the make code is continuously sent until the key is released. While two keys or over are held pushed simultaneously, the make code is sent for the key that was pushed later. When that key is released, the repeat function is canceled (cancelled) regardless of whether the other key that was pushed first remains pushed.

- Self diagnostic test
  When the power is turned on or the reset command is received, the keyboard performs the self-diagnostics test as follows :

  ① Check sum of ROM
  ② Check of RAM
  ③ Check of LED lighting (All LEDs are lit for 30msec.)

  After the test is finished, when the interface is enabled, the keyboard sends a completion code AAH/FCH if terminated normally/abnormally.

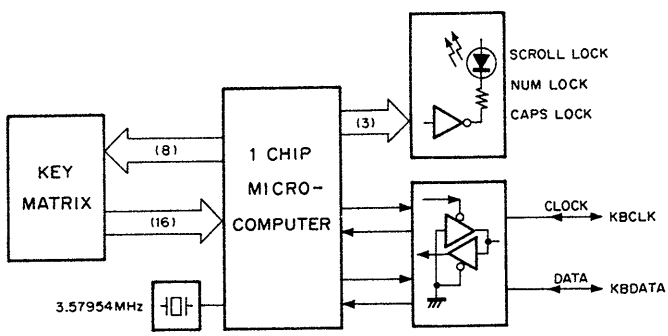


Fig. 3-7-1. Keyboard Block Diagram

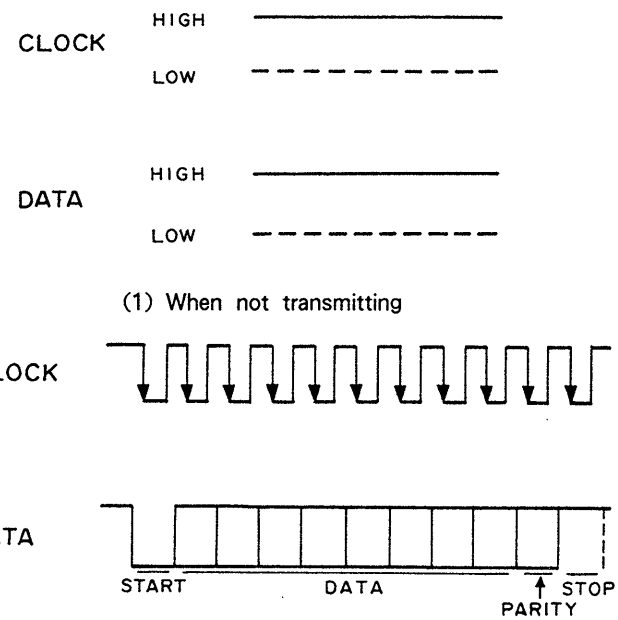
3-7-2. Communication Format

The keyboard and the (computer) system communicate with one another through CLOCK (KBCLK) line and DATA (KBDATA) line. While no communication is being performed, both the two lines are at the high level. Also refer to Fig. 3-7-2 (1). Open collectors are used for both the keyboard and the system, so that the two lines can be made to low level from either side. During communication, the keyboard sends a synchronization clock of approx. 16.6kHz. Also refer to Fig. 3-7-2 (2). Transmitting data format is as follows, also refer to Fig. 3-7-2 (2).

1st bit····· Start bit
2nd bit····· Data bit 0 (LSB)
3rd bit····· Data bit 1
4th bit ····· Data bit 2
5th bit ····· Data bit 3
6th bit ····· Data bit 4
7th bit ····· Data bit 5
8th bit ····· Data bit 6
9th bit ····· Data bit 7 (MSB)
10th bit····· Odd parity bit
11th bit····· Stop bit

3-7-2-1. Transmission from keyboard

See Fig. 3-7-2. Before sending any data, the keyboard first checks the status of CLOCK line and DATA line. When both are found high level, it assumes ready to send and starts sending data to the computer system. Even during the transmission of data, the keyboard checks the CLOCK line at least every 60 μsec. If the system forcibly sets it to low level, the keyboard assumes that data transmission is inhibited and immediately stops transmission.



(2) When transmitting to system

Fig. 3-7-2. Keyboard Output Data Timing

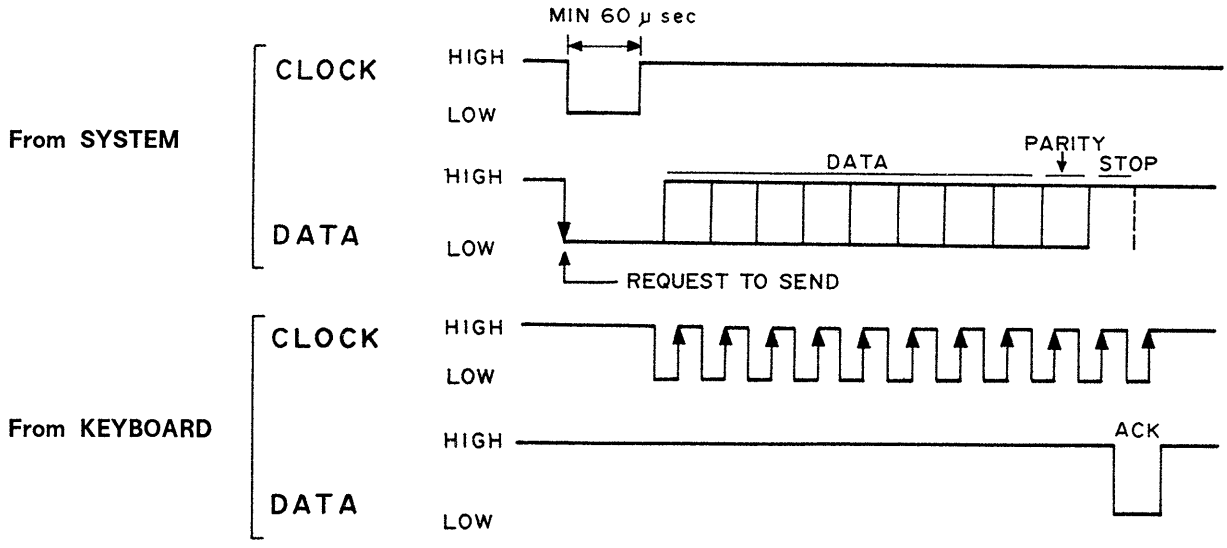


Fig. 3-7-3. Received Data Timing

3-7-2-2. Transmission to keyboard

See Fig. 3-7-3.

When sending command or option byte (parameter/data) to the keyboard, the system first changes DATA line to low level (request to send) while at the same time lowering the CLOCK line level for a duration of at least 60 μsec. When DATA line was set to low level, the keyboard waits for data to be sent from the system. Note that lowering the CLOCK line level makes it possible to inhibit transmission from the keyboard to the system, as well as to interrupt transmission if any data was being transmitted to the system.

When data from the system has been correctly received, the keyboard lowers the DATA level upon the reception of a stop bit in the 11th bit of data. By a change of the DATA line level the system confirms that the keyboard has received data correctly.

Interface Control

CLOCK	DATA	Function
H	H	Enable transmission of the keyboard.
*L	X	Inhibit transmission of the keyboard.
X	L	Request to send, to the keyboard.

* : It goes to low level for more than 60 μsec.
X : Don't care.

3-7-2-3. Command information

When a command is sent the keyboard responds to it within 20 msec.

1. Keyboard input command code

Receiving codes from the system.

- Reset (FFH)
  Puts the keyboard into the same state, as the power has been reset. Performs self-diagnostic test, clears the keyboard buffer, and sets the default values of repeat time and repeat cycle.
- Resend (FEH)
  Resends data that was previously sent.
- NOP (F7H – FDH)
  After sending an ACK code, the keyboard continues scanning.
- Set default (F6H)
  After clearing the keyborad buffer and setting the default values of repeat time and repeat cycle, the keyboard continues scanning.
- Default disable (F5H)
  Performs the same operation as with "Set default", except that the keyboard stops scanning and waits for the next command.
- Enable (F4H)
  By clearing the keyboard buffer, starts scanning.

- Repeat time and Repeat cycle setting (F3H)
  See Fig. 3-7-4. By this command and a subsequent 1 byte parameter, the system can change the repeat time (the time the key is pushed until repeat starts) and repeat cycle (the time intervals of repeat operation).
  The bit confifuration of the parameter is as follows :

  Bits 0 – 3 ····· RC1 ; Repeat cycle parameter 1 (0 – 7)
  Bits 3 and 4 ···· RC2 ; Repeat cycle parameter 2 (0 – 3)
  Bits 5 and 6 ···· RT ; Repeat time parameter (0 – 3)
  Bit 7 ····· Unused, fixed "0".

Repeat time = (1 + RT) × 250 [msec.]
Repeat cycle = (8 + RC1) × 2^{RT2} × 4.17 [msec.]

Note : The default values of repeat time is 500msec ± 20%.
The default values of repeat cycle is 100msec ± 20%.

- Keyboard ID (F2H)
  When this command has been received, the keyboard sends an ACK code and then the codes ABH and 83H which denote the 101 enhanced keyboard.

- Key code select (F0H)
  By this command and a subsequent option byte, the system changes the key codes sent from the keyboard. Refer to Section 3-7-3.

- Echo (EEH)
  Upon reception of this command, the keyboard sends EEH and continues scanning.

- LED control (EDH)
  By this command and a subsequent option byte, the system flickers the LED mode indicators on the keyboard. The bit configuration of the option byte is as follow :

LED Control

Bit	Function
0	SCROLL LOCK LED turn on/$\overline{\text{off}}$.
1	NUM LOCK LED turn on/$\overline{\text{off}}$.
2	CAPS LOCK LED turn on/$\overline{\text{off}}$
3-7	Unused, fixed "0".

2. Keyboard output command/code

Transmitting codes to the system.

- Resend command (FEH)
  The keyboard sends a resend code when it has received nonexistent commands or invalid option bytes (parameter /data) from the system, or when a Parity error has occurred to it.

- ACK code (FAH)
  The keyboard sends an ACK (Acknowledge) code when it received commands other than echo and resend.

- Overrun code (00H)
  An overrun code is written into the keyboard buffer in the following two cases.
  (1) When the keyboard buffer is filled. At this time an overrun code is written to the 17th place of the buffer which contains the last code.
  (2) When two or more keys were pushed simultaneously and the keyboard could not identify which key was pushed.

- Break code (F0H)
  This code is the first one byte of the break code which indicates that the key was released.

- Self-diagnostic test, normally code (AAH)
  When self diagnosis is terminated normally, this code is sent from the keyboard.

- Self-diagnostic test, abnormally code (FCH)
  If any fault is found by self-diagnostic, this code is sent from the keyboard.

- Keyboard ID code (ABH, 83H)
  This code is send in response to the keyboard ID command from the system.

- Answer echo code (EEH)
  This code is send in response to the echo command from the system.

3-7-3. Key Code

The 8-bit make code and the brake code are assigned to each key on the keyboard. Sends a make code when the key is pushed and a break code when the key is released. Three sorts of codes are transmitted.
Which key code to output is determined by the command of the F0H + option byte sent from the system. Also, this transmitting key cord is selected any of three cords from F0H (key code selection) + option byte command sent from the system.

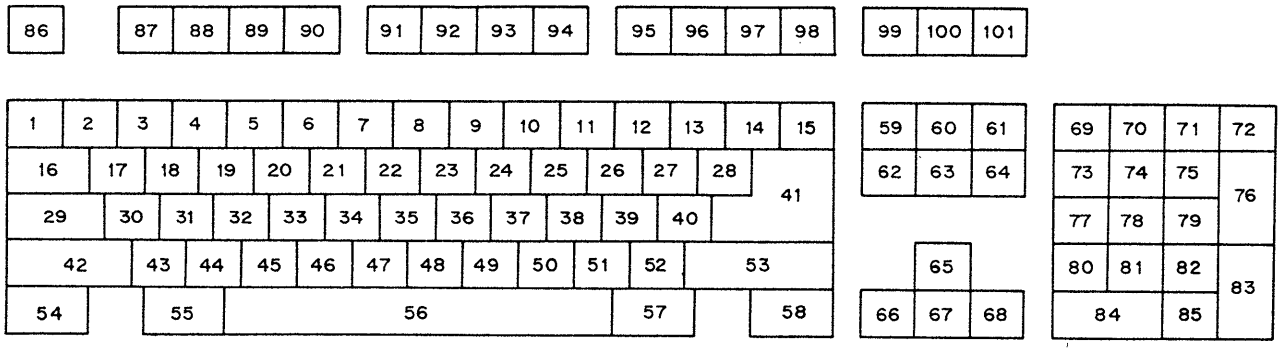


Fig. 3-7-4. Key Arrangement and Switch Number

Keyboard Output Code (PC-AT Version) Table 1

Switch Number	System Code F000/F002		System Code F001		System Code F003	
	Make Code	Break Code	Make Code	Break Code	Make Code	Break Code
1	0E	F00E	29	A9	0E	
2	16	F016	02	82	16	
3	1E	F01E	03	83	1E	
4	26	F026	04	84	26	
5	25	F025	05	85	25	
6	2E	F02E	06	86	2E	
7	36	F036	07	87	36	
8	3D	F03D	08	88	3D	
9	3E	F03E	09	89	3E	
10	46	F046	0A	8A	46	
11	45	F045	0B	8B	45	
12	4E	F04E	0C	8C	4E	
13	55	F055	0D	8D	55	
105	5D	F05D	2B	AB	53	
102	66	F066	0E	8E	66	
16	0D	F00D	0F	8F	0D	
17	15	F015	10	90	15	
18	1D	F01D	11	91	1D	
19	24	F024	12	92	24	
20	2D	F02D	13	93	2D	
21	2C	F02C	14	94	2C	
22	35	F035	15	95	35	
23	3C	F03C	16	96	3C	
24	43	F043	17	97	43	
25	44	F044	18	98	44	
26	4D	F04D	19	99	4D	
27	54	F054	1A	9A	54	
28	5B	F05B	1B	9B	5B	
29	58	F058	3A	BA	14	F014
30	1C	F01C	1E	9E	1C	

Note : The code shown in table is a hexadecimal code.

Keyboard Output Code (PC-AT Version) Table 2

Switch Number	System Code F000/F002		System Code F001		System Code F003	
	Make Code	Break Code	Make Code	Break Code	Make Code	Break Code
31	1B	F01B	1F	9F	1B	
32	23	F023	20	A0	23	
33	2B	F02B	21	A1	2B	
34	34	F034	22	A2	34	
35	33	F033	23	A3	33	
36	3B	F03B	24	A4	3B	
37	42	F042	25	A5	42	
38	4B	F04B	26	A6	4B	
39	4C	F04C	27	A7	4C	
40	52	F052	28	A8	52	
41	5A	F05A	1C	9C	5A	
42	12	F012	2A	AA	12	
43	1A	F01A	2C	AC	1A	
44	22	F022	2D	AD	22	
45	21	F021	2E	AE	21	
46	2A	F02A	2F	AF	2A	
47	32	F032	30	B0	32	
48	31	F031	31	B1	31	
49	3A	F03A	32	B2	3A	
50	41	F041	33	B3	41	
51	49	F049	34	B4	49	
52	4A	F04A	35	B5	4A	
53	59	F059	36	B6	59	F059
54	14	F014	1D	9D	11	F011
55	11	F011	38	B8	19	F019
56	29	F029	39	B9	29	
57	E011	E0F011	E01D	E09D	39	
58	* E014	* E0F014	** E04B	** E0CB	58	
59	* E070	* E0F070	** E052	** E0D2	67	
60	* E06C	* E0F06C	** E047	** E0C7	6E	
61	* E07D	* E0F07D	** E049	** E0C9	6F	
62	* E071	* E0F071	** E053	** E0D3	64	
63	* E069	* E0F069	** E04F	** E0CF	65	
64	* E07A	* E0F07A	** E051	** E0D1	6D	
65	* E075	* E0F075	** E048	** E0C8	63	
66	* E06B	* E0F06B	** E04B	** E0CB	61	
67	* E072	* E0F072	** E050	** E0D0	60	
68	* E074	* E0F074	** E04D	** E0CD	6A	
69	77	F077	45	C5	77	
70	E04A	E0F04A	E035	E0B5	4A	
71	7C	F07C	3F	BF	7E	
72	7B	F07B	4A	CA	84	
73	6C	F06C	47	C7	6C	
74	75	F075	48	C8	75	
75	7D	F07D	49	C9	7D	

* ; When the key is "Num Lock" state, E012 is added before the make cord and E0F012 before the break cord.
** ; When the key is "Num Lock" state, E02A is added before the make cord and E0AA before the break cord.

Note : The code shown in table is a hexadecimal code.

Keyboard Output Code (PC-AT Version) Table 3

Switch Number	System Code F000/F002		System Code F001		System Code F003	
	Make Code	Break Code	Make Code	Break Code	Make Code	Break Code
76	79	F079	4E	CE	7C	
77	6B	F06B	4B	CB	6B	
78	73	F073	4C	CC	73	
79	74	F074	4D	CD	74	
80	69	F069	4F	CF	69	
81	72	F072	50	D0	72	
82	7A	F07A	51	D1	7A	
83	E05A	E0F05A	E01C	E09C	79	
84	70	F070	52	D2	70	
85	71	F071	53	D3	71	
86	76	F076	01	81	08	
87	05	F005	3B	BB	07	
88	06	F006	3C	BC	0F	
89	04	F004	3D	BD	17	
90	0C	F00C	3E	BE	1F	
91	03	F003	3F	BF	27	
92	0B	F00B	40	C0	2F	
93	83	F083	41	C1	37	
94	0A	F00A	42	C2	3F	
95	01	F001	43	C3	47	
96	09	F009	44	C4	4F	
97	78	F078	57	D7	56	
98	07	F007	58	D8	5E	
99	E012E07C	E0F07CE0F012	E02AE037	E0B7E0AA	57	
100	7E	F07E	46	C6	5F	
101	E11477E1 F014F077		E11D45E19DC5		62	

Note : The code shown in table is a hexadecimal code.

CHAPTER 8
ADJUSTMENT

There is a LDP-1500-type videodisc player mounted on the VIW-3015A. Disconnect it as explained in Chapter 2 before adjustment.

8-1. TOOLS LIST

In general, adjustment of this unit requires the following equipments :

1. Checker VIW-3015A
2. Monitor (CPD-1302 etc.) and Monitor cable
3. SMW-3001B (MS-DOS)
4. Accessories floppydisk and AV cable
5. Frequency counter
6. Oscilloscope (refer to section 8-4-1-2)
7. EIA color-bar signal generator (refer to section 8-4-1-3)
8. IF-156 extension board : P/N J-6093-380-A
9. PU-59 extension board : P/N J-6093-540-A
10. Two extension boards : P/N J-6093-490-A 2 sets
11. Screwdrivers for adjustment
12. Soldering iron and solder

8-2. IF-156VA BOARD

8-2-1. Preparation

Insert the IF-156 extension board (J-6093-380-A) into a slot A for the IF-156VA board, and the IF-156VA board to adjust into this extension board.
Have to exact connect, because, to prevent troubles.
Power ON, the computer and frequency counter.

8-2-2. RTC Clock Adjustment

Measuring equipment : Frequency counter
Measuring point : TP204
Specification : 32,768 ± 0.1Hz
Adjustment : CV201

8-3. PU-59VA BOARD

8-3-1. Preparation

Insert the PU-59 extension board (J-6093-540-A) into a slot B for the PU-59VA board, and the PU-59VA board to adjust into this extension board.
Have to exact connect, because, to prevent troubles.
Power ON, the computer and frequency counter.

8-3-2. System Clock Adjustment

Measuring equipment : Frequency counter
Measuring point : TP301
Specification : 14,318,180 ± 100Hz
Adjustment : CV301

8-4. VS-38A BOARD

8-4-1. Preparations

8-4-1-1. Installing

1. Referring to Section 2-1-4 (① through ③), remove the VS-38A board from slot 5 and insert the extension board (J-6093-490-1) in its place.
2. Referring to Section 2-1-4 (④ and ⑤), remove the VGA-16 board from slot 4 and insert the extension board (J-6093-490-1) in its place.
3. Attach the VS-38A board and the VGA-16 board to the extension boards.
4. Attach the cable (referring to ① of section 2-1-4) to the VS-38A board and the VGA-16 board.
5. Attach the AV cable to CN004 (AV IN) of the VS-38A board.

8-4-1-2. About Oscilloscope

An oscilloscope capable of following three or more waveforms (or two, if it has an external trigger input terminal) and provided with a TV sync (field, line) separator is required for adjustment of the VS-38A board.

- Band width limit
  This function restraints high-frequency components to make the waveform easier to observe. However, adjustment is also possible without this function.

- TV-LINE and TV-FLD
  Shows the TV sync separator trigger mode.

8-4-1-3. About Video signal

EIA standard color-bar signal (NTSC, setup 0%, white level 100%, 1Vp-p) is used as the video signal for the adjustment. While adjust the VS-38A board, must always give this signal to the VS-38A board.

8-4-1-4. Initial setting

DISP. BOARD switch is C side.
STARTING DEV switch is FD.AUTO side.
Refer to section 1-2-3.

- VGA-16 Board
  SW1 ····· Only No.4 ON
  W1 ····· Connected
  W2 ····· Connected, below
- VS-38A Board
  J001 ····· All 0 side
  J003 ····· 0 side
  SL001 ····· Short by the solder
  SL002 ····· Short by the solder
  SL003 ····· Default setting*
  SL004 ····· Default setting*
  SW001 ····· Only No.3 OFF

* ; Connected by a lead cable when both SL003 and SL004 are open. Refer to the circuit diagram at the bottom of page 4-14.

8-4-10. Vertical Reset Timing Adjustment

Key operation : Cursor down key, twice
Measuring equipment : Oscilloscope
Vertical mode : CHOP
Trigger channel : ch-3
Trigger slope : Up edge
Trigger coupling : TV-FLD
Measuring point ch-1 : TP009 (coupling : DC)
Measuring point ch-2 : TP016 (coupling : DC)
Measuring point ch-3 : TP017

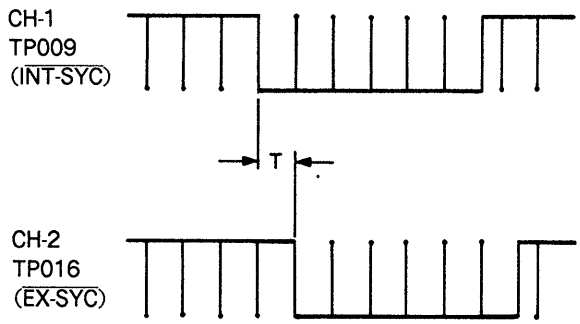


Fig. 8-4-10. TP009, TP016

Specification : T = ± 0.5H
Adjustment : RV010

Note : Set oscilloscope to 50 µsec/DIV.

8-4-11. H Position Adjustment

Measuring equipment : Oscilloscope
Vertical mode : ALT, Band width limit (20MHz)
Trigger channel : ch-2
Trigger slope : Down edge
Trigger coupling : DC
Measuring point ch-1 : TP002 (coupling : AC)
Measuring point ch-2 : TP010 (coupling : DC)

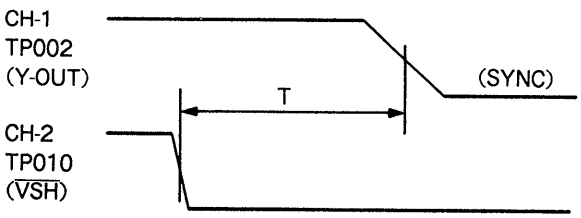


Fig. 8-4-11. TP002, TP010

Specification : T = 700 ± 20nsec
Adjustment : RV009

Note : Set oscilloscope to 20nsec/DIV, 0.1V/DIV at ch-1, and 2V/DIV at ch-2.

8-4-12. Vertical Blanking Adjustment

Measuring equipment : Oscilloscope
Vertical mode : ch-1
Trigger channel : ch-1
Trigger slope : Up edge
Trigger coupling : DC
Measuring point ch-1 : TP021 (coupling : DC)

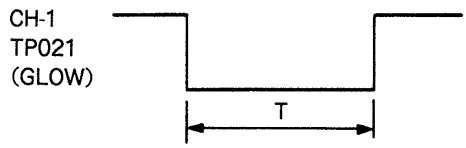


Fig. 8-4-12. TP021

Specification : T = 965 ± 20 µsec
Adjustment : RV011

8-4-13. Data Latch Clock Confirmation

Measuring equipment : Oscilloscope
Vertical mode : CHOP
Trigger channel : ch-2
Trigger slope : Up edge
Trigger coupling : DC
Measuring point ch-1 : TP018 (coupling : DC)
Measuring point ch-2 : TP019 (coupling : DC)

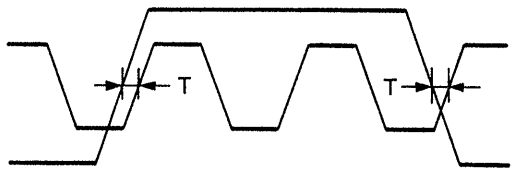


Fig. 8-4-13. TP018, TP019

Confirmation : T = ± 5nsec

Nonstandard case :
Remove the default set (refer to "* ;" on Section 8-4-1-4). T should fall within specifications when one of the three connection methods (SL003 or SL004 short-circuit, and lead cable), except the default one, is used.

Note : Set oscilloscope to 2V/DIV and 10nsec/DIV.

8-4-14. Setting in After Adjustment

- VGA-16 Board ..... Unchanged
- VS-38A Board
  - J001 ..... All 0 side
  - J003 ..... 0 side
  - SL001 ..... Short by the solder
  - SL002 ..... Open
  - SL003, SL004 ..... Refer to Section 8-4-13
  - SW001 ..... All ON side

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