THEORY OF OPERATION

Refer to the simplified block diagram of the Microprocessor showing the relationship of its major subassemblies.

Data from either the Read Only Memory (ROM) or from the keyboard is supplied to the ROM Multiplexer (Figure 4-2) which multiplexes 10 data bits from the ROM or 8 data bits from the keyboard. Depending upon which input is enabled, the 10 outputs are bussed to the Input Buffer Register (IBR/AUX), the IBR Multiplexer (IBR/MUX), the Channel Select/Interface, Flag, Master Control, Switch and Read Only Memory Address Register (RAR/MUX) as a paralled input.

With ROB signal high, keyboard data is enabled through the ROM Multiplexer (MP04-1) and supplied as inputs to the Buffer Multiplexer (MP12) which multiplexes the parallel inputs to the IBR. The ROB signal indicates whether or not the processor is busy. If the ROB signal is high, it indicates a "processor busy" condition and data from the ROM is enabled through the ROM Multiplexer. During this time, the keyboard data is temporarily shut off from the processor.

Assuming a ROB high condition, a data word from the keyboard is gated through the ROM Multiplexer. An XRI signal is generated by the Master Control thus gating the keyboard data through the Buffer/Multiplexer into the IBR. From the IBR, outputs are provided to the selected data channels or to the Main Memory for sub-

sequent display.

GENERAL PURPOSE SECTION

The general purpose section performs three functions common to any machine functional organization. These sections are:

(a) Input Control Unit - Selects and controls the transfer of data and control characters from the four primary storage areas: external devices, the recirculating main memory storage, the auxiliary storage registers, and the ROM.

(b) ROM Control Unit - Provides the control necessary to implement sequencing through a routine. It includes selection of the instruction to be executed, decoding of the type of instruction, and generation of execution commands which a particular functional unit will use to activate its logic. Not all instructions executed are functional section instructions. As will be determined in discussing each section of the general purpose unit in detail, some instructions are special purpose instructions.

(c) Output Control Unit - Selects controls and transfers characters to one of the three output channels: external, main memory, or auxiliary registers.

INPUT CONTROL UNIT

The input control unit is used to transfer the externally generated characters into the processor. It consists essentially of a set of selection gates; selection flags and ROB gates activate lines for the external inputs.

Inputs can originate from four general areas: external devices, main memory, auxiliary registers (2), or the ROM itself.

There are five sources of external data: VT1, VT2, DC1, DC2 and Keyboard. All input characters from these sources are in ASCII code. The eighth bit (MSB) of the inputted data character is used to differentiate between control characters and data characters.

Data and control characters can be externally inputted only when the Microprocessor is not BUSY. A flag termed ROB (Read Only Busy) performs this lock-out control and lights a lamp labelled BUSY on the Control Panel.

The "activate" line (Kx) from the inputting device turns ROB on (BUSY) and generates a signal which sets the R/E control, which in turn "starts" the Microprocessor.

The two auxiliary storage registers can only transfer, under microprogram control, to and from the Input Buffer Register (IBR). The auxiliary storage registers are named AUX and TEMP.

The main memory is broken down into five parallel sections: WRITE, READ, MASTER, CONTROL 1, and CONTROL 2. These five names should not be regarded here as operations pertaining to the general purpose section. They are merely names affixed to sections of memory for functional use. Each section holds 80 characters and each character is eight bits long.

A set of mutually exclusive selection flags determines what device (the particular external or the particular main memory section) will be able to input characters. These flags are set under microprogram control. This occurs through the Main Memory Read (MMR) instruction. This command activates the main memory selection gates and stops the instruction cycle. Data is read out of memory into the IBR when the static column counter matches the memory dynamic column count. The instruction cycle must be stopped during this operation since the match can vary in time depending on the position count when the read instruction is initially given. This match time can be as great as 250 microseconds.

ROM CONTROL UNIT

The ROM control unit is responsible for reading the address to be executed, decoding the instruction and providing the proper operation pulse to execute the instruction.

A ROM address may contain one of three types of instruction words. They are labelled execute logic enabler, execute data, and jump.

Associated with each word are two bit positions defining the Operation Code (OP Code). The OP code can be either JUMP (JMP), SET, RESET (RST), or TEST (TST).

The configuration of the ROM word is:

ROM Bit No.

11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X

OP Code Information

The OP codes are: ROM Bir No.

11	10	Operation
0	0	JMP
0	1	SET
1	0	RST
1	1	TST

(a) Execute Logic Enabler (LE) Word

11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X

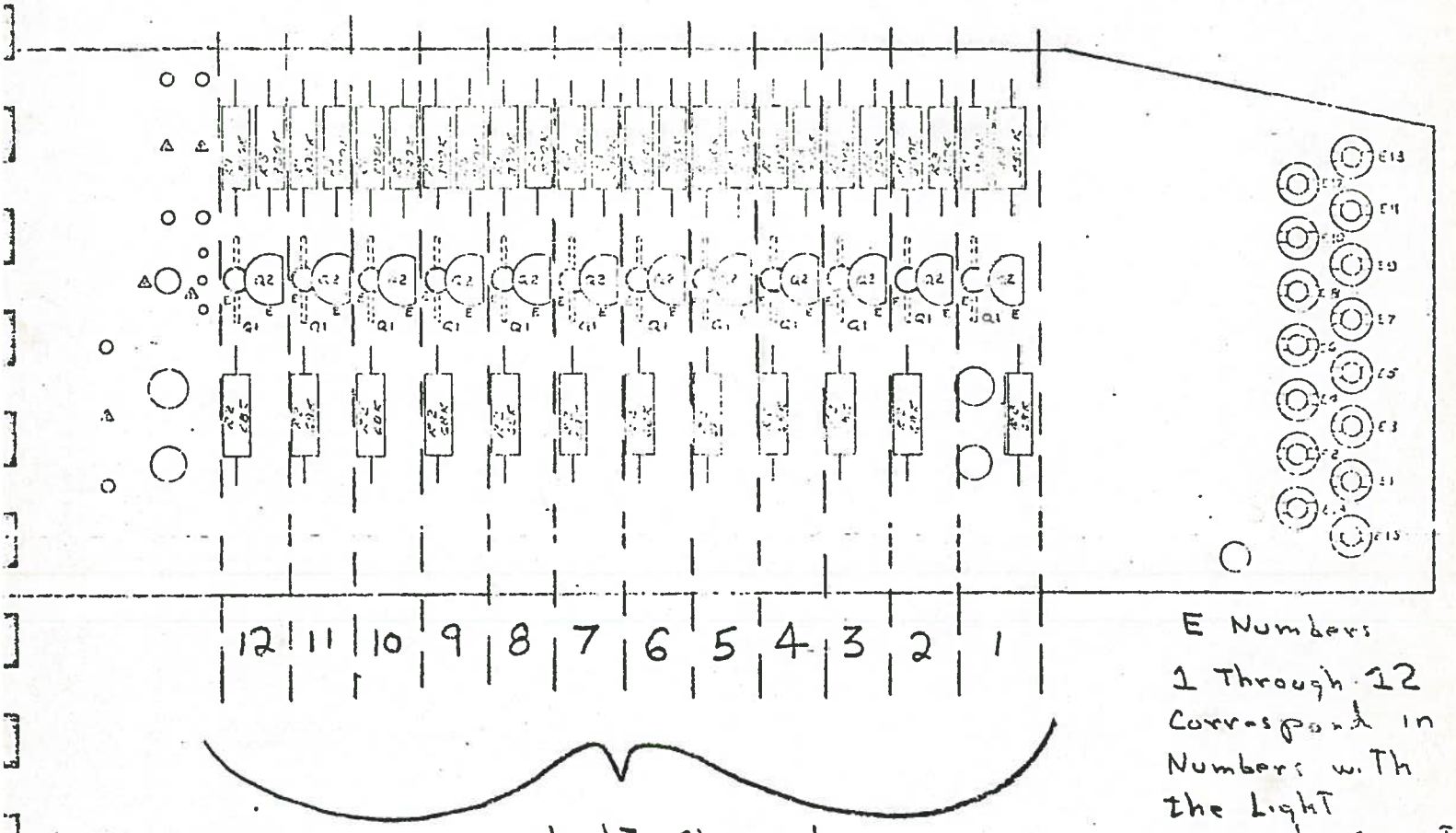
OP Code

(Not JMP) Logic Enabler Code

The execute LE ROM word addresses (as defined by the LE code) a particular portion of the Microprocessor where the execution (as defined by the OP code SET, RST or TST) is to take place. Bit eight, of the ROM word, in conjunction with the EXECUTION pulse, is used for unconditionally resetting the R/E flip-flop coincident with the execution of the operation specified (by the OP code and LE code). The resetting of the R/E will cause the Microprocessor to "halt" (ROB still busy) for any asynchronous operation (such as main memory Read or Write, etc.). The device addressed will, when appropriate, signal the restart of the processor by setting the R/E. The execute logic enabler word is defined as JMP-ROM# 9.

The SET OP code during the execution phase of the control cycle will usually cause the setting of the addressed (by means of decoding the LE's) flip-flop, the RESET (RST) OP code will usually reset the addressed flip-flop. The TEST (TST) OP code, during the execution phase of the control cycle, will usually cause the testing of an addressed flip-flop, decoder or control level, thus providing a "branching" capability. The branching is implemented by causing the result of true test to "do nothing", but a false test causes the RAR to be stepped (incremented by 1) during the execution phase in addition to being stepped again by the normal step phase following the execution phase of the two-phase control cycle.

The actual action cause by the SET, RST or TST OP codes is, of course, arbitrary as the execute pulses are provided to activate



Light Channel Circuits

E Numbers 1 Through 12 Correspond in Numbers with the Light Channels Circuit Referred To in Service Step 6 Table for Signal Identification.

Figure 5

Service Step 6 - Cable Continuity Check

Check continuity, using an ohmmeter, between the points indicated below.

FROM PIN	TO TERMINAL	SIGNAL	FUNCTION
2	E12	AD0	DATA
3	E11	AD1	DATA
4	E10	AD2	DATA
5	E9	AD3	DATA
6	E8	AD4	DATA
7	E7	AD5	DATA
8	E6	AD6	DATA
9	E5	AD7	DATA
10	E4	S0	SHIFT
11	E3	S1	SHIFT
12	E2	S2	SHIFT
13	E1	R/C	REPEAT
14	E14	VDD	-14 Volts
15	E15	Ground	Ground
16	XMFR-T1	115 VAC (Hot)	Optical Lights
17	XMFR-T2	115 VAC (Neut)	Optical Lights
18	E17	Chassis GND	Chassis Ground
19	E17	Chassis GND	Chassis Ground
20	INNTER SHIELD	INNER Shield	Shield
21	OUTER SHIELD	Outer Sheild	Shield
23	TO ALERT LAMP	KBLT	Keyboard Alert Light

If a discontinuity is observed, examine the cable to determine the cause. For service to a pin, refer to Service Step 1.

Service Step 7 - Service to Sticky Keys

1. Check for binding of the keys against the cover. If such binding exists, loosen the 8 screws on the bottom of the case and move the chassis so that the keys no longer touch the case. Retighten the 8 screws.

2. For keys sticking for other reasons, remove the cover and observe action of the key shaft. Some of the more likely problems and their solution are listed below.

PROBLEM	SOLUTION
Key shaft jammed out of line with rear spring reed.	Lift key shaft over spring height and shaft should re-align itself.
Excess adhesion from front rubber key lever bumper sticking to key shaft.	Remove adhesion from exposed portion of bumper.
Vertical upright.	Rebend carefully.
Front vertical part of key shaft bent in toward keyboard.	Bend out carefully.
Bent rear springs	Rebend into correct position.
Bent key shaft causing rubbing on guides.	Rebend carefully.
Burs on any parts with close tolerances.	Debur using appropriate material, i.e., energy paper, file, etc. Some cases it may be necessary to remove the key shaft in order to file the shaft slot.

Service Step 9 - Keytop Replacement

1. Remove old keytop by gripping firmly with pliers and pulling the keytop off its shaft (see Figure 6).
2. Install new keytop by placing it into position on the shaft and pressing down firmly.

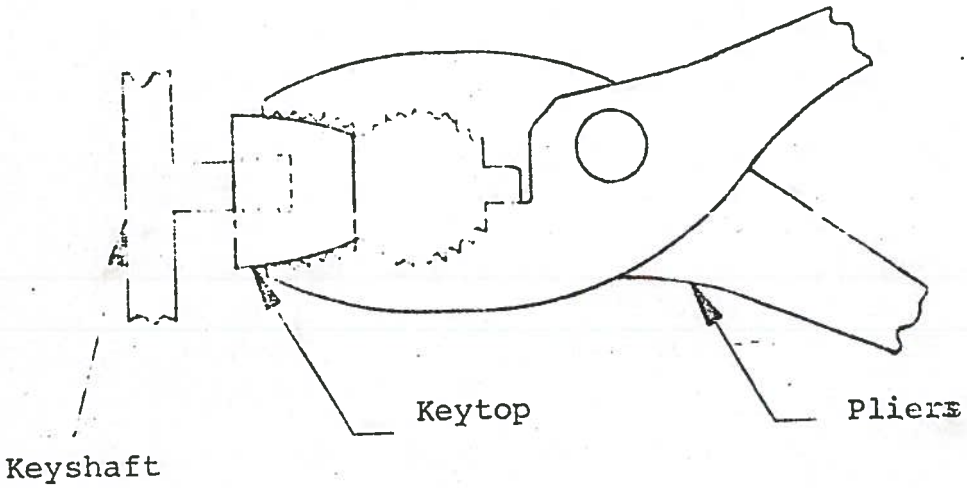


Figure 6