Document No. 154417-340

CIRCUIT CARD DESCRIPTION

INPUT/OUTPUT CARD

TOP ASSY. NO. 154417

CURRENT REVISION
including all changes as of
JUN 29 1976
ENGRG. DATA CONTROL

DSD RELEASE DATE 3-27-74
CATEGORY I RELEASE

PREPARED BY [signature] DATE 3/28/74

APPROVED BY C. Mayer DATE 3/28/74

TOTAL PGS 7

REV	DATE	BY	REVISION DESCRIPTION	APPROVED BY

CIRCUIT DESCRIPTION
INPUT/OUTPUT CARD
154417

1.0 CIRCUIT FUNCTION

The Input/Output, I/O, card is an interface card between the CPU and the other units that are controlled by the CPU. The scheme of the I/O card is a centralized control of the I/O to simplify the interface. The address and data assignments are summarized in figure 1.

1.1 Important Documents

Top Assembly	154417-100
Printed Wiring Master	
Schematic	154417-300
Test Specification	154417-720
Test Procedure	(TBD)

2.0 Electrical Operation

A block diagram of the I/O card is shown in figure 2.

2.1 Lower 8 Bit Address and Data Register with Buffers

The 8 bit data busses from the CPU card are the inputs to the two 4 bit 93L00 registers, U11 and U12. The data enters the registers in parallel thru the P0 - P3 inputs. The Clock on pin 22 normally is high. During T1 time of the CPU cycle, a clock is developed on the CPU card. This clock strobes pin 22 of the I/O card from high-to-low-to-high. The information on the bus is caught on the low to high clock transition. The information is an address when the CPU is fetching data from memory. The information is data during input and output commands.

The inverter chip, U5, inverts the information from the output of the registers and drives the 4 input gate buffers. The 4 input gate chips (U1, U2, U3 and U4) are the eight data buffers to many loads within the subscriber and RAM cards.

2.5 Output Control Pulse Decoder

The function of this circuit is to generate a pulse on a line that is addressed by the accumulator within the CPU during an output instruction. Chip U7 is the output control pulse decoder. The accumulator contents is caught in U12 which drives U7. The addressed output creates a pulse when an Output $37_{(8)}$ command is sent from the CPU.

3.0 Input Characteristics

All input lines are TTL logic levels, i.e., $+2.75 \leq$ High $\leq +5.5$ volts and $0 \leq$ Low $\leq +0.4$ volt.

4.0 Output Characteristics

All outputs are TTL as defined in paragraph 3.0. Rise and fall times are less than 100 nonoseconds.

5.0 Reliability

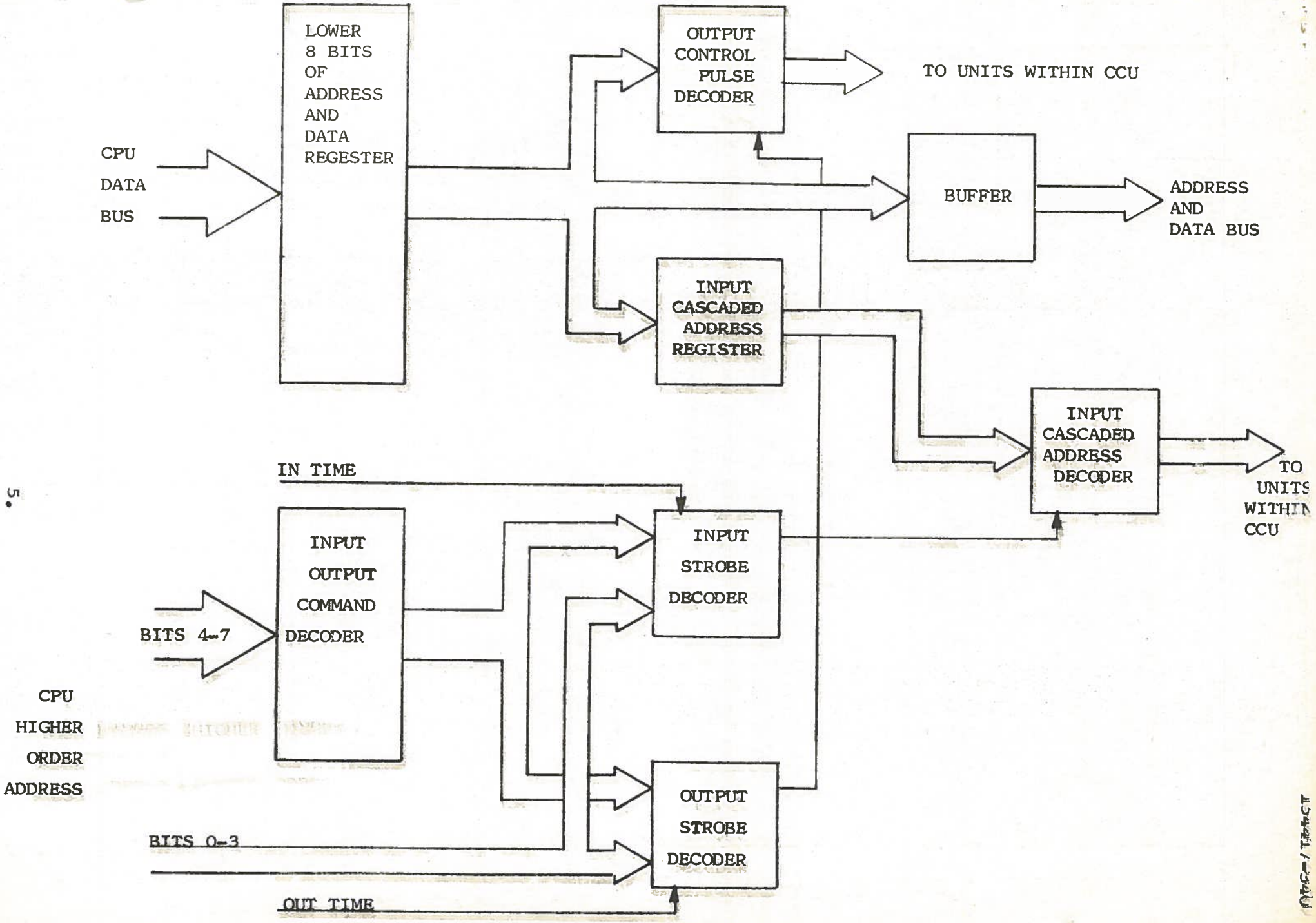
The reliability as calculated for the 154417 is as follows:

@ $50^{\circ}C$ is 2.29 FPM.

6.0 Attachments

Figure 1 - Address and Data Assignments

Figure 2 - Block Diagram of I/O card



Figure

Block Diagram of I/O Card

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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

NOTES: UNLESS OTHERWISE SPECIFIED

A. APPLICABLE DOCUMENTS:

FLOW SOLDER SPEC	893801
CONFORMAL COAT SPEC	893306
MARKING SPEC	894201

B. REFERENCE DOCUMENTS:

SCHEMATIC DIAGRAM	154417-300
TEST SPECIFICATION	154417-720

DO NOT SCALE DWG

INITIAL APPLICATION SHOWN. FOR COMPLETE USAGE DATA, SEE APPLICATION DATA INDEX 126603.

NEXT ASSY	USED ON
154184	TOS2

APPLICATION

UNLESS OTHERWISE SPECIFIED

INTERPRET PER MIL-STD-100. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI-Y14.5. DIMENSIONS ARE IN INCHES. SURFACE TEXTURE SHALL BE ✓. DIMENSIONS APPLY AFTER PLATING. REMOVE BURRS AND SHARP EDGES. PARENTHETICAL DATA FOR INTERNAL LITTON REFERENCE ONLY.

FINISH

TOLERANCES

ON DECIMAL DIMENSIONS	ON ANGULAR DIMENSIONS	
.X ± .1	CHAMFERS	± 5°
.XX ± .03	FORMED	± 2°
.XXX ± .030	LOCATING	± 0°30'
	MACHINED	± 0°30'

MATERIAL

CONTRACT NO. AAE01-72-1-0257

DWN. E. DIERKES

CHK.

ENGR.

TLEC/SYS

DSD

OTHER

LITTON DATA SYSTEMS VAN NUYS, CALIF.

INPUT-OUTPUT – MCS8, CIRCUIT CARD ASSEMBLY

SIZE	CODE IDENT NO.	DRAWING NO.
B	13973	PL 154417

SCALE NONE | WEIGHT | SHEET 1 OF 3

REV

DWG NO. PL 154417

3-2809 (R-3 12/72)

CATEGORY II RELEASE DSD Release Date 1-26-73

PARTS LIST	Litton DATA SYSTEMS VAN NUYS, CALIF.	CONTRACT NUMBER DAAB07-72-C-0257	CODE IDENT 13973	PL 154417	REVISION

TITLE INPUT-OUTPUT – MCS8, CIRCUIT CARD ASSEMBLY

SHEET 2

ITEM NO.	QTY REQD/DASH NO.			-100	UNIT OF MEASURE	CODE IDENT	PART OR IDENTIFYING NUMBER	DRAWING OR DOCUMENT NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REF DES	UNIT WEIGHT	REF SYM	ZONE	LINE REV
1				1			154826		PRINTED WIRING BOARD					
2														
3														
4														
5				5			M39014/01-1474	MIL-C-39014/1	CAPACITOR, 0.1 UF, ±20%, 50V	C1, 2, 4, 5, 6				
6				1			M39003/01-2268	MIL-C-39003/1	CAPACITOR, 3.3 UF, ±10%, 15 V	C3				
7														
8														
9														
10				3			862525-0016	93L00	MED-LOW POWER FOUR-BIT SHIFT REGISTER	U8, 11, 12				
11				1			888995-0002	54LS04	MED-HEX INVERTER, LOW POWER SCHOTTKY TTL	U5				
12				8			888995-0004	54LS138	MED - 3 TO 8 LINE DECODER LOW POWER SCHOTTKY TTL	U7, 9, 10, 14 THRU 18				
13				1			862226-14	MC525	MED-HEX INVERTER TTL-I	U19				
14				4			888997-0032	54H40	MED-DUAL 4 INPUT BUFFER	U1 THRU U4				
15														
16														
17														
18				9			RLR07C102GM	MIL-R-39017/1	RESISTOR, 1.0K, ±2%, 1/4W	R1 THRU R9				

3-2275C (R-1 12/72)

PARTS LIST	Litton DATA SYSTEMS VAN NUYS, CALIF.	CONTRACT NUMBER DAAB07-72-C-0257	CODE IDENT 13973	PL 154417	REVISION

TITLE INPUT-OUTPUT – MCS8, CIRCUIT CARD ASSEMBLY

SHEET 3

ITEM NO.	QTY REQD/DASH NO.			-100	UNIT OF MEASURE	CODE IDENT	PART OR IDENTIFYING NUMBER	DRAWING OR DOCUMENT NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REF DES	UNIT WEIGHT	REF SYM	ZONE	LINE REV
19														
20														
21														
22				AR				QQ-S-571	SOLDER	COMP Sn63 WRMAP2				

3-2275C (R-1 12/72)

EMC

Litton DATA SYSTEMS

ECO

ENGINEERING CHANGE ORDER

CONTROL NO.	1
ECO NO.	A1
DOCUMENT TITLE	PRINTED WIRING BOARD - INPUT-OUTPUT - MCS 8
DOCUMENT NO.	154826
ECR NO	0-43724
PROJECTS AFFECTED	TOS 2
OTHER DOCUMENTS AFFECTED	NONE
REASON FOR CHANGE	CORRECT KEYSLOT LOCATION
EFFECTIVITY	ALL SER NOS 1-3
	☐ FUNC. ☒ MECH.

DESCRIPTION OF CHANGE

ON F/D ZONE 5A VIEW A

IS: KEYSLOT
PINS 35 AND 37

WAS: KEYSLOT
PINS 33 AND 35

P26-L5

Sheet 8-29-73

INTERCHANGEABILITY AFFECTED YES ☐ NO ☐		CHANGE CLASSIFICATION CLASS I ☐ CLASS II ☒ RECORD ☐	
PREPARED BY R Dayton	DATE 20 AUG 73	– FOR CHANGE BOARD ONLY –	– FOR MANUFACTURING ONLY – 26355
CHECKED W. Tolchin	DATE 23 AUG 73		PRODUCTION CUT-IN 5/8/101 & UP OR 154817
MECH. STRESS	DATE 8/28/73		DISPOSITION PARTS OR MATERIALS REWORK AT VENDOR OR SCRAP
ELECTRICAL APPROVAL	DATE 8-30/73	APPROVED	REWORK ☒ SCRAP ☐ USE AS IS ☐
PROGRAMS OFFICE APPROVAL	DATE	DATE 8/30/73	APPROVED J Kaub 8/29/73
ENGRG CHANGE CONTROL	DATE 8-31-73	ENGR DOC CONTROL	DATE 9-4-73 PAGE 1 OF 1

3-949 R 4 (4 72)

Litton DATA SYSTEMS

ENGINEERING CHANGE ORDER

PROGRAMS AFFECTED: TOS 2, TAC

OTHER DOCUMENTS AFFECTED: NONE

REASON FOR CHANGE: HOLE CALLOUT DOES NOT AGREE WITH A/W

ECP NO. PROGRAM

CATEGORY I RELEASE ☐ CATEGORY II RELEASE ☒

ECP NO: NONE

EFFECTIVITY: ALL CASING ASSY

DOCUMENT NO. 154826

CONTROL NO. 2 ECO NO. A2

DOCUMENT TITLE: PRINTED WIRING BOARD INPUT-OUTPUT-MCS8

ADD DELE IS WAS	ITEM NO.	QTY REQD	DASH NO.	CODE IDENT	PART OR IDENTIFYING NO.	DRAWING OR DOCUMENT NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REF DES	REF DES ADD	REF DES DELE	REF SYM

DESCRIPTION OF CHANGE

1) SHEET 1
ZONE 2D
CHANGE HOLE COUNT

.028 ±.003 DIA
(321) HOLES
PLATED THRU

(WAS 301)

APPLICATION BLOCK
(ADD) 154417 TACFIRE

PREPARED P. Ouet DATE 23 Oct 74	CHANGE CLASSIFICATION CLASS I ☐ CLASS II ☒ CLASS II (MINOR) ☐	ENGRG CHANGE CONTROL Ken Weber DATE 11-13-74	PRODUCTION CUT-IN S/N 101 & UP on 154417
CHECKED 24 Oct 74	APPROVED TOS2 TAC DATE	APPROVED DATE	ENGRG DOCUMENT CONTROL S. Hayden 11-13-74
ENGINEERING 10-23-74	24 Oct 74	12 Nov 74	MANUFACTURING
APPROVED			DISPOSITION PARTS OR MATERIALS USE AS IS ☐ SCRAP ☐ REWORK ☐ PER ERI ☐

PARTS COMPLY 22473

SHEET 1 OF 1

3-949 REV. 6 (2/74)

35mm

Litton DATA SYSTEMS	Test Specification	No. 154417-720
Contract No. DAAB07-72-C-0257	UNIT TITLE INPUT/OUTPUT CARD	
CODE IDENT NO. 13973	ASSY DWG. 154417 SCHEMATIC 154417-340	

ORIGINATOR	Pinkham	8-26-74			
DESIGN ENG.	PINKHAM				
ENG. APPROVAL	C. Morgan	8-9-74		BF Cooper	9/5/74

REV.	DATE	ECO No.	DESCRIPTION	ORIG.	ENG.
A	30 DEC 74		INCORPORATED ECO A1 DIRECT DWG CHG.	J MORGAN	J Higgins R.T. Nelson

CURRENT REVISION
including all changes as of
JUN 2 9 1976
ENGRG. DATA CONTROL

DSD RELEASE DATE 1-20-75 JH
CATEGORY II RELEASE

1.0 DESCRIPTION

The Input-Output-MCS8 (I/O) card 154417, is one of eight cards that make up the Central Logic of the Communication Control Unit (CCU). The I/O card is an interface card between the Central Processing Unit card (CPU) and the other units (cards) that are controlled by the CPU. The scheme of the I/O card is a centralized control of the I/O to simply the interface.

2.0 GENERAL

2.1 All tolerances are ±5% unless otherwise specified.

2.2 All tests shall be performed at prevailing factory or laboratory atmospheric conditions.

2.3 Output Levels

1 = HIGH = 3.75 ± 1.25 VDC

0 = LOW = 0.45 ± 0.45 VDC

2.4 Input Levels

1 = HIGH = +3.50 ± 1.50 VDC

0 = LOW = +0.35 ± 0.35 VDC

TEST SPECIFICATION

CONTINUATION SHEET

NO. 154417-720
REV. A
PAGE 3

3.0 REQUIREMENTS

TEST NO.	INPUT	CONN PIN	CONDITIONS	CONN PIN	OUTPUT
3.1	Initial Conditions				
	+5 VDC @ ma average.	11, 12			
	+5 VDC Return	1, 2			
	Clock	22	See figure 1		
3.2	ADDRESS and DATA Register and Buffer				
3.2.1	CDATA 7	9		8	DATA B7
	CDATA 6	7		6	DATA B6
	CDATA 5	5		4	DATA B5
	CDATA 4	3		10	DATA B4
	CDATA 3	19		14	DATA B3
	CDATA 2	16		17	DATA B2
	CDATA 1	18		15	DATA B1
	CDATA 0	20		13	DATA B0
	Inputs as shown in Table 1		Step through Table 1		Outputs as shown in Table 1
3.3	Output Strobe Decoder				
3.3.1	Out Time	40		47	OUTSTR 18
				48	OUTSTR 17
	CHADD 7	30		66	OUTSTR 16
	CHADD 6	29		68	OUTSTR 15
	CHADD 5	27		70	OUTSTR 14
	CHADD 4	32		72	OUTSTR 13
	CHADD 3	34		74	OUTSTR 12
	CHADD 2	44		76	OUTSTR 11
	CHADD 1	46		78	OUTSTR 10
	CHADD 0	42		80	OUTSTR 9

TEST SPECIFICATION

CONTINUATION SHEET

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REV. A
PAGE 4

TEST NO.	INPUT	CONN PIN	CONDITIONS	CONN PIN	OUTPUT
3.3.1 (Contd)				65	OUTSTR 8 OUTSTR 8
				67	OUTSTR 7
				69	OUTSTR 6
				71	OUTSTR 5
				73	OUTSTR 4
				75	OUTSTR 3
				77	OUTSTR 2
				79	OUTSTR 1
	Inputs as shown in Table 2		Step through Table 2		Outputs as shown in Table 2
3.4	Input Strobes 2 Through 8				
3.4.1	IN TIME	49		51	INSTR B8
				57	INSTR B7
		30		55	INSTR B6
		29		53	INSTR B5
		27		59	INSTR B4
		32		61	INSTR B3
		34		63	INSTR B2
		44			
		46			
		42			
	Input as shown in Table 3		Step through Table 3		Output as shown in Table 3

TEST SPECIFICATION

CONTINUATION SHEET

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REV. A
PAGE 5

TEST NO.	INPUT	CONN PIN	CONDITIONS	CONN PIN	OUTPUT
3.5	Output Control Pulse				
3.5.1	Output Time	40		24	OCP 8
				26	OCP 7
	D7	30		31	OCP 6
	D6	29		33	OCP 5
	D5	27		39	OCP 4
	D4	32		41	OCP 3
	D3	34		43	OCP 2
	D2	44		45	OCP 1
	D1	46			
	DO	42			
	A3	19			
	A2	16			
	A1	18			
	AO	20			
	Inputs as shown in Table 4		Step through Table 4		Outputs as shown in Table 4

TEST SPECIFICATION

CONTINUATION SHEET

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REV. A
PAGE 6

TEST NO.	INPUT	CONN PIN	CONDITIONS	CONN PIN	OUTPUT
3.6	Input Address Strobe and Input Strobe 9 through 10				
3.6.1	Out Time	40	See Figure 1	50	
				52	
	In Time	49		54	
				56	
	D7	30		58	
	D6	29		60	
	D5	27		62	
	D4	32		64	
	D3	34			
	D2	44		21	
	D1	46		28	
	D0	42		23	
				25	
	A3	19			
	A2	16			
	A1	18			
	A0	20			
	Input as shown in Table 5		Step through Table 5		Output as shown in Table 5

TABLE 1

	INPUTS								OUTPUT							
Pin Numbers	9 A7	7 A6	5 A5	3 A4	19 A3	16 A2	18 A1	20 A0	8 B7	6 B6	4 B5	10 B4	14 B3	17 B2	15 B1	13 B0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0
	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

TABLE 2

| Pin Numbers | INPUTS | | | | | | | | OUTPUTS | | | | | | | |

TABLE 3

Pin Number	INPUT 49 IT	30 D7	29 D6	27 D5	32 D4	34 D3	44 D2	46 D1	42 DO (INSTRB)	OUTPUT 51 8	57 7	55 6	53 5	59 4	61 3	63 2
	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0
	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	0	0	1	1	0	0	0	0	1	1	1	1	1	1	1	1
	0	0	1	1	0	0	0	1	0	1	1	1	1	1	1	1
	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0
	0	0	1	0	0	0	1	0	1	1	1	1	1	1	0	1
	0	0	1	0	0	0	1	1	1	1	1	1	1	0	1	1
	0	0	1	0	0	1	0	0	1	1	1	1	0	1	1	1
	0	0	1	0	0	1	0	1	1	1	1	0	1	1	1	1
	0	0	1	0	0	1	1	0	1	1	0	1	1	1	1	1
	0	0	1	0	0	1	1	1	1	0	1	1	1	1	1	1

PEW

TABLE 4

Pin Number	INPUT 40 OT	30 D7	29 D6	27 D5	32 D4	34 D3	44 D2	46 D1	42 D0	19 A3	16 A2	18 A1	20 A0	OUTPUT (OCP) 24 8	26 7	31 6	33 5	39 4	41 3	43 2	45 1
	0	0	1	1	1	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
	1	0	1	1	1	1	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1
	0	0	1	1	1	1	1	0	1	0	0	0	0	1	1	1	1	1	1	1	0
	0	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	1	1	1	0	1
	0	0	1	1	1	1	1	0	1	0	0	1	0	1	1	1	1	1	0	1	1
	0	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	0	1	1	1
	0	0	1	1	1	1	1	0	1	0	1	0	0	1	1	1	0	1	1	1	1
	0	0	1	1	1	1	1	0	1	0	1	0	1	1	1	0	1	1	1	1	1
	0	0	1	1	1	1	1	0	1	0	1	1	0	1	0	1	1	1	1	1	1
	0	0	1	1	1	1	1	0	1	0	1	1	1	0	1	1	1	1	1	1	1

REV A

TABLE 5

Pin Number	INPUT												OUTPUT											
	49 IT	30 D7	29 D6	27 D5	32 D4	34 D3	44 D2	46 D1	42 D0	19 A3	16 A2	18 A1	20 A0	50 (INSTAD)8	52 7	54 6	56 5	58 4	60 3	62 2	64 1(INSTAD)	21 12	28 11	23 10	25 9
	0	0	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	0	0	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1
	0	0	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	0	0	1	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1
	0	0	1	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	0	0	1	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1
	0	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	0	0	1	0	0	0	0	0	1	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1
	0	0	1	1	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	0	0	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	1
	0	0	1	1	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	0	0	1	0	0	0	0	0	1	0	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1
	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	0	0	1	0	0	0	0	0	1	0	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1
	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	0	0	1	0	0	0	0	0	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	0	0	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0
	0	0	1	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0
	0	0	1	1	1	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1
	0	0	1	0	0	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1
	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
	0	0	1	0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1

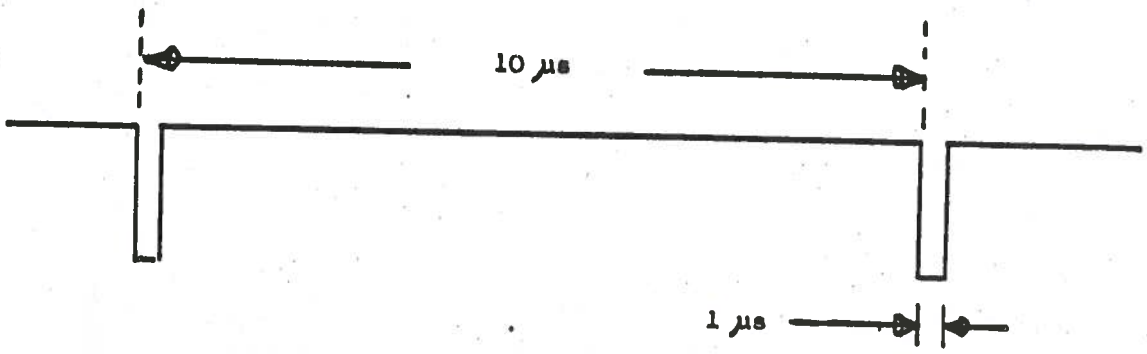

Figure 1. Clock