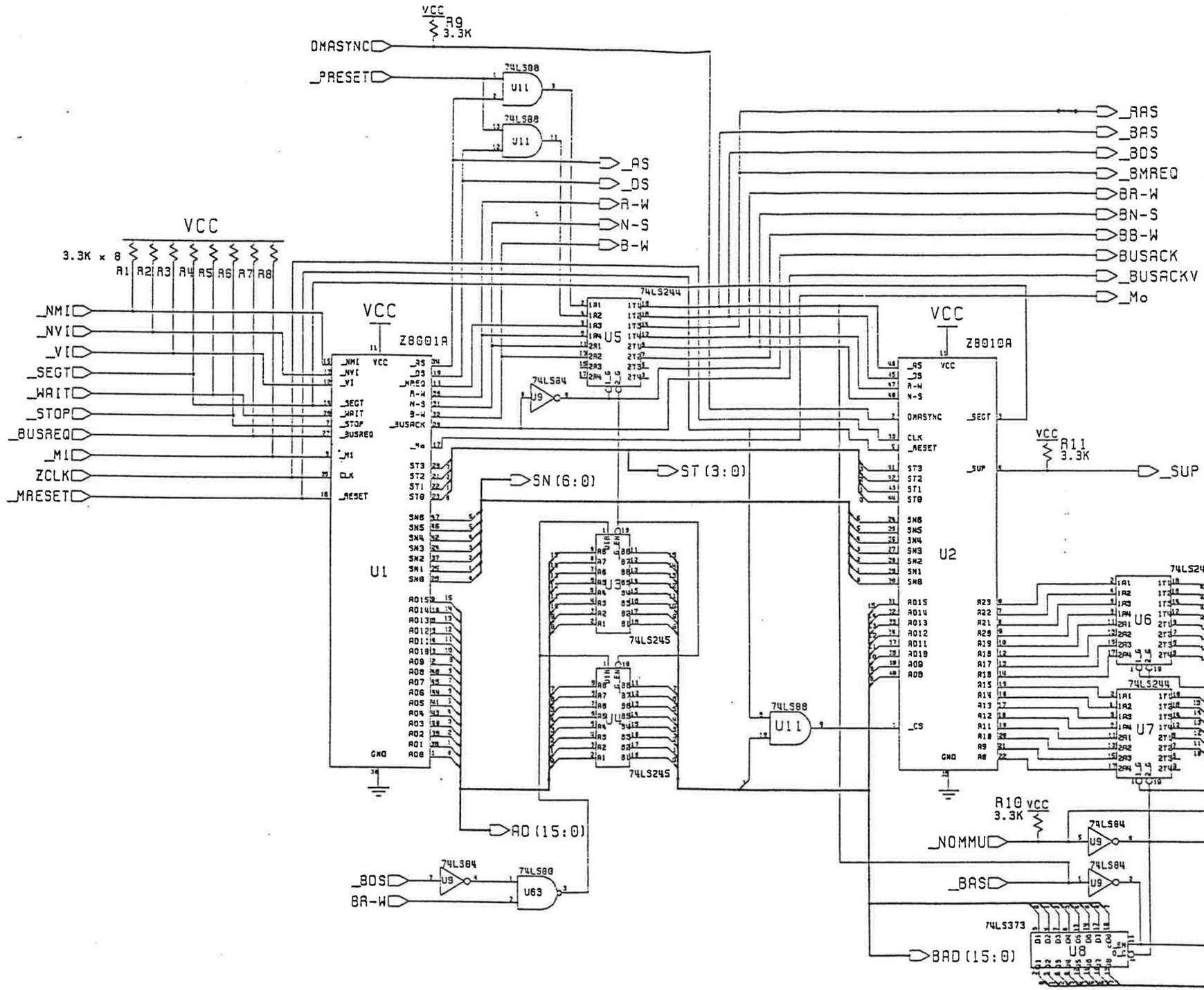
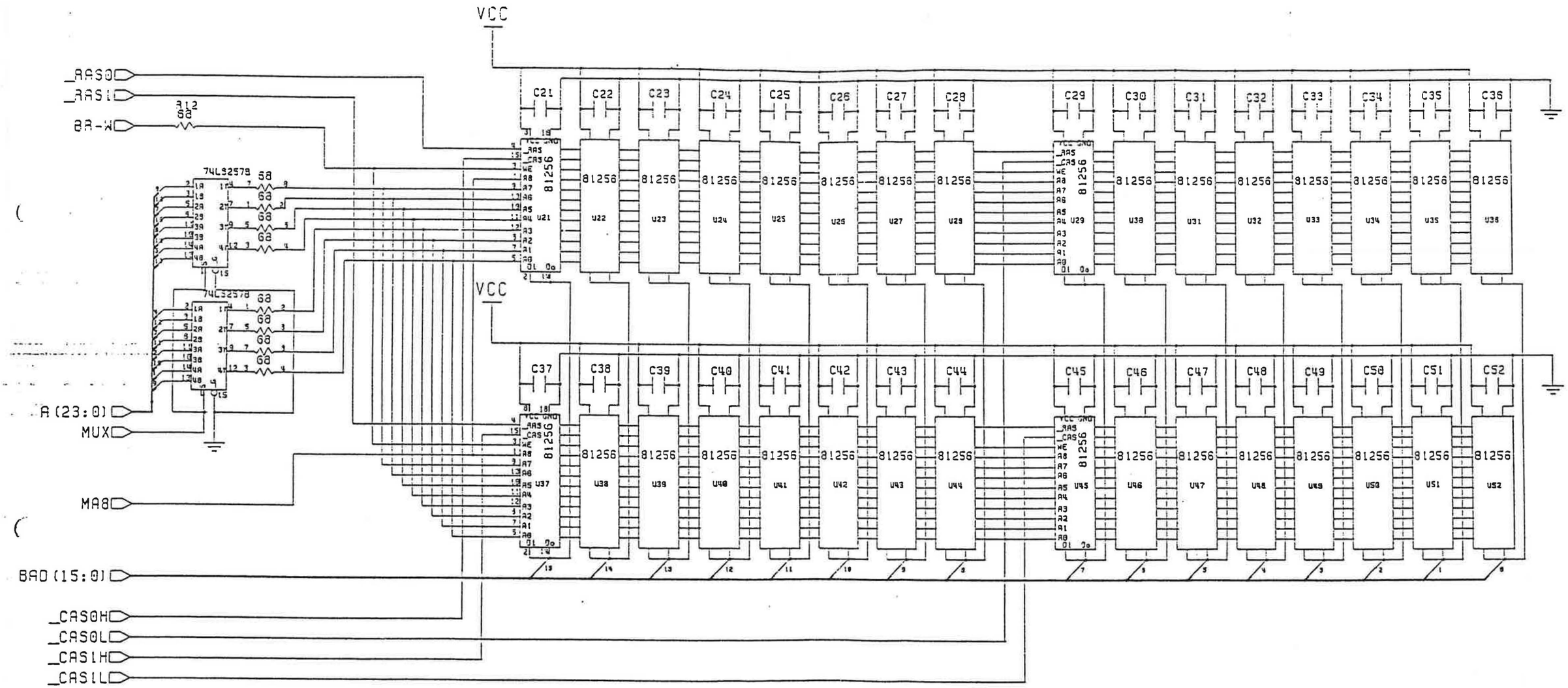


CPU and MMU Logic

DRAWN BY	DATE	COMMODORE	commodore
USED ON NEXT ASSY		DWG.NO. REV	Z8000HR
		SCALE SHEET OF	SIZE D REV C
DRAWN BY: D.Renn	DATE 2/15/84	MATERIAL:	SCALE 1 SHEET 1 OF 20
CHKD:		FINISH:	
ENGR:	2/28/84	USED ON NEXT ASSY	
MFG:			



NOTES UNLESS OTHERWISE SPECIFIED:
1. All capacitors 0.22uF.

System RAM

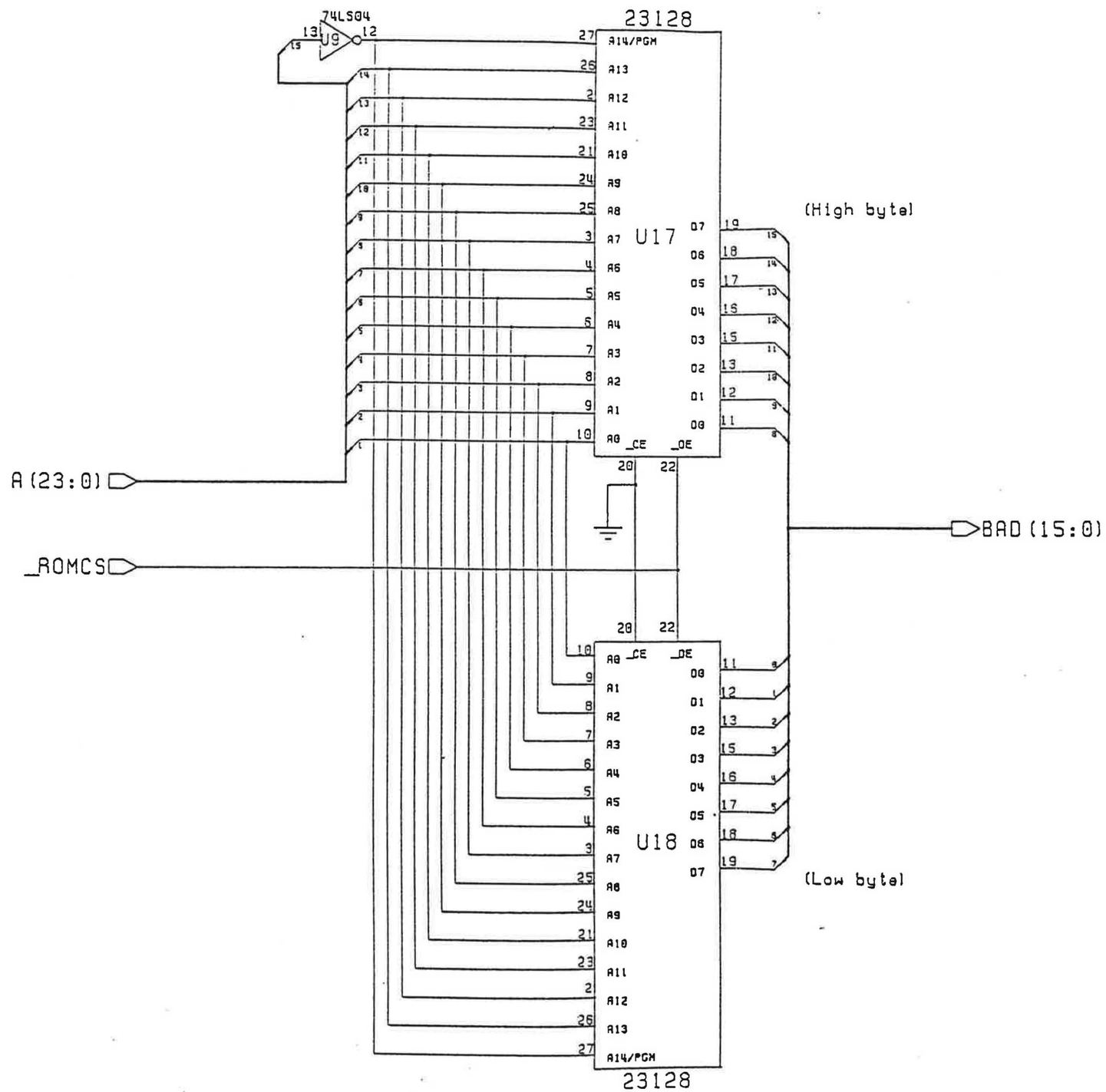
UNLESS OTHERWISE SPECIFIED	DRAWN BY: G. Kenn	DATE: 3/15/84
.X ±.1 .XX ±.05 .XXX ±.025 ∠'S ±1°	CHKD.	
	ENGRG. J. Hughes 4/18/84	
	APPR.	
MATERIAL:	USED ON	NEXT ASST
FINISH:		

commodore

Z8000HR

SIZE D | REV C

SCALE | SHEET 4 OF 20



System ROM

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	ENGR: J. Hughes	6/20/84	
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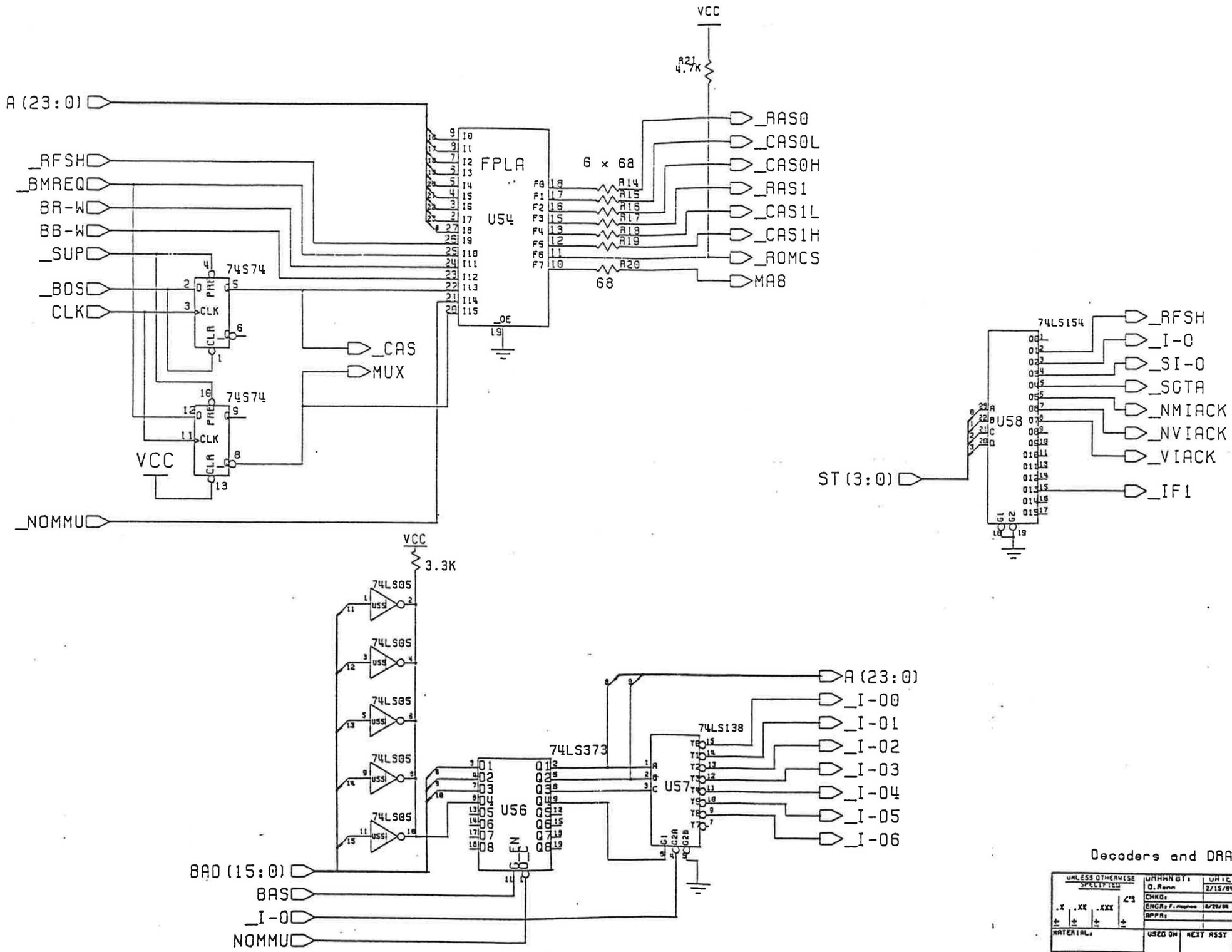

Decoders and DRAM Timing

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	ENGR: F. Magnus	6/29/84	
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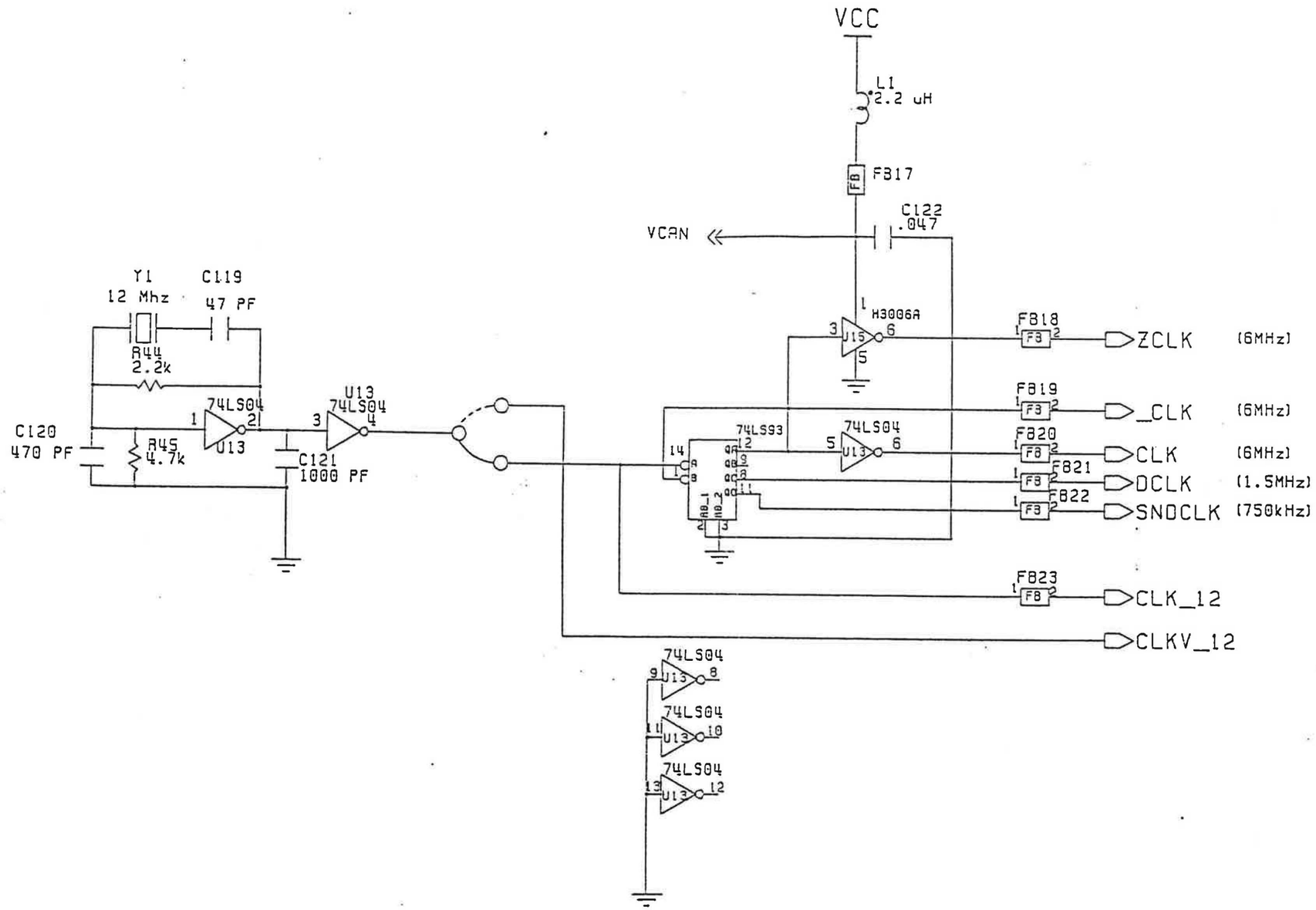

NOTES UNLESS OTHERWISE SPECIFIED:

1. All components on this page should be in a can.
2. VCC for all components in can is supplied by VCAN
3. All unused inputs must be grounded.

Timing Generation

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	CHKD:	Z8000HR
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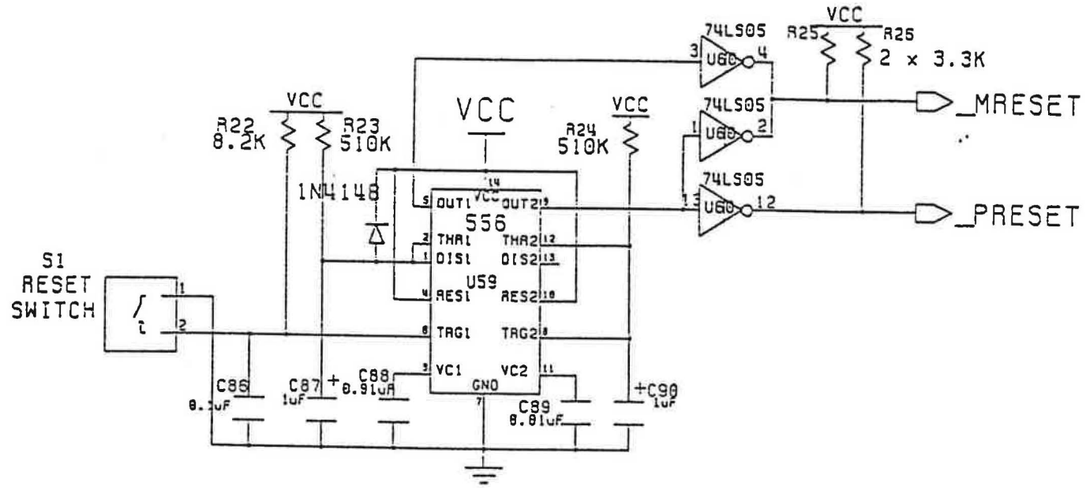
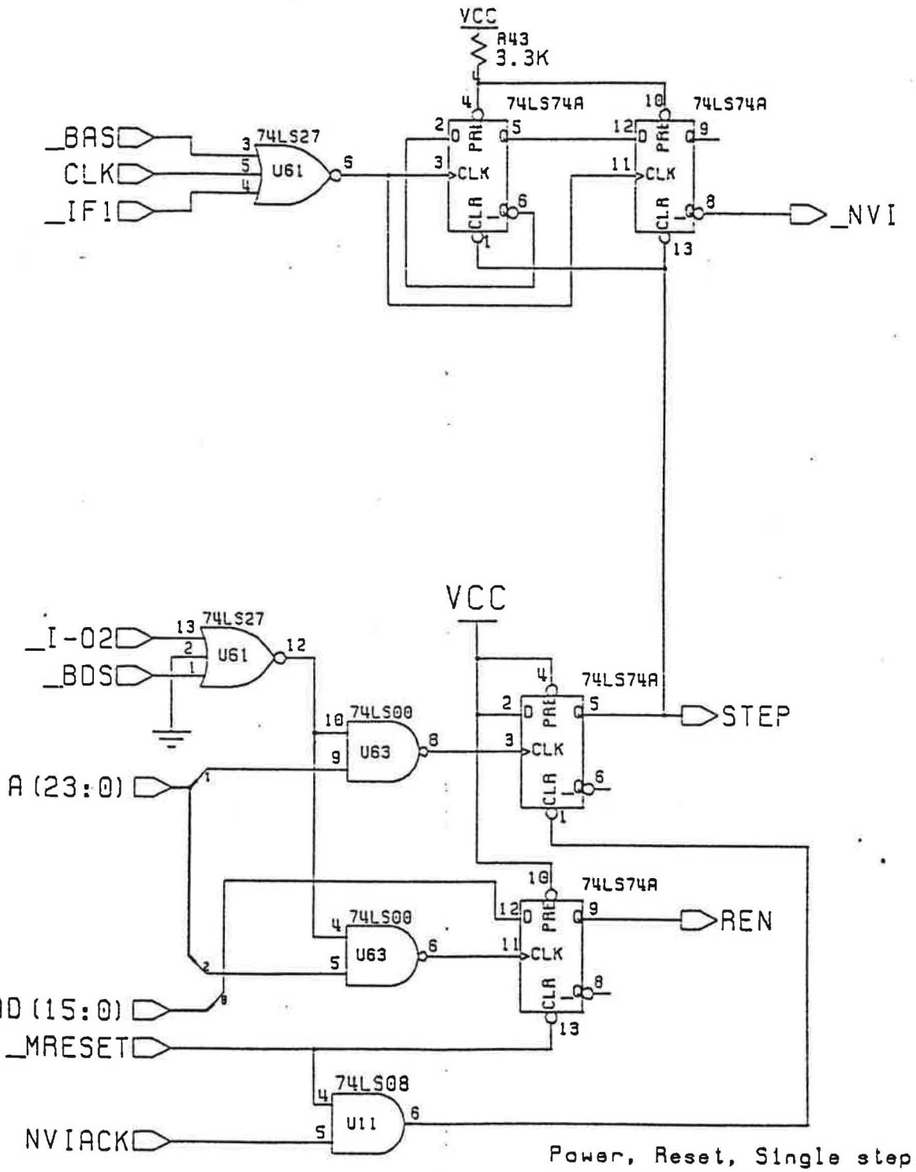
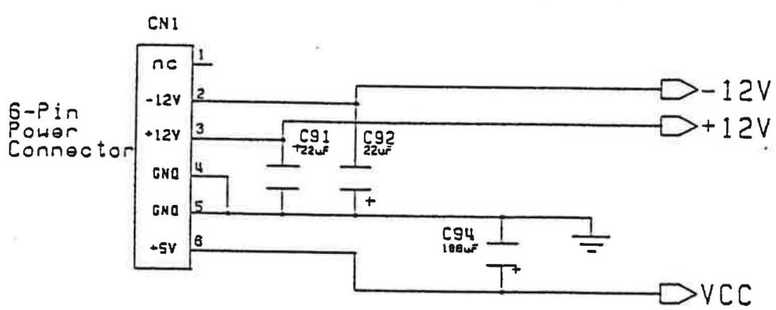






Power, Reset, Single step, and Latches

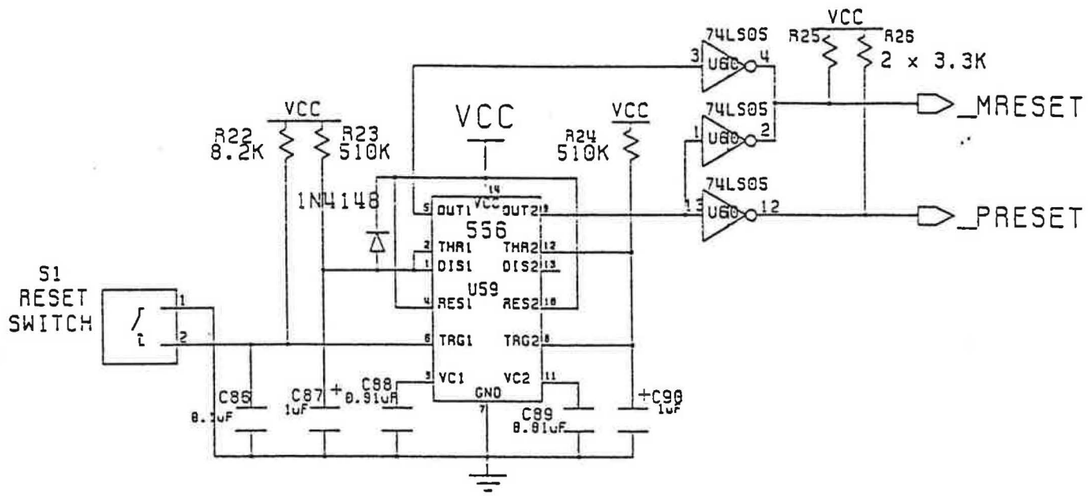
UNLESS OTHERWISE SPECIFIED .X ±, .XX ±, .XXX ±, ∠'S ±	DRAWN BY: D. Renn	DATE: 2/15/84
	CHKD:	
	ENGR:	
	APPR:	
MATERIAL:	USED ON	NEXT ASSY
FINISH:		

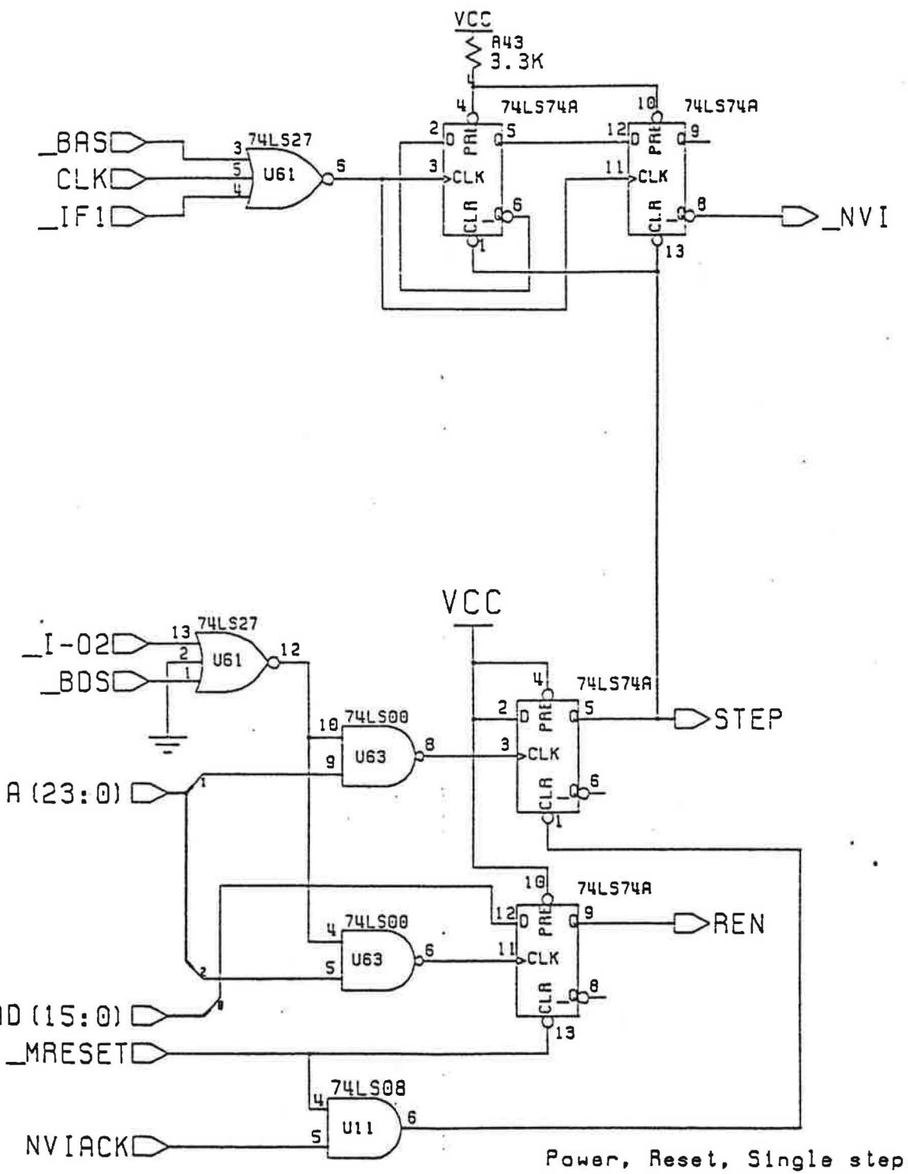
commodore

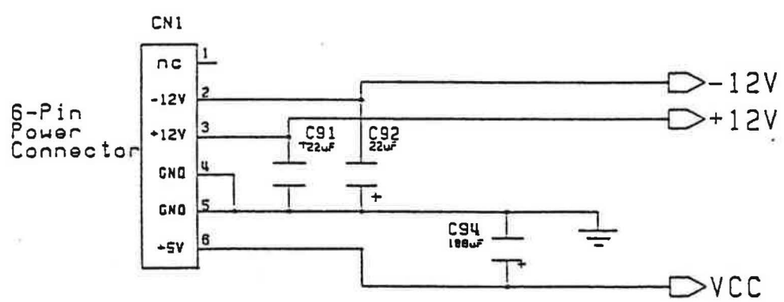
Z8000HR

SIZE D | REV C

SCALE | SHEET 6 OF 20

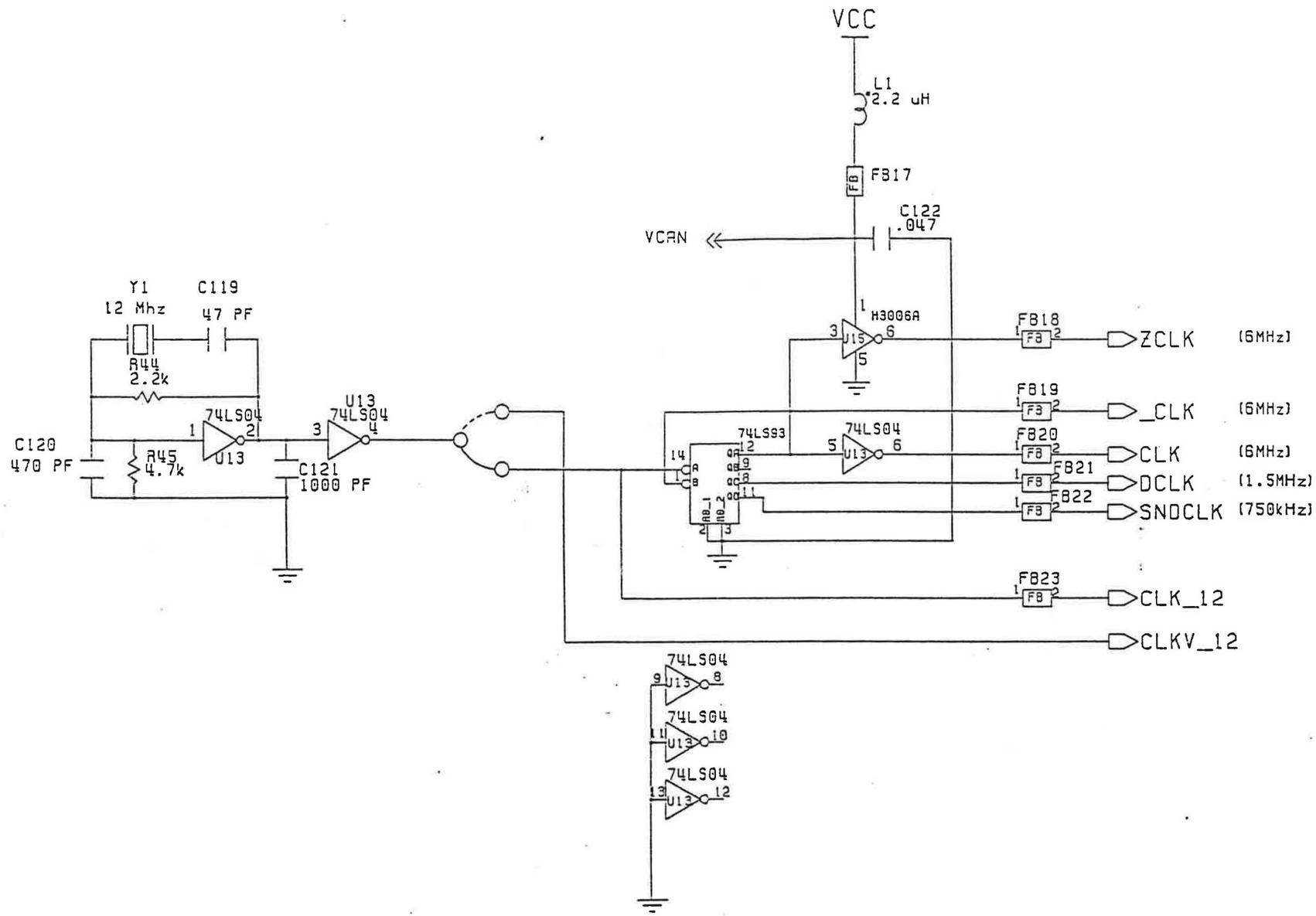






Power, Reset, Single step, and Latches

UNLESS OTHERWISE SPECIFIED .X ±, .XX ±, .XXX ±, ∠'S ±	DRAWN BY: D.Rann 2/15/84	commodore
	CHKD:	Z8000HR
	ENGR:	
	APPR:	
MATERIAL:	USED ON / NEXT ASSY	SIZE D / REV C
FINISH:		SCALE / SHEET 6 OF 20



NOTES UNLESS OTHERWISE SPECIFIED:

1. All components on this page should be in a can.
2. VCC for all components in can is supplied by VCAN
3. All unused inputs must be grounded.

Timing Generation

UNLESS OTHERWISE SPECIFIED .X ± .XX ± .XXX ± ∠'S ±	DRAWN BY: O. Rann	DATE 2/15/84	commodore
	CHKD:		Z8000HR
	ENGR: F. Hughes	2/28/84	
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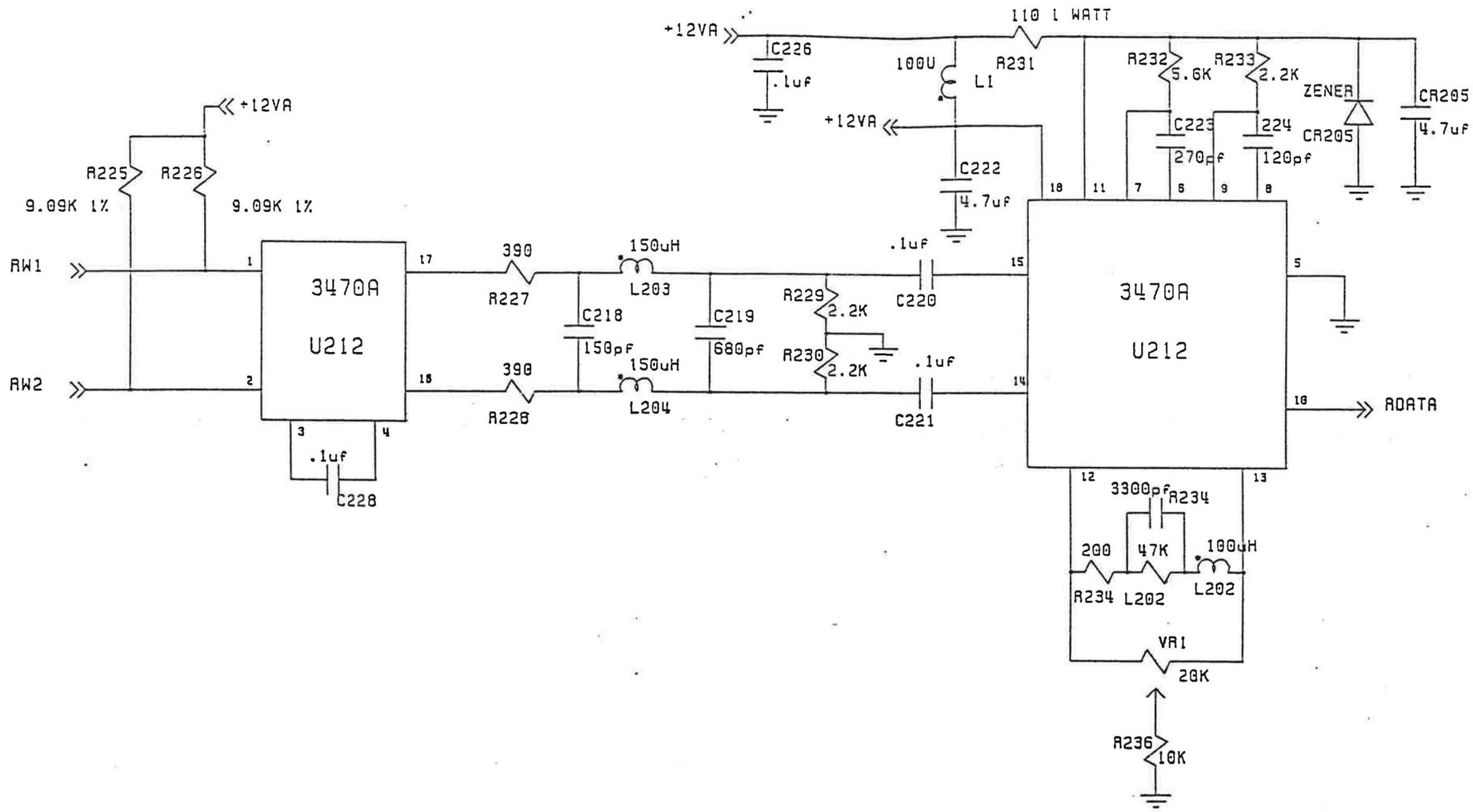
FINISH:			SCALE / SHEET 2 OF 20



FLOPPY CONTROLLER

UNLESS OTHERWISE SPECIFIED .X ± .XX ± .XXX ± ∠'S ±	DRAWN BY:	DATE	commodore
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	ENGR: J SOTER	10/30/85	
	APPR:		
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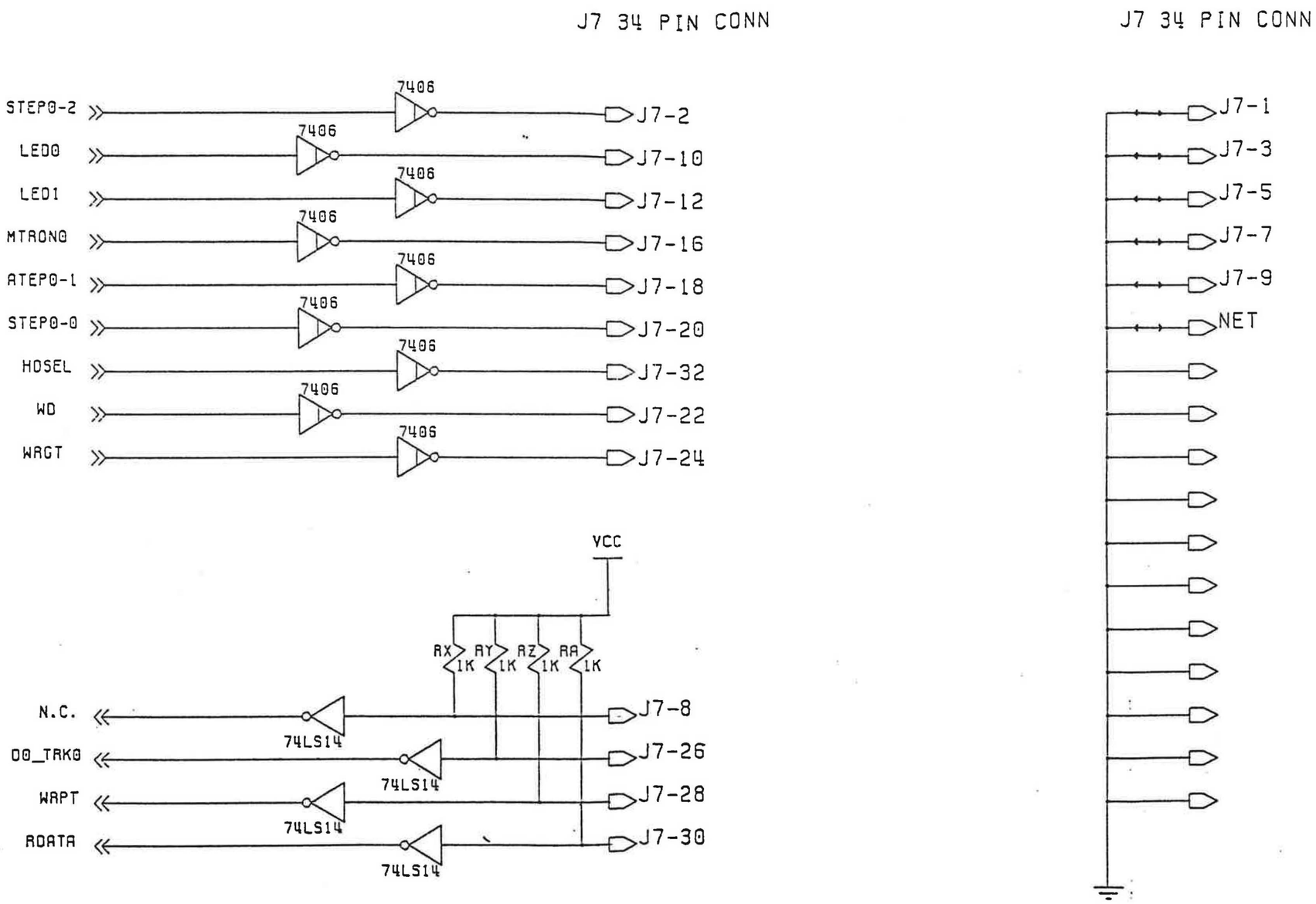

FLOPPY CONTROLLER

UNLESS OTHERWISE SPECIFIED .X ±, .XX ±, .XXX ±, ∠ ±	DRAWN BY:	DATE	commodore
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	ENGR: J BOTER	10/30/84	
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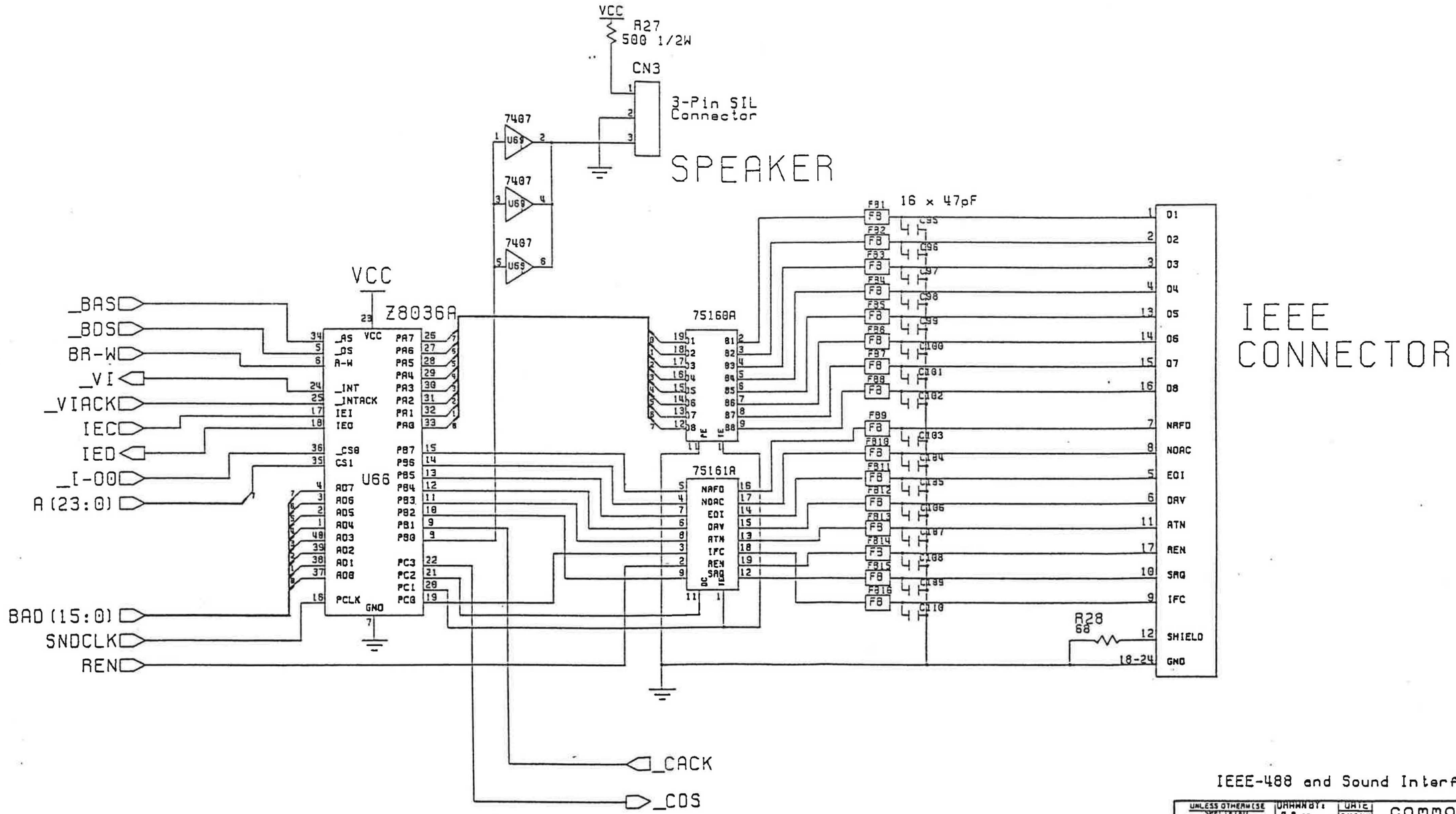
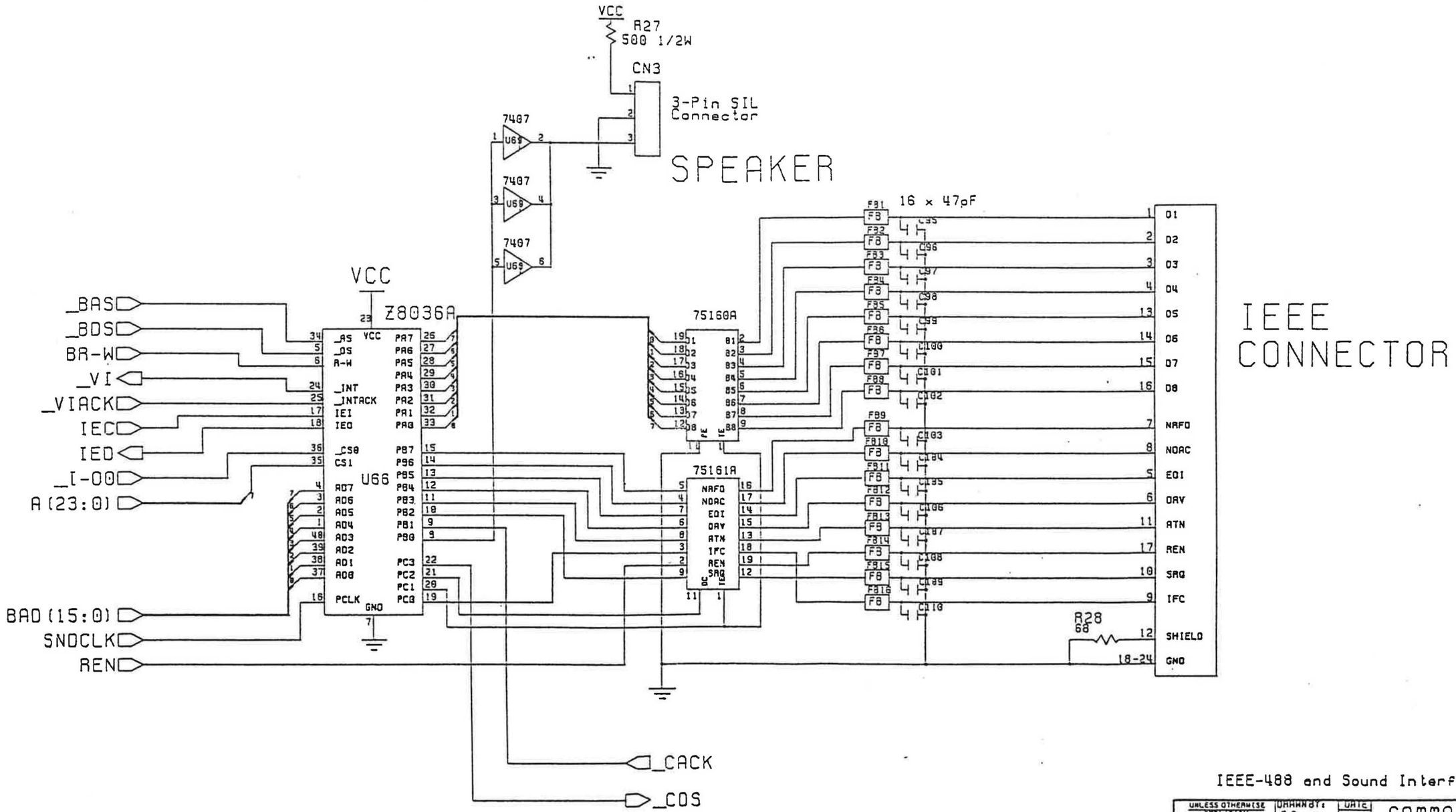
FINISH:			SCALE / SHEET 9 OF 20



IEEE-488 and Sound Interfaces

UNLESS OTHERWISE SPECIFIED .X ± .XX ± .XXX ± ∠ ±	DRAWN BY: D. Rene	DATE 2/13/86	commodore
	CHKD:		Z8000HR
	ENGR:	6/20/86	
	APPR:		
MATERIAL:	USED ON	NEXT ASSY	SIZE D / REV C
FINISH:			SCALE / SHEET 10 OF 20



IEEE-488 and Sound Interfaces

UNLESS OTHERWISE SPECIFIED .X ± .XX ± .XXX ± ∠'S ±	DRAWN BY: D.Renn	DATE 2/13/84	commodore
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	ENGR:		
	APPR:		
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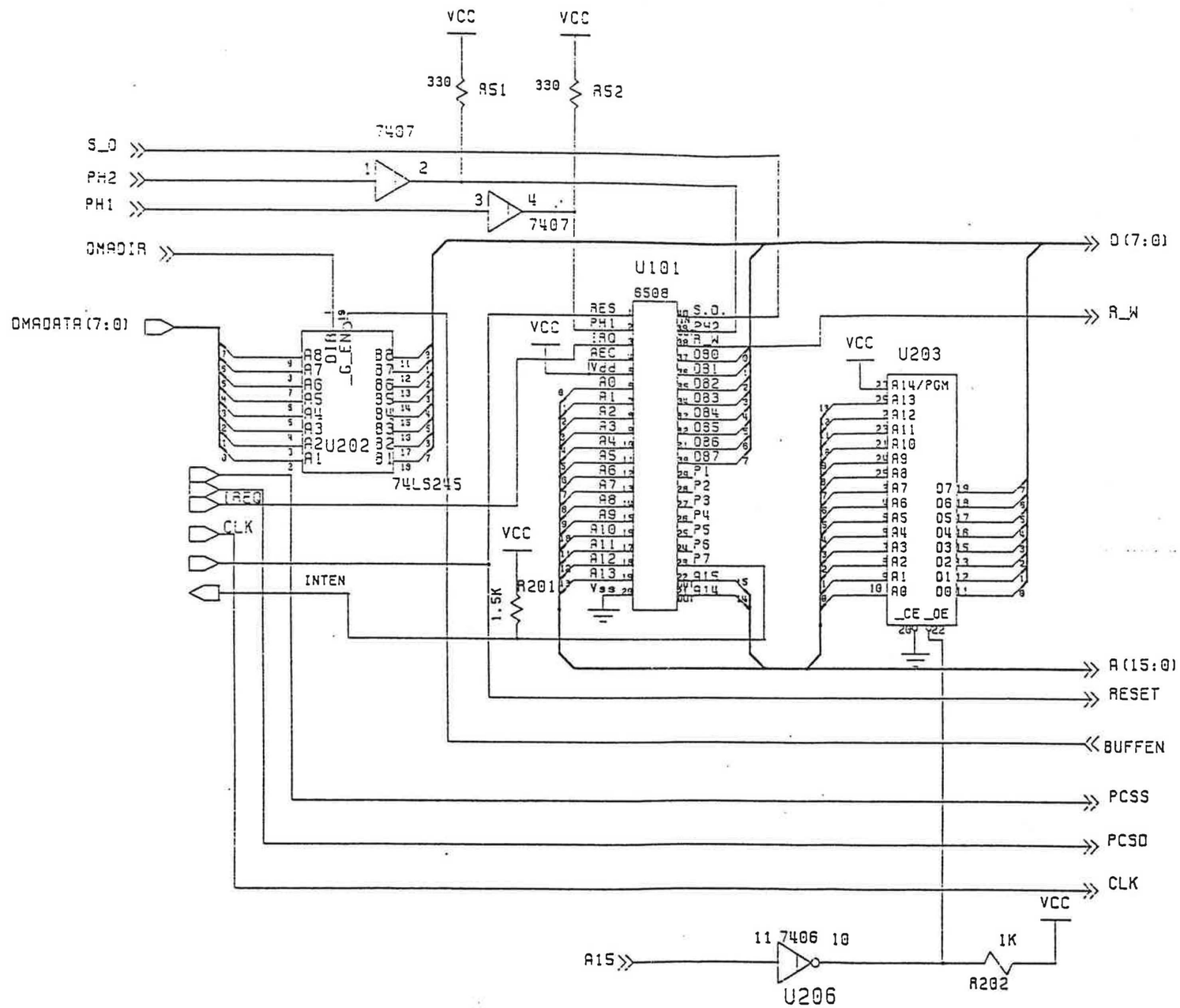
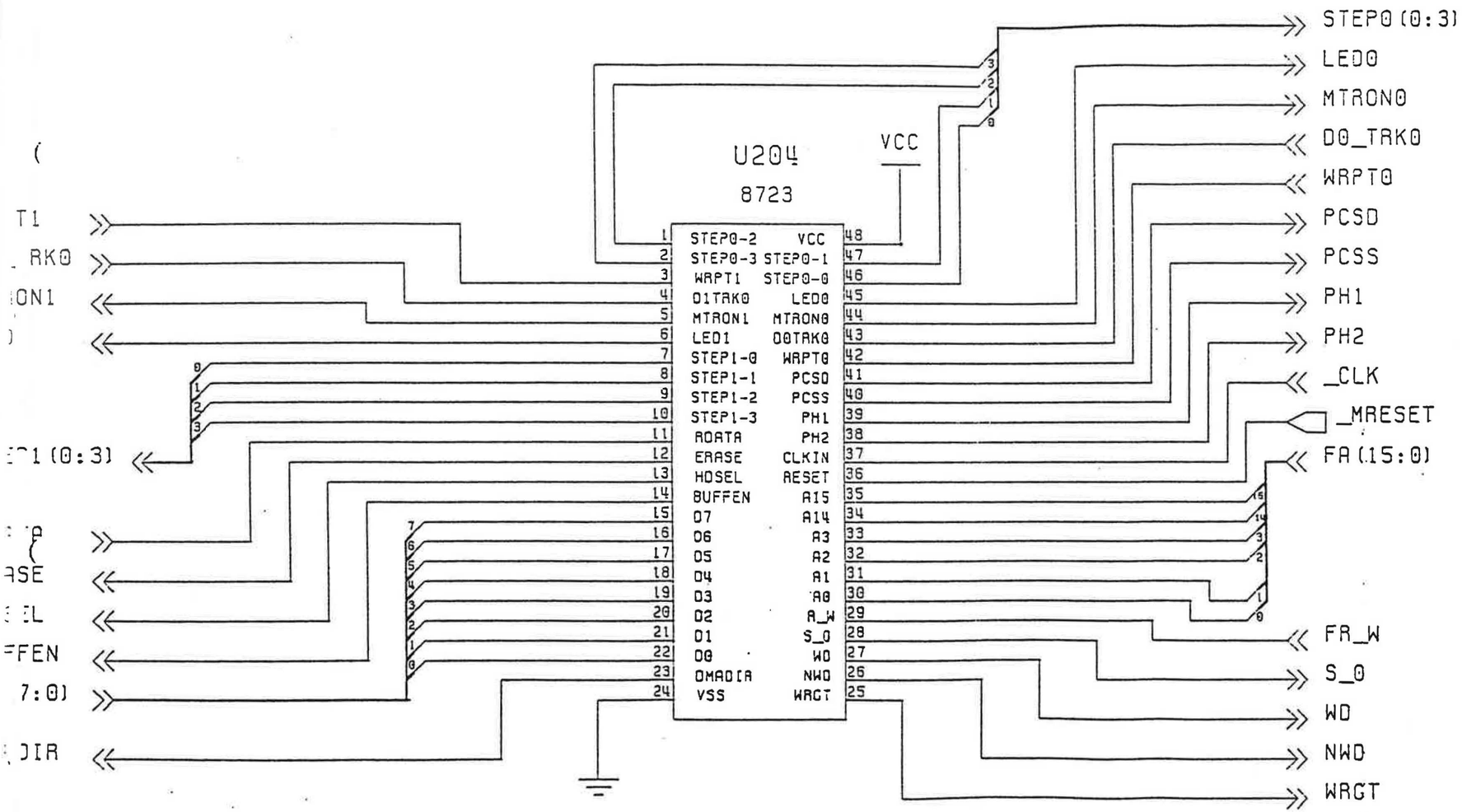
FINISH:			REV C
			SCALE / SHEET 10 OF 20



FLOPPY CONTROLLER

UNLESS OTHERWISE SPECIFIED .X ± .XX ± .XXX ± ∠'S ±	DRAWN BY: DATE	Z8000HR
	CHKD:	
	ENGR: J BOYER 10/30/84	
	APPR:	
MATERIAL:	USED ON / NEXT ASSY	SIZE D / REV C
FINISH:		SCALE / SHEET 1 OF 20



FLOPPY CONTROLLER

UNLESS OTHERWISE SPECIFIED .X ± .XX ± .XXX ± ∠'S ±	DRAWN BY:	DATE	commodore
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	ENGR: J BOYER	10/30/84	
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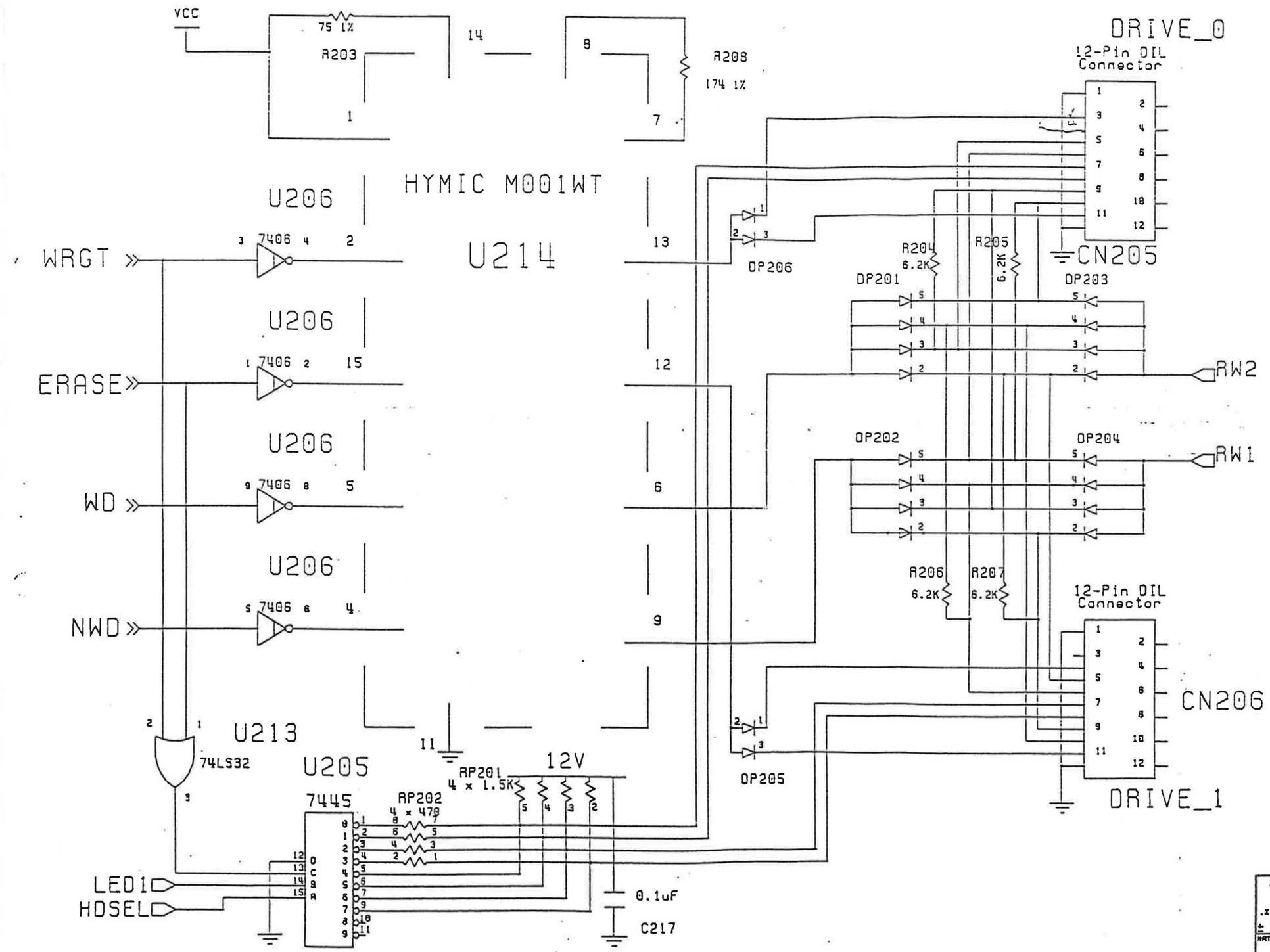

FLOPPY CONTROLLER

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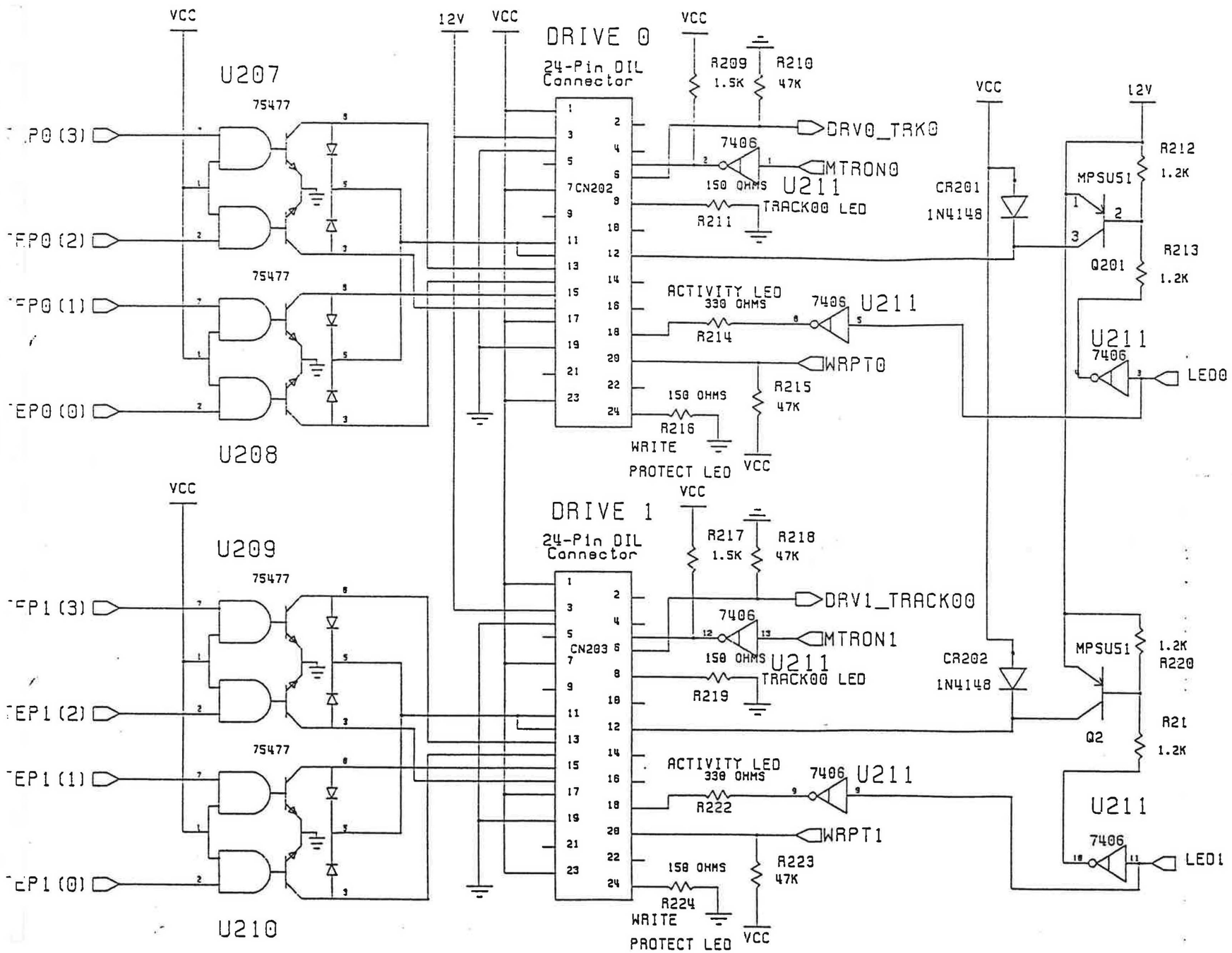
	CHKD:	
	ENGR: J. BOTER	10/30/84
	APPR:	
MATERIAL:	USED ON	NEXT ASSY
FINISH:		

commodore

Z8000HR

SIZE D | REV C

SCALE | SHEET 15 OF 20



FLOPPY CONTROLLER

UNLESS OTHERWISE SPECIFIED .X ±, .XX ±, .XXX ±, ∠ ±	DRAWN BY: DATE	commodore
	CHKD:	Z8000HR
	ENGR: J BOYER 10/30/85	
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MATERIAL:	USED ON / NEXT ASSY	SIZE D / REV C
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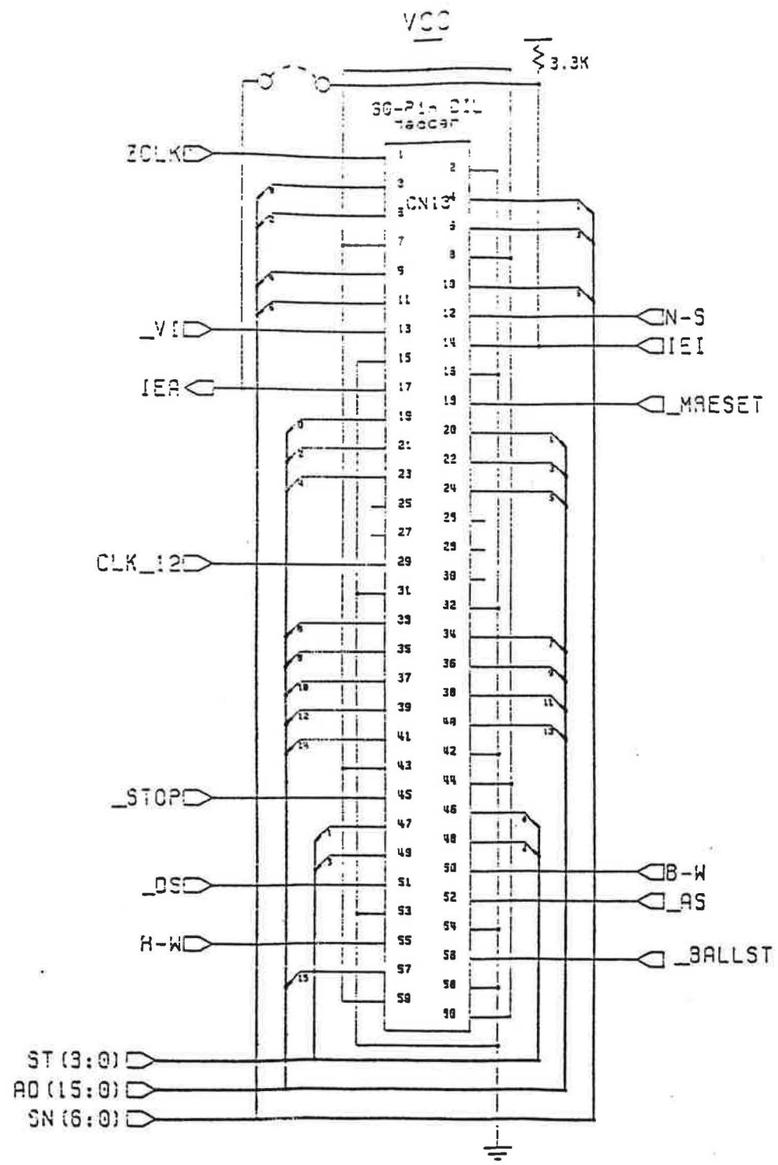


APU CONNECTOR

commodore

Z8000HR

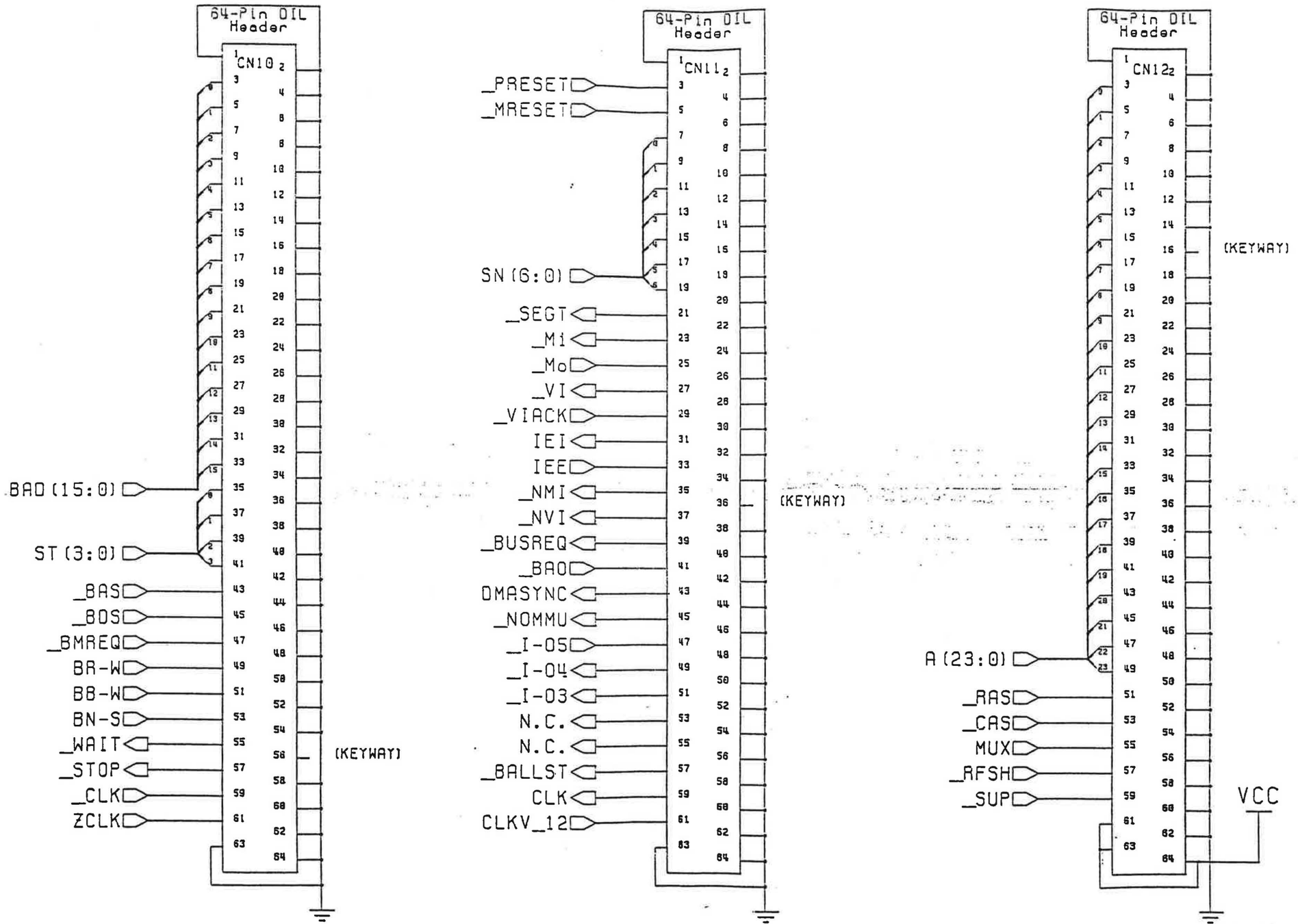
SIZE D

REV C

SCALE

SHEET 2 OF 2

V80:DEV.CHARLES.HIAGI.PLOT



Expansion Bus Connectors

UNLESS OTHERWISE SPECIFIED .X ± .XX ± .XXX ± ∠'s ±	DRAWN BY: D. Renn 2/15/84	commodore
	CHKD:	Z8000HR
	ENGR: F. Hughes 8/28/84	
	APPR:	
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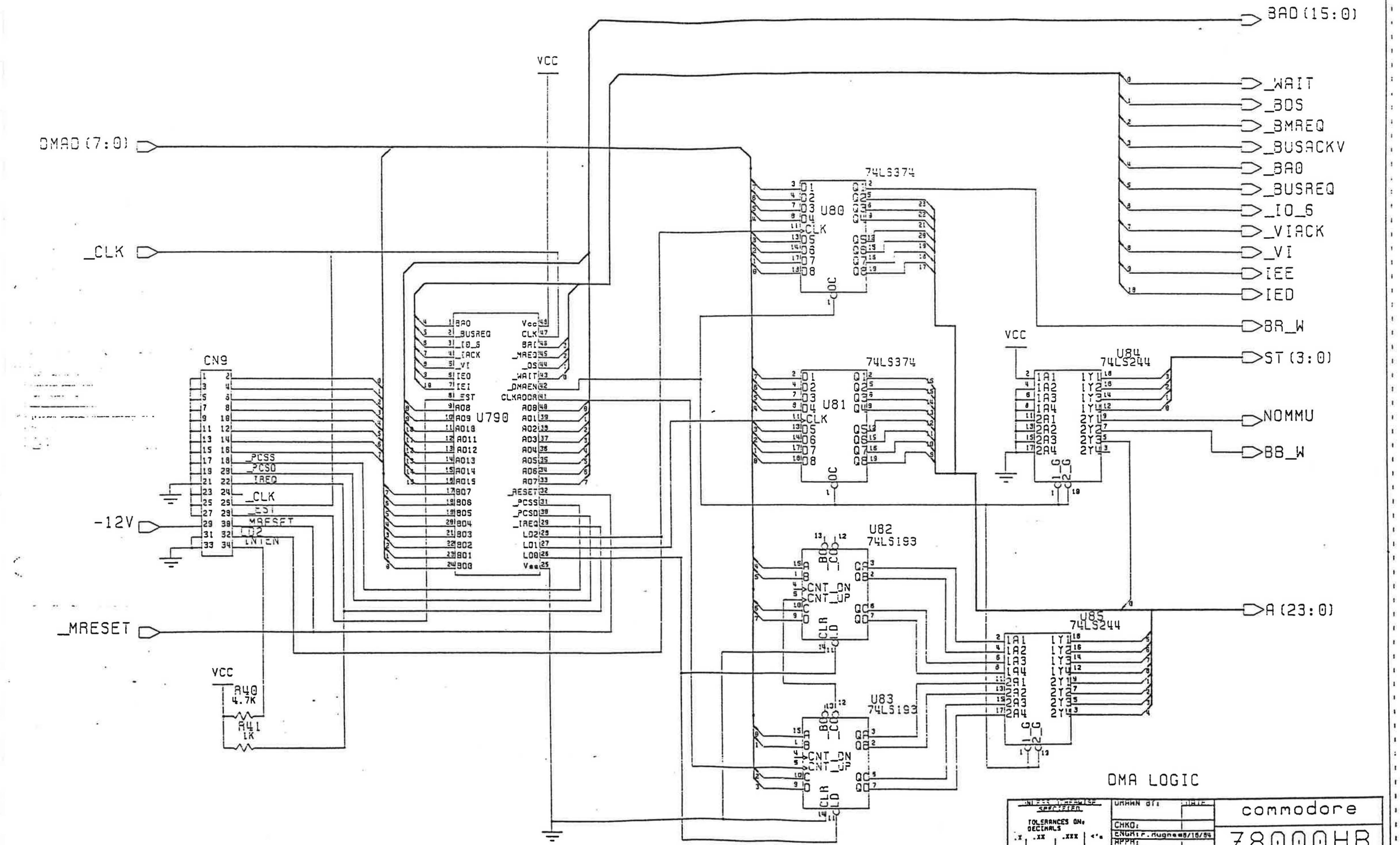
FINISH:		SCALE / SHEET 19 OF 20


BAD(15:0)
_WAIT
_BDS
_BMREQ
_BUSACKV
_BAO
_BUSREQ
_IO_S
_VIACK
_VI
IEE
IED
BR_W
ST(3:0)
NOMMU
BB_W
A(23:0)
DMAD(7:0)
_CLK
-12V
_MRESET
VCC
CN9
U790
U80
U81
U82
U83
U84
U85
74LS374
74LS193
74LS244
R40
4.7K
R41
1K
DMA LOGIC
commodore
Z8000HR
SIZE
D
REV
C
SCALE
SHEET 18 OF 20
TOLERANCES ON: DECIMALS
MATERIAL:
FINISH:
USED ON
NEXT ASSY
CHKD:
APPR:

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVE

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DESCRIPTION	SHEETS
INTRODUCTION	2
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SHEET																													
REV STATUS OF SHEETS	REV																												
	SHEET	1	2																										

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES
ANGLES ±1°
2 PLACE DECIMALS ±.02
3 PLACE DECIMALS ±.010

DRWN	
SYSTEMS ENG J. Hoenig/E.Yang	
TEST ENG	
CIRCUIT ENG	
COMP ENG	

COMMODORE

TITLE
Z8000 PHYSICAL DMA CONTROLLER WITH FIFO (8716) PRELIMINARY SPECIFICATION

SIZE A | DRAWING NO. 315046

SCALE | SHEET 1 OF 17

INTRODUCTION

This specification describes the physical DMA controller (PDMAC) with a bidirectional FIFO used in a hard disk controller board. The PDMAC is a 48 pin chip that has two basic functions. The first is to determine if one or more words are ready to be transferred to the Z8000 bus or be read from the Z8000 memory. The second function is to provide bufferring between the Z8000 and the hard disk and do byte to word funneling.

The first function requires that the Z8000 control signals be generated that adhere to the Z8000 timing diagrams for a 6MHz part. This will ensure that all setup and hold parameters for 200ns dynamic RAMs will not be violated.

The second function requires that when data is to be transferred from the Z8000 to the disk that there is no gap in the flow of data to or from the disk. To do this a minimum of 4usecs of data must be in the FIFO or there must be 4usecs of space available in the FIFO. This requirement implicitly relies on the use of half full signal (or half empyt). Bus request will be based on the level of th half full signal.

PIN DESCRIPTION

Pin#	Pin-Name	Function
	VSS	ground.
	VSS	ground.
	VCC	5V +-5%
		Z8000 EXPANSION BUS INTERFACE
	AD0 - AD15	These are the bi-directional data lines on the Z8000 multi-plexed address/data bus.
	MREQ	This is an active low output signal indicating that a valid address is on the address bus and that a memory access is requested. This signal becomes valid during T1 and is released at the end of T3
	WAIT	This is an active low input signal that is sampled during T2 and Twa to determine if a clock cycle is to be inserted in the memory transfer. It is ignored at all other times.
	CLK	This is the inverted system clock input. It is a 6Mhz square wave with a 50% duty cycle.
	BUSACK (BAI)	This is the bus acknowledge input that is daisy chained from the next higher priority device.
	BAO	This output is low if BUSACK is low and the PDMAC is not requesting the bus.
	IO/6 (control sel)	This is an input pin, when IO/6 and DS are both low then IREQ is set low.
	VI	This is an open drain output signal that is pull low when PCSS latches in state '11110111' on BD7 - BD0.
	IEI	This is an active high input pin, a high on IEI allows the PDMAC to place a vector on AD7 - AD0 if VI, IACK and DS are all low.
	IACK	This interrupt acknowledge input signal combined with DS and IEI place and interrupt vector on AD7 - ADO.
	IEO	This is an active low output pin, whenever IEI is low and VI is low and will cancel a low signal on this pin.

PIN DESCRIPTION (cont.)

Pin#	Pin-Name	Function
	BUSREQ	This is an open drain output signal that is pulled low to request the bus
	DS	This is an active low output signal that indicates that data is valid on the data bus for a write or memory devices are to turn their bus drivers on
		ADDRESS LATCH INTERFACE
	CLKADR	This is the clock output for incrementing the address
	DMAEN	This is an active low output that enables the address and data bus drivers when the disk controller has the bus
	LDØ	This is the output pin to enable address latch to load in 8 bit of low order address from B Bus.
	LD1	This is the output rise pin to enable address latch to load in 8 bit of high order address from B Bus.
	LD2	This is the output pin to enable address latch to load in 8 bit of high order address from B Bus.
		HARD DISK CONTROLLER INTERFACE
	RESET	A low on this signal will clear the FIFO and clear any DMA cycle in progress and clear the ERROR flag.
	PCSS	The rising edge of this signal clocks in the state placed on BD7 - BDØ. The state that is loaded in is determines the function implemented when PCSD is active (low).
	PCSD	The falling edge of PCSD indicates that either valid data is on BD7 - BDØ or that data is to be placed on BD7 - BDØ. The source is determined from the previous state latched in by PCSS.
	IREQ	This signal is set low by IO/6 and DS and is cleared when state '1111 1011' is latched in by PCSS. This is an open drain output.
	BDØ - BD7	This is the bi-directional byte wide data that is transferred from or to the disk controller

PDMAC FUNCTIONALITY

The hard disk board consists of three parts; (1) controller section, (2) PDMAC, (3) address latches. Before any DMA operation begins, controller will send a command to PDMAC which will then send the control signal to latch the address from controller to address latch, and the FIFO will be cleared unless a clear pulse is generated by the /R.Reset line going low. This line also sets the DMA logic in an idle state. It also clears the /ERROR line.

The Single Step ~~pulse~~ command is used to transfer 1 word to or from the Z8000. This line must be set before the Start line is activated.

The two signals /WRITETD and /READFD are used to control the direction of data transfer. If /WRITETD is low then DIR is set high indicating that data is to be transferred from the Z8000 to the disk.

Once the external latches have been set up a start ~~pulse~~ command can be issued which will initiate the /BUSREQ cycle and control transfer of data to the FIFO. A /Start pulse will clear DMADONE.

DMA on the Z8000 Expansion Bus

The Z8000 DMA is divided into 3 parts. The first is acquiring the bus, the second is being bus master and the third is releasing the bus.

1) Acquiring the Z8000 Bus

The Z8000 has two signals used for releasing the bus to other bus masters. They are /BUSREQ and /BAI. The signal /BUSREQ is pulled low by any device that can be a bus master but only if its respective /BAI signal is high. The /BAI is a diasy chained signal that propagates from the highest priority device to the lowest priority device. However since /BAI must be high for a device to pull bus request low it is possible for a low priority device to grab and hold the bus from all other devices. Therefore, although 4usecs is required to grab the bus from the CPU there is no maximum time limit if another device has hold of the bus. Under this constraint a FIFO equal to the size of a sector would be the design goal. This however places the disk controller on the bus for a minimum of 128 usecs for a single sector transfer. (Multiple sector transfers would hold the bus for upto 150usecs before the buffer would be empty.) A smaller buffer would permit other devices to share the bus at all times requiring only 16usecs at most for a 64 byte deep FIFO. On the average the disk controller would require the bus 9usecs once every 58usecs. This amounts to a 16% overhead for the cpu. This also permits the cpu to service interrupts, such as RS - 232 ports, with no loss of data.

2) Being Bus Master

Once the bus has been granted by the /BAI - /BAO daisy chain to the requesting device, actual data transfer can begin. In this case only three signals need to be generated to transfer data. These are /MREQ, /DS and R/W. The first two indicate the presence of a valid address to memory and the second indicates that either data is valid on the bus or that memory is to drive the data bus. These two lines are decoded to generate /RAS and /CAS for Drams. It is important that the setup and hold times for row address and column address be adhered to.

3) Releasing the Bus

At the end of the DMA transfer /BUSREQ is released and /BAO is driven low if /BUSREQ is low. Once /BUSREQ is released a minimum of two clock cycles will occur before the cpu drives /BAI high.

PDMAC TO DISK CONTROLLER INTERFACE

Interfacing to the DMA controller from the disk controller side is via the eight bit data bus (BD0 - BD7) and two control lines (/PCSS and /PCSD). The control line /PCSS latches the contents of BD7 - BD0 to be used to do one of the following functions determine by the value on BD7 - BD0.

on the falling edge of pcss

BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	Function
1	1	1	1	1	0	1	1	LD2 is set low. LD2 is set high on the falling edge of /PCSD. The BD7 contains the DIR information. (BD7 = 0 : wr, BD7 = 1 : rec)
1	1	1	1	1	1	0	1	LD1 is set low. LD1 is set high on the falling edge of /PCSD.
1	1	1	1	1	1	1	0	LD0 is set low. LD0 is set high on the falling edge of /PCSD and the DMA logic is enabled on the rising edge of LD0.
1	1	1	1	0	1	1	1	This state will either output data from the FIFO onto BD7 - BD0 on the falling edge of /PCSD or shift a byte into the FIFO. The direction is determined by BD7 on the rising edge of LD2. If BD7 was clocked in high then the output of the FIFO is driven onto BD7 - BD0.
1	1	1	0	1	1	1	1	On the falling edge of /PCSD internal status will be driven onto BD7 - BD0 as follows: BD7 - This will reflect the state of DMADONE. It is low until the end of either a word transfer in the single step mode or until 256 words have been transfered (one sector). BD6 - BYTERDY: this signal is high when a BYTE is ready in the FIFO to be read from or write to the B Bus. BD5 - ERROR: this signal is low if a BYTE is not available in the FIFO and a BYTE transfer is requested. BD4 - BD0 - reserved.
1	0	0	1	1	1	1	1	This state will force IREQ to a high impedance state. (IREQ is open drain.)
1	0	1	1	1	1	1	1	This will force the line VI to ground
1	1	0	1	1	1	1	~~1~~ 0	Single.Step- This will allow the DMA section to transfer one word. (The command sequence is LD2, LD1, S.S. no LD0 is allowed.)
0	1	1	1	1	1	1	1	Reset - this will clear the FIFO and ~~set~~ the direction of transfer ~~to be from the 38000 to the disk.~~ will not change.
1	1	1	1	1	1	1	1	After ~~power on~~ reset always do this command. (or power-on)

for single step

COMMODORE	TITLE 8716 PDMAC TO DISK CONTROLLER INTERFACE	
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KEY SIGNAL DESCRIPTION

/BUSREQ: /BUSREQ is controlled by two signals - /S.Busreq and /R.Busreq. Both signals are active low. /BUSREQ is an open drain signal capable of sinking2ma.

/S.Busreq: This signal will be active only if DMADONE is low and BAI is high. This is the protocol for requesting the Z8000 bus. IF DMADONE is low and BAI is high then if DIR is high (Z8000 => DISK) then the bus is requested if /H.FULL is high (FIFO is less than half full).

IF DIR is low (DISK => Z8000) then if DMADONE is low and BAI is high then /S.Busreq is active if /H.FULL is low (the FIFO has 32 or more bytes) or /EOT (/EOT is low if 16 or less words remain to be transferred) is low and W.Ready is high (W.Ready is high when two bytes have been transferred into the data latches).

/S.Busreq= *[*DMADONE @ BAI @ DIR @ /H.FULL @ /R.Busreq
*DMADONE @ BAI @ *DIR @ [*/H.FULL + */EOT @ W.Ready] + /R.Busreq]

/R.Busreq: This signal will clear /BUSREQ forcing the output to a high impedance. This will be low when DIR is high and Stopfl is high (Stopfl is set on the falling edge of /FULL and cleared on the rising edge of /H.FULL) or DIR is high and on the rising edge of /DS, /L.Ready is high (/L.Ready is high after a word is read into the latches and low after /R.Reset or after the two bytes have been transferred from the data latches to the FIFO) or if DIR is low and Stopemp is high (Stopemp is high on the falling edge of /EMPTY and low on the falling edge of /H.FULL) or if on the falling edge of /DS, W.ready is high (this indicates that the data latches were not written to from the FIFO). If an error condition occurs then /BUSREQ can be reset immediately. If there was not an error then /BUSREQ can be reset on the second half of T2. This is becuase /BUSREQ can not be reset until the /WAIT line is sampled. The /Wait line is sampled in the middle of T2.

/R.Busreq= *[*DMADONE + [DIR @ Stopfl + *DIR @ Stopemp] @ T2 @ /CLK + N.Ready]

N.Ready: This active high signal indicates that a data transfer is about to take place or has taken place but that data was written over or that the data written was not valid. This is set high on the rising edge of /DS and /L.Ready high or the falling edge of /DS and W.ready was high

Stopfl: This signal is used to indicate that /FULL has gone low. It is cleared when /H.FULL goes high.

Stopemp: This signal when high indictes that /EMPTY has gone low and is cleared when /H.FULL goes low

/FDODD: This signal when low enables the odd byte (AD0 - AD7) to the input to the FIFO. This signal is active when DIR is high and Odd is high.

/FDEVEN: When low the even byte (AD8 - AD15) is input to the FIFO. This is active if DIR is high and Even is high.

/Clkwd: On the rising edge of this signal the word on the data bus is clocked into the latches. The rising edge of /DS is used to clock this signal.

Clkeven (second): On the rising edge of Clkeven the data from the FIFO is clocked into the even latch (AD0 - AD7). This is active if DIR is low and even is high.

Clkodd (First): On the rising edge of Clkodd the data from the FIFO is clocked into the odd latch (AD~~X~~8 - AD~~X~~15). This is active if DIR is low and odd is high.

SI: This signal is normally low but when high it shifts into the FIFO the data that is on the inputs. SI is set with/S.SI and is reset by /R.SI.

/S.SI: This signal is active (low) if DIR is high (Z8000 => DISK) and IR is high and /L.Ready is high or if DIR is low and CREQ is low and IR is high and if N.Ready is low.

S.SI=*[DIR @ /L.Ready + *DIR @ IR @ CREQpulse]

/R.SI: This signal clears SI. When IR goes low/R.SI goes low

/R.SI = IR

/DMAEN: This is an active low signal that is set when the bus has been requested and a bus acknowledge is received. It is reset at the end of T3 if the bus is to be released or if an error occurred.

S0: This signal is normally low until data is requested. SO is set when DIR is high and /REQ goes low and OR is high or if DIR is low and W.Ready is low.It is reset when OR goes low or when /R.Reset goes low.

/BDENOUT: This signal enables the BD bus when low. It is low when DIR is high and CREQ is low.

/BDCLKOUT: This clocks the data into the output latch for BD0 - BD7. The data is clocked in on the rising edge of SO if DiR is high.

/BDCLKIN: This clocks the data on BD0 - BD7 into a latch on the rising edge of CREO if DIR is low.

/BDENIN: This enables the data from the BD latch to input to the FIFO when DIR is low and /FDODD is high and /FDEVEN is high.

T1: this signal represents the first state of the three clock data transfer cycle. /MREO becomes valid during the second half of T1 (T1 is high and /6MHz is high). It is set at the beginning of the bus acknowledge cycle if the bus is requested or at the end of T3. It is cleared at the beginning of T2.

T2: During T2 and T3 data is transferred. For a write data should be valid before /DS goes low. For a read, data will be valid 110ns after /DS goes low. During T2 /WAIT will be sampled on the rising edge of /CLK. If /WAIT is low during this time then T2 will remain high for an additonal clock and until /WAIT is high on the rising edge of /CLK.
/MREQ: /MREQ goes low to indicate to memory devices that the address on the bus is valid. It is also used to generate /RAS for Drams. At the beginning of the first DMA cycle BAI can go low at any time becuase of the delay in the daisy chain. Since BAI is variable and T1 will not be a full 166.66ns on the first cycle and /MREQ must be low at least 20ns before the falling edge of /CLK, BAI must be gated with /CLK to guarantee a setup time for /MREQ before the system clock. /MREQ is cleared during T3 when /CLK is high.

/DS: This signal goes low during T2 for a read or write. During a read /DS can go low 30ns after the beginning of T2. The 30ns allows the column address setup time.

PDMAC DC PARAMETRICS

PIN NAME	CHARACTERISTICS	MIN	MAX
1. General Information	Operating Temperature DC power	Ø C	70 C
	Supply Voltage	4.5V	5.5V
	Maximum Power Dissipation		750MW
2. Input From Z8000 Bus WAIT, CLK, BUSACK, ID/6, II-I, IACK ADØ - AD15	Capacitance		8PF
	V_{IL}		0.8V
	V_{IH}	2.0V	
	Input Leakage		10ua
3. Output to Z8000 Bus a) IEO, MREQ, BAO, ~~DS, ADØ - AD15~~ VI, (open drain only V , I applied)	Capacitance		100PF
	V_{OL}		0.4V
	I_{OL} (Sink current @) V_{OL} = Ø.4V		3.2ma ← 3.2 ma
	V_{OH}		~~2.4V~~ ← ~~2.4V~~
	I_{OH} (source current @) V_{OH} = 2.4V		200ua
b) DS, AD0 - AD15	I_{OL} @ V_{OL} = 0.4V		4.5ma
	I_{OH} @ V_{OH} = 2.4V		300 ma
4. Input From Controller BDØ - BD7 RESET, PCSS, PCSD	Same as 2		
5. Output to Controller BDØ - BD7 IREQ (open drain)	Same as 3		
6. Output to Address Latch CLKADR, DMAGN, LDØ, LD1, LD2	Same as 5		

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GENERAL TIMING

The Z8000 uses three clocks for each bus access, except for those bus accesses where the /WAIT line is activated. Three lines /AS, /MREQ and /DS are used to set up the address and control the transfer of data. Address strobe, /AS, is not used since the address is latched externally. Only /MREQ and /DS are needed along with R/W and the status lines ST0 - ST3 to transfer data on the expansion bus. The two lines /MREQ and /DS are used generate /RAS and /CAS for dynamic rams with 200ns access times. This requires that /MREQ be low 20ns before the rising edge of CLK and that the hold time from /DS low on a write must be 110ns. Also, /MREQ must be high for a minimum of 135ns to meet the precharge time for dynamic rams.

Data strobe, /DS, is used to generate /CAS for memory. The requirements for /DS are that on a write data must be valid before the falling edge of /DS and for a read the access time from /CAS is 110ns. In addition to the individual requirements for /MREQ and /DS there is a minimum cycle time of 375ns for any read or write cycle.

By emulating the Z8000 timing this will guarantee that compatibiltiy will be easily achieved since there are delays through PLAs used to generate /RAS and /CAS.

PDMAC AC SPEC

PARAMETER (Z8000 BUS)	SYMBOL	MIN	MAX
CLOCK cycle time	TCLK	160ns	240ns
BUSREQ to BUSACK	TBUS	500ns	
MREQ setup time	TMREQ	20ns	
DS delay from T2	TDSD	30ns	~~120ns~~
DS low to MREQ high	TDM	110ns	
MREQ precharge time	TMH	135ns	
Data set up time (write)	TDV	20ns	
Data hold time from DS	TDH	20ns	
WAIT set up time	TWSU	~~30ns~~ 35	
WAIT hold time	TWHD	30ns	
BUSACK to DMAEN	TBDMA		20 ~~30ns~~
CLKADDR low	TCLKLW	110 ~~40ns~~	
CLKADDR from DS rising edge	TDSCLK	~~50ns~~ ØnS	~~[illegible]~~
Data set up time from Fall edge of 6MHz (Read)	TCSS	20nS	
Data	TDWS	60nS	

all different

This table is the parameters for the 30 pin interface.

Table I

Parameter	Symbol	MIN	MAX
PCSS Low	T1	80ns	
PCSS to PCSD Delay	T2	80ns	
PCSD Low	T3	80 ~~200~~ns	
State Setup for PCSS	T4	30ns	
State Hold from PCSS	T5	30ns	
Data Setup for PCSD for LDC,1,2	T6	0ns	
Data Hold for PCSD for LDC,1,2	T7	50 ~~0~~ns	
PCSS to LDC,1,2 Delay	T8	30ns	100ns
PCSD to LDC,1,2 Delay	T9	30ns	100ns
Write Data Setup Time	T10	50ns	
Write Data Hold Time	T11	30ns	
Read Data Access Time	T12		100ns
Read Data Hold Time from PCSD	T13	30ns	

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APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVE
	Z8000				

1. Description/Part # 315017-01

The Z8000 floppy disk is an intelligent controller subsystem that will reside on one of the two floppy mechanisms it controls. The subsystem will use a 6508 CPU with RAM, 4K x 8 bit ROM, 74LS245 bus driver, custom IC, SCI575 analog read/write IC, a 7406 for LED and motor control, and four 75477 stepper drivers. The ROM will contain protocol interpreters, DMA interface drivers, and device driver code. The protocol interpreters will read commands from Z8000 memory and jump to device driver section(s) in rom that will perform the command for the specific device. The floppy disk driver will reside in the base system ROM and will be controlled by a custom IC. This custom IC provides a 1.5 MHz system clock from the Z8000 6MHz clock, address decode for ROM, selects for the 8716 Z8000 DMA controller, data separation and write precompensation for GCR and MFM formats, and I/O ports to control LED, motor, hed select, and steppers.

The interface to the Z8000 system will be via a 34 pin ribbon cable that connects to a 8716 DMA controller that resides on the main CPU board. The commands will be passed to the subsystem by writing a SCSI like command to a specified memory page in the Z8000 memory. Then the Z8000 will address a location in I/O space that will cause a I/O select and interupt the subsystem. The subsystem will then interupt the command, DMA any sector information to or from the physical device. It will then DMA back to the command area a SCSI like status information and cause a vectored interupt to the Z8000 with the 8716.

All MFM features are not implemented in this chip.

COMMODORE PART #	STATUS				
315017-01	Active				

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ±1° 2 PLACE DECIMALS ±.02 3 PLACE DECIMALS ±.010	DRWN SYSTEMS ENG TEST ENG CIRCUIT ENG COMP ENG	COMMODORE TITLE IC, LSI, Controller, Z8000 Floppy Disk 8723 SIZE A DRAWING NO. 315017 SCALE SHEET 1 OF 14

1.4 MEMORY MAP AND REGISTER ADDRESS DECODE

A15, A14, A3, A2, A1, A0, R/W and RD enable are decoded for the following memory map:

MFM register is not implemented in 8723.

0000	6508 I/O port data direction register			
0001	6508 I/O port			
0002-003F	6508 RAM			
4000	WOMLSSSS	DRIVE 0 CONTROL LINES		
	W	WRITE PROTECT		1=protected
	O	TRACK 0 DETECT		1=on track 0
	M	MOTOR ON		1=motor on
	L	LED		1=LED on
	SSSS	STEPPER CONTROL		
4001	WOMLSSSS	DRIVE 1 CONTROL LINES		1=protected
	W	WRITE PROTECT		1=on track 0
	O	TRACK 0 DETECT		1=motor on
	M	MOTOR ON		1=LED on
	L	LED		
	SSSS	STEPPER CONTROL		
4002	SMWEHPGG	CONTROL LINES		
	S	SYNC DETECT/GENERATE	(read)	1=detected
			(write)	1=generate
	M	MFM MODE		0=GCR
	W	WRITE GATE		1=on
	E	ERASE GATE		1=on
	H	HEAD SELECT		0=lower
	P	PCSS/PCSD ENABLE		0=drive 0
	GG	GCR DENSITY REGION		00=GCR 16 (2.66us)
4003		8716 PCSS REGISTER SELECT		
4004		DATA TO AND FROM DISK		
4005		DATA WITH PCSD SELECT		
4006		8716 PCSD REGISTER SELECT		
4007	TRWCSCPS	CONTROL LINES		
	T	TEST MODE	R/W	1=test mode
	R	READ ENABLE	R/W	
	W	WRITE CURRENT	R/W	
	C	CRC ERROR	READ ONLY	
	S	SET CRC	R/W	
	C	CLEAR CRC	R/W	
	P	PRECOMP	R/W	
	S	SET OVERFLOW	READ ONLY	
400C	UWNCOOOO	TEST		
	U	Δ FLUX CHANGE	RØ	
	T	WRITE DATA	RO	
	N	SHIFT REGISTER CLK	RO	
	C	STATE	RO	
	OOOO			
E000-F000		ROM select		

TEST MODE: In the test mode, the state is slowed from clocking at 6 Mhz to 1.5 Mhz. This enables the tester to read the state of the state machine during phase two high. In order to be able to read valid data from 400c, the chip must be in test mode.

1.5 GCR ENCODE/DECODE

When the MFM bit in the control register is low the disk data select will use the GCR encode/decode logic. When the write gate bit of the control register is set hi then the GCR encode logic is enabled by the state machine. The GCR 8 to 10 bit conversion is done with GCR PLA #1 and GCR PLA #2 as two seperate 4 and 5 bit conversions. The PLAs will perform a 4 bit to 4 bit conversion, the fifth bit is routed to the output (note* the gcr PLA #1 & #2 could best be implemented with descrete logic instead of a PLA). An additional input for sync generate will force all the data outputs of the PLAs hi (note* since bit 2 and 6 are routed without conversion, to generate sync then bit 2 and bit 6 should also be hi). The 10 bit converted output is then input to the shifters and latched at the next GCR-BRDY (byte ready) output from the divide by 10 counter. GCR-BRDY also signals the 6508 that another byte can be written by creating a negative edge on the SO (set overflow) pin of the 6508. The shifter is then controlled by the GCR state machine and the three most significant bits are inputs to the precompensation for the middle bit. GCR 0 and GCR 1 are also inputs to the state machine to determine the bit rate. Data output is on GCR-D and GCR-ND outputs of the state machine.

When the write gate bit of the control register is low then GCR decode logic is enabled by the state machine. Data from the disk is synchronized to the 6MHz state machine clock and is input to the state machine. This read pulse is sampled will perform phase locked data separation for the GCR density region specified by the GCR 0 & GCR 1 signals. The ouputs of the shifter connected to the GCR PLA #1 and GCR PLA #2 for GCR decode. The PLAs will also generate a sync detect signal if all the data inputs are hi, this will reset the divide by 10 counter to establish byte synchronization. Shifts are counted by the divide by 10 counter to generate the GCR-BRDY signal. This signal will then in turn latch the decoded outputs into the GCR read latch and generate a negative edge on the SO (set overflow) pin of the 6508 to signal the processor a byte is available to be read. For more details on the internal operation of the GCR state machine see section 3.2.5 GCR STATE MACHINE.

1.6 MFM ENCODE/DECODE

When the MFM bit in the control register is Hi the disk data select will use the MFM encode/decode logic. When the write gate bit of the control register is low then MFM decode logic is enabled.

1.7 GCR FORMAT

The Z8000 computer will run a version of the unix operating system and will require a 512 byte sector size. This format will use the existing commodore GCR data encode scheme with variable density (see table 3.2.2). This format will allow for 1,224,704 bytes of storage per drive. The data rate for one track will vary from 41K to 33K bytes/second for the different regions. Th multi-track transfers including step settle and latency will be 38K to 31K bytes/second.

1.7.1 ID FIELD

	SYNC	SECTOR	TRACK	GAP 1
BITS	40	10	10	120

SYNC	-	40 bits of 1's for synchronization
SECTOR	-	Sector (0-15) with bit 4 as parity (even)
TRACK	-	Track # 0-79 with bit 7 as parity(even)
GAP 1	-	Time required to turn on write gate

1.7.2 DATA FIELD

	SYNC	AM	DATA	CHECKSUM	GAP2
BITS	40	10	5120	10	120

SYNC	-	40 bits of 1's for synchronization
AM	-	Address mark=hex 88
DATA	-	512 bytes of data
CHECKSUM	-	Exclusive OR of data bytes and checksum = 0
GAP 2	-	Variable determined by drive speed

1.7.3 GAP 2 DETERMINATION

During format gap 2 must allow for 2% speed variation at the end of each sector, so that fast running drives will not write over the beginning of the next sector. This 2% is for drives that are running at the correct speed, so this figure must be adjusted for the drive speed at the time of format. Compensating for motor speed error in format will allow gap 2 to be 2% vs. 4% if th format speed is not known. This will generate another 2% of disk space for storage and will check the drive for an out of specification speed. The format will perform a speed check to by writing 38*256 bytes of GCR 0 (210,773ms or 105%) followed by 4 bytes of sync. The gcr 0 bytes are then counted until sync is found. This number is the total number of bytes that can be written on track 1 at the current speed. A minimum gap 2 of 12 bytes is selected for a drive that is running 2% fast and this is incremented by 1 byte for every 16 bytes/track extra. The same procedure is followed for all four of the density regions.

1.7.4 GCR DATA RATES/FORMATTED CAPACITY

TRACK REGION	BIT TIME	SECTORS/TRACK	SECTORS/REGION
1-39	2.16	16	624
40-53	2.33	15	210
54-64	2.50	14	154
65-80	2.66	13	208

SECTORS/SIDE = 1 196
SECTORS/DISK = 2,392
BYTES/DISK = 1,224,704
BYTES/CONTROLLER = 2,449,408

1.7.5 GCR CODE CONVERSION

#	BINARY	GCR	#	BINARY	GCR
0	0000	01010	8	1000	01001
1	0001	01011	9	1001	11001
2	0010	10010	a	1010	11010
3	0011	10011	b	1011	11011
4	0100	01110	c	1100	01101
5	0101	01111	d	1101	11101
6	0110	10110	e	1110	11110
7	0111	10111	f	1111	10101

1.8 GCR STATE MACHINE

The GCR state machine will reform phase locked data separation during read operations, and write precompensation during write operations. The state machine is constructed as a PLA with outputs connected to a latch that is clocked at 6MHz. Some of the outputs of the latch are then returned as inputs to the PLA to determine the next state. This will cause the PLA to change states at a 6MHz rate. A base of 16 states are chosen for the lowest density region. This is derived by 16* 166.66ns (6MHz) = 2.66us bit cell time. This is varied for the other regions by skipping states 3,5, and 13 to arrive at 2.166, 2.333 and 2.5us bit cell times as shown by Figure 3 GCR STATE DIAGRAMS below as the GG input. During read operations (write gate=0) the read pulse should occur near state #8. The active transition of RP will have a twofold ??? effect. First, the data output to the shift registers will go hi so that during state 15 when the shifter is clocked the data will be one (note: data into the shifter will go low on state #0). And, second, if RP occurs early or late of state #8 the state machine will change the current state number closer to state #8. The ??? further away from state #8 the greater the correction. This will create a phase locking on the transition for proper data separation.

During write operations, the data output eill be toggled when the input data in high. This toggling is done at state 7,8 or 9 depending on the data before and after the current bit. This is shown in Figure 4 GCR WRITE STATE DIAGRAMS as +0-.

Figure 3

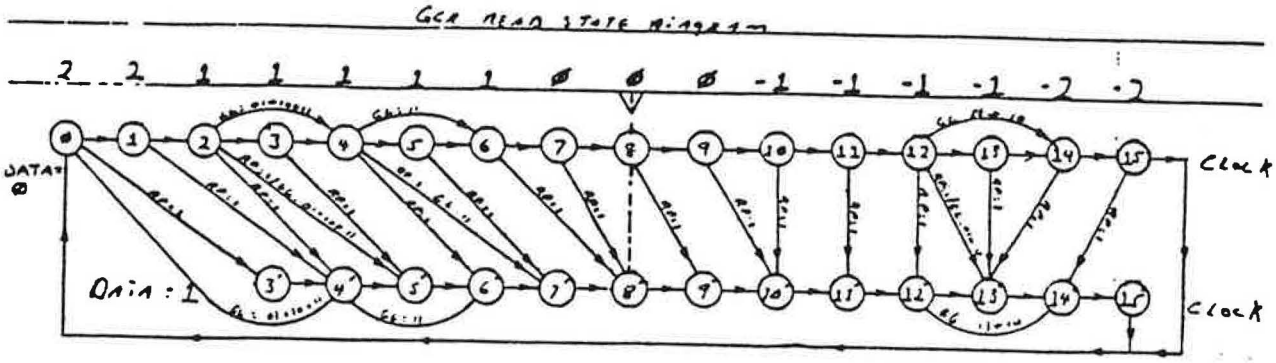
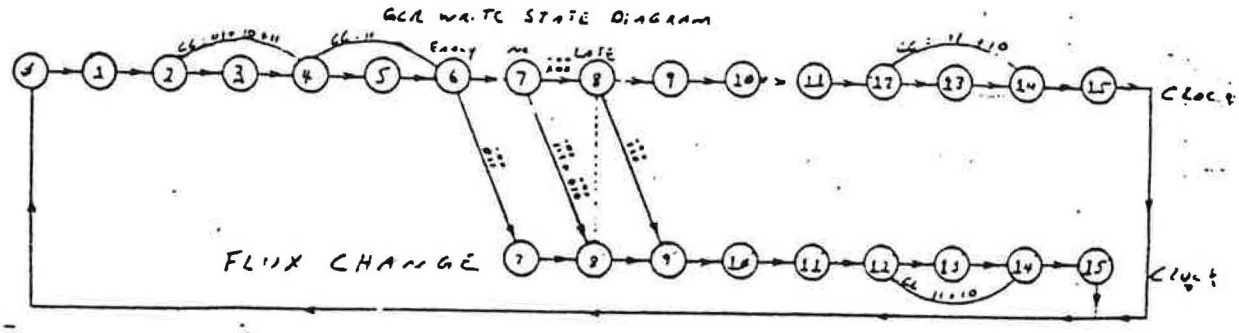


Figure 4



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1.9

The rules of MFM are:

1 - The data bit still appears in the middle of a bit frame

2 - The clock bit is written at the beginning of the frame only if 2 conditions are met:

21 - No data bit will appear in the current frame

22 - There was no data bit in the previous frame.

In other words, a clock bit is inserted only if two consecutive frames would contain "00".

When reading data from the disk, FM must be converted to digital, with absolute accuracy. In addition a separate detection is required for Clock and Data bits. Special problems may occur with some bit patterns. This is known as the "bit-shifting" problem, and a PLO (phase locked oscillator) is normally used for precise bit detection.

All data on the disk is structured in bytes. Bytes (groups of 8-bits) must also by synchronized. This function is performed by starting every block of information with a special marker. When the diskette is first used, it must be initialized, or "formatted" with these markers. Byte counts are initialized when these ID or data marks are read.

Finally, a serial to parallel conversion must be performed to assemble 8 bits into a byte. This is done by the disk-controller.

The operations required by a "write" are naturally the reverse of those described above for a "read".

1.9.1

For this reason, a blank gap must be provided between the end of one record, and the beginning of the next one. In fact, a gap must be provided between any two zones which might be updated separately. Most often the IBM disk-track format is used, sometimes with minor variations. This format is illustrated on Fig.4-100. Four kinds of gaps are used:

Gap 4 is used only once on the track. It is the free-index gap. It appears at the end of the track just before the index-hole position.

Gap 1 is called the index-gap, and is used at the beginning of every track. It contains 20 bytes: the first 16 bytes contain the hexadecimal pattern "FF" followed by 4 bytes containing "00". These four bytes of 0's are the classical way to provide the synchronization for the data-separator. The length of gap 1 may never vary in length. The index-gap is followed by the identification of the first record.

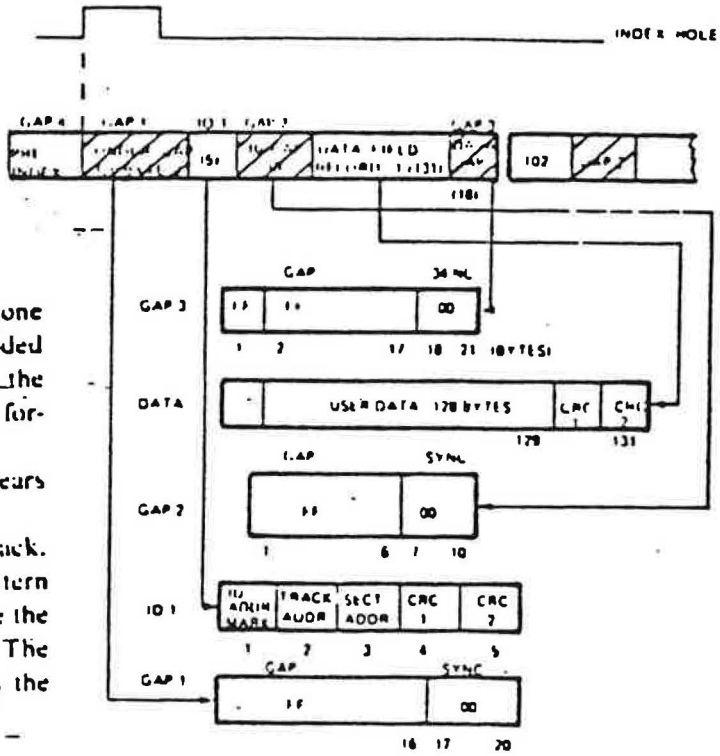

Fig. 4-100: IBM Floppy-Disk Format

Figure 5

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FORM NO. 151

ID 1 is the identification-field of the first record. It uses 8 bytes: the ID address-mark, the track-address, the sector-address, and two CRC check-sum bytes to verify the integrity of the field. The track-address and the sector-address provide a verification that the right track and sector have indeed been accessed.

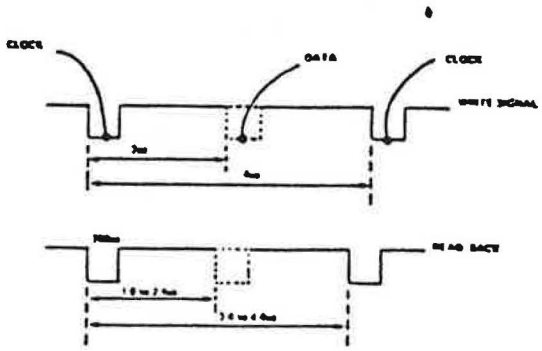

Figure 6 Timing

1.9.2

Gap 2 is called the ID-gap and separates each successive identification field from its data field. It uses 10 bytes. The first 6 bytes contain the hexadecimal pattern "F". It is followed by the four usual synchronization bytes containing "00". The length of gap 2 may vary in length after file updating.

The first *record*, or data-field follows. It uses 131 bytes (see Fig. 4-100.) The first bytes contains data or deleted address-mark. It is followed by the actual 128 bytes of user data. It is terminated by the two usual CRC check-sum bytes.

Finally, *Gap 3* terminates the first record. It is called the data-gap and uses 18 bytes. The first 17 bytes are set to the pattern "FF", and the four last bytes contain "00", for the sync. Every successive record on the disk, or sector, will start with ID, gap 2, and so on.

1.9 [illegible] Hard-sectoring

When using hard-sectoring, a special diskette and drive are used. A hole is punched at the beginning of every sector on the disk. Each sector is then started by a physical sector pulse. In the case of the mini-floppy disk, two configurations are used: 16 sectors of 128 bytes or 10 sectors of 256 bytes per track. The track is started by the index pulse. This is illustrated on Fig. 4-102. figure 7

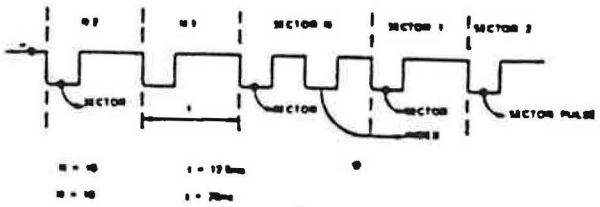

Fig. 7 Hard-Sectored Disk Timing

1.9.4

Error Detection and Correction

Three types of errors are distinguished:

Write Error

This corresponds to the case where the data being written on the disk is not written correctly. The way to verify whether data has been correctly written is to use a "write-check" procedure, where the data is read again during the next revolution of the disk. Normally, the user will simply write again data which has not been correctly written on the disk, and attempt to do so repeatedly (up to 10 times). If this effort fails continuously, the sector or the track must be considered as damaged and not usable.

Read Error

Two types of read errors must be distinguished:

1. Soft: this corresponds to the case where the error has been transient and is corrected by simple re-reading (up to 10 times) or by moving the head back and forth once.

Typically the head is moved one more step in its previous direction, then

COMMODORE	TITLE FC, LSI, Controller, Z8000 Floppy Disk 8723	
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moved back. Usually this corrects most reading errors. If this procedure fails, we have a hard error:

2. Hard: Whenever usual correction procedures fail to read data from the disk, it must be deemed unrecoverable. This is a fatal error. Data is lost.

..9.5 *SEEK ERROR*

This corresponds to the case where the head does not reach the correct track. This can be verified by reading the ID field at the beginning of the track. It contains the track address. Whenever an error is detected, the track-counter of the disk drive must be recalibrated. The head is moved back to track 00 and a new Seek order is issued.

..9.6 *DETECTING ERRORS*

Universally, the error-detection for any data written on a disk is accomplished by using a *checksum* method. Cyclic-redundancy-check (CRC) is used for this purpose. Each field is terminated with two CRC bytes. The data bits are divided by a generator polynomial G(X) such as $G(X) = X^{16} + X^{12} + X^5 + 1$. The remainder of this division is called the CRC. It is written in the two bytes that follow the data. When reading back data from the diskette: everything is read, including data in the CRC bytes. If the remainder of the division by the G(X) polynomial is not 0, an error has been detected.

Single-chip CRC's exist such as the Fairchild 9401, the Motorola 8501, and others, that will detect such failures in a single chip. One-chip floppy-disk-controllers (FDC) also accomplish the CRC generation and checking, within the single chip.

1.9.7 **Cyclic Redundancy Check**

CRC is the favorite method for verifying the integrity of memory areas with a minimal waste of bits. Parity will detect a single-bit error within a word. Whenever parity is not available, or would be too costly to provide, CRC is used to detect errors in a block of words. In particular CRC is almost always used in the case of floppy-disks, and tape-cassettes. In addition, it is often used to verify the integrity of a ROM. The principle of a CRC technique is the following: the eight bits of the word are treated as coefficients of a polynomial of degree 7.

The bit pattern $B_7\ B_6\ B_5\ B_4\ B_3\ B_2\ B_1\ B_0$ is interpreted as $B_7 X^7 + B_6 X^6 + B_5 X^5 + B_4 X^4 + B_3 X^3 + B_2 X^2 + B_1 X^1 + B_0 X^0$.

X is called here a dummy variable.

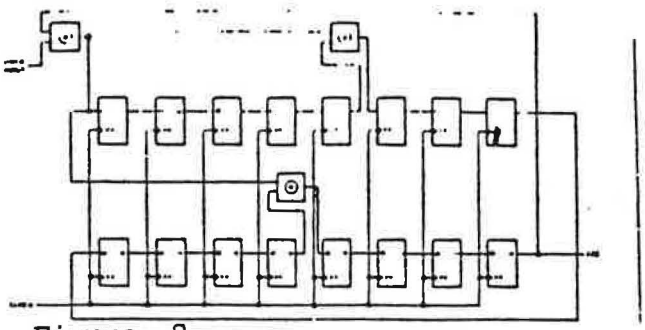

Figure 8

CRC Check Hardware Detail

For example, the binary word: "10000011" will represent:
$B(X) = 1 X^7 + 0 X^6 + 0 X^5 + 0 X^4 + 0X^3 + 0 X^2 + 1 X^1 + 1 X^0$
$= X^7 + X^0 + 1$.

A generator polynomial G(X) will be used. The polynomial B(X) corresponding to the binary word is divided by this generator G(X). The result is the quotient Q(X) and a remainder R(X).

$B(X) = G(X)\ Q(X) + R(X)$

The value of CRC-redundancy-checking is to append to a bit string an extra byte (or bytes), equal to R(X), so that the total string will be exactly divisible by the generator polynomial. The above equation can be rewritten: $B(X) - R(X) = Q(X) \cdot G(X)$. The string formed by B and the remainder R is exactly divisible by G(X). The extra bits appended to the string B are called the CRC bits (or bytes). When receiving for the first time a string B, the CRC generator will compute the remainder R which will be appended to the string. When the string will be retrieved another time, the complete sequence of bits, including the CRC bits will be read. They should then be exactly divisible by the generator polynomial G(X). If they are not, an error has been detected. If they are divisible, no error has occurred, or else a non-detectable error has occurred.

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SIZE A	DRAWING NO. 315017	REV	SCALE / SHEET 11 OF 1

FORM NO. 161

2.0 ELECTRICAL PARAMETERS

2.1 Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the circuit. This is a stress rating only. Functional operation of the device at these or any conditions other than those indicated in the operational sections of this specification is not implied.

	MIN	MAX
Operating Temperature	0 C	70 C
Supply Voltage	4.5V	5.5V
Maximum Power Dissipation		1W

2.2 D.C. Characteristics

	PIN NAME	CHARACTERISTICS	MIN	MAX
2.2.1	Input from 6508 Bus	Capacitance		8PF
	CLK, R/W, RESET,	Vil		0.8V
	A0-A3,A14,A15,D0-D7	Vih	2.0V	
2.2.2	Clock Output to 6508	Capacitance		30PF
	PH1, PH2	Vol		0.4V
		Voh	2.4V	
		Iol(@Vol=0.4)	3.2ma	
		Ioh(@Voh=2.4)	200ua	
2.2.3	Output to 6508 Bus	Capacitance		100PF
	DMADIR, SO,	Vol		0.4V
	D0-D7	Voh	2.4V	
		Iol(@Vol=0.4)	3.2ma	
		Ioh(@Voh=2.4)	200ua	
2.2.4	Input from Floppy Disk			
	RDATA, WPO, WP1,	Same as 2.2.1		
	DO TRO, D1 TRO			
2.2.5	Output to Floppy Disk			
	LED0, STEP00-3	Same as 2.2.3		
	LED1, STEP10-3,WRGT			
	HDSEL,BUFEN,ERASE			
	NWD, WD, MTRONO, MTRON1			
2.2.6	Tri-State Output	Capacitance		100PF
		Vol		0.4V
	PCSS, PCSD	Voh	2.4V	
		Iol(@Vol=0.4)	3.2ma	
		Ioh(@Voh=2.4V)	200ua	

2.3 A.C CHARACTERISTICS

Clock Time (TCLK)	6 MHz
PH1	1.5 MHz
PH2	1.5 MHz

See figure 8 for timing.

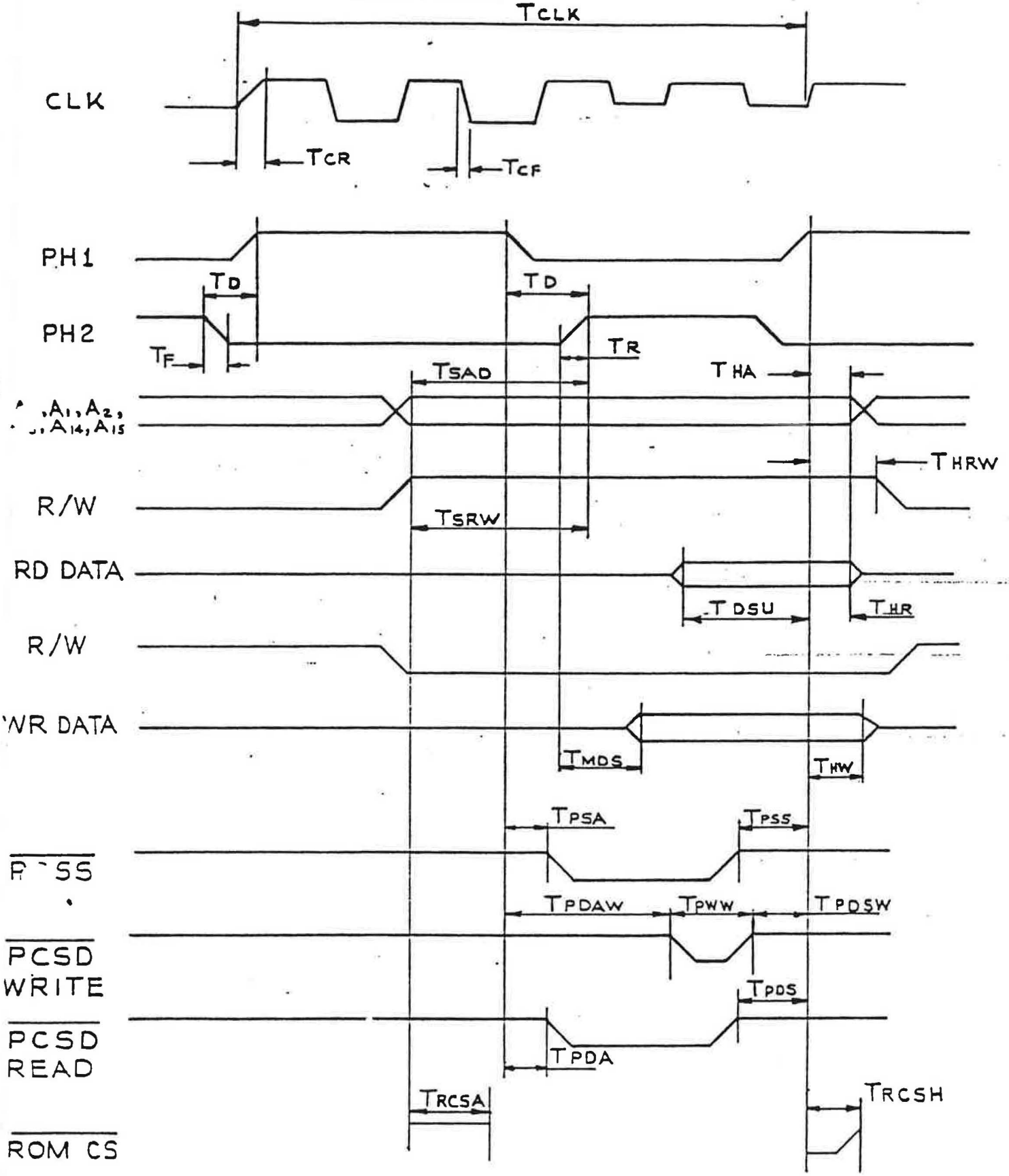
Parameters	Min.	Max.
Delay between clocks (TD)	0 ns	
Falltime, Risetime (TF,TR)		20 ns
Address Setup Time (TSAD)	180 ns	
Address Hold Time (THA)	10 ns	
Read/Write Setup Time (TSRW)	180 ns	
R/W Hold Time (THRW)	10 ns	
Data Stable Time (TDSU)	50 ns	
Data Hold Time-Read (THR)	10 ns	
Data Setup Time (TMDS)		100 ns
Data Hold Time Write (THW)	10 ns	
PCSS Strobe (TPSS)	20 ns	170 ns
PCSS Active (TPSA)		70 ns
PCSD Write Active (TPDAW)	130 ns	200 ns
PCSD Write Strobe (TPSDW)	20 ns	
PCSD Write Width (TPWW)	80 ns	
PCSD Active Read (TPDA)		125 ns
PCSD Strobe Read (TPDS)		20 ns
ROMCS Active (TRCSA)		250 ns
ROMCS Hold Time (TRCSH)	10 ns	

2.4 SWITCHING CHARACTERISTICS

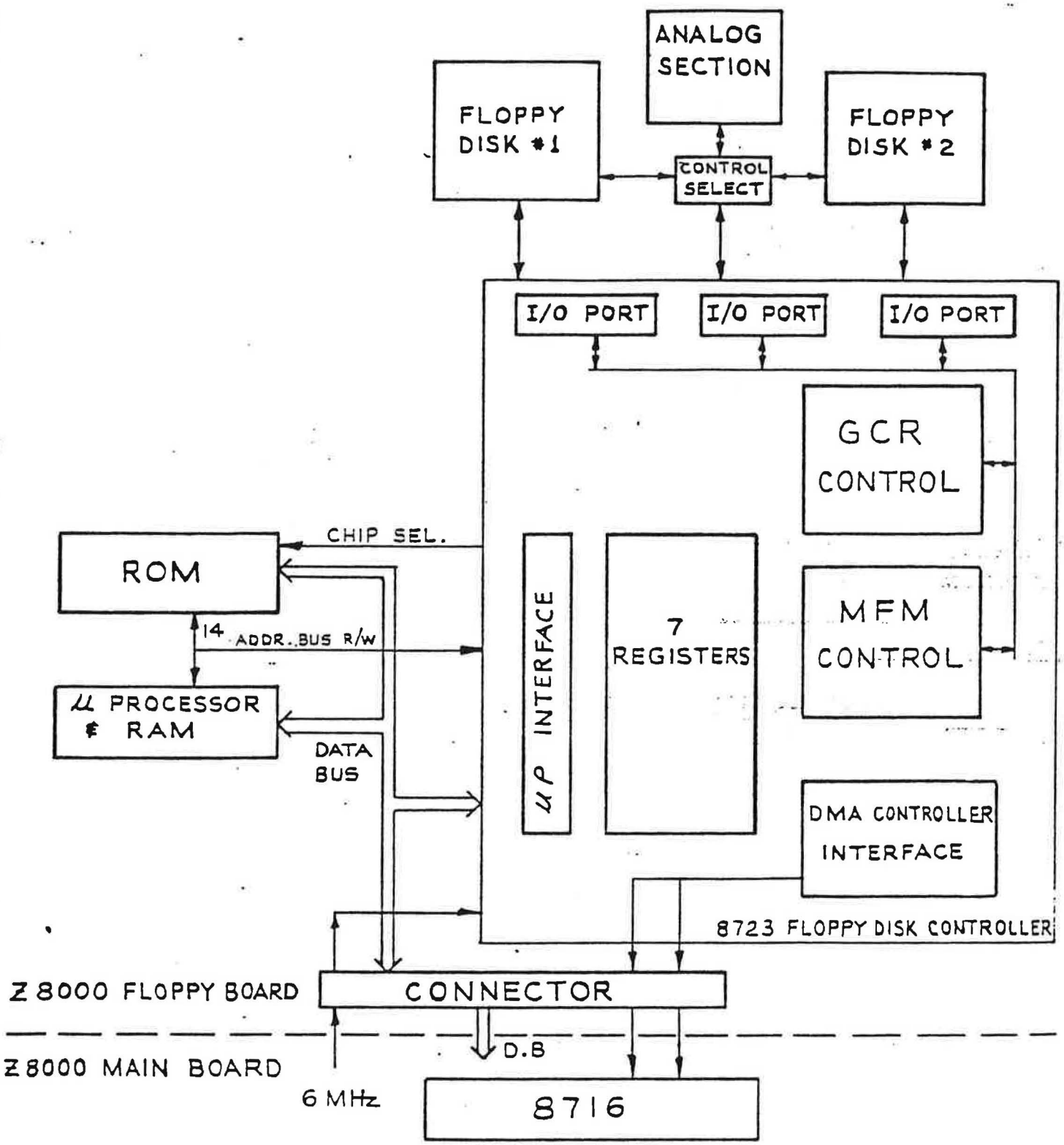
Switching characteristics are specified for input waveforms switching between 0.4V low level and 2.4V high level with 10% - 90% rise and fall times of 10ns. Outputs are loaded at the rated interface conditions with 130pf total capacitive load (including fixturing). All time measurements of driven signals are referenced to 1.5V on inputs and outputs. Time measurements of high impedance signals are referenced to Vol + 0.2V levels. See Figure (xx) for timing relationships.

FIGURE 8

A.C. TIMING



COMMODORE			TITLE: IC, LSI, CONTROLLER, Z8000 FLOPPY DISK 8723
SIZE	DRAWING NO. 315017	REV	SCALE — / SHEET 14 OF



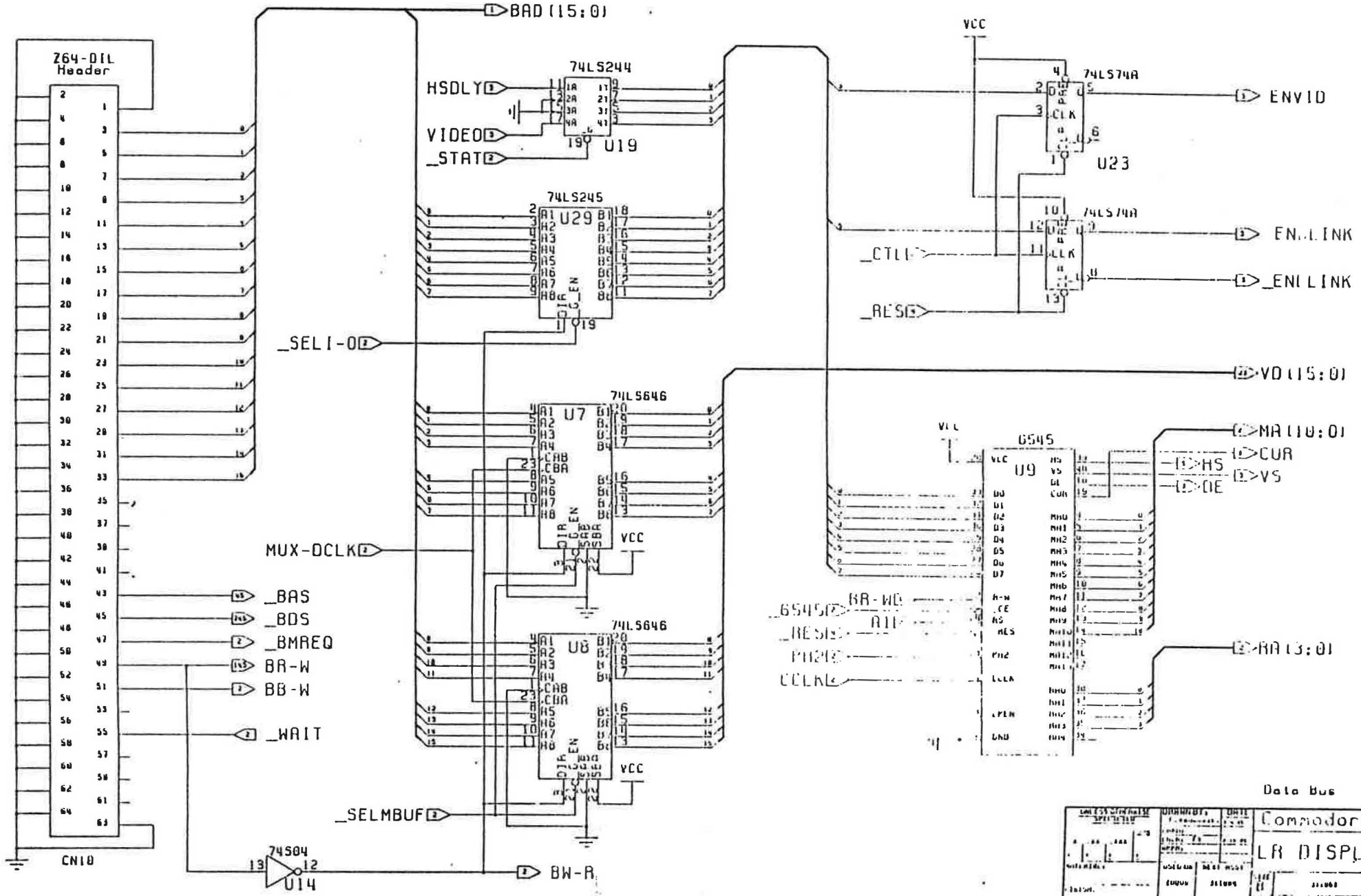
COMMODORE			TITLE IC, LSI, CONTROLLER, Z 8000 FLOPPY DISK 8723
SIZE A	DRAWING NO. 315017	REV	SCALE — / SHEET 15 OF 15

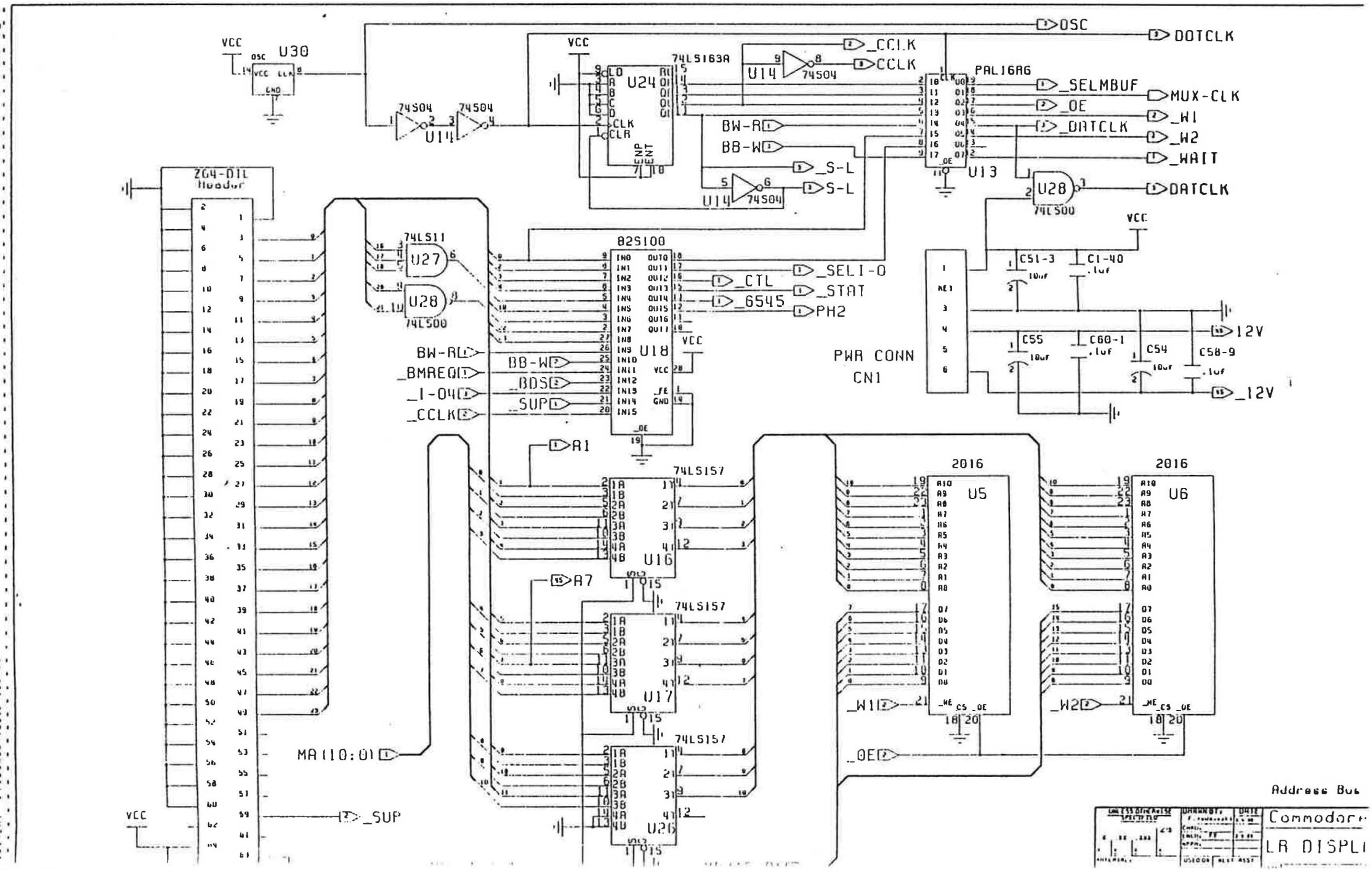
APPROVED VENDOR LIST

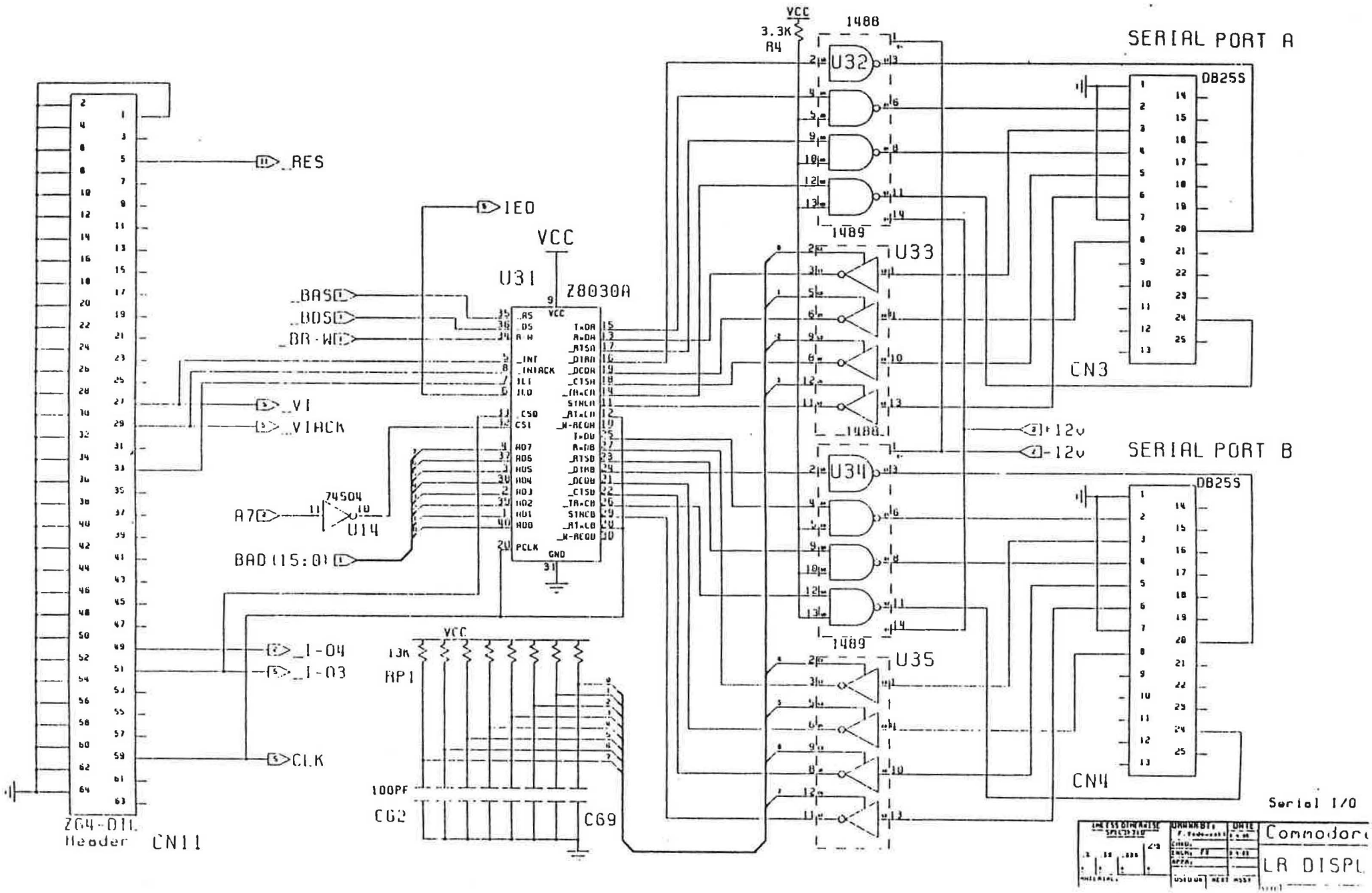
This page must be detached from the remainder of the drawing whenever this drawing is shown or transmitted to vendors.

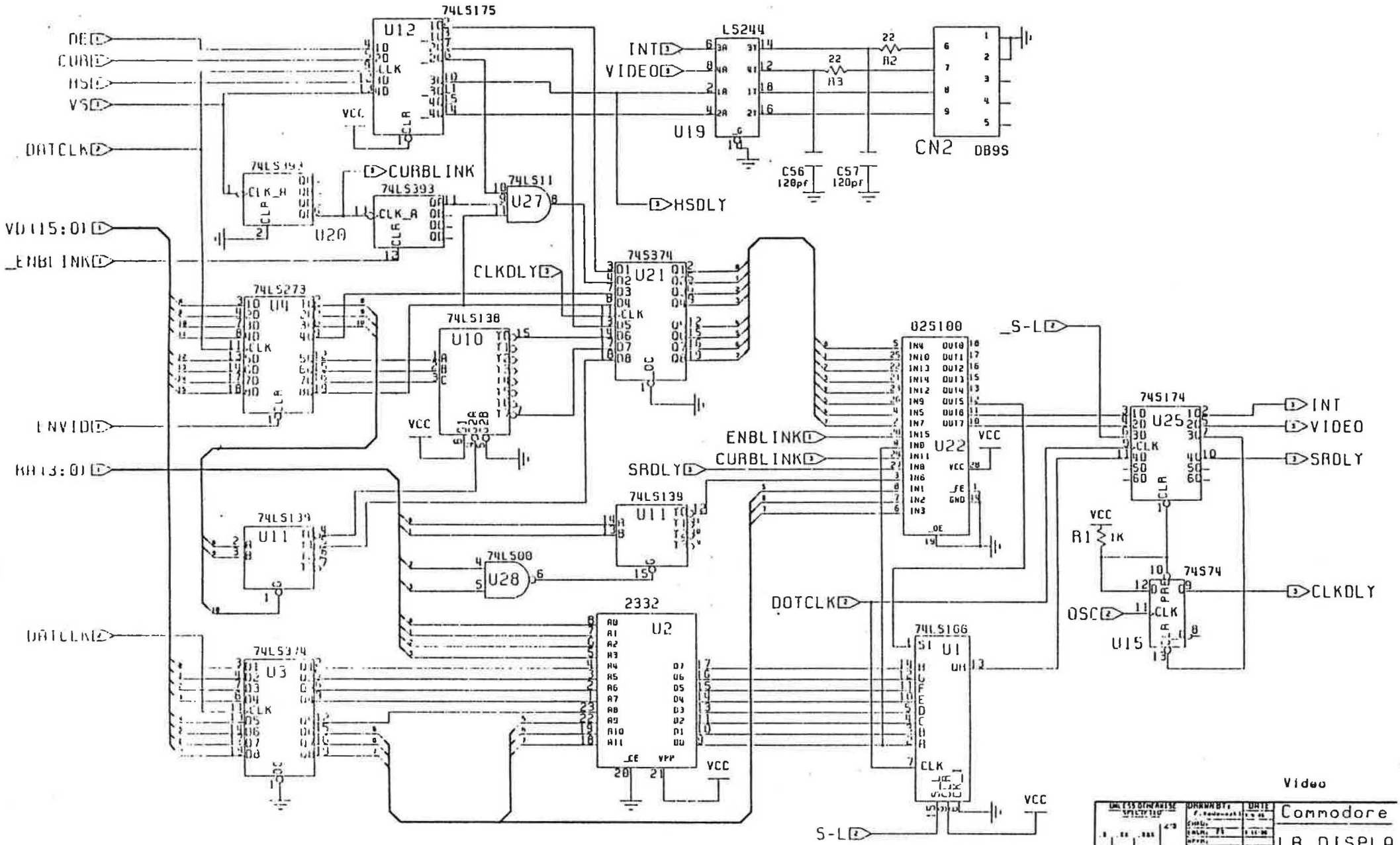
VENDORS	UNPROGRAMMED VENDOR PART NO.
MOS TECHNOLOGY	8723

COMMODORE			TITLE IC, LSI, Controller, Z8000 Floppy Disk 8723
ZE	DRAWING NO. 315017	REV	SCALE / SHEET i OF i


Z64-DIL Header
CN10
BAD(15:0)
74LS244
U19
HSDLY
VIDEO
_STAT
74LS245
U29
_SELI-0
74LS646
U7
U8
MUX-DCLK
VCC
_BAS
_BDS
_BMREQ
BR-W
BB-W
_WAIT
_SELMBUF
74S04
U14
BW-R
74LS74A
U23
ENVID
ENLINK
_ENLINK
_CTLI
_RES
VD(15:0)
6545
U9
MA(10:0)
CUR
HS
VS
DE
RA(3:0)
_6545
BR-WD
A11
PH2
CCLK
Data Bus
Commodore
LR DISPLAY


OSC
DOTCLK
VCC
U30
OSC
VCC CLK
GND
74S04
U14
74S04
U14
74LS163A
U24
LD
A
B
C
D
CLK
CLR
RC
QA
QB
QC
QD
NP
INT
_CCLK
CCLK
U14
74S04
PAL16A6
U13
_SELMBUF
MUX-CLK
_OE
_W1
_W2
_DATCLK
_WAIT
BW-R
BB-W
_S-L
S-L
U14
74S04
U28
74LS00
DATCLK
264-DIL
Header
74LS11
U27
U28
74LS00
82S100
U18
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
IN9
IN10
IN11
IN12
IN13
IN14
IN15
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
VCC
GND
_OE
_SELI-0
_CTL
_STAT
_6545
PH2
BW-R
BB-W
_BMREQ
_BDS
_I-O4
_SUP
_CCLK
VCC
PWR CONN
CN1
C51-3
10uF
C1-40
.1uF
C55
10uF
C60-1
.1uF
C54
10uF
C58-9
.1uF
12V
_12V
A1
74LS157
U16
A7
74LS157
U17
74LS157
U26
2016
U5
2016
U6
_W1
_W2
_OE
MA[10:0]
_SUP
VCC
Address Bus
Commodore
LR DISPLI


SERIAL PORT A
SERIAL PORT B
DB25S
CN3
CN4
U32
U33
U34
U35
1488
1489
VCC
3.3K
R4
U31
Z8030A
_RES
IEO
_BAS
_BDS
_BR-W
_VI
_VIACK
A7
74S04
U14
BAD(15:0)
_I-04
_I-03
CLK
13K
RP1
100PF
C62
C69
+12v
-12v
Z64-DIL
Header
CN11
Serial I/O
Commodore
LR DISPL


74LS175
U12
DE
CURB
HSB
VS
DATCLK
VCC
LS244
U19
INT
VIDEO
22
R2
22
R3
CN2
DB9S
C56
120pf
C57
120pf
CURBLINK
74LS393
U20
74LS11
U27
HSDLY
VD[15:0]
_ENBLINK
74S374
U21
CLKDLY
74LS273
U4
74LS138
U10
ENVID
RA[3:0]
74LS139
U11
74LS00
U28
DATCLK
74LS374
U3
2332
U2
DOTCLK
74LS166
U1
S-L
_S-L
82S100
U22
ENBLINK
CURBLINK
SRDLY
74S174
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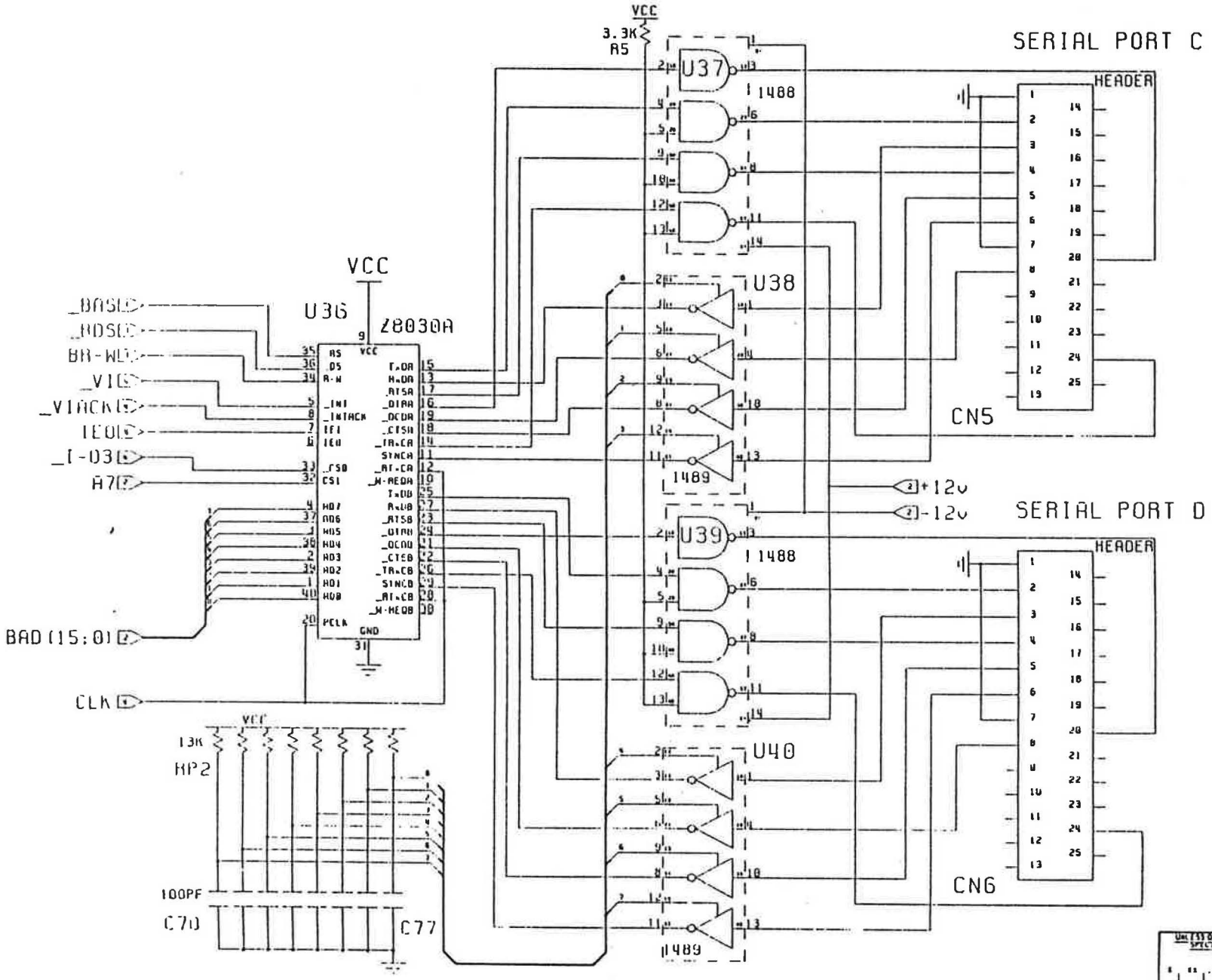
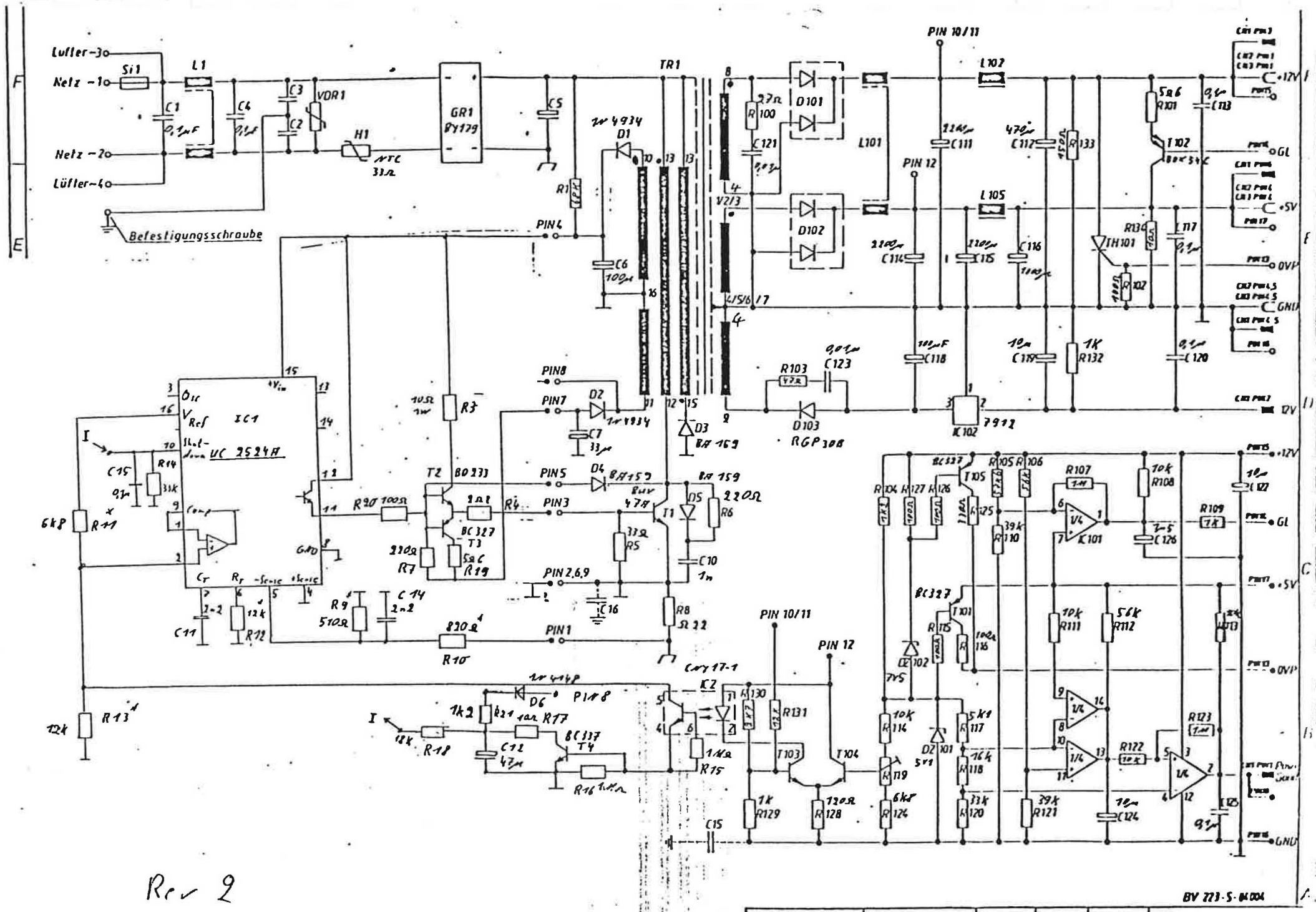
74S74
CLKDLY
OSC
U15
Video
Commodore
LR DISPLA



Serial I/O

Commodore

LR DISPLA



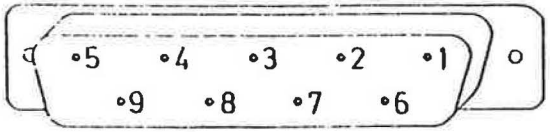
Rev 2

BV 223-S-84004

Werkstoff	Oberfläche	Gezeichnet	18.12.84	Br	2-64-3
		Geprüft			

Character-Mode Video Connector

Female DB-9



PIN	Description
1	GND
2	GND
3	Not used
4	Not used
5	Not used
6	+Intensity
7	+Video
8	+Horizontal
9	-Vertical

RS 232 CONNECTOR

PIN	SIGNAL NAME
1	CHASSIS GROUND
2	TxD
3	RxD
4	RTS
5	CTS
6	DSR
7	SIGNAL GROUND
8	DCD
20	DTR

PRINTER CONNECTOR

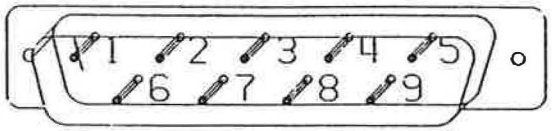
PIN	SIGNAL NAME
1	_CDS
2	CD0
3	CD1
4	CD2
5	CD3
6	CD4
7	CD5
8	CD6
9	CD7
10	_CACK
11	CBSY
18-25	GROUND

NOTES:

- The printer connector has the same pinout as the printer connector on the IBM PC.
- Both connectors are female DB25.

Mouse connector

MALE DB-9



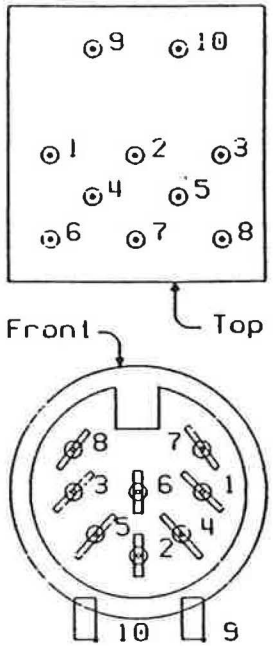
PIN	Description
1	Y(A) quadrature
2	X(A) quadrature
3	Y(B) quadrature
4	X(B) quadrature
5	BUTTON(2)
6	BUTTON(1)
7	+5
8	GND
9	BUTTON(3)

Commodore 906 High Resolution Video Card

Monochrome video connnector

DIN-8

PIN	Description
1	-ECL Video out
2	GND
3	GND
4	+ECL Intensity
5	Vertical sync
6	GND
7	+ECL Video out
8	Horizontal sync
9	GND
10	GND



Corrections for

"C O H E R E N T Version 0.7.3 Preliminary Release Notes"

Page 5:

Near Center of the page,

"/dev/wd2"

should read

"/dev/hd2"

Page 8:

Section near the bottom of the page reading

"...standard time zone is Eastern Standard Time (EDT), your daylight-savings time zone is Easter..."

should read

"...standard time zone is Eastern Standard Time (EST), your daylight-savings time zone is Eastern..."

NAME
fdformat - format a floppy disk

USAGE
/etc/fdformat filesystem

DESCRIPTION
fdformat formats a floppy disk. This action will erase the previous contents of the disk.

Only the superuser may use fdformat.

EXAMPLES
/etc/fdformat /dev/fd1
This command will format a disk in the built in drive.

DIAGNOSTICS
"I/O error" for a bad floppy, write protected floppy, or no floppy in drive.