SERVICE MANUAL

PC40-III

MARCH, 1989

PN-314134-01

commodore COMPUTERS

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PC40-III

MARCH, 1989 **PN-314134-01**

CBM INTER-COMPANY
(NOT FOR RESALE)

Commodore Business Machines, Inc.
1200 Wilson Drive, West Chester, Pennsylvania 19380 U.S.A.

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SECTION 1

SPECIFICATIONS

DESCRIPTION

This specification describes the Functional Requirements for the PC40-III computer. This system consists of a processor, memory, control unit and keyboard. This system is compatible with the IBM AT series of computers. The monitor for the system is an independent unit and must be VGA compatible.

STANDARD FEATURES

MICROPROCESSOR	80286
SPEEDS	6, 8, 12 MHz user selectable
MEMORY CAPACITY	1 MByte on board
VIDEO OUTPUT	Video Graphics Array compatible Horizontal scan frequency 31.5 KHz
VIDEO DISPLAY RAM	256 KByte
PARALLEL OUTPUT	Centronics (IBM) Compatible
SERIAL OUTPUT	RS-232 IBM Compatible
MOUSE PORT	Commodore 1352 mouse Hardware and Software Compatible with Microsoft Bus Mouse
AutoConfig BIOS	
BATTERY BACKED UP CLOCK	
EXPANSION SLOTS	3 AT style slots 1 XT style slot
DISK STORAGE	40 MByte hard disk (formatted) (AT style drive with embedded controller) 1.2 MByte Floppy Disk (formatted)
112 WATT POWER SUPPLY	

OPTIONAL FEATURES

Math Coprocessor 80287.

Disk and Tape storage

1 40 MByte hard disk drive inside the case.
1 5.25″ 1.2 MByte floppy drive accessible from the front of the unit.
1 unused slot that can be used for a second floppy or a streaming tape unit.
Either or both floppy drives may be 3.5″ drives.

Expansion slots

The three full length expansion slots conform to the standard AT bus structure, therefore, all options that are available for the AT on the after sale market are available on this unit.

The one XT expansion slot is for short cards that do not require a full length slot.

VIDEO FEATURES

ALPHANUMERIC MODES

MODE #	COL X ROW	CHAR MATRIX	RESOLUTION	COLORS	STANDARD
0, 1	40 X 25	8 X 8	320 X 200	16	CGA (1)
		9 X 16	360 X 400	16 OF 256K	VGA (2)
2, 3	80 X 25	8 X 8	640 X 200	16	CGA (1)
		9 X 16	720 X 400	16 OF 256K	VGA (2)
7	80 X 25	9 X 14	720 X 350	MONOCHROME	MDA
		9 X 16	720 X 400	MONOCHROME	VGA (2)
54	132 X 43	7 X 9	924 X 387	COLOR	ENHANCED
55	132 X 25	7 X 16	924 X 400	COLOR	ENHANCED
56	132 X 43	7 X 9	924 X 387	MONOCHROME	ENHANCED
57	132 X 25	7 X 16	924 X 400	MONOCHROME	ENHANCED

GRAPHICS MODES:

MODE #	RESOLUTION	COLORS	STANDARD
4, 5	320 X 200	4	CGA (1)
		4 OF 256K	VGA (1) & (2)
6	640 X 200	2	CGA
		2 OF 256K	VGA (1) & (2)
D	320 X 200	16 OF 256K	VGA (1)
E	640 X 200	16 OF 256K	VGA (1)
F	640 X 350	MONOCHROME	VGA
10	640 X 350	16 OF 256K	VGA
11	640 X 480	2 OF 256K	VGA/MCGA
12	640 X 480	16 OF 256K	VGA
13	320 X 200	256 OF 256K	VGA/MCGA (1)

NOTES

(1) All 200 line modes are double scanned for 400 line resolution.
(2) The VGA implementation of these modes is the default.

VIDEO SIGNALS

Vertical	Horizontal sync		Vertical sync	
Resolution	**Frequency**	**Polarity**	**Frequency**	**Polarity**
350 lines	31.5 KHz	+	70.1 Hz	–
400 lines	31.5 KHz	–	70.1 Hz	+
480 lines	31.5 KHz	–	59.9 Hz	–
600 lines*	35.2 KHz	–	56.2 Hz	–

*Requires an Analog MultiSync compatible monitor.

BLOCK MEMORY MAP

Standard Memory
640 KBytes range 0 to 655360 decimal (0h to 9FFFFh)
384 KBytes range 1048576 to 1441792 decimal (100000h to 160000h)
The top 384 KBytes of memory can be disabled to function with third party add on boards.

KEYBOARD FEATURES

standard

United States	ASCII 101
International	102 key

optional

Dvorak

Special keyboards and drivers are available to customize the keyboard for the following countries. Germany, Spain, France, Italy and the United Kingdom.

ADDITIONAL FEATURES

Numeric keypad
4 cursor keys in an inverted T formation

OTHER FEATURES

Security lock for keyboard lock out
Built in speaker
External Configuration switches
Battery backed-up real time clock/calendar.
Metal Case (can support monitor)

MultiSync is a registered trademark of NEC

SPEED SELECTION

One of the three operating speeds is selected by either a program or by the operator.
Default speed is 6 MHz. The operator or program can change the speed by issuing the following command strings.
Control Alternate S for standard 6 MHz
Control Alternate T for turbo 8 MHz
Control Alternate D for double 12 MHz

PHYSICAL SPECIFICATIONS

Height	5.75 inches	14.6 cm
Depth	15 inches	38.1 cm
Width	14 inches	35.6 cm
Weight	21 pounds	9.55 Kg
Minimum Clearances		
Right side	4 inches	10.2 cm
Back side	4 inches	10.2 cm

ENVIRONMENT SPECIFICATION

ENVIRONMENTAL	
—temperature—	
Operational	4 to 40 C. (+39 to +122 F)
Storage	−40 to +60 C. (−40 to +160 F)
Gradient	+10 C/Hour (+18 F/Hour)
—humidity—	
Relative	8% to 80% RH (no condensation)
Gradient	20% per Hour (no condensation)
Wet Bulb	26 C, 78 C (no condensation), maximum
VIBRATION	
Operational	0.048 in. Dbl. Amplitude (5 - 17 Hz) 0.73 G, 17 - 150 Hz 0.33 G, 200 to 500 Hz use linear interpolation for acceleration levels between 150 Hz and 200 Hz
Non-Operate	1.0 G, 5 - 2000 Hz, sweep of .067 decades/minute
SHOCK	
Operational	10 G, 11 mS Half Sine Wave; any axis.
Non-Operate	50 G, 25 mS Square Wave; any axis. 25 G, 25 mS Square Wave; heads over data.
ALTITUDE	
Operational	−457 to 2,972 Meters (−1,500 to + 9,750 Ft)
Non-Operate	−457 to 12,192 Meters (−1,500 to +40,000 Ft)
ACOUSTIC NOISE	45 dBA at 1 meter

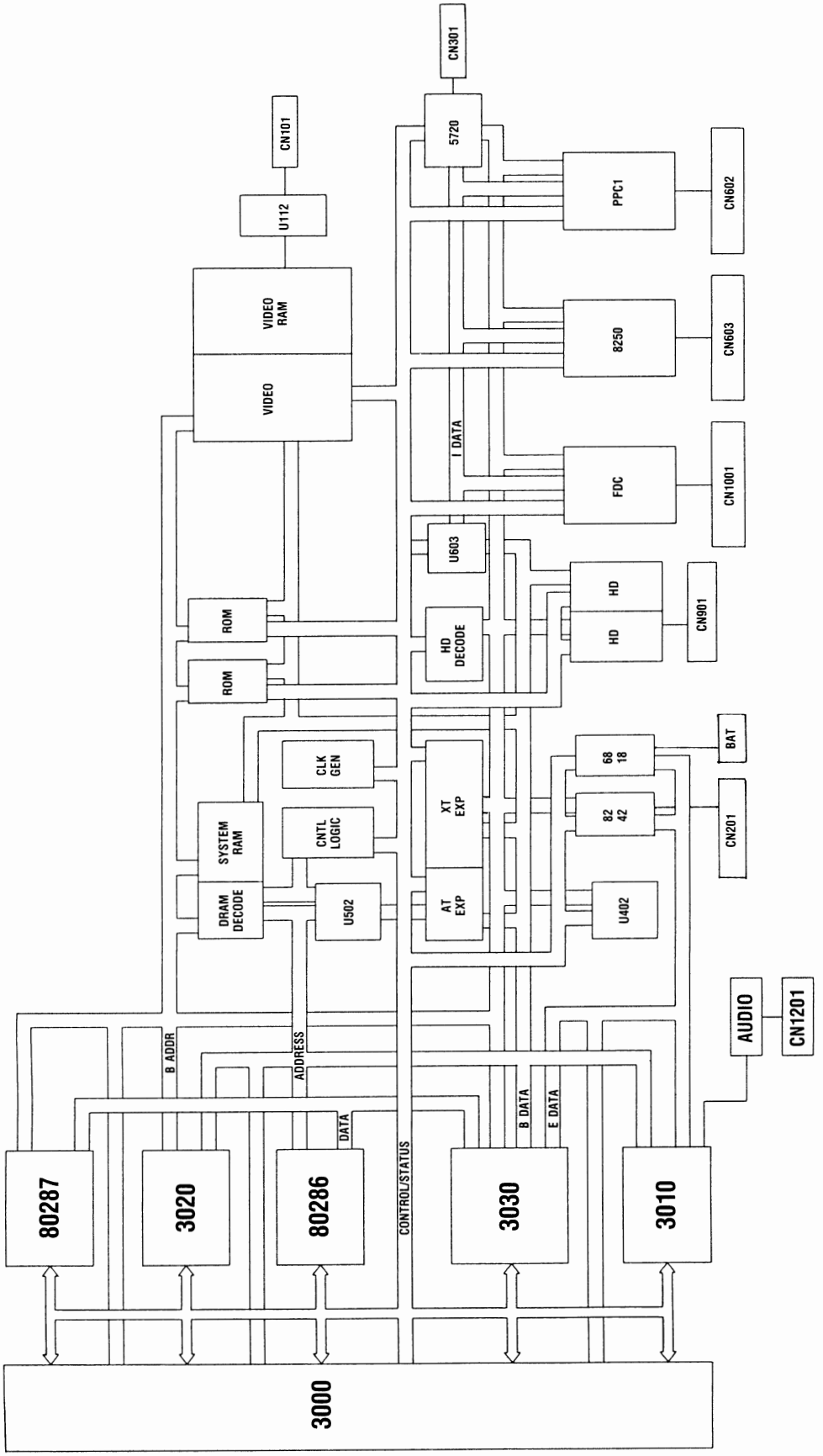
REGULATORY APPROVALS:

STANDARD	**DESCRIPTION**
USA/Canada:	Electronic Data Processing Units and Systems FCC Class B, Part 15 Subpart J Data Processing Equipment, Consumer and Commercial Products.
UL 478	
FCC	
CSA 22.2	
EUROPE	
VDE	
IEC 435	

SECTION 2

THEORY OF OPERATIONS

- **SYSTEM BLOCK DIAGRAM**
- **SYSTEM OVERVIEW**
- **NOTES — OPERATIONS GUIDE**



SYSTEM BLOCK DIAGRAM

SYSTEM OVERVIEW

(To be released)

NOTES FROM OPERATIONS GUIDE

AUTOCONFIG™

AUTOCONFIGuration is a unique feature of Commodore PC personal computers like the PC40-III, allowing the computer to automatically sense additional peripheral devices plugged into the expansion bus. Once these additional devices are detected, the resident peripherals on the PC40-III motherboard are adjusted so as not to conflict with expansion peripherals. The AUTOCONFIG™ feature can prevent hardware damage to peripherals and motherboard, as well as ease the installation of expansion cards.

The AUTOCONFIG™ process is described in this section.

Video

The PC40-III first examines the expansion bus for any expansion Advanced Video Adapter BIOS in the OC0000h — 0C7FFFh memory range. If an expansion video BIOS is found, then an external VGA or EGA controller is assumed to be on the bus and the onboard VGA controller is disabled to avoid conflict. If an expansion video BIOS is not found, the video output is configured in accordance with the default CONFIG Control video setting, as defined by the CONFIG dip switches 1, 2 and 3.

You can add an expansion MDA or CGA compatible controller in conjunction with the onboard VGA controller or provide two video screens. (This makes many CAD packages easier to use.)

NOTE: When using the PC40-III's onboard video controller, a VGA compatible monitor such as Commodore Models 1403 and 1450 (monochrome) or 1950 (color) must be connected to the 15 pin video output connector (no matter what video mode you have selected).

If you want to use two video screens, there are several things you should remember. First, you should use a CGA, MDA or compatible adapter — one that has no BIOS ROM of any kind.

Also, if you were to use an MDA/Herc adapter (monochrome) and you have the CONFIG switches set for VGA color, the PC40-III will boot using your VGA monitor and you will see a blinking cursor on your monochrome monitor, indicating that it has been initialized. If, while using the MDA/Herc adapter in the expansion port, you have the CONFIG switches on the back of the System Unit set to MDA/Herc, your PC40-III will use the monochrome monitor as the boot monitor and the VGA monitor will be initialized with the blinking cursor.

In either case, you can switch between the VGA and the monochrome monitors by using the MS-DOS **MODE** command. The syntax for the MODE command is as follows:

- **MODE MONO** — sets the MDA as the default monitor
- **MODE co80** — places the onboard VGA adapter into 80 column mode and sets it as the default monitor
- **MODE co40** — places the onboard VGA adapter into 40 column mode and sets it as the default monitor

Serial Port (COMn:)

Before the onboard serial port is enabled a scan of the two standard COMn: hardware locations is made. If serial hardware (serial card/modem) is found operational, possible bootup message(s) may be:

EXPANSION COM at 03F8h

and/or

EXPANSION COM at 02F8h

If both available COM: addresses are occupied by expansion boards, then the onboard serial port will not be enabled. The onboard serial port will be configured and tested at I/O address 03F8h if no expansion COM:'s are found and will be configured and tested to the unused COM: address if only one expansion COM: is found.

If the onboard serial port is configured and tested successfully a message will be output during bootup:

ONBOARD COM at 03F8h

or

ONBOARD COM at 02F8h

Parallel Port (LPTn: or PRN:)

Before the onboard parallel port is enabled a scan of the three standard LPTn: hardware locations is made. If parallel hardware (e.g., a printer card) is found operational, possible bootup message(s) may be:

EXPANSION LPT at 0378h

and/or

EXPANSION LPT at 0278h

and/or

EXPANSION LPT at 03BCh

If all available LPT: addresses are occupied by expansion boards, then the onboard parallel port will not be enabled. The onboard parallel port will be configured and tested at I/O address 03BCh if no expansion LPT:'s are found, and will be configured and tested to the unused LPT: address if two expansion LPT:'s are found. If only one expansion LPT: is found, the onboard parallel port will be enabled to the first available I/O address, when searching in the following sequence:

03BCh, 0378h, 0278h

If the onboard parallel port is configured and tested successfully, a message will be output during bootup:

ONBOARD LPT at 03BCh

or

ONBOARD LPT at 0378h

or

ONBOARD LPT at 0278h

Mouse Port

A check is made for a standard Microsoft Bus Mouse. If it is found in the I/O channel then the onboard Microsoft compatible mouse hardware is never enabled. The following message will appear during bootup:

EXPANSION MOUSE at 023Ch

If no expansion mouse is found the onboard mouse is enabled and tested. If mouse is operational then the following message will appear during bootup:

ONBOARD MOUSE at 023Ch

NOTE: The onboard mouse hardware is enabled/tested independent of the presence of the actual mouse. The bootup messages will appear even if the Commodore PC Mouse Kit is not attached.

80287 Numeric Coprocessor

A test is made for the presence of an 80287 Numeric Coprocessor during bootup. If an 80287 is detected the following message will be output:

80287 Numeric Coprocessor

NOTE: 80287 coprocessors are available in 5, 6, 8 and 12 MHz speeds. However, the units are downwardly compatible only — for example, an 8 MHz coprocessor will function if the PC40-III is running at 6 or 8 MHz, but a 6 MHz unit will not function properly if the PC40-III is running at 12 MHz. In order to use the 80287 at all three CPU speeds (6, 8, 12 MHz), an 80287-8 (an 8 MHz part) is necessary.

NOTES FOR THE PROGRAMMER

It is possible to override the configuration done at bootup. We STRONGLY recommend that only advanced programmers with experience with low-level hardware/software interaction attempt this.

NOTE: If software override of the default configuration is performed, the presence of any expansion hardware should be taken into account to prevent hardware conflict resulting in damage of the expansion hardware or the PC40-III motherboard.

Configuration is performed via the COMMODORE CONFIGURATION REGISTER at I/O address 0230h. This register is read/write with only bit7 changing its meaning from read to write. The register values are shown in the following table.

COMMODORE CONFIGuration REGISTER — I/O addr 230h

R/W	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
R	mono	rtc	X	mouse	com1	com0	lpt1	lpt0
W	venb'	rtc	X	mouse	com1	com0	lpt1	lpt0

mono — indicates that the onboard video adapter is setup as a monochrome adapter when high, color when low.

venb' — when set low the onboard video adapter will be enabled.

rtc — when set high the onboard real-time clock will be enabled.

X — this bit is reserved for future use.

mouse — when set high the onboard mouse will be enabled.

com1	com0	
low	low	— onboard serial port is disabled.
low	high	— serial port enabled at I/O addr 02F8h
high	low	— serial port enabled at I/O addr 03F8h
high	high	— this configuration is reserved.

lpt1	lpt0	
low	low	— onboard parallel port is disabled.
low	high	— parallel port enabled at I/O addr 03BCh
high	low	— parallel port enabled at I/O addr 0378h
high	high	— parallel port enabled at I/O addr 0278h

THE PC40-III HARDWARE CONFIGURATION

Using the PC40-III Setup Utility

Once MS-DOS has finished booting and the C> prompt has appeared, you can use the built-in Setup utility to give the system detailed information on your PC40-III configuration. To run the Setup utility, hold down the Control and Alt keys and simultaneously press the Esc key. The main menu of the Setup utility will appear and will look like this:

Commodore Setup Utility

Date	23.08.88
Time	14:23:08
Diskette 1	1.2M
Diskette 2	NONE
Hard Disk 1	28
Hard Disk 2	NONE
Video	SPECIAL
Coprocessor	NONE
Base Memory	640 KB
Extended Memory	384 KB
Base memory found:	640 KB
Extended memory found:	384 KB

Use ↑, ↓ to select items
Use →, ← to select predefined values
Use <PgDn> to view more hard disk types
Press <Esc> to abort SETUP
Press <End> to exit and update

Hard Disk Type Information

Type	Cyln	Head	Sect	W-pc	L-zone	Size
1	306	4	17	128	305	10 MB
2	615	4	17	300	615	20 MB
3	615	6	17	300	615	30 MB
4	940	8	17	512	940	62 MB
5	940	6	17	512	940	46 MB
6	615	4	17	NONE	615	20 MB
7	462	8	17	256	511	30 MB
8	733	5	17	NONE	733	30 MB
9	900	15	17	NONE	901	112 MB
10	820	3	17	NONE	820	20 MB
11	855	5	17	NONE	855	35 MB
12	855	7	17	NONE	855	49 MB
13	306	8	17	128	319	20 MB
14	733	7	17	NONE	733	42 MB
15	0	0	0	0	0	0 MB
16	612	4	17	0	633	20 MB

COMMODORE SETUP UTILITY MAIN MENU

As noted on the Setup screen, you can use the cursor keys and the keyboard to define or change the system configuration, as follows:

- ***Use the up and down cursor keys to move from option to option in the main menu.***
- ***Use the left and right cursor keys to select the predefined entries for each option.***
- ***Use the keyboard to type in any information that is not predefined.***
- ***Use PgDn to tell the pulldown menu (see Figure below) to display additional hard disk types.***

Following is specific information about the various Setup menu options.

Setting the Date and Time for the Real Time Clock/Calendar

The PC40-III has a Real Time Clock/Calendar with a battery backup. This means that once set, the clock/calendar will keep the correct date and time even when the computer is turned off. You use the first two lines of the Setup Utility to set the Real Time Clock/Calendar, as follows:

Date: Allows you to set the correct date into the Real Time Clock. This option does not have any predefined entries; simply **enter the date from the keyboard, in the format *dd/mm/yy*.**

Time: Allows you to set the correct time into the Real Time Clock, without invoking MS-DOS. This option also does not have any predefined entries; simply **enter the time from the keyboard, in the format *hh:mm:ss,*** where hh = 00-23, mm = 00-59, and ss = 00-59.

Setting the Floppy Disk Drive Options

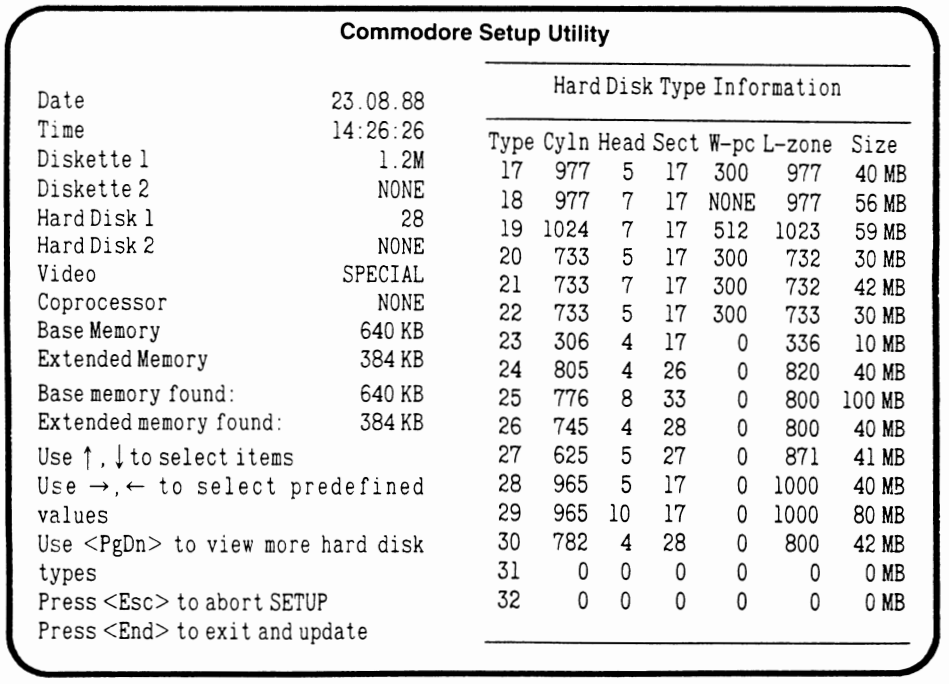
You can have a maximum of two floppy diskettes configured into your PC40-III. The next two Setup menu options, Diskette 1 and Diskette 2, allow you to tell the system how many floppy drives are available and what type they are. Here's how to set these options:

Diskette 1: Predefined entries: None, 360 Kb 5.25, 1.2 Mb 5.25, 720 Kb 3.5, 1.44 Mb 3.5. The floppy drive in your PC40-III is always considered Diskette 1. Since PC40-III is equipped with a high density (1.2 MB) drive, select **1.2 Mb 5.25** for Diskette 1.

Diskette 2: Predefined entries: None, 360 Kb 5.25, 1.2 Mb 5.25, 720 Kb 3.5, 1.44 Mb 3.5. If you **have not** installed a second floppy drive in your PC40-III, select ***None*** for Diskette 2. If you ***have*** installed a second floppy drive, select whichever drive type **(360 Kb 5.25, 1.2 Mb 5.25, 720 Kb 3.5, 1.44 Mb 3.5)** applies to the installed drive.

Setting the Hard Disk Drive Options

Hard Disk 1 and Hard Disk 2, the next two options in the Setup utility, define how many hard disk drives are available and what kind of hard disk drives they are. Hard disk drives are identified by a pre-assigned ***Drive Type*** (1, 2, etc.). This number tells the PC40-III the *drive manufacturer* and *capacity*.



SETUP UTILITY PULLDOWN MENU FOR HARD DISK DRIVE TYPE

Here's how to define your hard disk configuration:

Hard Disk 1: Your PC40-III comes equipped with a 40 MB hard disk drive. This drive is always considered *Hard Disk 1.* The ***Drive Type*** for this drive is shown on a sticker located on the back of your System Unit. **Find this number and type it in after *Hard Disk 1.***

The PC40-III Setup utility includes a menu of hard disk drive types with their individual ID numbers. You can page through the menu by pressing the PgDn key. For example, the opening Setup screen on Page 2-3 lists drive types 1 through 16. If you press PgDn, the Setup screen will be as shown on Page 2-4, with drive types 17 through 32 listed.

Hard Disk 2: This option is not supported by the onboard controller.

Other Setup Options

Video: Tells system what the default video is. Factory-set default is ***special***. To change this setting, see the permissible default modes listed in Appendix H.

Coprocessor: Tells system if an 80287 Numeric Coprocessor (NCP) is installed. Factory-set default is ***none.*** Select Yes if you have installed an 80287 Numeric Coprocessor (see Appendix N for information on using an 80287 Numeric Coprocessor).

Base memory: Lets you customize base memory for specific applications.

Extended Memory: Tells system how much extended memory is available. The default 384 Kbytes of extended memory can be enabled or disabled as required by setting the CONFIG Control dip switch 4.

SETTING THE MICROPROCESSOR CLOCK SPEED

The 80286 microprocessor in the PC40-III is capable of running at three different clock (i.e., processor or CPU) speeds:

- **Standard speed = 6 Mhz**
- **Turbo speed = 8 MHz**
- **Double speed = 12 MHz**

The PC40-III is preset to the standard 6 MHz speed. You can switch between the clock speeds by using special key combinations or by using the MS-DOS ATSPEED command.

To set the clock speed from the keyboard, use these key sequences:

- **CTRL-ALT-S for standard speed (6 MHz)**
- **CTRL-ALT-T for turbo speed (8MHz)**
- **CTRL-ALT-D for double speed (12 MHz)**

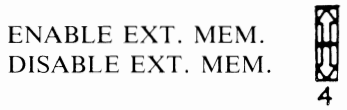
NOTE: Some software may require that you select standard or turbo speeds for normal operation.

To set the clock speed using the ATSPEED command, first make sure the MS-DOS prompt is showing on the screen. Then type the word ATSPEED, followed by a space, a dash (—), and then a letter (S, T, or D) denoting the desired speed. For instance, if you are in standard speed and you want to change to turbo speed (8 MHz), type the following and press Enter:

ATSPEED —T

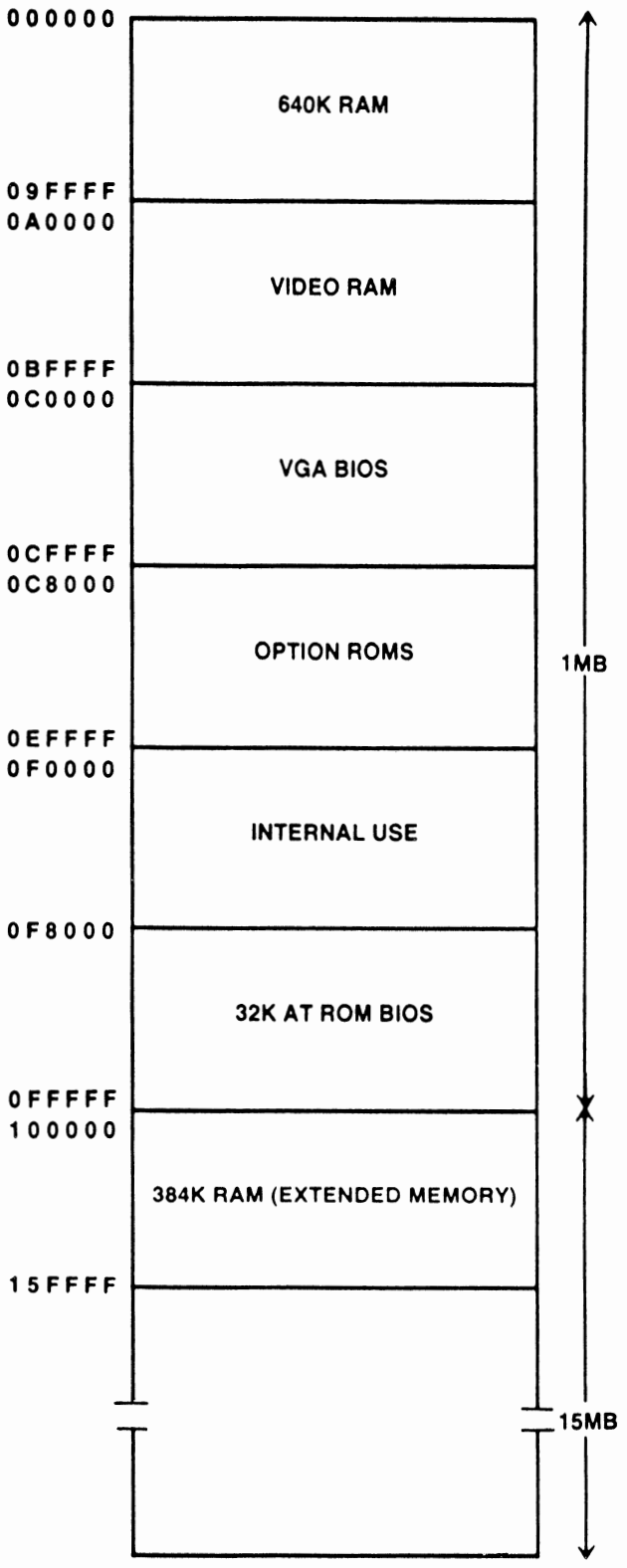
Extended Memory Dip Switch

Dip switch 4 enables or disables the 384K of extended memory in the PC40-III.



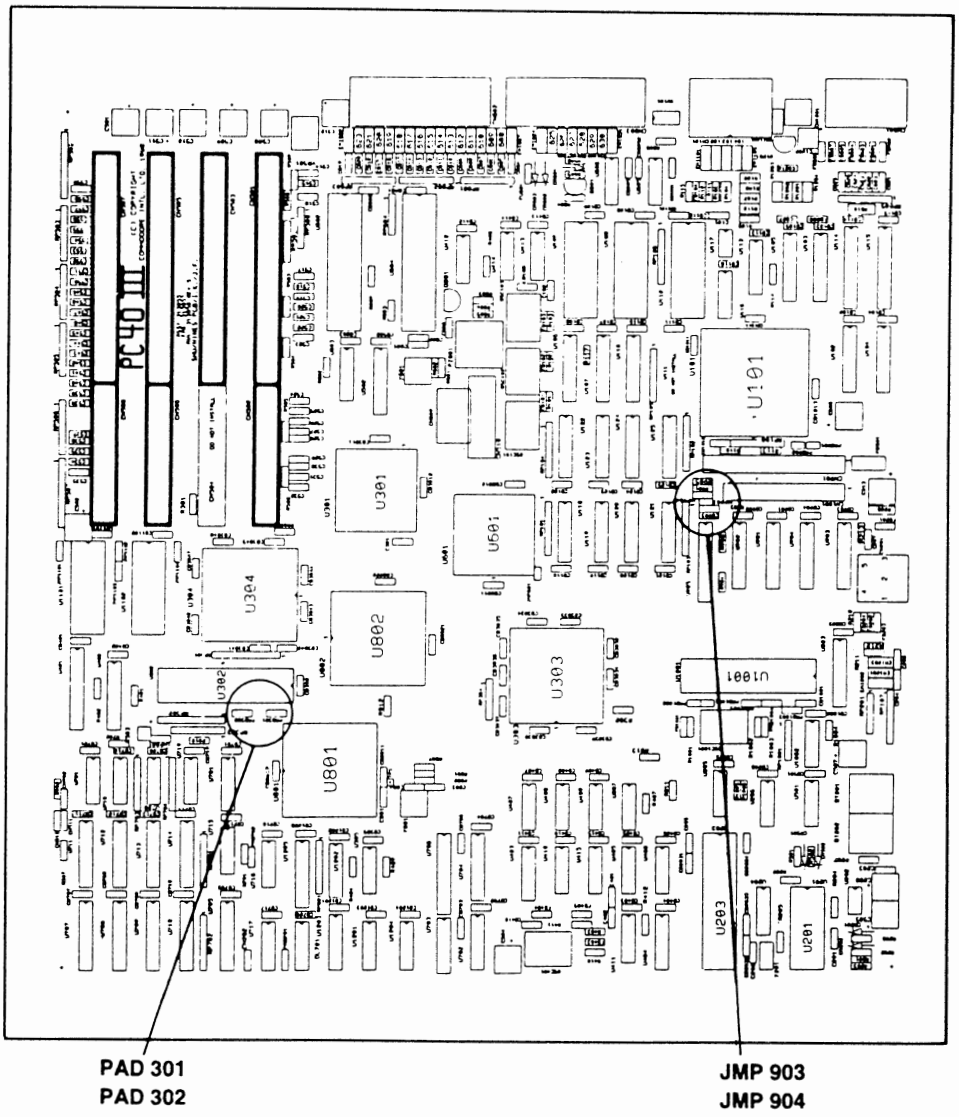
THE RESET SWITCH

The Reset switch protrudes slightly on the right side of the machine, just behind the keyboard connector. The switch provides an alternative to cycling power when an application program may have "crashed" the computer. Pressing this switch will effectively reboot the computer as if the power had been cycled OFF and then ON. All information in the computer's RAM memory will be lost. Be careful not to press this button during disk access, or you may lose information that was being written to mass storage devices (e.g., hard disks or floppy disks) while the switch was depressed.



PC40-III MEMORY MAP

JUMPER SETTINGS ON MOTHERBOARD



Jumper Locations on Motherboard

JUMPER	FUNCTION	DEFAULT	RESULT
JMP 903	Disable HD	Not Installed	HD Installed
JMP 904	HD Type	Location A Location B	Conner HD Quantum HD
PAD 301	80287 Clock Mode	÷3 Mode	8 MHz Part runs up to 12 MHz
PAD 302	80287 Clock Speed	CPU Clock (÷3)	8 MHz Part runs up to 12 MHz

PAD 301 & PAD 302 may be changed to take full advantage of using a 12 MHz 80287. This is a dealer installation only.

IRQ Vectors Used in the PC40-III

There are two interrupt controllers on the PC40-III:

#1

CPU Interrupt	
	IRQ 0 — System Timer (built-in)
	1 — Keyboard (built-in)
	2 — Cascade #2
	3 — COM2 (built-in or expansion)
	4 — COM1 (built-in or expansion)
	5 — XT Compact HD (unused)
	6 — Floppy (built-in)
	7 — LPT1,2,3 (All ports: built-in plus expansion)

#2

Cascade 2	
	IRQ 8 — Real Time Clock
	9 — Onboard Mouse
	10 — Unused
	11 — Unused
	12 — Unused
	13 — Unused
	14 — AT Hard Disk (built-in or expansion)
	15 — Unused

SECTION 3

TROUBLESHOOTING GUIDE

TECHNICAL SERVICE NOTES

WARNING: **PC40-III PRINTED CIRCUIT BOARD CONTAINS CMOS CIRCUITRY, USE STATIC PRECAUTIONS WHEN HANDLING OR SERVICING THIS PRODUCT.**

IMPORTANT:

- **PC40-III PCB'S RETURNED FOR CREDIT MUST BE SHIPPED IN AN ANTI-STATIC BAG, AVAILABLE THROUGH THE COMMODORE PARTS DEPT. ANY PCBS RETURNED FOR CREDIT BY SERVICE CENTERS WHICH ARE NOT PACKAGED CORRECTLY WILL BE SENT BACK TO THE SERVICE CENTER AND NO CREDIT WILL BE ISSUED.**
- **PC40-III HARD DRIVES RETURNED FOR CREDIT MUST BE INSERTED IN AN ANTI-STATIC BAG AND PACKED IN A COMMODORE SPECIFIED HIGH DENSITY FOAM SHIPPING BOX, BOTH AVAILABLE THROUGH THE PARTS DEPT. FAILURE TO DO SO WILL VOID WARRANTY.**

COMPONENT REPAIR:

PC40-III MAIN BOARD IS A MULTI-LAYERED PCB ASSEMBLY. COMPONENT REPAIR BEYOND THE SOCKETTED CHIP LEVEL RESULTING IN NON-REPAIRABLE DAMAGE WILL VOID WARRANTY. USE STATIC PRECAUTIONS WHEN SERVICING THIS PCB ASSEMBLY.

TROUBLESHOOTING ERROR MESSAGES

Troubleshooting Guide

Error Messages	Customer Response	Service POD Test (H)
1. DMA 1 error	See your dealer	Test 0B
2. DMA 2 error	See your dealer	Test 0C
3. Interrupt controller 1 error	See your dealer	Test 0D
4. Interrupt controller 2 error	See your dealer	Test 0E
5. PIO error	See your dealer	Test 0F
6. Parity error	See your dealer	Test 10
7. Real time clock is not working	See your dealer	Test 1E
8. Illegal shutdown code in CMOS	See your dealer	Test 02
9. Virtual Mode CPU error	See your dealer	Test 26
10. Parity error on main circuit board	See your dealer	Misc
11. Parity error on expansion bus	See your dealer	Misc
12. Non-recoverable error-Processor halted	See your dealer	Misc
13. Press F1 key to continue	Press F1 key	Misc
14. Battery Failure	Run Setup Utility/See your dealer	Test 11
15. Base memory configuration error	Run Setup Utility	Test 17
16. Extended memory configuration error	Run Setup Utility	Test 18
17. Floppy 0 configuration error	Run Setup Utility	Test 1A
18. Floppy 1 configuration error	Run Setup Utility	Test 1A
19. Coprocessor (80287) configuration error	Run Setup Utility	Test 1D
20. The realtime clock has not been initialized	Run Setup Utility	Test 1E
21. Keyboard	Check keyboard	Test 14
22. Key switch is off. Turn it on to continue	Turn keylock on	
23. Boot failure, check disk and hit any key to try again	Check for non-MS-DOS disk in Drive A:; run Setup Utility	Misc

POWER ON DIAGNOSTICS

PC40-III Trouble Shooting — Section 3

The Commodore 80286 ROM bios contains a "Power on Diagnostic" program which tests the functions of hardware and checks the configuration prior to passing control to the operating system.

The number of the test routine being run is passed to addr 03 78 (H) prior to the start of each test section.

The 80286 processor is initialized by the "RESET" signal. Refer to RESET description in IC pinout section, note that "VCC" and "CLK" to CPU must be correct and "HOLD" must not be active for 34 ticks from leading edge to trailing edge of initial reset.

RESET will terminate all instruction execution and local bus activity until it is negated. Prior to fetching, decoding and executing, the first instruction, located at physical address FF FF F0 (H), the 80286, in real address mode, processes some micro code located in its internal ROM, this takes about 38 ticks.

Test 01 (H) 0000 0001 (B)

The first test performed by the power on diagnostic checks the 8088 flags, the arithmetic logical unit, and the CPU registers.

If a failure is detected in Test 01, a "HALT" instruction is executed. This will stop program execution and prevent the CPU from using the local bus. The 80286 can be forced out of the halted state by "RESET", "NMI" or "INTR" (when "INTR" is used for RESTART, the interrupt enable bit of flag register must be on (set to 1), and the effective address computed from CS:IP will point to the next instruction after the halt instruction).

***Failure in test 01 indicates defective 80286.

Test 02 (H) 0000 0010 (B)

This routine checks to see if a "SHUTDOWN" has occurred. A shutdown can indicate a severe error which would prevent the CPU from further processing.

NOTE: A halt or shutdown condition is signaled externally, by the 80286 as a bus operation. Low states on S0′, S1′, COD/INTA′, and a high state on M/IO′ indicate a halt or shutdown. The state of address line 1 will indicate which condition, A1 high is halt, A1 low is shutdown.

After the test number is moved to the parallel port a check for keyboard reset is conducted and the program branches to test 04 (H) if it has.

The check for shutdown begins by examining the 8242 keyboard controller status port. In all ten shutdown conditions are tested, of these, three unexpected shutdown conditions, numbers 6, 7 or 8, any one of which if true, will generate the console message:

"Illegal Shutdown Code in CMOS"

NOTE: Branch information for shutdown routines are stored in CMOS memory. The shutdown command is sent to the 8242, the UPI status port, which will halt the CPU. Return depends on the shutdown code in CMOS memory.

An error code, F6, F7 or F8, (HEX) is sent to the parallel port before calling the display routine which generates the above message.

In real address mode a shutdown could occur under the following conditions:

Interrupt number 8, interrupt number 13, or a "CALL INT" or "PUSH" instruction which wraps stack segment when SP is ODD.

Routines also perform valid shutdowns to exit protected mode. During these the DMA page register will be initialized and interrupt control words (ICW) 1, 2, 3 and 4 will be reinitialized. Other routines within the test enable "NMI", parity and set the I/O check bit.

***Failures in test 02 could indicate problems on the local bus, or expansion bus. This would include: 80286, FE3000, FE3010, or any third party cards.

Test 03 (H) 0000 0011 (B)

Eprom checksum test verifies contents of eprom by adding bytes and checking for result of zero. A compensation byte is factored into the addition to make the sum zero.

Detection of an error results in a halt condition and would invalidate tests 01 and 02.

***Failure in test 03 indicates defective ROM.

Test 04 (H) 0000 0100 (B)

Test 04 checks the DMA page registers by writing and reading bits starting at address 80 (H).

***Failure in test 04 indicates possible defective FE3010, or local bus.

Test 05 (H) 0000 0101 (B)

Timer 1 and timer 2 are checked for correct operation. Interrupts are masked off during the test.

***Failure in test 5 indicates possible defective FE3010.

Test 06 (H) 0000 0110 (B)

Memory refresh test. Timer and DMA are setup to initiate refresh cycles every 15.1 microseconds. Size of virual memory is calculated.

***Failure in test 06 indicates possible FE3010, Refresh logic or memory problem.

Test 07 (H) 0000 0111 (B)

Test 07 checks the 8242 keyboard controller by writing and reading the keyboard buffers.

***Failure in test 07 indicates possible defective 8242 or associated circuitry.

Test 08 (H) 0000 1000 (B)

Test 08 writes and reads the first 128K of RAM and verifies block size is 128K. First pass writes addresses into data, the second pass writes the complement of the address into data. Memory is cleared after test. The battery status is also confirmed in test 08.

***Failure in test 08 indicates possible defective RAM or RAM logic.

Test 09 (H) 0000 1001 (B)

Test and configure video. A search is made to determine if MDA, CGA or a special video adapter is configured, if not the onboard VGA is enabled and a call to VGA bios is executed. The dip switches are read to determine the default video mode.

NOTE: The mode register setting in the 5720 controls the reset signal to the onboard VGA controller chip. If no special video adapters are found on the expansion bus then "NOVID" from the 5720 to the PVGA is negated.

On completion of this test the title and copyright message are displayed.

Test 0A (H) 0000 1010 (B)

Test RAM from 128K to 640K. A display message is generated indicating that the base RAM of 128K, Test 08, is OK.

Blocks of 128K, starting at 128K are then tested by writing, reading and verifying RAM. The first pass writes addresses to data, that is, the address which defines the physical location is also used as the bit pattern that is being written. The second pass writes complement of address into data.

The test displays results in blocks of 128K to the console each time a 128K boundary is reached.

At completion of the onboard memory test the CPU is placed in virual mode and a test for virtual memory (over 1 MEG) is started.

NOTE: See test 26 (H).

***Failure in test 0A indicates a defective RAM.

Test 0B (H) 0000 1011 (B)

DMA controller #1 register check.

NOTE: Appendix L of the PC40-III operator guide lists error messages starting with this test, see page 85 of operations guide part number 319983-01.

Four current address registers (16 bits wide, each) and four current word count registers (16 bits wide, each) for each of the four DMA channels are written to and read from to verify operation.

A failure in test 0B will generate the following display on the console:

"DMA 1 error"

The beeper will sound, and a halt instruction will be executed.

***Failure in test 0B indicates A defective FE3010.

Test 0C (H) 0000 1100 (B)

DMA controller #2 register check. The second functional 8237 containing four current address registers (16 bits wide, each) and four current word count registers (16 bits wide, each) within the FE3010 are written to and read from to verify operation.

Successful completion of the test 0C will set the modes for DMA channels 0 through 3 and enable cascading by channels 4, 5 and 6 (DMA 1).

A failure in test 0C will generate the following display on the console:

"DMA 2 error"

The beeper will sound, and a halt instruction will be executed.

***Failure in test 0C indicates a defective FE3010.

Test 0D (H) 0000 1101 (B)

Interrupt controller #1 test. Patterns are written to, and read from the interrupt mask register (IMR) which controls the interrupt request register (IRR).

A verification is made that no interrupts can occur if "IMR" is set to FF (H). A vector is initialized to a temporary interrupt service routine in the event of a failure.

A test for correct timer 0 interrupt is also made.

A failure in test 0D will generate the following display on the console:

"Interrupt controller 1 error"

The beeper will sound, and a halt instruction will be executed.

***A failure in test 0D indicates a defective FE3010.

Test 0E (H) 0000 1110 (B)

Interrupt controller #2 test. The second functional 8259 contained in the FE3010 is tested as in test 0D, without timer test.

A failure in test 0E will generate the following display on the console:

"Interrupt controller 2 error"

The beeper will sound, and a halt instruction will be executed.

***A failure in test 0E indicates a defective FE3010.

Test 0F (H) 0000 1111 (B)

Check peripheral in/out register. Write and read from PIO register.

A failure in test 0F will generate the following display on the console:

"PIO error"

The beeper will sound, and a halt instruction will be executed.

***A failure in test 0F indicates a defective FE3010.

Test 10 (H) 0001 0000 (B)

RAM parity test. Blocks of RAM are written to and read from, parity check for odd parity is made. Parity disabled after successful test.

NOTE: PC40-III does not use parity, third parity boards that use parity will enable parity.

"NMI" is enabled and a service routine for a parity error generates the following console message.

"Parity error"

The beeper will sound, and a halt instruction will be executed.

***Failure in test 10 indicates a defective RAM, third party card, NMI, or local bus.

Test 11 (H) 0001 0001 (B)

Test CMOS clock for battery failure and checksum failure.

Beeper will sound if failure is detected. Console will display:

"Battery failure" or "CMOS checksum failure" or both.

***Failure of test 11 indicates a defective battery, defective oscillator, or M146818A.

Test 12 (H) 0001 0010 (B)

This test is disabled. It is used only in manufacturing tests.

The beeper will sound for a set length prior to the start of test 13 (H). In a system which has passed all tests to this point the beeper sound heard now would be the one heard in the power up routine.

Test 13 (H) 0001 0011 (B)

Setup interrupt controller and move vector tables to RAM. Vector addresses are fetched from top 8K module.

NOTE: Vectors for video were setup in test 09.

Master and slave interrupts are enabled at this point.

Test 13 does not create any error messages.

Test 14 (H) 0001 0100 (B)

Keyboard test. Functional test of the 8242 keyboard controller at U203. A test for a stuck key on keyboard is performed. Check is made to see if key lock is locked.

A failure in test 14 will display the following error message on console:

"Keyboard error"

***Error indicates a defective 8242 controller or a defective keyboard.

Test 15 (H) 0001 0101 (B)

Test and configure the parallel port. Parallel port addresses are setup, reads and writes to ports are done. Set time out.

No error messages are generated by this test.

NOTE: PPC1 at U602 controls parallel output.

Test 16 (H) 0001 0110 (B)

Configure serial COM1 and COM2 for 8250 at U604. Read serial interrupt ID, set number of serial channels.

No error messages are generated by this test.

Test 17 (H) 0001 0111 (B)

Configure memory less than 640K. Parity (for EXPANSION RAM) is enabled.

Memory was tested in test 0A, and "CMOS STATUS" set. A check for a warm boot (ALT/CNTRL/DEL) is made and a comparison of the old and new memory configuration is performed. If a memory size mismatch is detected, the beeper will sound and the following non-fatal error message will be displayed on the console:

"Base memory configuration error"

The new configuration is stored.

***Check the settings for RAM size in the setup utility if you encounter this message.

Test 18 (H) 0001 1000 (B)

Configure memory over 1 megabyte (virtual memory). Check is made on address line 20, a low indicates virtual address mode.

CMOS status is checked as in test 17, a memory size mismatch will sound the beeper and generate the following non-fatal error message on the console:

"Extended memory configuration error"

The new configuration is stored.

***Check the settings for RAM size in the setup utility if you encounter this message.

Test 19 (H) 0001 1001 (B)

Configure keyboard test. Setup keyboard buffers, enable keyboard interrupt and test if key switch is turned to the on position.

If the key switch is off the following message will be displayed on the console:

"Key switch is off. Turn it on to continue."

NOTE: You are in a loop until you turn on the key switch.

Test 1A (H) 0001 1010 (B)

Configure the floppy disk drive. Calculate number of floppy drives present. Check drive type, compare settings stored in CMOS, if a mismatch the following message will be displayed on console:

"Floppy 0 configuration error"

***Check settings in setup utility if above message is displayed.

Test checks second floppy configuration, if a mismatch the following message will be displayed on the console:

"Floppy 1 configuration error"

***Check settings in setup utility if above message is displayed.

New configuration is stored in CMOS. Floppy interrupt is enabled.

NOTE: Refer to installation instructions when adding a second floppy to the system. It may be necessary to change jumpers on drive for proper operation.

Test 1B (H) 0001 1011 (B)

Configure the hard drive. Check configuration if a mismatch hard drive will not be setup.

No error message is generated.

Test 1C (H) 0001 1100 (B)

Test number is not moved to parallel port for this configuration. This routine only turns on the game card bit in the "EQUIP FLAG".

No error message is generated.

Test 1D (H) 0001 1101 (B)

Configure 80287 coprocessor. Check if 80287 is present. Enable 80287 interrupt and set "EQUIP FLAG" if it is.

Compare configuration with CMOS, store new configuration, beep the speaker, and display the following message is setup changed.

"-- Coprocessor (80287) configuration error"

***Check setup utility for correct settings if this message is displayed.

Test 1E (H) 0001 1110 (B)

Check CMOS clock to see if it was initialized and is working. Enable timer interrupt. Sound beeper, and initialize if failure detected, then display one of the following messages on the console:

"-- The Real Time Clock has not been initialized"

OR: "-- Real Time Clock error"

***Check the RTC chip, M146818A at U201 if second message above is displayed.

Test 1F (H) 0001 1111 (B)

Generate a new CMS checksum and save it in CMOS RAM. Call made to auto configuration program at this point.

No error message generated.

Test 20 (H) Not Implemented

Test 21 (H) 0010 0001 (B)

Initialize ROM drivers, including hard drive. Checksum generated, and all ROMS tested.

System will now begin boot up.

System speed is determined, 6 MHz, 8MHz or 12MHz.

***Refer to operations manual for opening screen display.

Tests 22, 23 Not Implemented

Test 24 (H) 0010 0100 (B)

Test operation of the RTC chip. Recheck battery, make sure clock is counting, test memory.

System will execute a halt instruction on memory failure. No error message is generated.

Test 25 (H) 0010 0101 (B)

Used in manufacturing to loop through diagnostics.

Test 26 (H) 0010 0110 (B)

Virutal memory test (over 1 megabyte). Call made to this routine from test 09.

Display Message: "Testing Extended RAM"
Display Message: "Total System RAM = XXXX" at finish.

During this test the exception interrupt vector tables and descriptor tables are built, and moved from ROM to RAM.

A test of address line 20 is made (controls real or virtual CPU mode). If not in virtual mode display following message:

"Test __ 26: Virtual Mode CPU error"

And send F3 (H) (1111 0011 to parallel port. Then execute a halt instruction.

Test address lines 19 through 23 are tested. Shutdown if error. Exception interrupt codes are moved to the parallel port prior to shutdown. The following list defines the code sent to the port and the type of exception interupt (EXECP INT).

81	(H)	EXECP INT 01	Single Step
82	(H)	EXECP INT 02	NMI
83	(H)	EXECP INT 03	Breakpoint
84	(H)	EXECP INT 04	Into Detect
85	(H)	EXECP INT 05	Boundary
86	(H)	EXECP INT 06	Invalid OP Code
87	(H)	EXECP INT 07	—
88	(H)	EXECP INT 08	Double Exception
89	(H)	EXECP INT 09	Processor Segment Error
8A	(H)	EXECP INT 10	—
8B	(H)	EXECP INT 11	Segment Not Present
8C	(H)	EXECP INT 12	Stack Segment Not Present
8D	(H)	EXECP INT 13	General Protection Error
8E	(H)	EXECP INT 14	—
8F	(H)	EXECP INT 15	—
90	(H)	EXECP INT 16	Processor Extension Error

Power on diagnostic program is finished at the time of boot up (end of test 21).

Note that during execution of "POD" calls are made to auto configure and to miscellaneous interrupt routines.

All error messages listed in appendix L of operations guide are listed in the overview above with the exception of the following which are generated from the miscellaneous interrupt routines.

10 "Parity error on main circuit board"

11 "Parity error on expansion bus"

12 "Non-recoverable error - Processor halted"

13 "Press F1 key to continue"

Messages 10, 11 are generated after a parity error has been detected and a memory check has determined that it was on the main board, or the expansion bus. If the check finds the error the CPU is halted and message 12 is displayed. If no error is found after the check, message 13 is displayed and processing will continue.

SECTION 4

PARTS SECTION

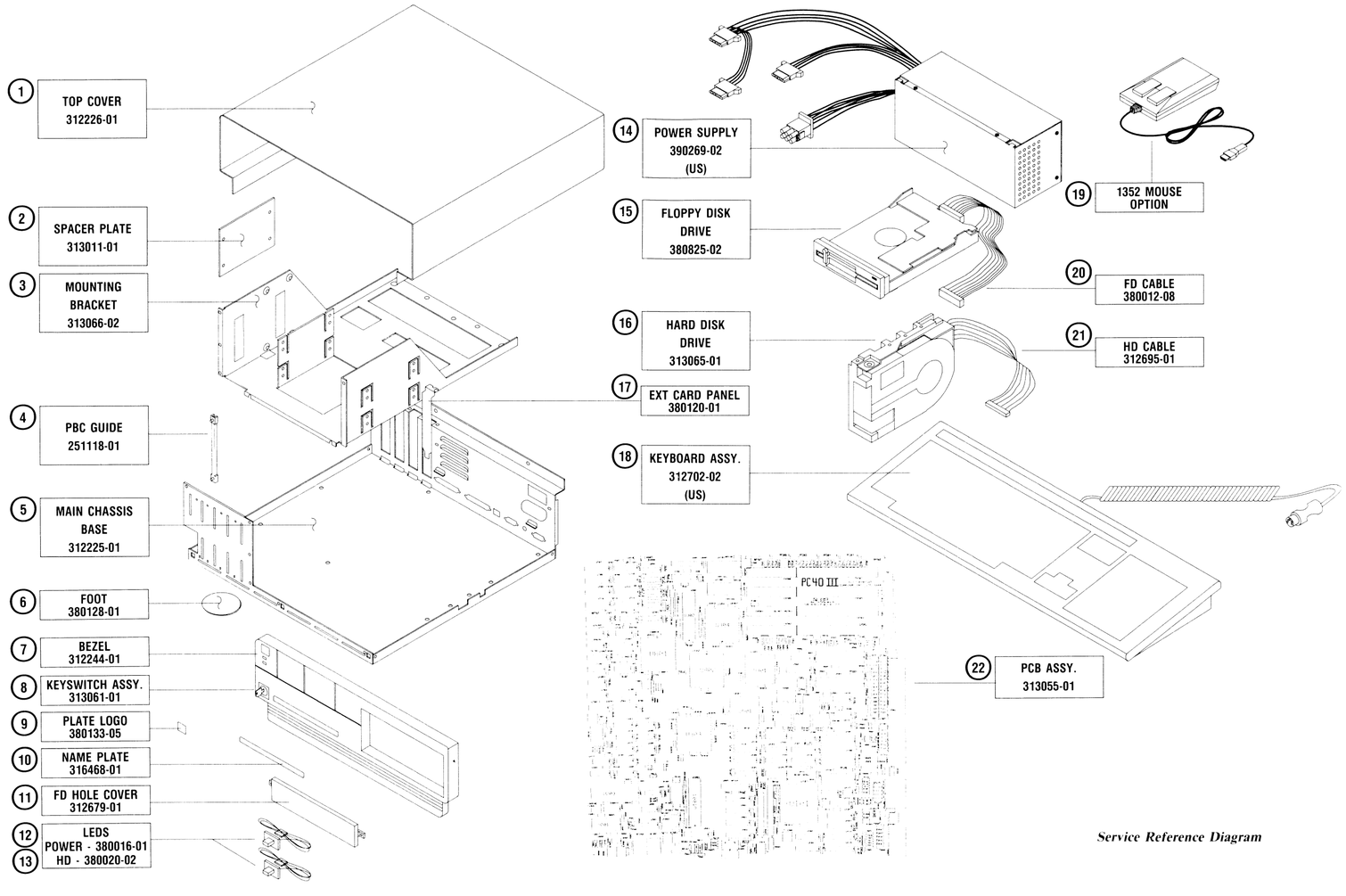
PC40-III MAJOR PARTS LIST

Refer to Service Reference Diagram

1.	Top Cover	312226-01
2.	Spacer Plate	313011-01 Sub:-02
3.	Mounting Bracket	313066-02 Sub:-01
4.	PBC Guide	251118-01
5.	Main Chassis Base	312225-01
6.	Foot	380128-01
7.	Bezel	312244-01
8.	Keyswitch Assy.	313061-01
9.	Plate Logo	380133-05
10.	Name Plate	316468-01
11.	FD Hole Cover	312679-01
12.	LED Power On	380016-01
13.	LED Hard Drive	380020-02
14.	Power Supply Assy	390269-02 (US)
15.	Floppy Disk Drive	380825-02
16.	Hard Disk Drive	313065-01
17.	Extension Card Panel	380120-01
18.	Keyboard Assy.	312709-01 (US/Canada)
19.	1352 Mouse Option	-1352
20.	Floppy Drive Cable	380012-08
21.	Hard Drive Cable	312695-01
22.	PCB Assy.	313055-01
	Ground Cable (HD)	380811-01 (Not shown)
	Power Cord	903508-15 (US) (Not shown)
	PC40-III Service Manual	314134-01
	1403 Monitor Service Manual	314882-01

PC40-III MAJOR PARTS LIST

Software Sub. Assy. (US) 315835-01	
Includes	
DOS 3.30A Manual	319293-01
Basis 3.22 Manual	319292-01
Operations Guide	319983-01
Disk Assembly	317768-01



Service Reference Diagram

COMPONENT PARTS LIST
PCB ASSEMBLY #313055-01

Commodore part numbers are provided for reference only and do not indicate the availability of parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Approved cross-references for TTL chips, Transistors, etc. are available in manual form through the Service Department, order #314000-01.

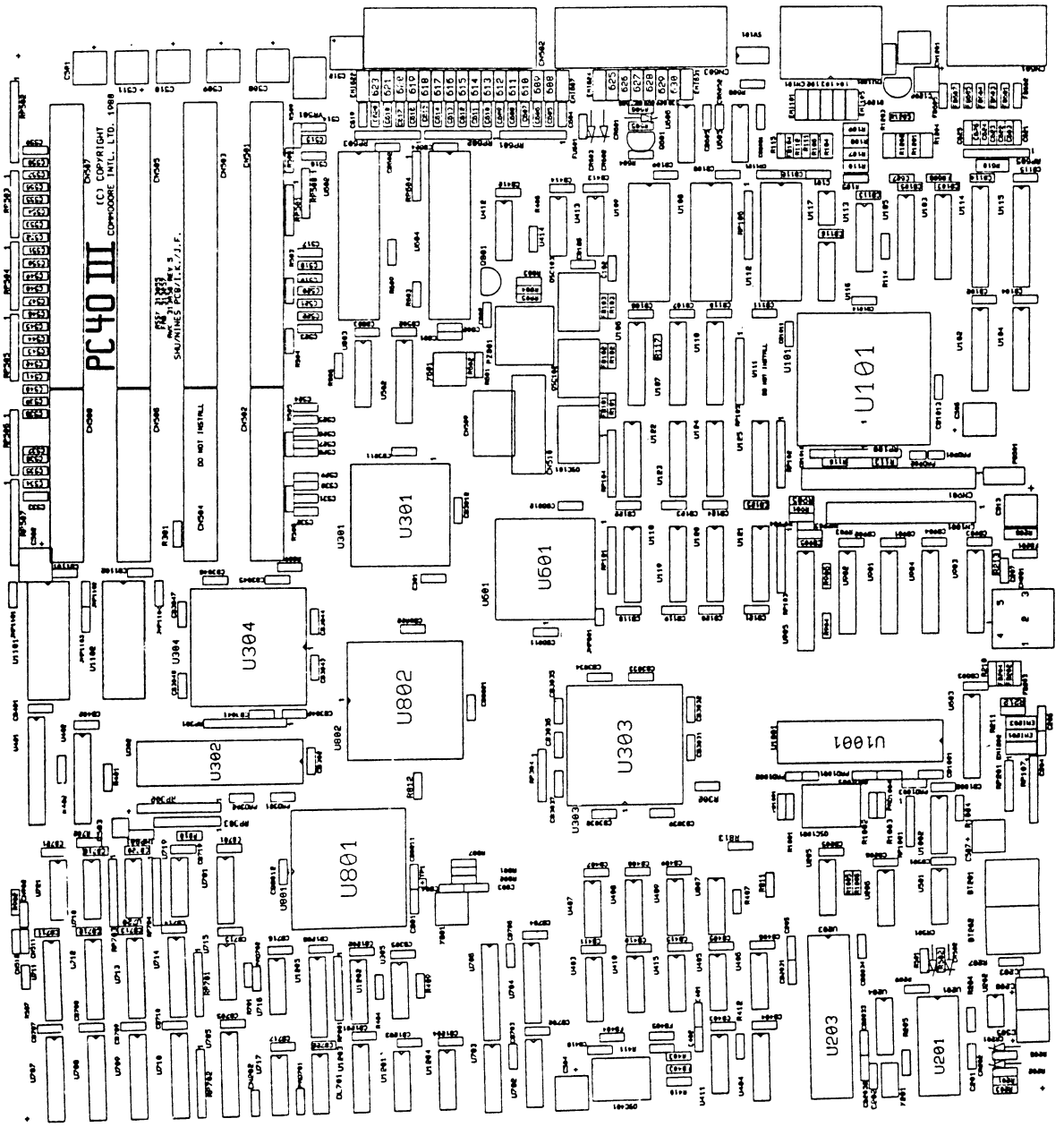
IC COMPONENTS		
390300-04	80286 12 MHZ PROCESSOR	U301
309316-01	FE3000A	U801
390317-02	FE3010B	U802
390319-01	FE3020	U303
390318-01	FE3030	U304
390302-01	PVGA-1A PARADISE VIDEO	U101
318091-01	PPC1, PRINTER INTERFACE	U602
390304-03	WD37C65, FLOPPY CONTROLLER	U1001
390303-01	IMS171, INMOS COLOR LOOKUP TABLE	U112
380205-01	8250, SERIAL INTERFACE	U604
380259-01	M14818A RTC/CMOS RAM	U201
390341-01	8242 KEYBRD CONTROL	U203
318087-01	MOS 5720, MOUSE-I/O CONTROL	U601
390307-02	PAL20L8 VGA DECODER #0	U114
390335-02	PAL20L8 VGA DECODER #1	U115
390308-01	PAL20L10 I/O DECODER	U401
390336-02	PAL20L10 HDC DECODER	U905
390309-02	PAL16L8 DRAM DECODER	U706
390083-04	DRAM, 64 X 4 (256K BIT) @100NS	U118-U125
318099-02	DRAM, 256 X 4 (1 MEG BIT DRAM) @ 100NS	U707-U714
390337-02	EPROM1, VGA BIOS - LOW (27128-15)	U108
390338-02	EPROM2, VGA BIOS - HIGH (27128-15)	U109
390339-01	EPROM3, PC40 III BIOS - LOW (21728-12)	U1101
390340-01	EPROM4, PC40-III BIOS - HIGH (27128-12)	U1102
901521-02	74LS04	U206
901521-30	74LS14	U501
901521-20	74LS125A	U205,U414
901521-63	74LS174	U113
901521-13	74LS244	U102,U103,U107,U110, U901,U902,U106
901521-46	74LS245	U104,U105,U502,U603
318066-01	74F00	U721,U807
390110-01	74F04	U413,U715,
390203-01	74F08	U718,U719,U1201
390313-01	74F10	U717
390279-01	74F20	U1204
390077-01	74F32	U305
390080-01	74F138	U803,U1202
390611-01	74F153	U403
390312-01	74F175	U404
390109-01	74F240	U704
390314-01	74F253	U701
390315-01	74F258	U702,U703
390578-01	74F573	U705,U1205
390089-01	74F245	U903,U904
390310-01	74HCT74	U412,U411,U716
390579-01	74ALS244A	U402
901522-06	7406	U1002
390359-01	74ACT00	U720
390081-01	74F74	U405-U409,U410
390323-01	4069	U204
318827-01	LM339	U116
390322-01	LM10CN	U202
390324-01	TL431	U117
901527-03	7905	VR501
390364-01	74LS175	U1203
901882-01	1488	U605
901883-01	1489	U606
CRYSTAL, OSCILLATORS		
390273-01	OSCILLATOR, 48.00 MHZ	OSC401
325566-20	OSCILLATOR, 36.00 MHZ	OSC103
325566-18	OSCILLATOR, 25.175 MHZ	OSC102
315566-19	OSCILLATOR, 28.322 MHZ	OSC101
325566-17	OSCILLATOR, 9.6 MHZ	OSC1001

CRYSTAL, OSCILLATORS *(Continued)*		
900560-01	CRYSTAL, 32.768 KHZ	Y201
900556-13	CRYSTAL, 1.8 MHZ	Y601
900558-01	CRYSTAL, 14.318 MHZ	Y801
RESISTOR NETWORKS		
902441-11	150 OHM 6P, 5EL SIP	RP1001
902442-06	68 OHM, 8PIN, 4 ELEMENT	RP701,702
902422-03	33 OHM, 8 PIN, 4 ELEMENT, SIL	RP101-106,601,602, RP703,RP704
902422-02	1K OHM, 8 PIN, 4 ELEMENT, SIL	RP801
902441-31	4.7K 6 PIN, 5 ELEMENT, SIP	RP107,201,304,604, RN401
902442-55	4.7K, 8 PIN, 7 ELEMENT, SIP	RP303,603,605
902442-35	10K, 8 PIN, 7 ELEMENT, SIP	RP108
902410-08	4.7K, 10 PIN, 9 ELEMENT, SIP	RP301,302
902410-07	10K, 10 PIN, 9 ELEMENT, SIP	RP502,507
902441-15	330 OHM, 6 PIN, 5 ELEMENT, SIP	RP508
RESISTORS 5% @ 1/4 WATT		
901550-39	CARBON FILM, 3.9K OHM	R1203
901550-64	CARBON FILM, 10 OHM	R503-R506,R210-R212
901550-63	CARBON FILM, 22 OHM	R102,812
901550-105	CARBON FILM, 33 OHM	R402,603,R1206,609, 701,813,410
901550-94	CARBON FILM, 68 OHM	R114,1001,101,409,401, R209
901550-45	CARBON FILM, 75 OHM	R801,R411
901550-124	CARBON FILM, 160 OHM	R1201
901550-52	CARBON FILM, 220 OHM	R804,R902,R507,R207
901751-70	CARBON FILM, 210K OHM, 1%	R210
901550-12	CARBON FILM, 22K OHM	R1202
901550-58	CARBON FILM, 470 OHM	R206,207
901550-01	CARBON FILM, 1K OHM	R204,407,702,1204,412, 502,508,1003,1004
901550-49	CARBON FILM, 100 OHM	R115,R117
901550-18	CARBON FILM, 2.2K OHM	R604,R608
901550-19	CARBON FILM, 4.7K OHM	R105,R404,R606,901, R803,R1002,R904,806, R406,R509,R903,811
901550-03	CARBON FILM, 5.1K OHM	R805
901550-20	CARBON FILM, 10K OHM	R202,R501,R605,905, 302,R113,R116
901550-84	CARBON FILM, 1M OHM	R203,R601,R602,R807, 205
901600-28	CARBON FILM, 2.2 OHM	R208,R610
901550-17	CARBON FILM, 1.2 OHM	R1205
901550-110	CARBON FILM, 51 OHM	R403
901550-92	CARBON FILM, 20K OHM	R301
901550-70	CARBON FILM, 300 OHM	R809
RESISTORS 1% @ 1/4 WATT		
901751-44	CARBON FILM, 150 OHM	R107-R109,1005,1006
901751-61	CARBON FILM, 365 OHM	R110
901751-55	CARBON FILM, 2K OHM	R111,R112
901751-38	CARBON FILM, 4.64K OHM	R104
901751-62	CARBON FILM, 340 OHM	R106
RADIAL CERAMIC CAPACITORS 5% @ 50 VOLT		
900019-13	RADIAL LEAD, 22pF	C601,C402
900019-25	RADIAL LEAD, 27pF	C202
900019-17	RADIAL LEAD, 47pF	C204,C205,C602,C803, C804
900020-04	RADIAL CERAMIC .0047uF	C201
900019-15	RADIAL LEAD, 100pF	C603,C621-626,C514-C532
900019-20	RADIAL LEAD, 10pF	C401
900019-21	RADIAL LEAD, 1000pF	C206,C627,C207
900022-03	MONO., RAKIAL LEAD, .1uF	C203-CB102,CB115, CB1011,CB1014, CB2031-2034,CB205, CB206,CB3011,CB3012,

COMPONENT PARTS LIST
PCB ASSEMBLY #313055-01 *(Continued)*

RADIAL CERAMIC CAPACITORS- 5% @ 50 VOLT *(Continued)*		
900022-03	MONO., RAKIAL LEAD, .1uF *(continued)*	CB302,CB3031-3039, CB3041-3048,CB401-412 CB501,CB502,CB6011, CB6012,CB602-605, CB6051,CB6052,CB706, CB716,CB722,CB8011, CB8012,CB8021, CB8022,CB902,1001, CB901,CB905,116, CB1002,1121,CB1101, CB1102
900019-07	.047 UF	C301,C101
900022-05	MONO., RADIAL LEAD, .33uF	CB118-125,707-714,403-407,409-411,CB415, CB416,CB701-705,715, 717-721,803,CB903, 904,1201-1205,413, CB305
900022-01	MONO., RADIAL LEAD, .22uF	C511,CB126
ELECTROLYTIC CAPACITORS		
390101-08	ELECT., ALUM., RADIAL, 1uF	C507,C513
900402-01	CAP ELECT., TAN, 10uF	C208
390101-01	ELECT., ALUM., RADIAL, 47uF	C501-C506,C508-C510, C512
390101-06	ELECT., ALUM., RADIAL 10uF	C1202
MISCELLANEOUS		
251842-02	EMI FILTER 100PF	EM1624-1631,1201
390257-01	EMI FILTER 22000PF	EMI1203
390297-03	EMI FILTER 2200PF	EMI1201,202
390297-02	EMI FILTER MURRATA DSS306-55Y5101M	EMI101-105
390275-04	EMI FILTER 150 PF	EMI607-623
903025-08	FERRITE BEADS (AXIAL)	FB403,404,101,1001, FB103
903025-01	FERRITE BEADS (AXIAL)	FB104,601-608,405,102
390253-02	FERRITE BEADS THREE TURN	FB201-204
900850-01	DIODE 1N4148	CR201,CR202,CR501, CR502,CR601-CR603

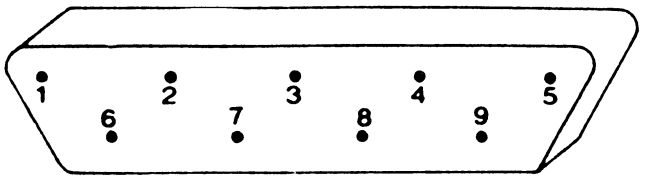
MISCELLANEOUS *(Continued)*		
380393-01	BATTERY, NICAD 3.6V	BT201,BT202
390280-01	FUSE, PICO, 4A	FU601
390321-01	DELAY LINE 10 TAP @ 20 NS	DL701
902658-01	TRANSISTOR 2N3904	Q601,Q801,Q1201
312680-01	PIEZO BEEPER QMB12	PZ801
251260-01	PUSH BUTTON N.O. SWITCH	PB501
904775-01	PIANO DIP SWITCH, I PIN, 4 POS.	SW101
904150-05	SOCKET, 28 PIN, DIP	U108,U109,U1101, U1102
904150-06	SOCKET, 40 PIN, DIP	U302
390185-02	SOCKET, 68 PIN, PLCC	U301,U601
390185-01	SOCKET, 84 PIN, PLCC	U303,304,801,802
390185-04	SOCKET, 100 PIN, PLCC	U101
390242-01	D-SUB, 9 PIN, RT. ANGLE MALE	CN601
390334-01	D-SUB, 15 PIN, RT. ANGLE FEMALE	CN101
390242-05	D-SUB, 25 PIN, RT. ANGLE MALE	CN603
390241-05	D-SUB, 25 PIN, TR. ANGLE FEMALE	CN602
903446-25	EXPANSION CONNECTOR, 62 PIN	CN501,CN503
903446-04	EXPANSION CONNECTOR, 36 PIN	CN505,CN507,CN502, CN504,CN506,CN507
252166-03	DIN, TK PIN, ROUND, FEMALE	CN201
252122-01	JACK, RCA RT. ANGLE, FEMALE	CN1201
903326-03	HEADER, 3 PIN, SIL	CB902,JMP904,CN512, CN202
903326-02	HEADER, 2 PIN, SIL	JMP 903 (REMOVE PINS 3,20)
903345-17	HEADER, 34 PIN, DIL	CN1001
903345-20	HEADER, 40 PIN, DIL	CN901
903349-01	POWER CONNECTOR, 6 PIN.	CN509
390043-01	SHORTING BLOCKS, 2 POS.	SEE 8 OF 8
390186-01	JUMPER	R810, R213, R103
SUBSTITUTE PARTS		
390317-01	IC, FE3010A	U802 SUB:
390304-01	IC, WD37C65	U1001 SUB:
390304-02	IC, WD37C65A	U1001 SUB:



PCB Assembly #313055-01, Rev. 5

MOUSE PORT

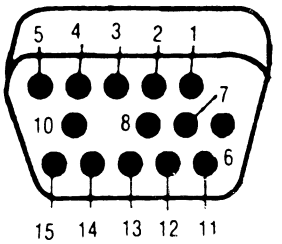
CN601 (5mm)



Pin No.	Signal
1	Vertical
2	Horizontal
3	Vertical Q
4	Horizontal Q
5	Button (3)
6	Button (1)
7	+ 5V
8	Ground
9	Button (2)

VIDEO PORT

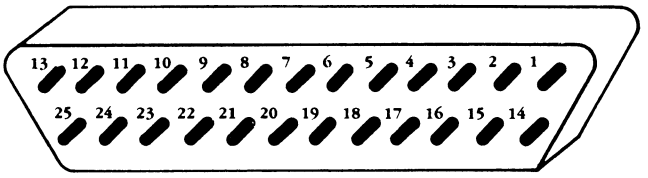
CN101 (3/16")



Pin	Function
1.	Red Video
2.	Green Video
3.	Blue Video
4.	Monitor ID Bit 2 (not used)
5.	ground
6.	Red Return (ground)
7.	Green Return (ground)
8.	Blue Return (ground)
9.	Key (no pin)
10.	Sync Return (ground)
11.	Monitor ID Bit 0 (not used)
12.	Monitor ID Bit 1 (not used)
13.	Horizontal Sync
14.	Vertical Sync
15.	not used

SERIAL PORT

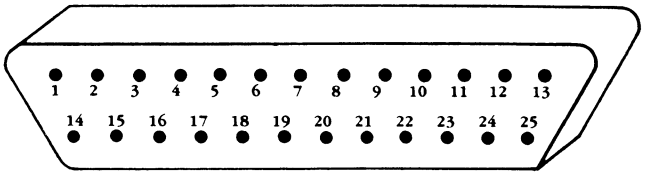
CN603 (5mm)



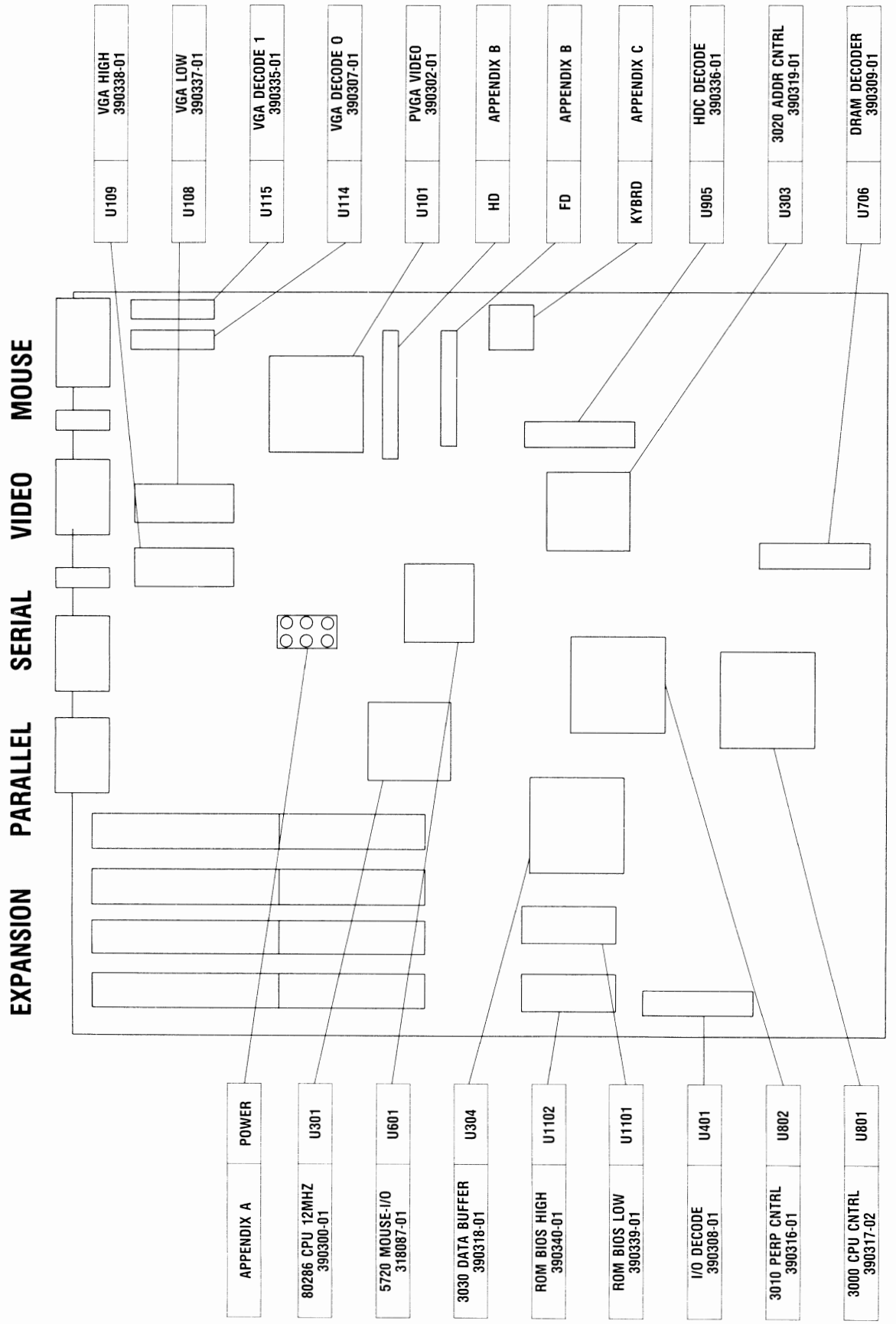
Computer Side		Peripheral Side
	1	CHASSIS GROUND
→	2	T x D
←	3	R x D
→	4	RTS
←	5	CTS
←	6	DSR
	7	SIG GND
←	8	DCD
	9	+ 12V
	10	- 12V
→	20	DTR
←	22	RI

PARALLEL PORT

CN602 (5mm)



Computer Side		Printer Side
→	1	STROBE
→	2	DO
→	3	D1
→	4	D2
→	5	D3
→	6	D4
→	7	D5
→	8	D6
→	9	D7
←	10	ACK
←	11	BUSY
←	12	PE
←	13	SLCT
→	14	AUTO FDXT
←	15	ERROR
→	16	INIT
→	17	SLCT IN
	18-25	GND



PC40-III MAJOR ICs AND CONNECTORS

SECTION 5

- **IC PINOUTS**
- **SCHEMATICS**

INFORMATION IN THIS SECTION IS FOR REFERENCE ONLY. COMMODORE WILL NOT SUPPLY COMPONENT PARTS FOR OEM ASSEMBLIES.

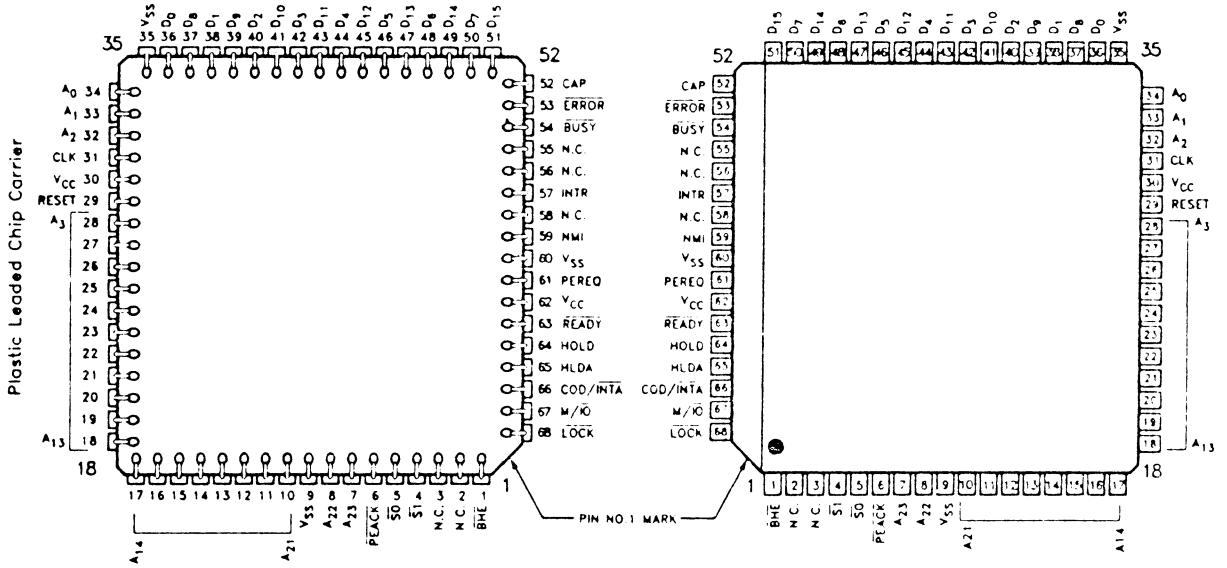
IC PIN OUTS & SIGNAL DESCRIPTIONS

1)	80286	CPU	390300-01
2)	FE3000A	CPU CNTRL	390316-01
3)	FE3010B	PERP CNTRL	390317-02
4)	FE3020	ADDR BUFFER	390319-01
5)	FE3030	DATA BUFFER	390318-01
6)	PVGA-1A	PARADISE VIDEO	390302-01
7)	PPC1	PRINTER INTERFACE	318091-01
8)	WD37C65	FDC	390304-03
9)	8250	SERIAL INTERFACE	380205-01
10)	5720	MOUSE CONTROL	318087-01

1) 80286 CPU 390300-01

Component Pad Views—As viewed from underside of component when mounted on the board.

P.C. Board Views—As viewed from the component side of the P.C. board.



SYMBOL	*TYPE*	*NAME AND FUNCTION*
CLK	I	SYSTEM CLOCK provides the fundamental timing for 80286 systems. It is divided by two inside the 80286 to generate the processor clock. The internal divide-by-two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.
D15-D0	I/O	DATA BUS inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.
A23-A0	O	ADDRESS BUS outputs physical memory and I/O port addresses. A0 is LOW when data is to be transferred on pins D7-0. A23-A16 are LOW during I/O transfers. The address bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.
$\overline{BHE}$	O	BUS HIGH ENABLE indicates transfer or data on the upper byte of the data bus. D15-8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use $\overline{BHE}$ to condition chip select functions. BHE is active LOW and floats to 3-state OFF during bus hold acknowledge.

$\overline{BHE}$ and A0 Encodings

$\overline{BHE}$ Value	A0 Value	Function
0	0	Word transfer
0	1	Byte transfer on upper half of data bus (D15-8)
1	0	Byte transfer on lower half of data bus (D7-0)
1	1	Will never occur

$\overline{S1}$, $\overline{S0}$	O	BUS CYCLE STATUS indicates initiation of a bus cycle and, along with M/$\overline{IO}$ and COD/$\overline{INTA}$, defines the type of bus cycle. The bus is in a Ts state whenever one or both are LOW, $\overline{S1}$ and $\overline{S0}$ are active LOW and float to 3-state OFF during bus hold acknowledge.

80286 Bus Cycle Status Definition

COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0 (LOW)	0	0	0	Interrupt acknowledge
0	0	0	1	Will not occur
0	0	1	0	Will not occur
0	0	1	1	None; not a status cycle
0	1	0	0	IF A1 = 1 then halt; else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None; not a status cycle
1 (HIGH)	0	0	0	Will not occur
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	None; not a status cycle
1	1	0	0	Will not occur
1	1	0	1	Memory instruction read
1	1	1	0	Will not occur
1	1	1	1	None; not a status cycle

SYMBOL	*TYPE*	*NAME AND FUNCTION*
M/$\overline{IO}$	O	MEMORY I/O SELECT distinguishes memory access from I/O access, if HIGH during Ts, a memory cycle or a halt/shutdown cycle is in progress. It LOW, an I/O cycle or an interrupt acknowledge cycle is in progress. M/$\overline{IO}$ floats to 3-state OFF during bus hold acknowledge.
COD/$\overline{INTA}$	O	CODE/INTERRUPT ACKNOWLEDGE distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{INTA}$ floats to 3-state OFF during bus hold acknowledge. Its timing is the same as M/$\overline{IO}$.
$\overline{LOCK}$	O	BUS LOCK indicates that other system bus masters are not to gain control of the system bus for the current and the following bus cycle. The $\overline{LOCK}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by 80286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{LOCK}$ is active LOW and floats to 3-state OFF during bus hold acknowledge.
$\overline{READY}$	I	BUS READY terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{READY}$ LOW. $\overline{READY}$ is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{READY}$ is ignored during bus hold acknowledge.
HOLD	I	BUS HOLD REQUEST AND HOLD ACKNOWLEDGE control ownership of the 80286 local bus. The HOLD input allows another local bus master to
HLDA	O	request control of the local bus. When control is granted, 80286 will float its bus drivers to 3-state OFF and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the 80286 deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition. HOLD may be asynchronous to the system clock. These signals are active HIGH.
INTR	I	INTERRUPT REQUEST requests the 80286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the 80286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active HIGH, and may be asynchronous to the system clock.
NMI	I	NON-MASKABLE INTERRUPT REQUEST interrupts the 80286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the 80286 flag word does not affect this input. The NMI input is active HIGH, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles and remain HIGH for at least four system clock cycles.
PEREQ	I	PROCESSOR EXTENSION OPERAND REQUEST AND ACKNOWLEDGE extend the memory management and protection capabilities of the 80286
$\overline{PEACK}$	O	to processor extensions. The PEREQ input requests the 80286 to perform a data operand transfer for a processor extension. The $\overline{PEACK}$ output signals the processor extension when the requested operand is being transferred. PEREQ is active HIGH and floats to 3-state OFF during bus hold acknowledge. $\overline{PEACK}$ may be asynchronous to the system clock. $\overline{PEACK}$ is active LOW.
$\overline{BUSY}$	I	PROCESSOR EXTENSION BUSY AND ERROR indicate the operating condition of a processor extension to the 80286. An active $\overline{BUSY}$ input stops 80286 pro-
$\overline{ERROR}$	I	gram execution on WAIT and some ESC instructions until $\overline{BUSY}$ becomes inactive (HIGH). The 80286 may be interrupted while waiting for $\overline{BUSY}$ to become inactive. An active $\overline{ERROR}$ input causes the 80286 to perform a processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock. These inputs have internal pull-up resistors.
RESET	I	SYSTEM RESET clears the internal logic of the 80286 and is active HIGH. The 80286 may be reinitialized at any time with a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the 80286 enter the state shown below:

80286 Pin State During Reset

Pin Value	Pin Names
1 (HIGH)	$\overline{S0}$, $\overline{S1}$, $\overline{PEACK}$, A23-A0, $\overline{BHE}$, $\overline{LOCK}$
0 (LOW)	M/$\overline{IO}$, COD/$\overline{INTA}$, HLDA (Note 1)
3-state OFF	D15-D0

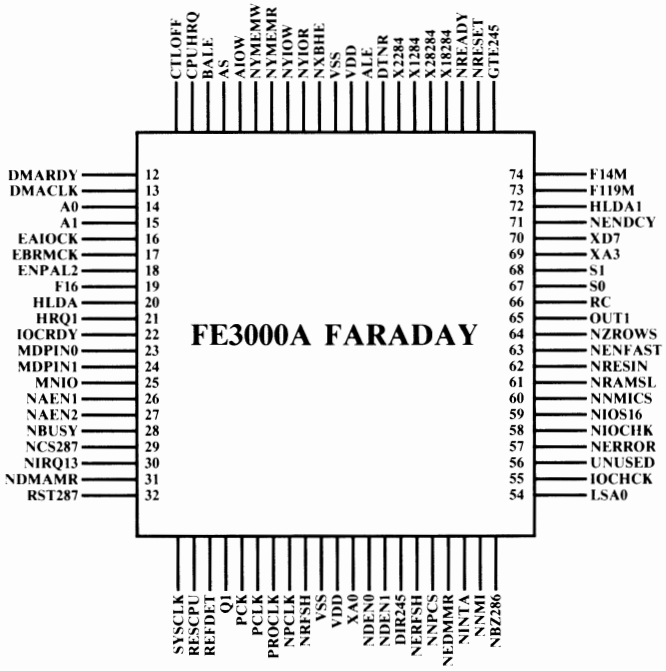
Operation of the 80286 begins after a HIGH to LOW transition on RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 38 CLK cycles from the trailing edge of RESET are requried by the 80286 for internal initialization before the first bus cycle, to fetch code from the power-on execution address, occurs.

A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the system clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase synchronous to another clock.

Vss	I	SYSTEM GROUND: 0 Volts.
Vcc	I	SYSTEM POWER: +5 Volt Power Supply.
CAP	I	SUBSTRATE FILTER CAPACITOR: a 0.047 μF $\pm$ 20% 12V capacitor must be connected between this pin and ground. This capacitor filters the output of the internal substrate bias generator. A maximum DC leakage current of 1 μA is allowed through the capacitor. For correct operation of the 80286, the substrate bias generator must charge this capacitor to its operating voltage. The capacitor chargeup time is 5 milliseconds (max.) after Vcc and CLK reach their specified AC and DC parameters. RESET may be applied to prevent spurious activity by the CPU during this time. After this time, the 80286 processor clock can be synchronized to another clock by pulsing RESET LOW synchronous to the system clock.

NOTE: HLDA is only Low if HOLD is inactive (Low).

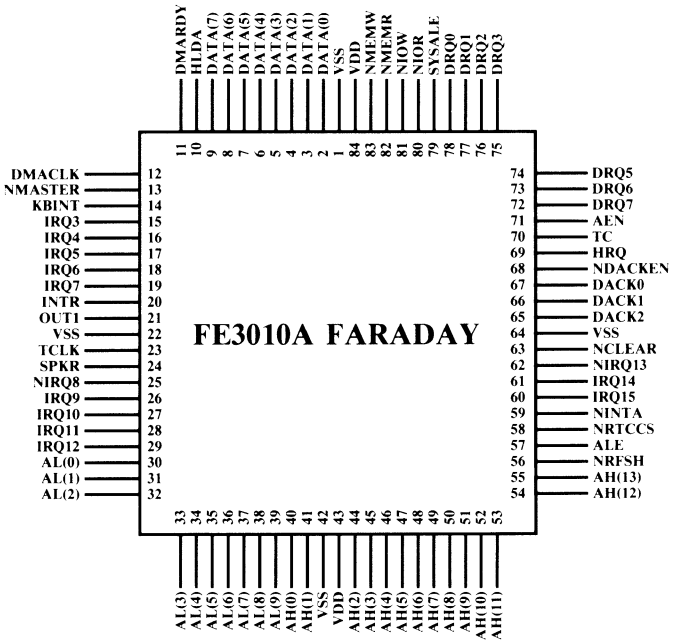
2) FE3000A CPU CNTRL 390316-01



PIN	*TYPE*	*SYMBOL*	*FUNCTION*
1		VSS	GROUND
2	I/O	NXBHE	BUS HIGH ENABLE Active low — Indicates the current bus cycle will transfer a byte on the upper byte.
3	I/O	NYIOR	I/O READ COMMAND Active low — Indicates a read of an I/O device.
4	I/O	NYIOW	I/O WRITE COMMAND Active low — Indicates a write of an I/O device.
5	I/O	NYMEMR	MEMORY READ COMMAND Active low — Indicates a read of memory.
6	I/O	NYMEMW	MEMORY WRITE COMMAND Active low — Indicates a write of memory.
7	O	AIOW	EXTENDED I/O WRITE COMMAND Active high — Used for external wait state generator.
8	O	AS	REAL TIME CLOCK ALE Active high — Used to latch the address in the clock calender chip (Motorola 146818)
9	O	BALE	BUS ADDRESS LATCH ENABLE Active high — Or of ALE and HLDA.
10	O	CPUHRQ	BUS HOLD REQUEST TO 80286 Active high — Bus request to 80286 CPU caused by refresh or a DMA cycle.
11	O	CTLOFF	DATA LATCH CONTROL Active high — Latch data bits 0-7 of first bus cycle of a word transfer on a byte device.
12	O	DMARDY	READY TO DMA Active high — Indicates that the DMA may complete its cycle.
13	O	DMACLK	CLOCK TO DMA DEVICES Clock in sync with and half the frequency of the SYSCLK (ie: 3, 4, or 5 MHz)
14	I	A0	80286 ADDRESS A0 Active high — Address bit 0 from the 80286.
15	I	A1	80286 ADDRESS A1 Active high — Address bit 1 from the 80286.
16	I	EAIOCK	ENABLE I/O CHECK Active high — Enable error signal from the expansion bus.
17	I	EMBRMCK	ENABLE RAM PARITY CHECK CONTROL Active high — Enable parity check from on board RAM.
18	I	ENPAL2	ENABLE EXTERNAL WAIT STATE Active high — Disables external wait state generator.
19	I	F16	16 BIT MEMORY OPERATION Active high — Indicates that the current memory cycle
20	I	HLDA	HOLD ACKNOWLEDGE FROM THE 80286 Active high — Indicates that the 80286 has released the bus in response to a CPUHRQ signal.
21	I	HRQ1	HOLD REQUEST Active high — Bus request from a DMA controller.
22	I	IOCRDY	EXPANSION BUS READY Active high — Signal from the expansion bus to indicate that the current cycle may complete.
23	I	MDPIN0	PARITY BIT FROM RAM BANK 0 Parity bit from on board RAM bits 0-7.
24	I	MDPIN1	PARITY BIT FROM RAM BANK 1 Parity bit from on board RAM bits 8-15.
25	I	MNIO	MEMORY I/O SELECT Active high — Signal from the 80286 indicating the next cycle is a memory cycle.
26	I	NAEN1	ENABLE DMA CHANNELS 0-3 TO USE DATA BUS Active low
27	I	NAEN2	ENABLE DMA CHANNELS 5-7 TO USE DATA BUS Active low
28	I	NBUSY	BUSY STATUS ASSERTED BY 80287 Active low
29	I	NCS287	80287 I/O CHIP DECODE Active low
30	O	NIRQ13	INTERRUPT REQUEST 13 Active low — Co-processor error
31	I	NDMAMR	DMA MEMORY READ COMMAND Active low — Memory read command from a DMA controller
32	O	RST287	RESET TO 80287 Active high
33	O	SYSCLK	SYSTEM CLOCK System clock in phase with and half the frequency of the PROCLK. (ie: 6, 8, or 10MHz)
34	O	RESCPU	RESET TO 80286 Active high — Reset to CPU from a command to exit protected mode or an external reset.
35	O	REFDET	REFRESH DETECT Signal that toggles each time there is a refresh cycle to the RAM.
36	O	Q1	START OF BUS CYCLE. Active high — Indicates start of a bus cycle to the external wait state generator.
37	O	PCK	PARITY CHECK Active high — Indicates a RAM parity error has been detected.
38	O	PCLK	CLOCK TO 8042
39	O	PROCLK	PROCESSOR CLOCK TO 80286 Clock twice the processor speed. (ie: 12, 16, or 20 MHz)
40	O	NPCLK	INVERTED CLOCK TO 8042
41	I/O	NRFSH	REFRESH CYCLE Active low — Indicates the current bus cycle is a RAM refresh cycle.
42		VSS	GROUND
43		VDD	+5 VOLTS SUPPLY
44	I/O	XA0	ADDRESS A0 Active high — System address bit 0
45	O	NDEN0	GATE DATA 0-7 Active low
46	O	NDEN1	GATE DATA 8-15 Active low
47	O	DIR245	BYTE SWAP DIRECTION Signal to control byte swap direction on a 16 bit transfer on a 8 bit device.
48	O	NERFSH	ENABLE REFRESH ADDRESS Active low — Signal to enable the refresh address to the address bus during a RAM refresh cycle.
49	O	NNPCS	80287 CHIP SELECT Active low

PIN	*TYPE*	*SYMBOL*	*FUNCTION*
50	O	NEDMMR	ENABLE DMA MEMORY READ Active low — Gates a memory read to the bus during a DMA cycle.
51	O	NINTA	INTERRUPT ACKNOWLEDGE Active low — Interrupt acknowledge to the interrupt controllers.
52	O	NNMI	NMI OUTPUT TO 80286 Active low — Non-maskable interrupt to 80286.
53	O	NBZ286	80287 BUSY TO 80286 Active low
54	O	LSA0	LATCHED SYSTEM ADDRESS A0 Active high — System address bit 0 during a CPU bus cycle.
55	O	IOCHCK	I/O DEVICE ERROR Active high — Indicates an error from the expansion bus.
56		UNUSED	UNUSED Must be left open
57	I	NERROR	80287 ERROR Active low — Error from the 80287.
58	I	NIOCHK	I/O CHECK Active low — Error signal from the expansion bus.
59	I	NIOS16	16 BIT I/O TRANSFER Active low — Signal from the expansion bus to indicate that the current bus cycle is a 16 bit I/O transfer.
60	I	NNMICS	NMI PORT DECODE Active low — Decode of NMI enable port.
61	I	NRAMSL	ON BOARD RAM DECODE Active low
62	I	NRESIN	RESET IN Active low — External reset in used to generate a system reset.
63	I	NENFAST	ENABLE LOOK AHEAD DECODE Active low — Causes early eneration of memory read and write signals with zero wait states.
64	I	NZROWS	ZERO WAIT STATES Active low — Indicates the current bus cycle should have no wait states.
65	I	OUT1	TERMINAL COUNT OF TIMER CHANNEL 1 Active high — Terminal count from timer channel 1.
66	I	RC	RESET TO CPU 80286 Active high — Input to generate RESET to CPU.
67	I	S0	BUS CYCLE STATUS S0 FROM 80286
68	I	S1	BUS CYCLE STATUS S1 FROM 80286
69	I	XA3	ADDRESS A3 Active high — System address bit 3
70	I	XD7	SYSTEM DATA BUS BIT 7 Active high
71	I	NENDCY	TERMINATE CURRENT CYCLE Active low — Signal from external wait state generator to end the current bus cycle.
72	O	HLDA1	HOLD ACKNOWLEDGE TO DMA Active high — Hold acknowledge to one of DMA controllers.
73	O	F119M	1.19 MHz CLOCK TO TIMER
74	O	F14M	14.318 MHz SIGNAL TO EXPANSION BUS
75	O	GTE245	ENABLE BUS SWAP Active low — Gates data during the swap of a byte on a 16 bit transfer on a 8 bit device.
76	O	NRESET	RESET TO SYSTEM LOGIC Active low
77	O	NREADY	SYNCHRONIZED READY TO CPU Active low — Ready to CPU indicating that the current bus cycle may terminate.
78	I	X18284	CRYSTAL TO 8284 CLOCK GENERATOR
79	O	X28284	CRYSTAL TO 8284 CLOCK GENERATOR
80	I	X1284	CRYSTAL TO 82284 CLOCK GENERATOR
81	O	X2284	CRYSTAL TO 82284 CLOCK GENERATOR
82	O	DTNR	DATA DIRECTION CONTROL Active low — A low indicates a bus read cycle.
83	O	ALE	ADDRESS LATCH ENABLE Active high — Signal to latch the address from the 80286.
84		VDD	+5 VOLTS SUPPLY

3) FE3010A (B) PERP. CNTRL 390317-02 (-02)

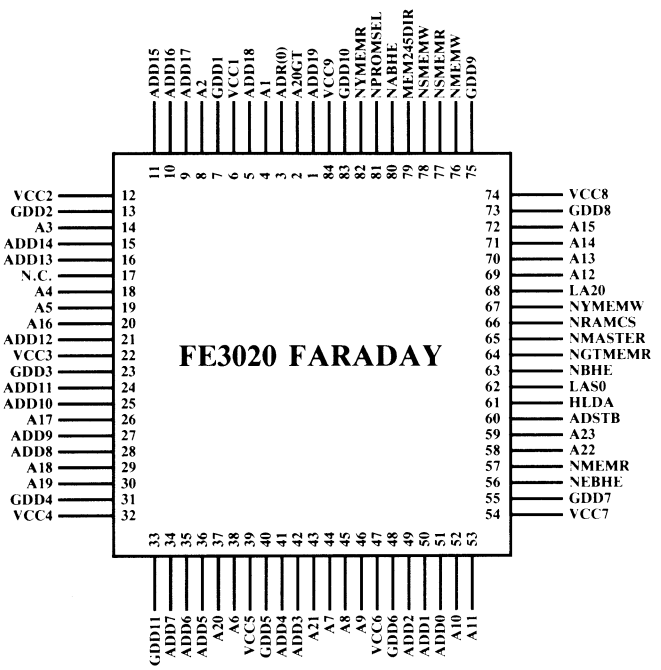


PIN	*TYPE*	*SYMBOL*	*FUNCTION*
1		VSS	GROUND
2	I/O	DATA(0)	DATA BIT 0
3	I/O	DATA(1)	DATA BIT 1
4	I/O	DATA(2)	DATA BIT 2
5	I/O	DATA(3)	DATA BIT 3
6	I/O	DATA(4)	DATA BIT 4
7	I/O	DATA(5)	DATA BIT 5
8	I/O	DATA(6)	DATA BIT 6
9	I/O	DATA(7)	DATA BIT 7
10	I	HLDA	HOLD ACKNOWLEDGE Active high — Acknowledge from the CPU (80286) for a request for the bus from the DMA controller.
11	I	DMARDY	DMA READY Active high — Signal to indicates that DMA may complete its current cycle.
12	I	DMACLK	DMA CLOCK System Clock / DMACLK 6 MHz / 3 or 6 MHz 8 MHz / 4 or 8 MHz 10 MHz / 5 MHz
13	I	NMASTER	BUS MASTER Active low — Signal to indicate that a master on the expansion bus has control of the bus.
14	I	KBINT	KEYBOARD INTERRUPT Active high
15	I	IRQ3	INTERRUPT REQUEST 3 Active high
16	I	IRQ4	INTERRUPT REQUEST 4 Active high
17	I	IRQ5	INTERRUPT REQUEST 5 Active high
18	I	IRQ6	INTERRUPT REQUEST 6 Active high
19	I	IRQ7	INTERRUPT REQUEST 7
20	O	INTR	INTERRUPT REQUEST TO CPU (80286) Active high
21	O	OUT 1	TIMER CHANNEL 1 OUTPUT
22		VSS	GROUND
23	I	TCLK	TIMER CLOCK (1.19 MHz clock for timer)
24	O	SPKR	SPEAKER
25	I	NIRQ8	INTERRUPT REQUEST 8 Active low
26	I	IRQ9	INTERRUPT RQUEST 9 Active high
27	I	IRQ10	INTERRUPT REQUEST 10 Active high
28	I	IRQ11	INTERRUPT REQUEST 11 Active high
29	I	IRQ12	INTERRUPT REQUEST 12 Active high
30	I/O	AL(0)	ADDRESS BIT 0
31	I/O	AL(1)	ADDRESS BIT 1
32	I/O	AL(2)	ADDRESS BIT 2
33	I/O	AL(3)	ADDRESS BIT 3
34	I/O	AL(4)	ADDRESS BIT 4
35	I/O	AL(5)	ADDRESS BIT 5
36	I/O	AL(6)	ADDRESS BIT 6
37	I/O	AL(7)	ADDRESS BIT 7
38	I/O	AL(8)	ADDRESS BIT 8
39	I/O	AL(9)	ADDRESS BIT 9
40	I/O	AH(0)	ADDRESS BIT 10
41	I/O	AH(1)	ADDRESS BIT 11
42		VSS	GROUND
43		VDD	+5 VOLTS SUPPLY
44	O	AH(2)	ADDRESS BIT 12
45	O	AH(3)	ADDRESS BIT 13
46	O	AH(4)	ADDRESS BIT 14
47	O	AH(5)	ADDRESS BIT 15
48	O	AH(6)	ADDRESS BIT 16
49	O	AH(7)	ADDRESS BIT 17
50	O	AH(8)	ADDRESS BIT 18
51	O	AH(9)	ADDRESS BIT 19
52	O	AH(10)	ADDRESS BIT 20
53	O	AH(11)	ADDRESS BIT 21
54	O	AH(12)	ADDRESS BIT 22
55	O	AH(13)	ADDRESS BIT 23
56	I	NRFSH	REFRESH ADDRESS Active low — Signal to enable the refresh to the address bus during a RAM refresh cycle.
57	I	ALE	ADDRESS LATCH ENABLE Active high
58	O	NRTCCS	REAL TIME CLOCK CHIP SELECT Active low
59	I	NINTA	INTERRUPT ACKNOWLEDGE FROM CPU (80286) Active low — Interrupt acknowledge to the interrupt controllers.
60	I	IRQ15	INTERRUPT REQUEST 15 Active high
61	I	IRQ14	INTERRUPT REQUEST 14 Active high
62	I	NIRQ13	INTERRUPT REQUEST 13 Active low — Error interrupt from (80287).
63	I	NCLEAR	SYSTEM CLEAR Active low
64		VSS	GROUND
65	O	DACK2	DMA ACKNOWLEDGE BIT 2
66	O	DACK1	DMA ACKNOWLEDGE BIT 1
67	O	DACK0	DMA ACKNOWLEDGE BIT 0
68	O	NDACKEN	DMA ACKNOWLEDGE ENABLE Active low — Signal to enable DACK0, DACK1, and DACK2 decodes.
69	O	HRQ	DMA REQUEST TO CUP (80286) Active high
70	O	TO	DMA END OF OPERATION Active high — Signal to indicate the DMA controller has finished its cycle.
71	O	AEN	DMA AEN Active high — Signal to indicate that the current bus is a DMA cycle.
72	I	DRQ7	CHANNEL 7 DMA REQUEST Active high

DACK2	DACK1	DACK0	DMA Channel Acknowledge
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Illegal
1	0	1	
1	1	0	6
1	1	1	7

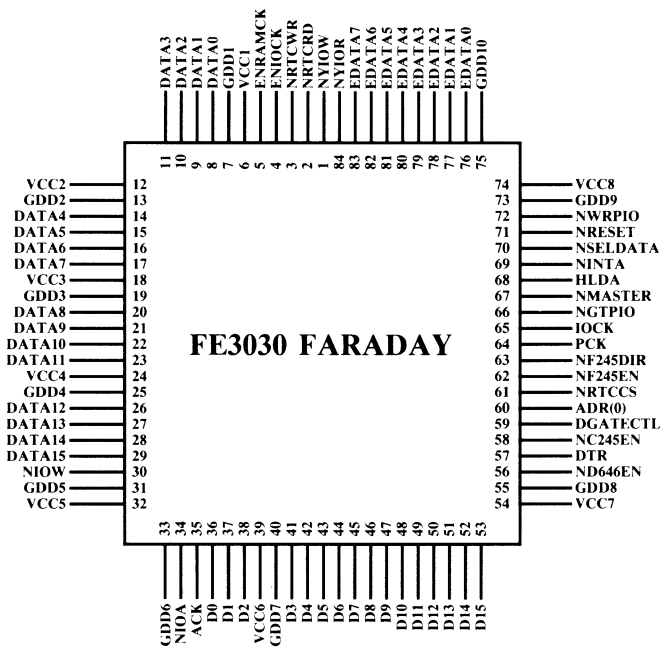
PIN	*TYPE*	*SYMBOL*	*FUNCTION*
73	I	DRQ6	CHANNEL 6 DMA REQUEST Active high
74	I	DRQ5	CHANNEL 5 DMA REQUEST Active high
75	I	DRQ3	CHANNEL 3 REQUEST Active high
76	I	DRQ2	CHANNEL 2 DMA REQUEST Active high
77	I	DRQ1	CHANNEL 1 DMA REQUEST Active high
78	I	DRQ0	CHANNEL 0 DMA REQUEST Active high
79	O	SYSALE	SYSTEM ALE Active high — Signal to latch the address in the address latch.
80	I/O	NIOR	I/O READ COMMAND Active low
81	I/O	NIOW	I/O WRITE COMMAND Active low
82	O	NMEMR	MEMORY READ COMMAND Active low
83	O	NMEMW	MEMORY WRITE COMMAND Active low
84		VDD	+5 VOLTS SUPPPLY

4) FE3020 ADDR BUFFER 390319-01



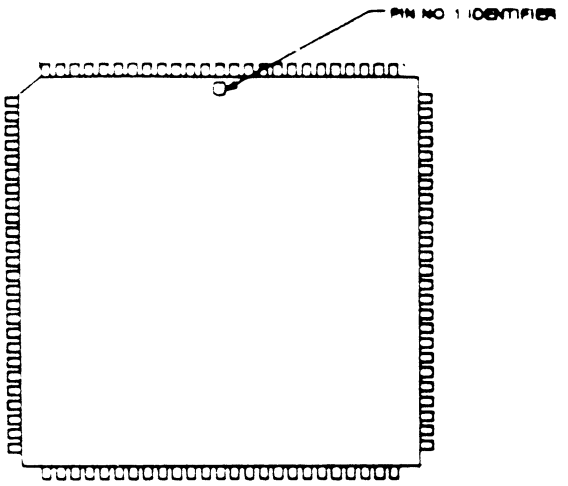
PIN	*TYPE*	*SYMBOL*	*FUNCTION*
65	I	NMASTER	MASTER Active low — Signal from the AT bus which allows the bus master to control the bus.
61	I	HLDA	HOLD ACKNOWLEDGE Active high — Signal from the 80286 to indicate that the bus has been released in response to a CPU HRQ signal.
62	I	ADSTB	ADDRESS STROBE Active high — Signal from the FE3010 that latches the address.
63	I	NRAMCS	RAM CHIP SELECT Active low — On board RAM chip select.
64	I/O	NYMEMW	MEMORY WRITE COMMAND Active low — Signal to indicate a write of memory during a CPU, DMA, or Master cycle.
82	I/O	NYMEMR	MEMORY READ COMMAND Active low — Signal to indicate a read of memory during a CPU or Master cycle.
64	I	NGTMEMR	GATE MEMORY READ Active low — Signal to indicate a read memory during a DMA cycle.
76	I/O	NMEMW	AT BUS MEMORY WRITE COMMAND Active low — Signal to indicate a write of memory during a CPU, DMA, or Master cycle.
57	I/O	NMEMR	AT BUS MEMORY WRITE COMMAND Active low — Signal to indicate a read of memory during a CPU, DMA, or Master cycle.
78	O	NSMEMW	PC BUS MEMORY WRITE COMMAND Active low — Signal to indicate a write of memory below 1MB during a CPU, DMA, or Master cycle.
77	O	NSMEMR	PC BUS MEMORY READ COMMAND Active low — Signal to indicate a read of memory below 1 MB during a CPU, DMA, or Master cycle.
56	I/O	NEBHE	AT BUS BYTE HIGH ENABLE Active low — Indicates a transfer of data on the upper byte of the data bus.
63	I	NBHE	80386 BUS BYTE HIGH ENABLE Active low — Indicates a transfer of data on the upper byte of the data bus.
80	I/O	NABHE	FE3000 BUS BYTE HIGH ENABLE Active low — Indicates a transfer of data on the upper byte of the data bus.
81	O	NPROMSEL	PROM SELECT Active low — BIOS PROM select
79	O	MEM245 DIR	MEMORY BUFFER DIRECTION Direction control for the on board memory buffers.
62	I	LAS0	FE3000 ADDRESS BIT 0
3	I/O	ADR(0)	FE3000/FE3010 ADDRESS BIT 0
4	I/O	A1	80286/FE3010 ADDRESS BIT 1
8	I/O	A2	80286/FE3010 ADDRESS BIT 2
14	I/O	A3	80286/FE3010 ADDRESS BIT 3
18	I/O	A4	80286/FE3010 ADDRESS BIT 4
19	I/O	A5	80286/FE3010 ADDRESS BIT 5
38	I/O	A6	80286/FE3010 ADDRESS BIT 6
44	I/O	A7	80286/FE3010 ADDRESS BIT 7
45	I/O	A8	80286/FE3010 ADDRESS BIT 8
46	I/O	A9	80286/FE3010 ADDRESS BIT 9
52	I/O	A10	80286/FE3010 ADDRESS BIT 10
53	I/O	A11	80286/FE3010 ADDRESS BIT 11
69	I/O	A12	80286/FE3010 ADDRESS BIT 12
70	I/O	A13	80286/FE3010 ADDRESS BIT 13
71	I/O	A14	80286/FE3010 ADDRESS BIT 14
72	I/O	A15	80286/FE3010 ADDRESS BIT 15
20	I/O	A16	80286/FE3010 ADDRESS BIT 16
26	I/O	A17	80286/FE3010 ADDRESS BIT 17
29	I/O	A18	80286/FE3010 ADDRESS BIT 18
30	I/O	A19	80286/FE3010 ADDRESS BIT 19
37	I/O	A20	80286 ADDRESS BIT 20
68	I/O	LA20	FE3010 ADDRESS BIT 20
2	I/O	A20GT	8042 GATE ADDRESS Active high — ENable address bit 20
43	I	A21	80286/FE3010 ADDRESS BIT 21
58	I	A22	80286/FE3010 ADDRESS BIT 22
59	I	A23	80286/FE3010 ADDRESS BIT 23
51	I/O	ADD0	AT BUS ADDRESS BIT 0
50	I/O	ADD1	AT BUS ADDRESS BIT 1
49	I/O	ADD2	AT BUS ADDRESS BIT 2
42	I/O	ADD3	AT BUS ADDRESS BIT 3
41	I/O	ADD4	AT BUS ADDRESS BIT 4
36	I/O	ADD5	AT BUS ADDRESS BIT 5
35	I/O	ADD6	AT BUS ADDRESS BIT 6
34	I/O	ADD7	AT BUS ADDRESS BIT 7
28	I/O	ADD8	AT BUS ADDRESS BIT 8
27	I/O	ADD9	AT BUS ADDRESS BIT 9
25	I/O	ADD10	AT BUS ADDRESS BIT 10
24	I/O	ADD11	AT BUS ADDRESS BIT 11
21	I/O	ADD12	AT BUS ADDRESS BIT 12
16	I/O	ADD13	AT BUS ADDRESS BIT 13
15	I/O	ADD14	AT BUS ADDRESS BIT 14
11	I/O	ADD15	AT BUS ADDRESS BIT 15
10	I/O	ADD16	AT BUS ADDRESS BIT 16
9	I/O	ADD17	AT BUS ADDRESS BIT 17
5	I/O	ADD18	AT BUS ADDRESS BIT 18
1	I/O	ADD19	AT BUS ADDRESS BIT 19
17		N/C	
6		VCC1	5V ± 5%
12		VCC2	5V ± 5%
22		VCC3	5V ± 5%
32		VCC4	5V ± 5%
39		VCC5	5V ± 5%
47		VCC6	5V ± 5%
54		VCC7	5V ± 5%
74		VCC8	5V ± 5%
84		VCC9	5V ± 5%
7		GDD1	GROUND
13		GDD2	GROUND
2		GDD3	GROUND
31		GDD4	GROUND
33		GDD11	GROUND
40		GDD5	GROUND
48		GDD6	GROUND
55		GDD7	GROUND
73		GDD8	GROUND
75		GDD9	GROUND
83		GDD10	GROUND

5) FE3030 DATA BUFFER 390318-01



PIN	*TYPE*	*SYMBOL*	*FUNCTION*
65	I	IOCK	I/O DEVICE ERROR Active high — This signal from the FE3000 indicates an error from the PC/AT bus.
64	I	PCK	PARITY CHECK Active high — This signal from the FE3000 indicates a parity error from the on board RAM.
66	I	NGTPIO	GATE PIO Active low — This signal gates the IOCK and PCK signals on to the data bus during a status read.
72	I	NWRPIO	WRITE PIO Active low — Write the error enable register.
4	O	ENIOCK	ENABLE IO CHECK Active high
5	O	ENRAMCK	ENABLE PARITY CHECK Active high
71	I	NRESET	RESET Active low — System reset from the FE3000.
70	I	NSELDATA	SELECT DATA Active low — This signal gates the E data bus.
69	I	NINTA	INTERRUPT ACKNOWLEDGE Active low — This signal gates the interrupt vector on the EDATA bus to the CPU.
68	I	HLDA	HOLD ACKNOWLEDGE Active high — Signal from the 80286 to indicate that the bus has been released in response to a CPU HRQ signal.
35	O	ACK	ACKNOWLEDGE Active high — Signal to indicate that the current cycle is a DMA cycle.
67	I	NMASTER	MASTER Active low — Signal from the AT bus which allows the bus master to control the bus.
63	I	NF245DIR	BYTE SWAP DIRECTION Controls the data bus direction for byte swap.
62	I	NF245EN	BYTE SWAP ENABLE Active low — This signal enables the byte swap bus.
57	I	DTR	DATA DIRECTION This signal determines the data direction on the bus.
60	I	ADDRESS(0)	AT BUS ADDRESS BIT 0
56	I	ND646 EN	DATA BUS ENABLE D (0:7) Active low — This signal enables the data bit 0-bus.
59	I	DGATECTL	DATA GATE CONTROL Active high — Signal to latch read data 0-7 on a 16 bit read of a 8 bit device.
58	I	NC245EN	DATA BUS ENABLE D (8:15) Active low — This signal enables the data bit 8-15 bus.
1	I/O	NYIOW	I/O WRITE COMMAND Active low — Signal to indicate a I/O write during a CPU, DMA, or Master cycle.
84	I/O	NYIOR	I/O READ COMMAND Active low — Signal to indicate a I/O read during a CPU, DMA, or Master Cycle.
30	I/O	NIOW	PC BUS I/O WRITE COMMAND Active low — Signal to indicate a I/O write during a CPU, DMA, or Master Cycle.
34	I/O	NIOR	PC BUS I/O WRITE COMMAND Active low — Signal to indicate a I/O read during a CPU, DMA, or Master Cycle.
61	I	NRTCCS	REAL TIME CLOCK CHIP SELECT Active low
2	O	NRTCRD	REAL TIME CLOCK READ Active low
3	O	NRTCWR	REAL TIME CLOCK WRITE Active low
36	I/O	D0	80286 DATA BIT 0
37	I/O	D1	80286 DATA BIT 1
38	I/O	D2	80286 DATA BIT 2
41	I/O	D3	80286 DATA BIT 3
42	I/O	D4	80286 DATA BIT 4
43	I/O	D5	80286 DATA BIT 5
44	I/O	D6	80286 DATA BIT 6
45	I/O	D7	80286 DATA BIT 7
46	I/O	D8	80286 DATA BIT 8
47	I/O	D9	80286 DATA BIT 9
48	I/O	D10	80286 DATA BIT 10
49	I/O	D11	80286 DATA BIT 11
50	I/O	D12	80286 DATA BIT 12
51	I/O	D13	80286 DATA BIT 13
52	I/O	D14	80286 DATA BIT 14
53	I/O	D15	80286 DATA BIT 15
8	I/O	DATA0	AT DATA BUS BIT 0
9	I/O	DATA1	AT DATA BUS BIT 1
10	I/O	DATA2	AT DATA BUS BIT 2
11	I/O	DATA3	AT DATA BUS BIT 3
14	I/O	DATA4	AT DATA BUS BIT 4
15	I/O	DATA5	AT DATA BUS BIT 5
16	I/O	DATA6	AT DATA BUS BIT 6
17	I/O	DATA7	AT DATA BUS BIT 7
20	I/O	DATA8	AT DATA BUS BIT 8
21	I/O	DATA9	AT DATA BUS BIT 9
22	I/O	DATA10	AT DATA BUS BIT 10
23	I/O	DATA11	AT DATA BUS BIT 11
26	I/O	DATA12	AT DATA BUS BIT 12
27	I/O	DATA13	AT DATA BUS BIT 13
28	I/O	DATA14	AT DATA BUS BIT 14
29	I/O	DATA15	AT DATA BUS BIT 15
76	I/O	EDATA0	PERIPHERAL DATA BUS BIT 0
77	I/O	EDATA1	PERIPHERAL DATA BUS BIT 1
78	I/O	EDATA2	PERIPHERAL DATA BUS BIT 2
79	I/O	EDATA3	PERIPHERAL DATA BUS BIT 3
80	I/O	EDATA4	PERIPHERAL DATA BUS BIT 4
81	I/O	EDATA5	PERIPHERAL DATA BUS BIT 5
82	I/O	EDATA6	PERIPHERAL DATA BUS BIT 6
83	I/O	EDATA7	PERIPHERAL DATA BUS BIT 7
6		VCC1	5V ± 5%
12		VCC2	5V ± 5%
18		VCC3	5V ± 5%
24		VCC4	5V ± 5%
32		VCC5	5V ± 5%
39		VCC6	5V ± 5%
54		VCC7	5V ± 5%
74		VCC8	5V ± 5%
7		GDD1	GROUND
13		GDD2	GROUND
19		GDD3	GROUND
25		GDD4	GROUND
31		GDD5	GROUND
33		GDD6	GROUND
40		GDD7	GROUND
55		GDD8	GROUND
73		GDD9	GROUND
75		GDD10	GROUND

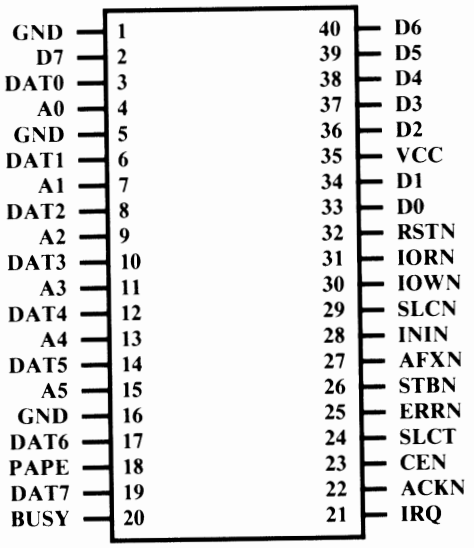
6) PVGA-1A VIDEO CNTRL 390302-01



PIN SYMBOL	*PIN TYPE*	*PLCC PINS*	*PGA PINS*	*DESCRIPTION*
RSET	IN	36	L1	Active high signal from external circuit during power up
MCLK	IN	76	G12	Up to 36 MHz for 120 ns DRAMS Up to 44.5 MHz for 100 ns DRAMS
VCLKO	IN	75	H13	25.175 MHz reference clock input
VCLK1	IN/OUT	74	H12	28.322 MHz clock input*
VCLK2	IN/OUT	73	H11	User defined external clock input*
A19	IN	28	G1	Address bus bit 19
A18	IN	27	G3	Address bus bit 18
A17	IN	24	F2	Address bus bit 17
A16	IN	23	F3	Address bus bit 16
A15	IN	22	E1	Address bus bit 15
DA15	IN/OUT	20	D1	Multiplexed data bit 15 with Monitor type input
DA14	IN/OUT	19	D2	Multiplexed data/address bus bit 14
DA13	IN/OUT	18	C1	Multiplexed data/address bus bit 13
DA12	IN/OUT	17	C2	Multiplexed data/address bus bit 12
DA11	IN/OUT	16	B1	Multiplexed data/address bus bit 11
DA10	IN/OUT	14	A1	Multiplexed data/address bus bit 10
DA9	IN/OUT	13	B3	Multiplexed data/address bus bit 9
DA8	IN/OUT	12	A2	Multiplexed data/address bus bit 8
DA7	IN/OUT	46	M5	Multiplexed data/address bus bit 7
DA6	IN/OUT	45	N4	Multiplexed data/address bus bit 6
DA5	IN/OUT	44	M4	Multiplexed data/address bus bit 5
DA4	IN/OUT	43	N3	Multiplexed data/address bus bit 4
DA3	IN/OUT	42	M3	Multiplexed data/address bus bit 3
DA2	IN/OUT	41	N2	Multiplexed data/address bus bit 2
DA1	IN/OUT	40	M2	Multiplexed data/address bus bit 1
DA0	IN/OUT	39	N1	Multiplexed data/address bus bit 0
EMEM	IN	21	E2	Enable display memory. Active high
EION	IN	33	J2	Programmable enable I/O. Active low or high
BHEN	IN	9	A4	Bus high byte enable. Active low
MRDN	IN	31	H3	Display memory read strobe. Active low
MWRN	IN	32	J1	Display memory write strobe. Active low
IORN	IN	29	H1	I/O read strobe. Active low
IOWN	IN	30	H2	I/O write strobe. Active low
MD15	IN/OUT	89	A13	Display memory data bit 15
MD14	IN/OUT	90	B12	Display memory data bit 14
MD13	IN/OUT	91	A12	Display memory data bit 13
MD12	IN/OUT	92	B11	Display memory data bit 12
MD11	IN/OUT	93	A11	Display memory data bit 11
MD10	IN/OUT	94	B10	Display memory data bit 10
MD9	IN/OUT	95	A10	Display memory data bit 9
MD8	IN/OUT	96	B9	Display memory data bit 8

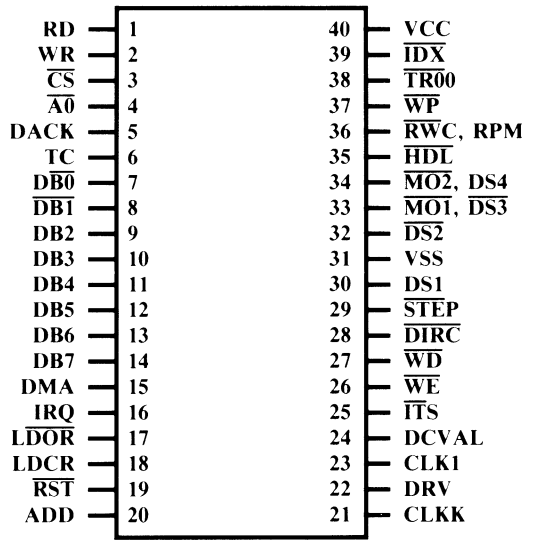
PIN SYMBOL	*PIN TYPE*	*PLCC PINS*	*PGA PINS*	*DESCRIPTION*
MD7	IN/OUT	97	A9	Display memory data or configuration bit 7 upon power up
MD6	IN/OUT	98	C8	Display memory data or configuration bit 6 upon power up
MD5	IN/OUT	99	B8	Display memory data or configuration bit 5 upon power up
MD4	IN/OUT	2	C7	Display memory data or configuration bit 4 upon power up
MD3	IN/OUT	3	A7	Display memory data or configuration bit 3 upon power up
MD2	IN/OUT	4	A6	Display memory data or configuration bit 2 upon power up
MD1	IN/OUT	5	B6	Display memory data or configuration bit 1 upon power up
MD0	IN/OUT	6	C6	Display memory data or configuration bit 0 upon power up
RAS10N	OUT	79	F13	Row address strobe bank 0 (Memory Maps 1 & 0). Active low
CAS10N	OUT	80	F12	Column address strobe bank 0. Active low
OE10N	OUT	81	F11	Output enable bank 0. Active low
WE1N	OUT	86	C13	Write enable bank 0 upper byte (Memory map 1). Active low
WE0N	OUT	85	D12	Write enable bank 0 lower byte (Memory map 0). Active low
RAS32N	OUT	82	E13	Row address strobe bank 1 (Memory maps 3 and 2). Active low
CAS32N	OUT	83	E12	Column address strobe bank 1. Active low
OE32N	OUT	84	D13	Output enable bank 1. Active low
WE3N	OUT	88	C12	Write enable bank 1 upper byte (Memory map 3). Active low
WE2N	OUT	87	B13	Write enable bank 1 lower byte (Memory map 2). Active low
MA8	OUT	63	M11	Display memory multiplexed RAS/CAS address bit 8
MA7	OUT	65	M12	Display memory multiplexed RAS/CAS address bit 7
MA6	OUT	66	M13	Display memory multiplexed RAS/CAS address bit 6
MA5	OUT	67	L12	Display memory multiplexed RAS/CAS address bit 5
MA2	OUT	70	K13	Display memory multiplexed RAS/CAS address bit 2
MA1	OUT	71	J12	Display memory multiplexed RAS/CAS address bit 1
MA0	OUT	72	J13	Display memory multiplexed RAS/CAS address bit 0
MA4	OUT	68	L13	Display memory multiplexed RAS/CAS address bit 4
MA3	OUT	69	K12	Display memory multiplexed RAS/CAS address bit 3
VID7	OUT	48	L6	Video color look up table address bit 7
VID6	OUT	49	M6	Video color look up table address bit 6
VID5	OUT	50	N6	Video color look up table address bit 5
VID4	OUT	53	N7	Video color look up table address bit 4
VID3	OUT	54	N8	Video color look up table address bit 3
VID2	OUT	55	M8	Video color look up table address bit 2
VID1	OUT	56	L8	Video color look up table address bit 1
VID0	OUT	57	N9	Video color look up table address bit 0
PLCK	OUT	59	N10	Pixel clock
BLNKN	OUT	62	N12	Color monitor blank pulse. Active low
HSYNC	OUT	60	M10	Color monitor horizontal synchronization pulse. Active high
VSYNC	OUT	61	N11	Color monitor vertical synchronization pulse. Active high
RPLTN	OUT	47	N5	Read color look up pallet. Active low
SKDBKN	OUT	10	B4	Card select feedback during memory or I/O access. Active low
WPLTN	OUT	58	M9	Write color look up pallet. Active low
REDY	OUT	34	K1	A tristate active high ready output to signal processor that memory access is available
IRQ	OUT	35	K2	Programmable processor interrupt request. Active low or high with tristate
DS16N	OUT	8	B5	Programmable enable 16 bit word transfer. Active low
EBROMN	OUT	7	A5	Enable BIOS ROM. Active low
EABUFN	OUT	11	A3	Enable processor address buffer. Active low
EDBUFN	OUT	38	L2	Enable processor data buffer. Active low
DIR	OUT	37	M1	Directional control for processor data bus. Bits 0 through 15 high for read cycles
VDD	---	25	F1	+5V DC
VDD	---	52	L7	+5V DC
VDD	---	78	G13	+5V DC
VDD	---	100	A8	+5V DC
VSS	---	1	B2	GND
VSS	---	15	G2	GND
VSS	---	26	M7	GND
VSS	---	51	N13	GND
VSS	---	64	G11	GND
VSS	---	77	B7	GND

7) PPC1 PARALLEL PRINTER CNTRL 318091-01



PIN	*CODE*	*DESCRIPTION*
1	GND	Ground
2	D7	Data Bit 7 In
3	DAT0	Data Bit 0 Out
4	A0	Address Line 0
5	GND	Ground
6	DAT1	Data Bit 1 Out
7	A1	Address Line 1
8	DAT2	Data Bit 2 Out
9	A2	Address Line 2
10	DAT3	Data Bit 3 Out
11	A3	Address Line 3
12	DAT4	Data Bit 4 Out
13	A4	Address Line 4
14	DAT5	Data Bit 5 Out
15	A5	Address Line 5
16	GND	Ground
17	DAT6	Data Bit 6 Out
18	PAPE	Paper Out
19	DAT7	Data Bit 7 Out
20	BUSY	Printer busy
21	IRQ	Interrupt #7
22	$\overline{\text{ACKN}}$	Acknowledge
23	$\overline{\text{CEN}}$	Chip Select
24	SLCT	Printer Select
25	$\overline{\text{ERRN}}$	Error
26	$\overline{\text{STBN}}$	Strobe
27	$\overline{\text{AFXN}}$	Autofeed
28	$\overline{\text{ININ}}$	Initial Reset
29	$\overline{\text{SLCN}}$	Select From Printer
30	$\overline{\text{IOWN}}$	I/O Write
31	$\overline{\text{IORN}}$	I/O Read
32	$\overline{\text{RSTN}}$	Reset
33	DO	Data Bit 0 In
34	D1	Data Bit 1 In
35	VCC	+5V
36	D2	Data Bit 2 In
37	D3	Data Bit 3 In
38	D4	Data Bit 4 In
39	D5	Data Bit 5 In
40	D6	Data Bit 6 In

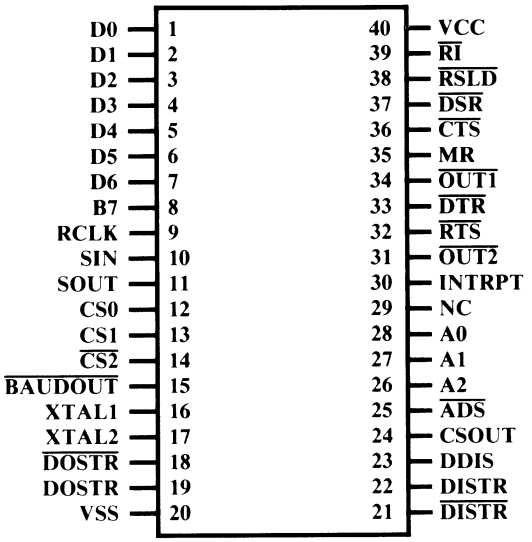
8) WD37C65 FDC 390304-03



D/P PIN NUMBER	*MNEMONIC*	*SIGNAL NAME*	*I/O*	*FUNCTION*
1/1	RD	READ	I	Control signal for transfer of data or status onto the data bus by the WD37C65.
2/2	WR	WRITE	I	Control signal for latching data from the bus into the WD37C65 Buffer Register.
3/3	CS	CHIP SELECT	I	Selected when 0 (low) allowing RD or WR operation from the Host.
4/4	A0	ADDRESS LINE	I	Address line selecting data (-1) or status (-0) information. (A0 - logic 0 during WR is illegal).
5/5	DACK	DMA ACKNOWLEDGE	I	Used by the DMA controller to transfer data from the WD37C65 onto the bus. Logical equivalent to CS and A0-1. In Special or PC/AT Mode, this signal is qualified by DMAEN from the Operations Register.
6/6	TC	TERMINAL COUNT	I	This signal indicates to WD37C65 that data transfer is complete. If DMA operational mode is selected for command execution, TC will be qualified by DACK, but not in the programmed I/O execution. In PC/AT or Special Mode, qualification by DACK requires the Operations Register signal DMAEN to be logically true. Note also that in PC/AT Mode, TC will be qualified by DACK, whether in DMA or non-DMA Host operation. Programmed I/O in PC/AT Mode will cause an abnormal termination error at the completion of a command.
7-14	DBO thru	DATA BUS 0 thru	I/O	8-Bit, bi-directional, tri-state, data bus. D0 is the least significant bit (LSB). D7 is the most significant bit (MSB).
7-14	DB7	DATA BUS 7		
15/15	DMA	DIRECT MEMORY ACCESS	O	DMA request for byte transfers of data. In Special or PC/AT mode, this pin is tri-stated, enabled by the DMAEN signal from the Operation Register. This pin is driven in the Base Mode.
16/16	IRQ	INTERRUPT	O	Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode). Normally driven in base mode. In Special or PC/AT Mode, this pin is tri-stated, enabled by the DMAEN signal from the Operations Register.
17				Not connected in the 44 Pin PLCC.
17/18	LDOR	LOAD OPERATIONS REGISTER	I	Address decode which enables the loading of the Operations Register. Internally gated with WR creates the strobe which latches the data bus into the Operations Register.
18/19	LDCR	LOAD CONTROL REGISTER	I	Address decode which enables loading of the Control Register. Internally gated with WR creates the strobe which latches the two LSBs from the data bus into the Control Register.
19/20	RST	RESET	I	Resets controller, placing microsequencer in idle. Resets device outputs. Puts device in Base Mode, not PC/AT or Special Mode.
20/21	RDD	READ DISK DATA	I	This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
21/	CLK2	CLOCK2	I	TTL level clock input used for non-standard data rates; is 9.6MHz for 300 Kb/s, and can only be selected from the Control Register.
/22	XT2	XTAL2	O	XTAL oscillator drive output for 44 Pin PLCC (See Figure 6). Should be left floating if TTL inputs used at pin 23.
/23	XT2	XTAL2	I	XTAL oscillator input used for non-standard data rates. It may be driven with TTL level signal.
22/24	DRV	DRIVE TYPE	I	Drive type input indicates to the device that a two-speed spindle motor is used if logic is 0. In that case, the second clock input will never be selected and must be grounded.
23/	CLK1	CLOCK1	I	TTL level clock input is used to generate all internal timings for standard data rates. Frequency must be 16MHz ± 0.1%, and may have 40/60 or 60/40 duty cycle.
/25	XT1	XTAL1	O	XTAL oscillator drive output for 44 Pin PLCC (See Figure 6). Should be left floating if TTL inputs used at pin 26.
/26	XT1	XTAL1	I	XTAL oscillator input requiring 16MHz crystal. This oscillator is used for all standard data rates, and may be driven with a TTL level signal.
24/27	PCVAL	PRECOMPENSATION VALUE	I	PRECOMPENSATION VALUE select input. This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1 - 125ns, Logic 0 - 187 ns.

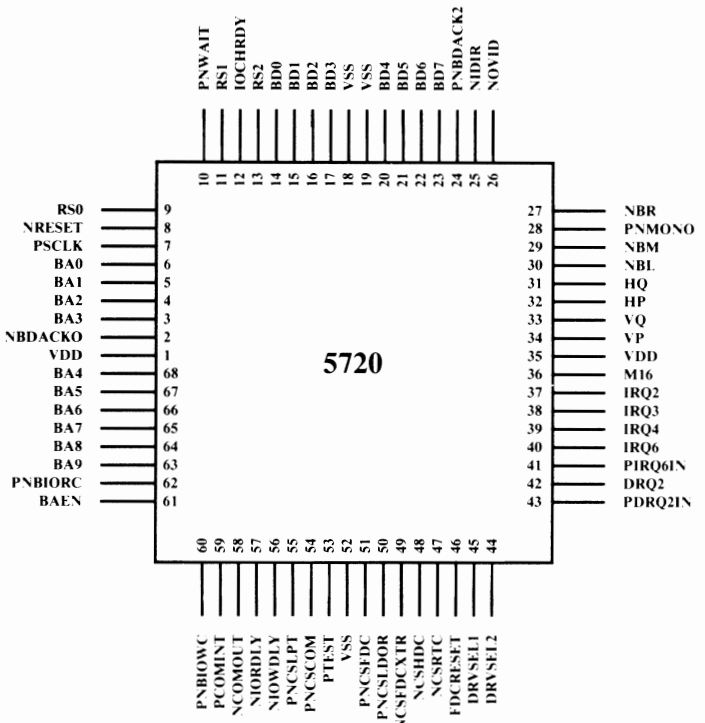
D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
25/28	$\overline{HS}$	$\overline{HEAD\ SELECT}$	O	High current driver (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic 1 - side 0. Logic 0 - side 1.
26/29	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	O	This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.
27/30	$\overline{WD}$	$\overline{WRITE\ DATA}$	O	This HCD output is $\overline{WRITE\ DATA}$. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
28/31	$\overline{DIRC}$	$\overline{DIRECTION}$	O	This HCD output determines the direction of the head stepper motor. Logic 1 - outward motion. Logic 0 - inward motion.
29/32	$\overline{STEP}$	$\overline{STEP\ PULSE}$	O	This HCD output issues an active low pulse for each track to track movement of the head.
30/33	$\overline{DS1}$	$\overline{DRIVE\ SELECT\ 1}$	O	This HCD output, when active low is $\overline{DRIVE\ SELECT\ 1}$ in PC/AT Mode, enabling the interface in this disk drive. This signal comes from the Operations Register. In Base, or Special Mode, this output is #1 of the four decoded Unit Selects, as specified in the device command syntax.
31/34	VSS	GROUND		Ground.
32/35	$\overline{DS2}$	$\overline{DRIVE\ SELECT\ 2}$	O	This HCD output when active low is $\overline{DRIVE\ SELECT\ 2}$, in PC/AT Mode, enabling the interface in this disk drive. This signal comes from the Operations Register. in Base or the Special Mode, this output is #2 of the four decoded Unit Selects as specified in the device command syntax.
33/36	$\overline{MO1}$, $\overline{DS3}$	$\overline{MOTOR\ ON\ 1}$, $\overline{DRIVE\ SELECT\ 3}$	O	This HCD output when active low is MOTOR ON enable for disk drive #1, in PC/AT Mode. This signal comes from the Operations Register. In the Base or Special Mode, this output is #3 of the four decoded Unit Selects as specified in the device command syntax.
34/37	$\overline{MO2}$, $\overline{DS4}$	$\overline{MOTOR\ ON\ 2}$, $\overline{DRIVE\ SELECT\ 4}$	O	This HCD output when active low is MOTOR ON enable for disk drive #2, in PC/AT mode. This signal comes from the Operations Register. In the Base or Special Mode, this output is #4 of the four decoded Unit Selects as specified in the device command syntax.
35/38	$\overline{HDL}$	$\overline{HEAD\ LOADED}$	O	This HDC output when active low causes the head to be loaded against the media in the selected drive.
36/39	$\overline{RWC}$, $\overline{RPM}$	$\overline{REDUCED\ WRITE\ CURRENT}$ $\overline{REVOLUTIONS\ PER\ MINUTE}$	O	This HCD output when active low causes a $\overline{REDUCED\ WRITE\ CURRENT}$ when bit density is increased toward the inner tracks, becoming active when tracks greater than 28 are accessed. This condition is valid for Base or Special Mode, and is indicative of when write precompensation is necessary. In the PC/AT mode, (on two-speed disk drives) this signal will be active when 250 MFM or 125 FM data rate is selected.
40				Not connected in the 44 Pin PLCC.
37/41	$\overline{WP}$	$\overline{WRITE\ PROTECTED}$	I	This Schmitt Trigger (ST) input senses status from the disk drive indicating active low, when a diskette is $\overline{WRITE\ PROTECTED}$.
38/42	$\overline{TR00}$	$\overline{TRACK\ 00}$	I	This ST input senses status from disk drive indicating active low, when the head is positioned over the outermost track, $\overline{TRACK\ 00}$.
39/43	$\overline{IDX}$	$\overline{INDEX}$	I	This ST input senses status from the disk drive indicating active low, when the head is positioned over the beginning of a track marked by an index hole.
40/44	VCC	+5VDC		Input power supply.

9) 8250 SERIAL INTERFACE 380205-01



PIN NUMBER	*PIN NAME*	*SYMBOL*	*FUNCTION*
1-8	DATA BUS	D0-D7	3-state input/output lines. Bi-directional communication lines between WD8250 and Data Bus. All assembled data TX and RX, control words, and status information are transferred via the D0-D7 data bus.
9	RECEIVE CLK	RCLK	This input is the 16X baud rate clock for the receiver section of the chip (may be tied to BAUDOUT pin 15).
10	SERIAL INPUT	SIN	Received Serial Data In from the communications link (Peripheral device, modem or data set).
11	SERIAL OUTPUT	SOUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12	CHIP SELECT	CS0	When CS0 and CS1 are high, and $\overline{CS2}$ is low, chip is selected. Selection is complete when the address strobe $\overline{ADS}$ latches
13	CHIP SELECT	CS1	the chip select signals.
14	CHIP SELECT	$\overline{CS2}$	
15	BAUDOUT	$\overline{BAUDOUT}$	16X clock signal for the transmitter section of the WD8250. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The BAUDOUT signal may be used to clock the receiver by tying to (pin 9) RCLK.
16	EXTERNAL CLOCK IN	XTAL 1	These pins connect the crystal or signal clock to the WD8250 baud rate divisor circuit. See Fig. 3 and Fig. 4 for circuit
17	EXTERNAL CLOCK OUT	XTAL 2	connection diagrams.
18	DATA OUT STROBE	$\overline{DOSTR}$	When the chip has been selected, a low $\overline{DOSTR}$ or high DOSTR will latch data into the selected WD8250 register (a CPU
19	DATA OUT STROBE	DOSTR	write). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DOSTR}$ — high or DOSTR — low.
20	GROUND	VSS	System signal ground.
21	DATA IN STROBE	$\overline{DISTR}$	When chip has been selected, a low $\overline{DISTR}$ or high DISTR will allow a read of the selected WD8250 register (a CPU read).
22	DATA IN STROBE	DISTR	Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DISTR}$ — high or DISTR — low.
23	DRIVER DISABLE	DDIS	Output goes low whenever data is being read from the WD8250. Can be used to reverse data direction of external transceiver.
24	CHIP SELECT OUT	CSOUT	Output goes high when chip is selected. No data transfer can be initiated until CSOUT is high.
25	ADDRESS STROBE	$\overline{ADS}$	When low, provides latching for Register Select (A0, A1, A2,) and Chip Select (CS0, CS1, $\overline{CS2}$) NOTE: The rising edge (↑) of the $\overline{ADS}$ signal is required when the Register Select (A0, A1, A2) and the Chip Select (CS0, CS1, $\overline{CS2}$) signals are not stable for the duration of a read or write operation. If not required, the $\overline{ADS}$ input can be tied permanently low.
26	REGISTER SELECT A2	A2	These three inputs are used to select a WD8250 internal register during a data read or write. See Table below.
27	REGISTER SELECT A1	A1	
28	REGISTER SELECT A0	A0	
29	NO CONNECT	NC	No Connect
30	INTERRUPT	INTRPT	Output goes high whenever an enabled interrupt is pending.
31	OUTPUT 2	$\overline{OUT2}$	User-designated output that can be programmed by Bit 3 of the modem control register = 1, causes $\overline{OUT2}$ to go low.
32	REQUEST TO SEND	$\overline{RTS}$	Output when low informs the modem or data set that the WD8250 is ready to transmit data. See Modem Control Register.
33	DATA TERMINAL READY	$\overline{DTR}$	Output when low informs the modem or data set that the WD8250 is ready to communicate.
34	OUTPUT 1	$\overline{OUT1}$	User designated output can be programmed by Bit 2 of Modem Control Register = 1 causes $\overline{OUT1}$ to go low.
35	MASTER RESET	MR	When high clears the registers to states as indicated in Table 1.
36	CLEAR TO SEND	$\overline{CTS}$	Input from DCE indicating remote device is ready to transmit. See Modem Control Register.
37	DATA SET READY	$\overline{DSR}$	Input from DCE used to indicate the status of the local data set. See Modem Control Register.
38	RECEIVED LINE SIGNAL DETECT	$\overline{RSLD}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Control Register.
39	RING INDICATOR	$\overline{RI}$	Input, when low, indicates that a ringing signal is being received by the modem or data set. See Modem Control Register.
40	+5V	VCC	+5 Volt Supply.

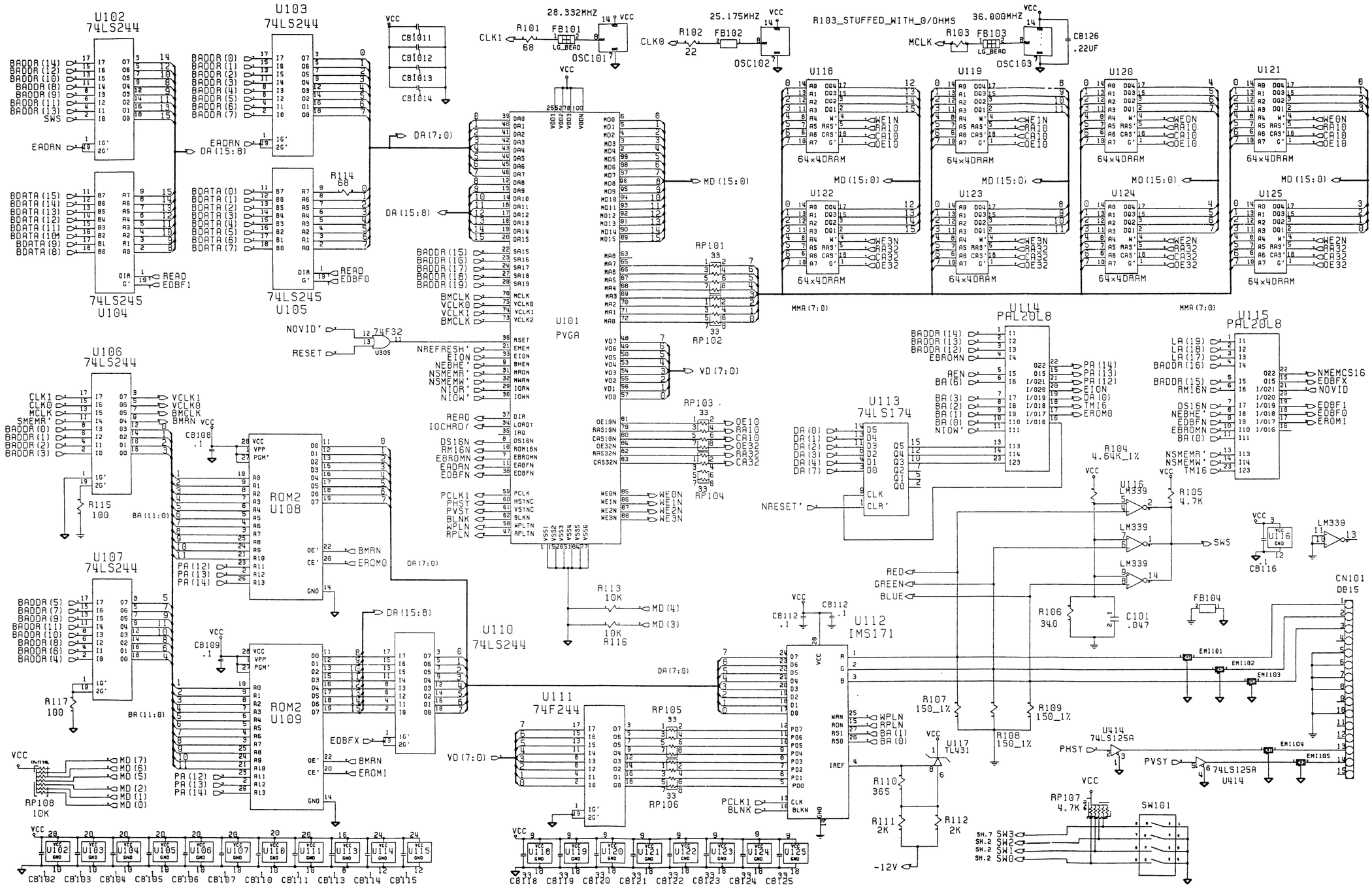
10) 5720 MOUSE CONTROL 318087-01



PIN	*SIGNAL NAME*	*PAD TYPE*
1	VDD	
2	NBDACK0	INP
3	BA3	INP
4	BA2	INP
5	BA1	INP
6	BA0	INP
7	PSCLK	INP
8	NRESET	INP Schmitt trigger
9	RS0	INP
10	PNWAIT	INP with pullup
11	RS1	INP
12	IOCHRDY	OUT open drain
13	RS2	INP
14	BD0	I/O with pullup
15	BD1	I/O with pullup
16	BD2	I/O with pullup
17	BD3	I/O with pullup
18	VSS	
19	VSS	
20	BD4	I/O with pullup
21	BD5	I/O with pullup
22	BD6	I/O with pullup
23	BD7	I/O with pullup
24	PNBDACK2	INP
25	NIDIR	OUT
26	NOVID	OUT open drain with pullup
27	NBR	INP Schmitt trigger with pullup
28	PNMONO	INP with pullup
29	NBM	INP Schmitt trigger with pullup
30	NBL	INP Schmitt trigger with pullup
31	HQ	INP Schmitt trigger with pullup
31	HP	INP Schmitt trigger with pullup
33	VQ	INP Schmitt trigger with pullup
34	VP	INP Schmitt trigger with pullup
35	VDD	
36	M16	INP Schmitt trigger
37	IRQ2	OUT tristate
38	IRQ3	OUT tristate
39	IRQ4	OUT tristate
40	IRQ6	OUT tristate
41	PIRQ6IN	INP
42	DRQ2	OUT tristate
43	PDRQ2IN	INP
44	DVRSEL2	OUT
45	DRVSEL1	OUT
46	FDCRESET	OUT
47	NCSRTC	OUT
48	NCSHDC	OUT
49	NCSFDCXTR	OUT
50	PNCSLDOR	OUT
51	PNCSFDC	OUT
52	VSS	
53	PTEST	INP
54	PNCSCOM	OUT
55	PNCSLPT	OUT
56	NIOWDLY	OUT
57	NIORDLY	OUT
58	NCOMOUT	INP Schmitt trigger
59	PCOMINT	INP Schmitt trigger
60	PNBIOWC	INP
61	BAEN	INP
62	PNBIORC	INP
63	BA9	INP
64	BA8	INP
65	BA7	INP
66	BA6	INP
67	BA5	INP
68	BA4	INP

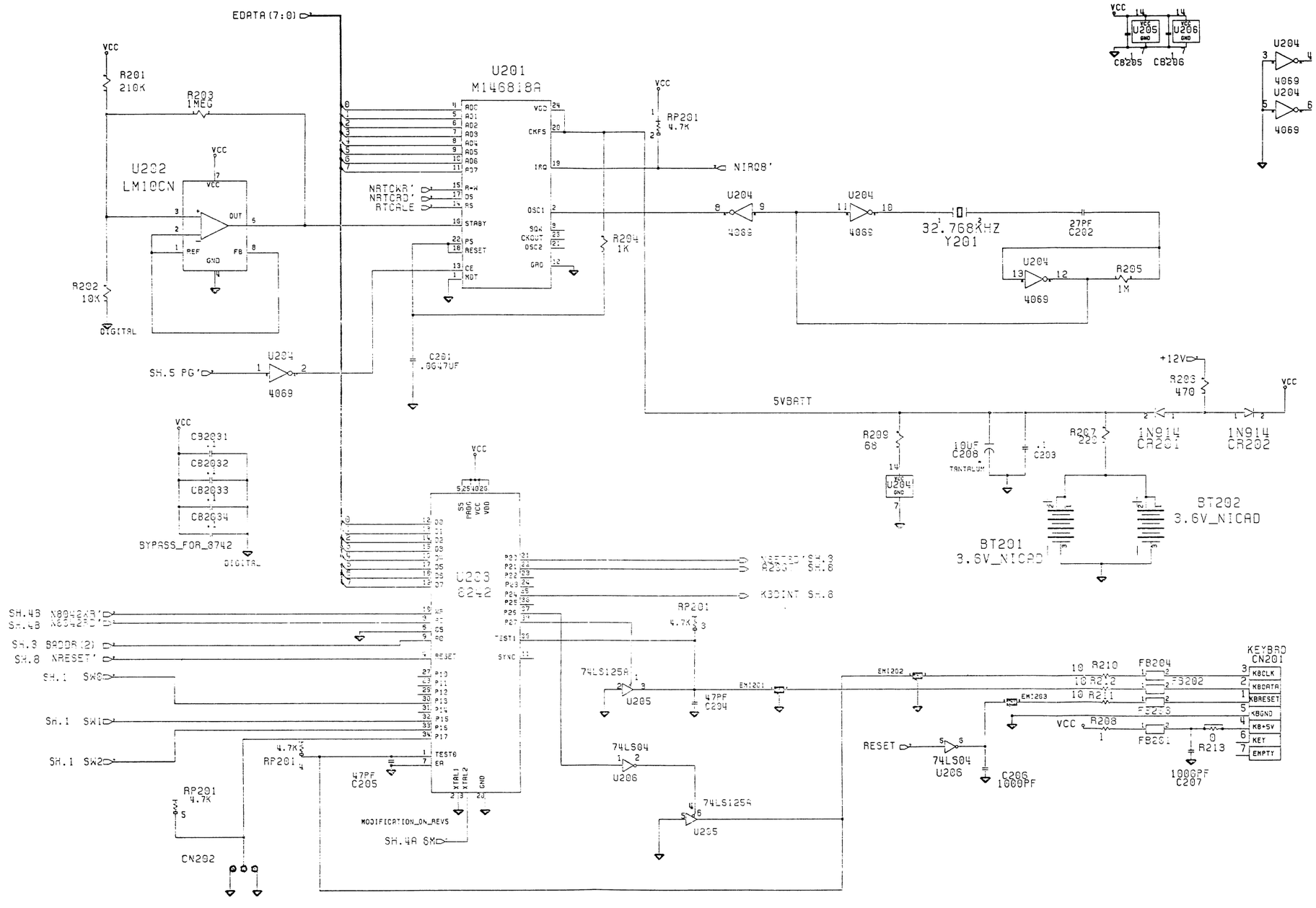
Schematic #313056, Rev. C

Sheet 1 of 12



Schematic #313056, Rev. C

Sheet 2 of 12



Schematic #313056, Rev. C

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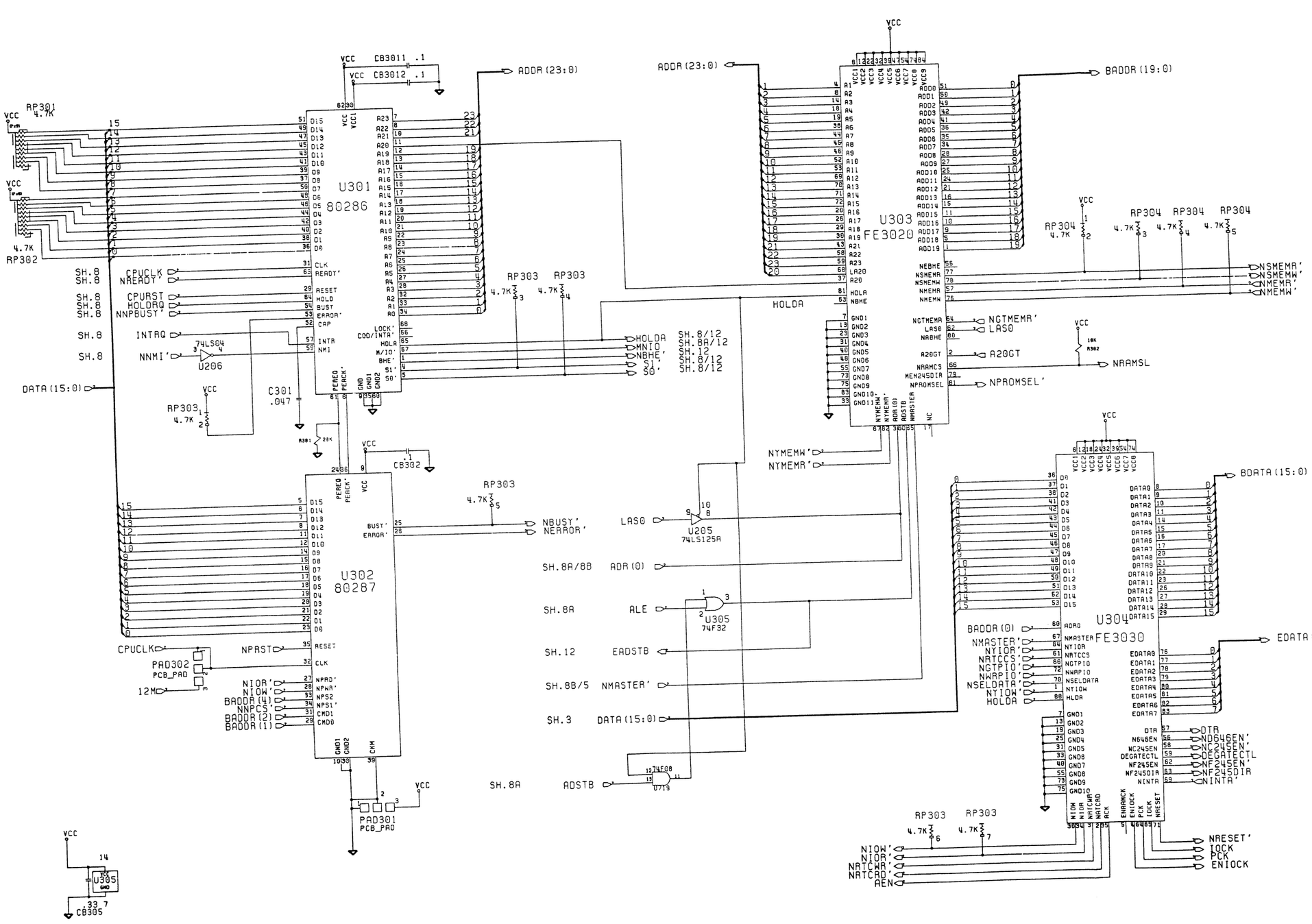
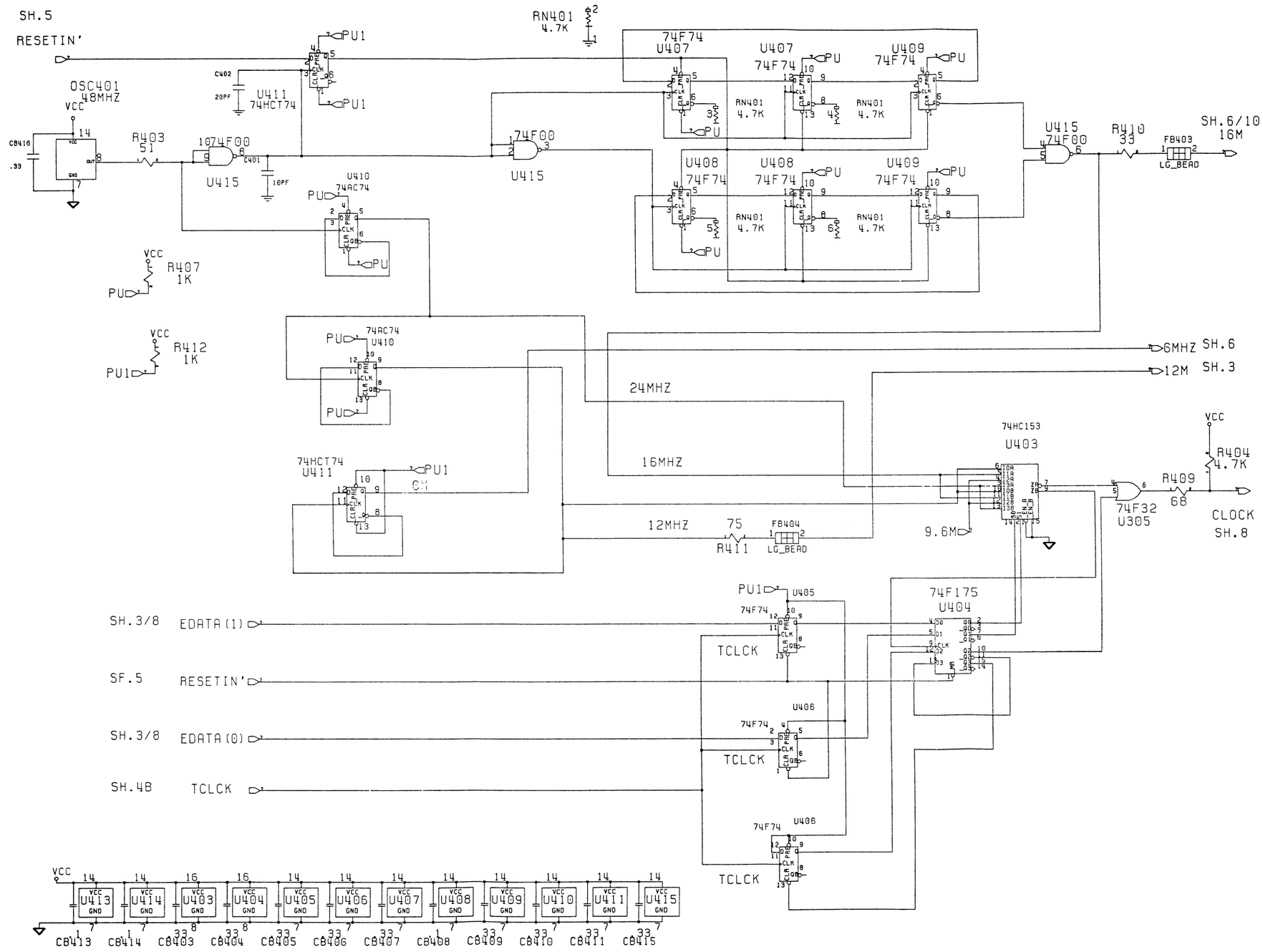


Schematic #313056, Rev. C
Sheet 4A of 12



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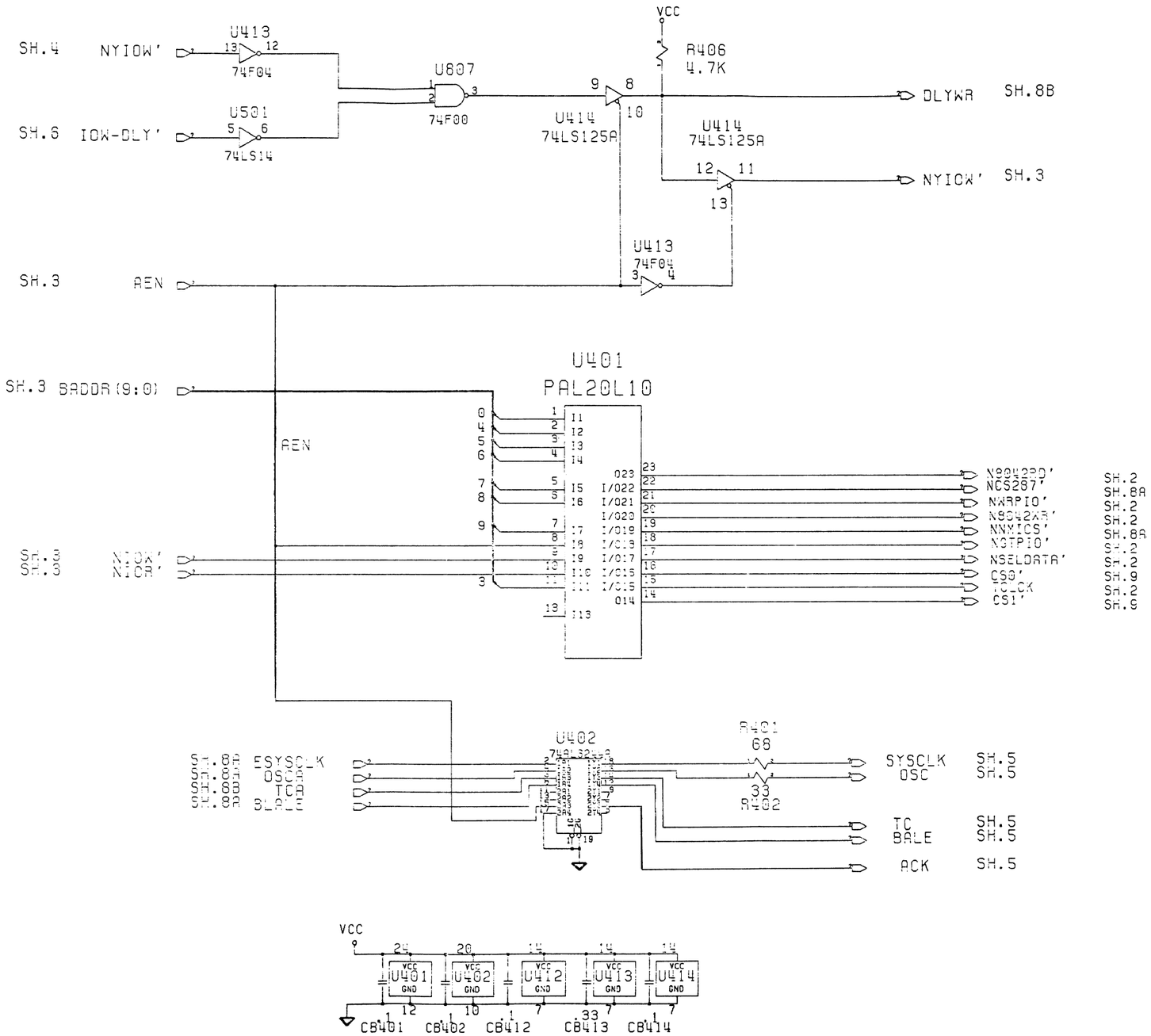
Sheet 4B of 12



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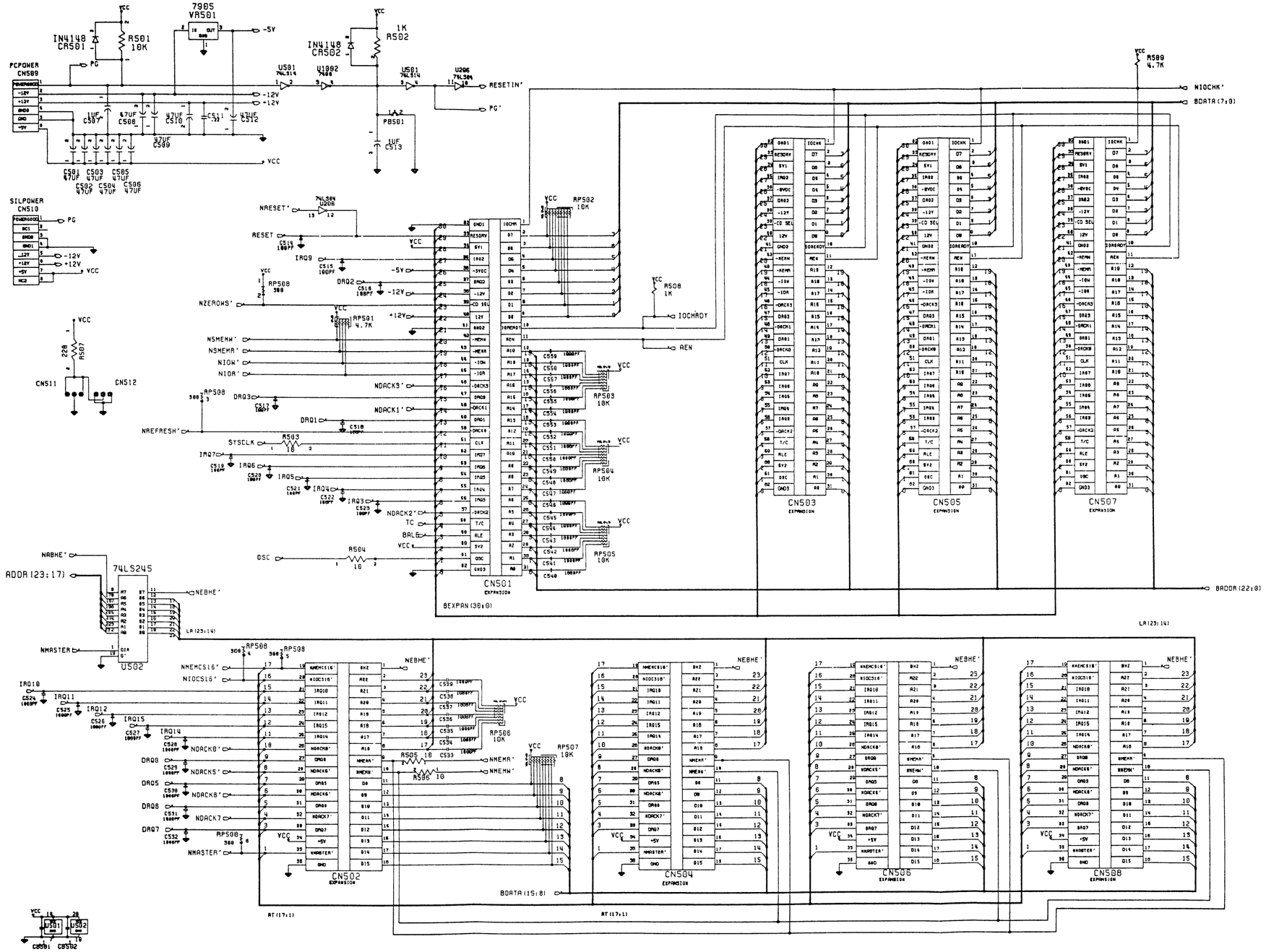
Sheet 5 of 12



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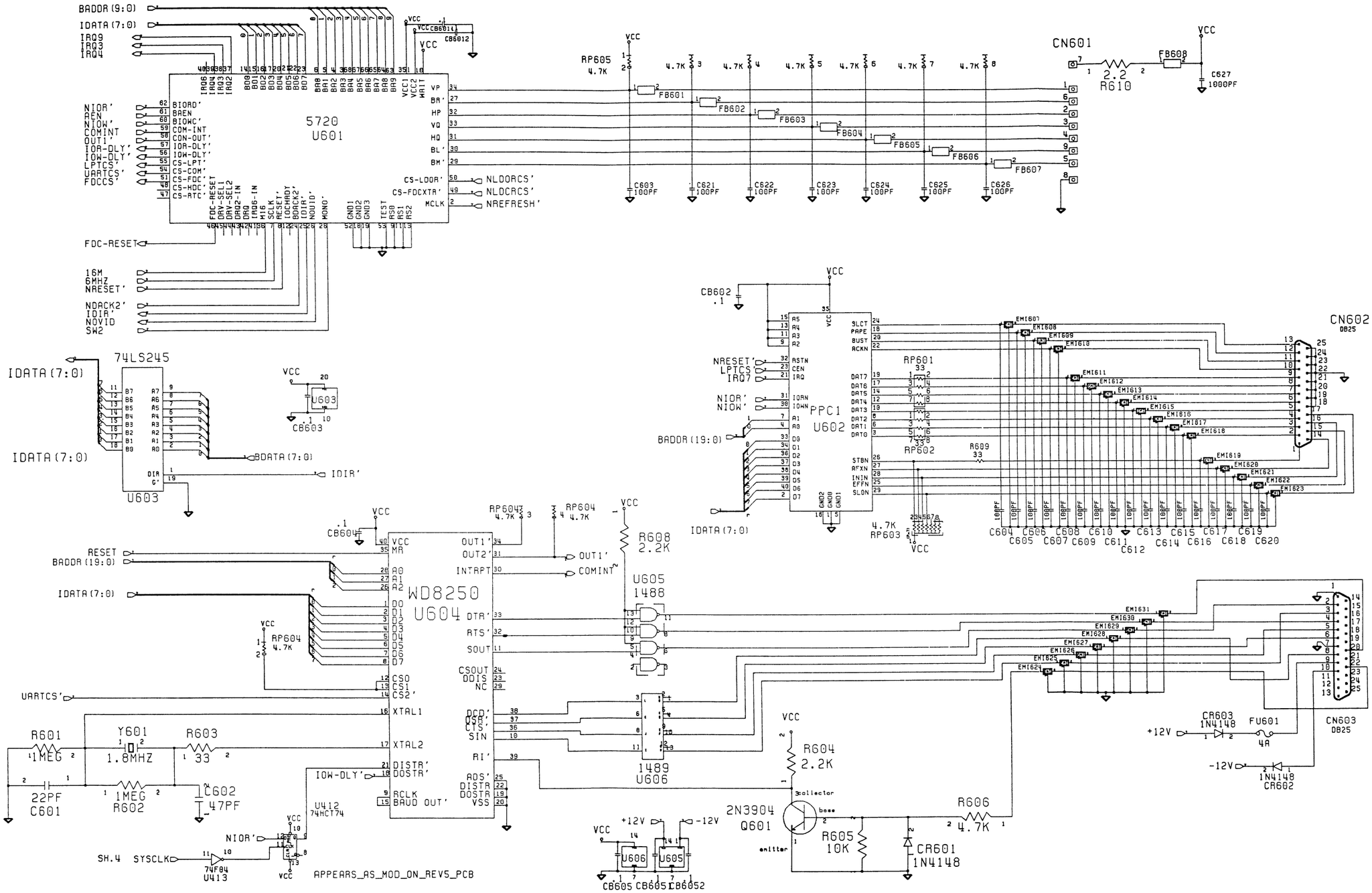
Sheet 6 of 12



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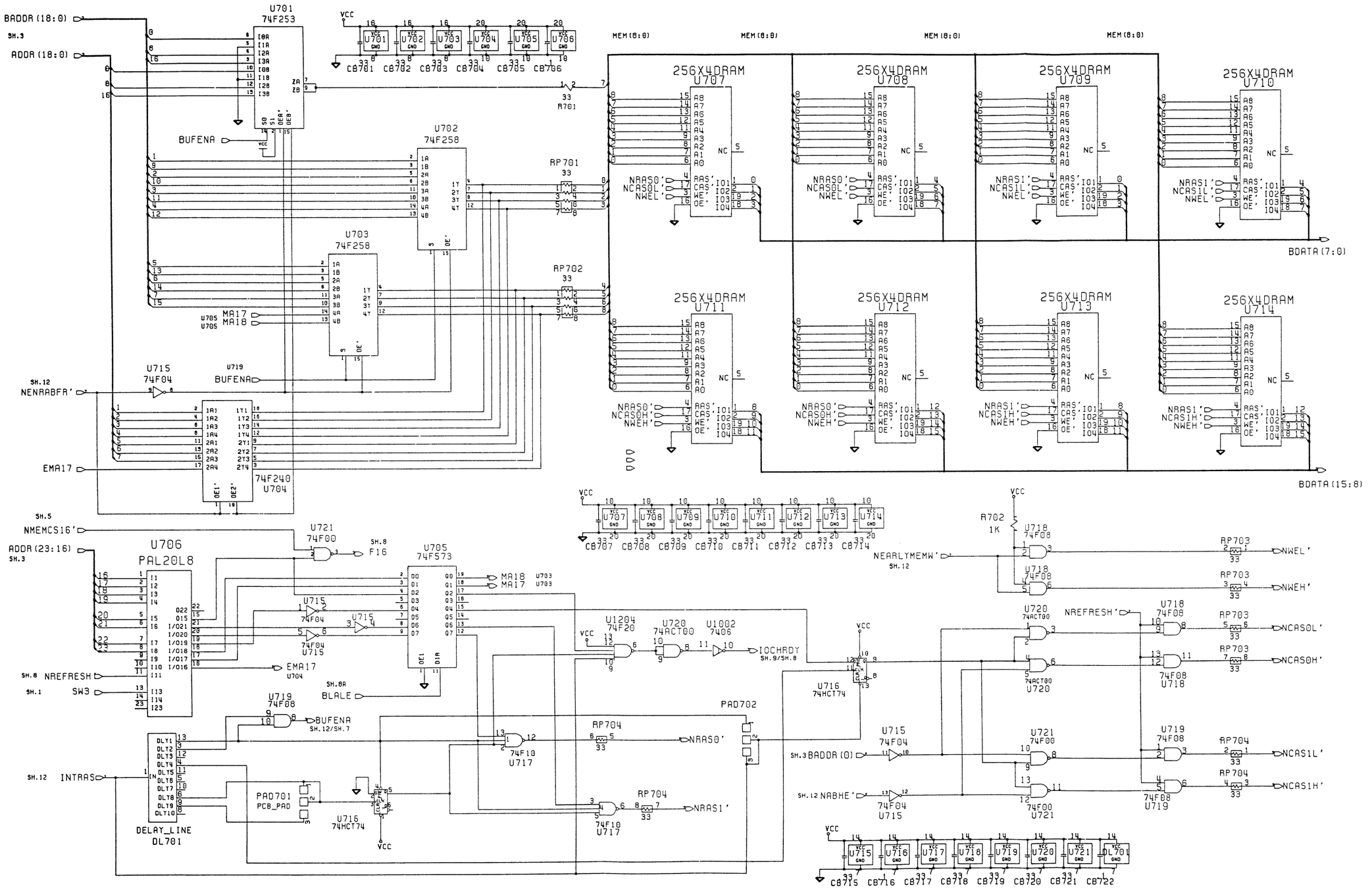
Sheet 7 of 12



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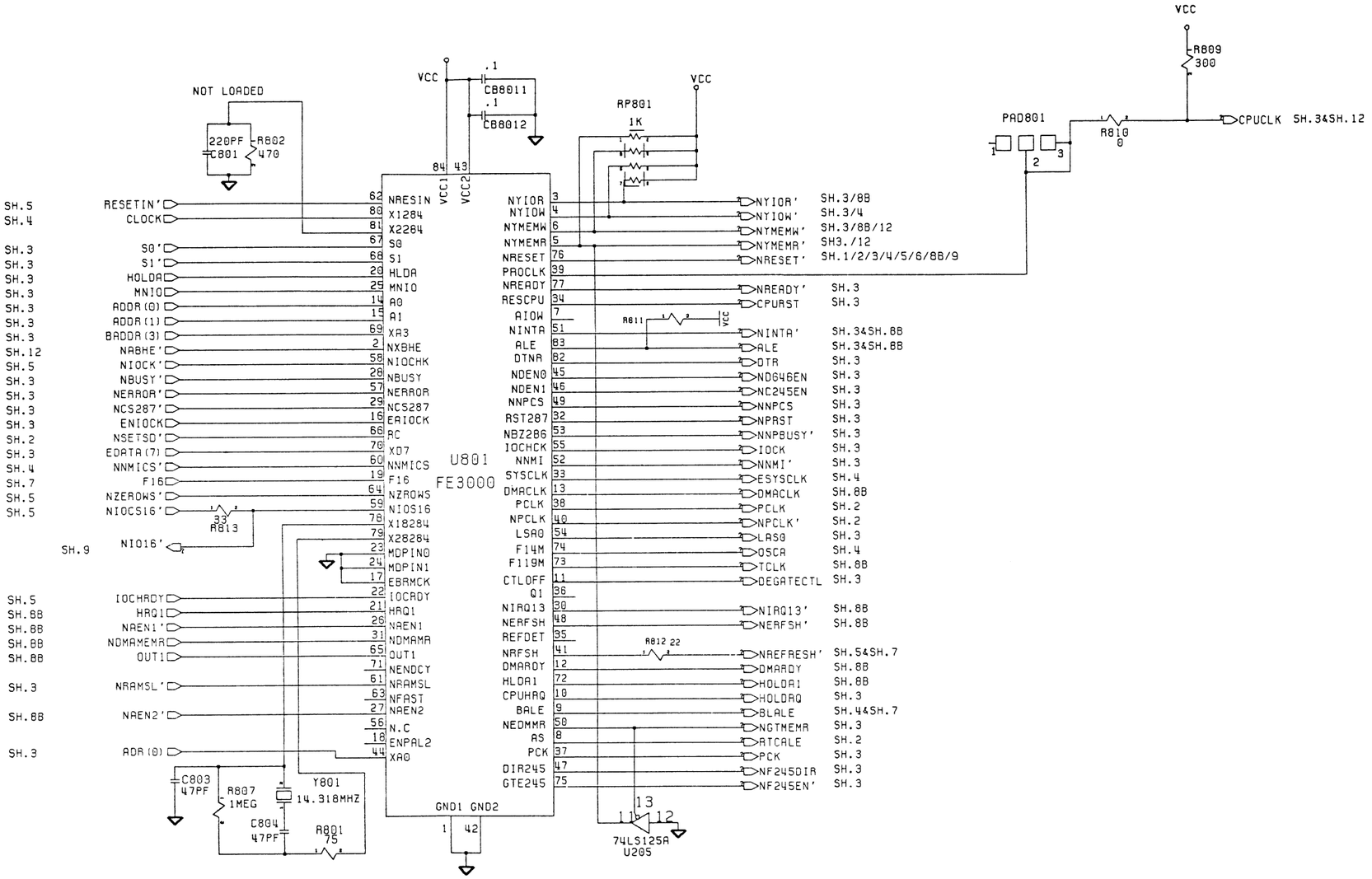

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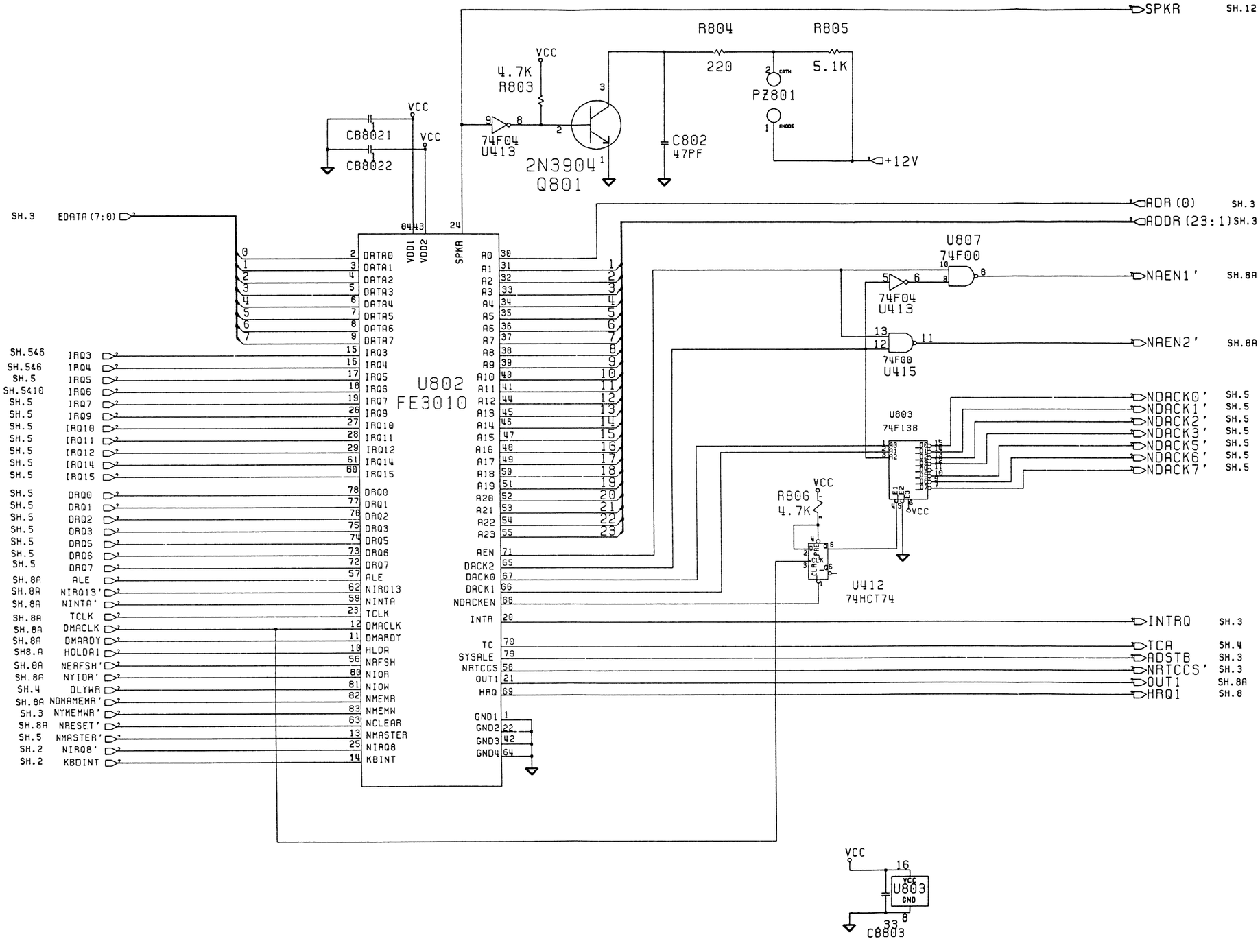
Sheet 8B of 12



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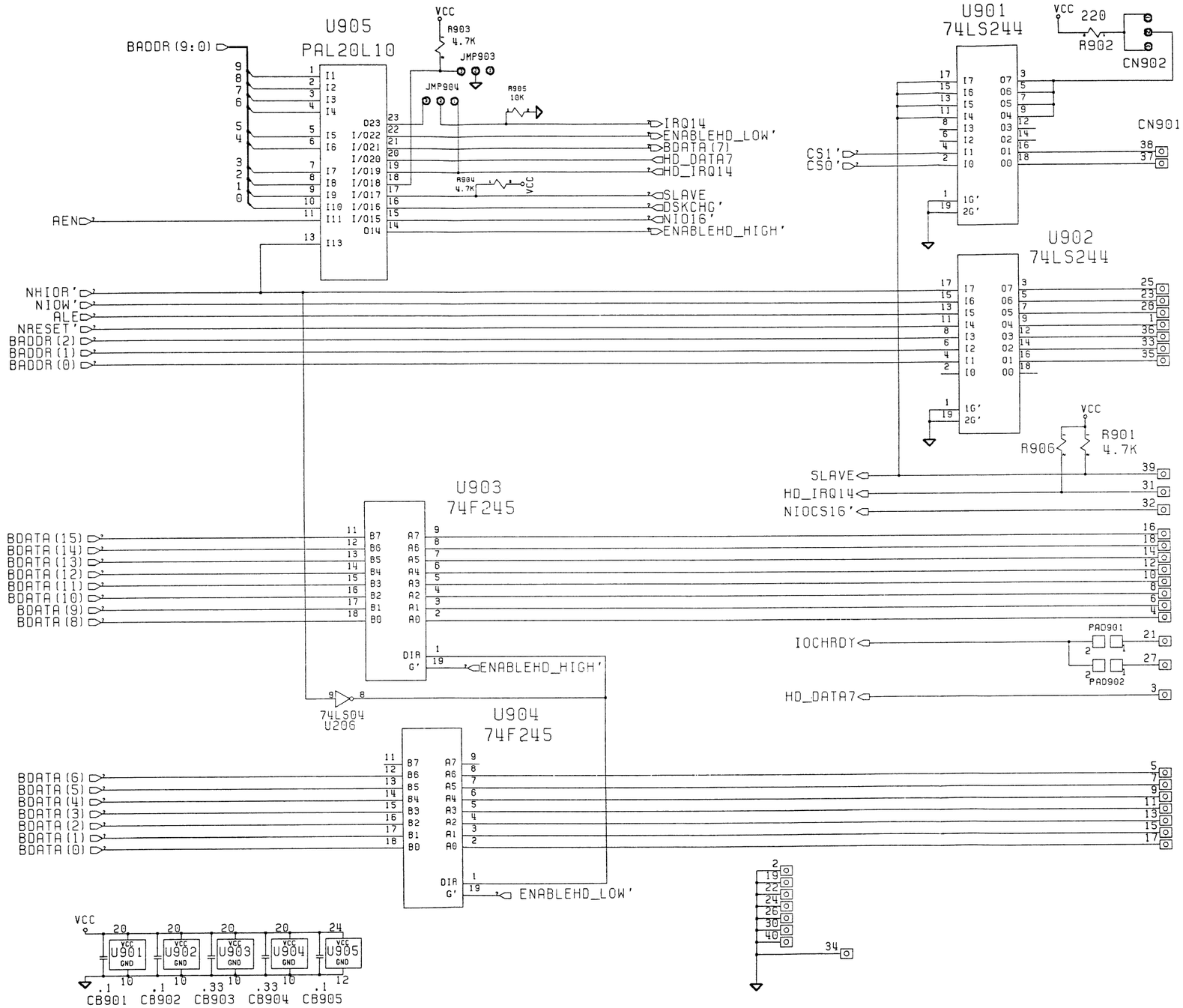
Sheet 9 of 12



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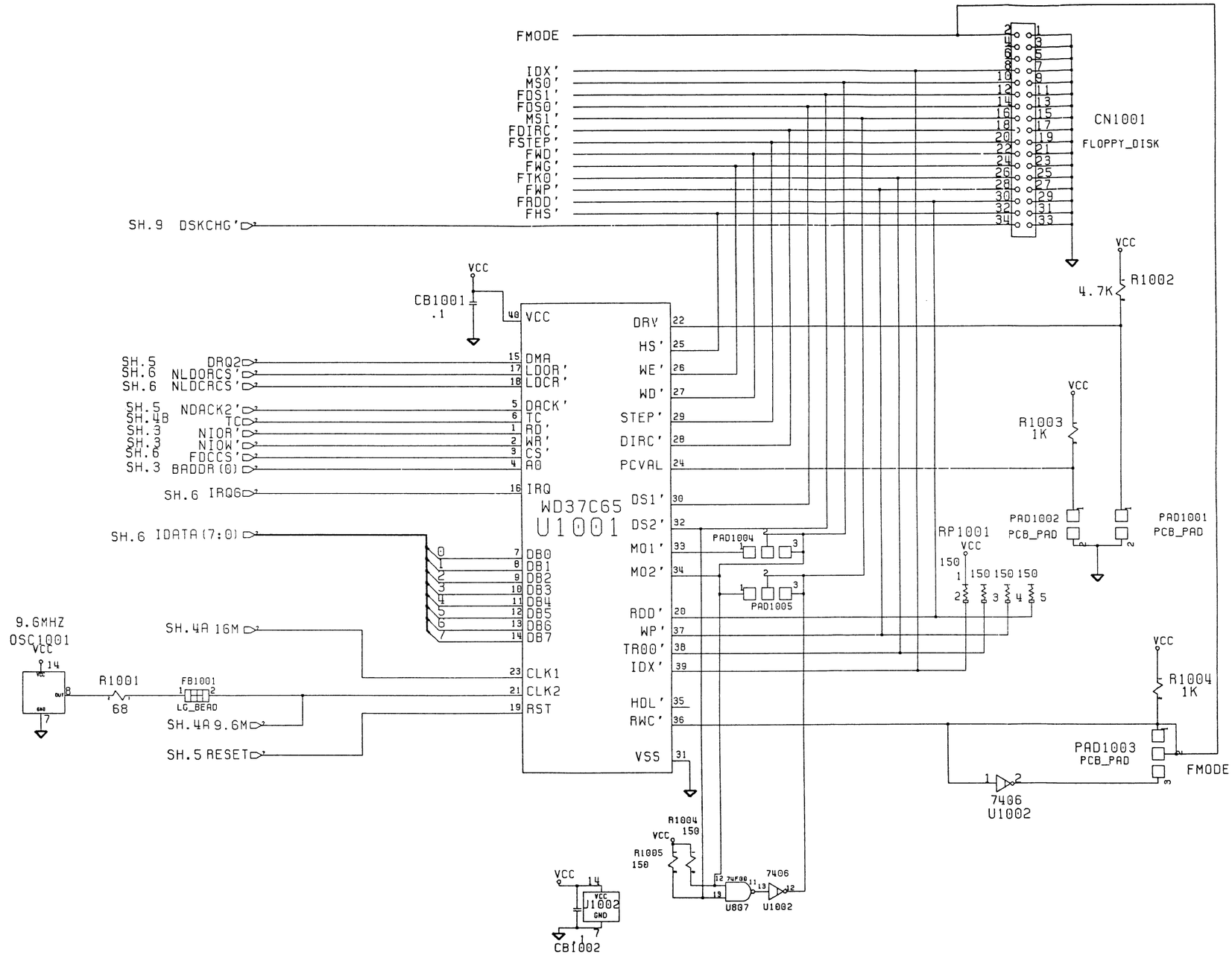
Sheet 10 of 12



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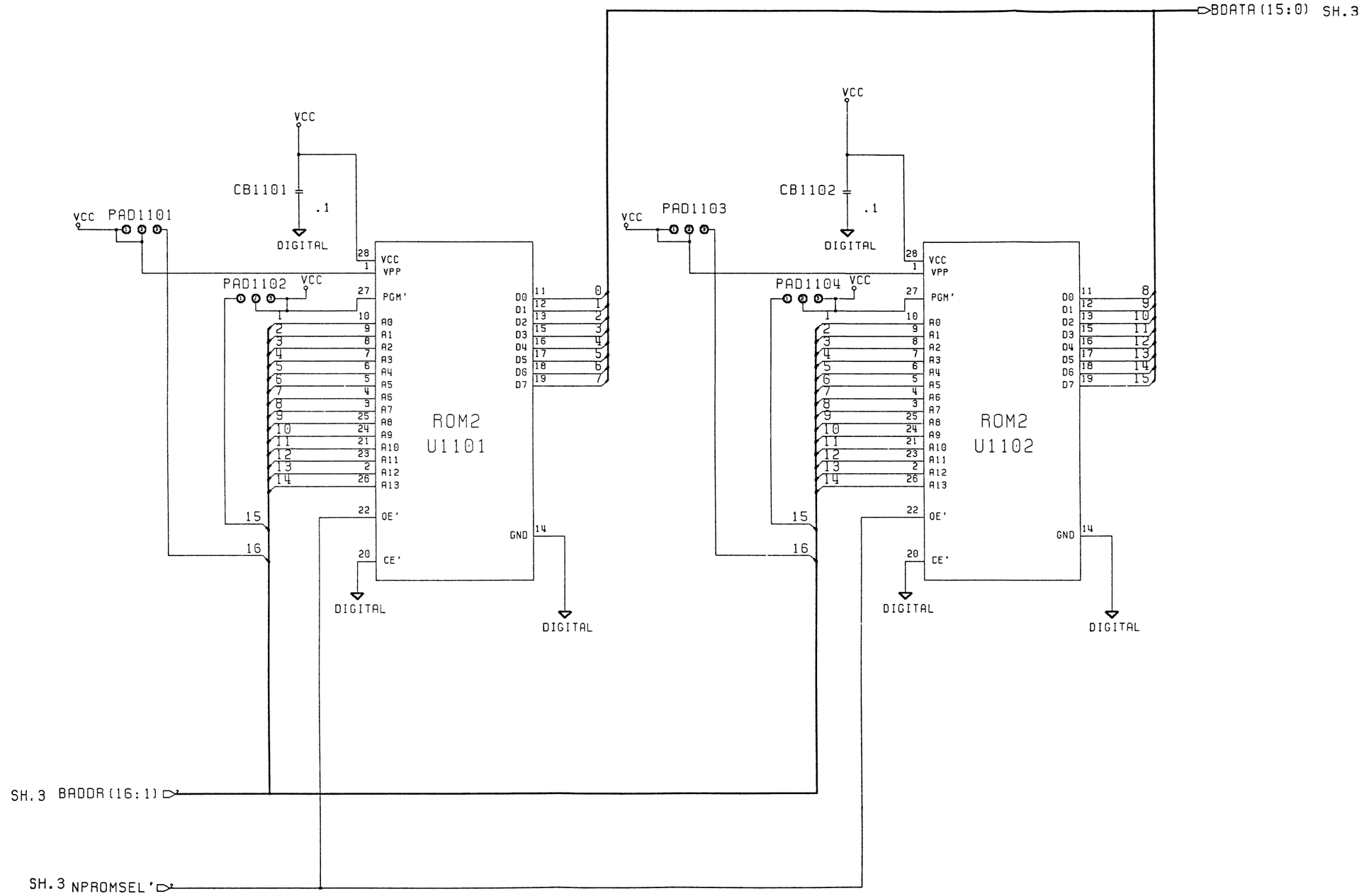

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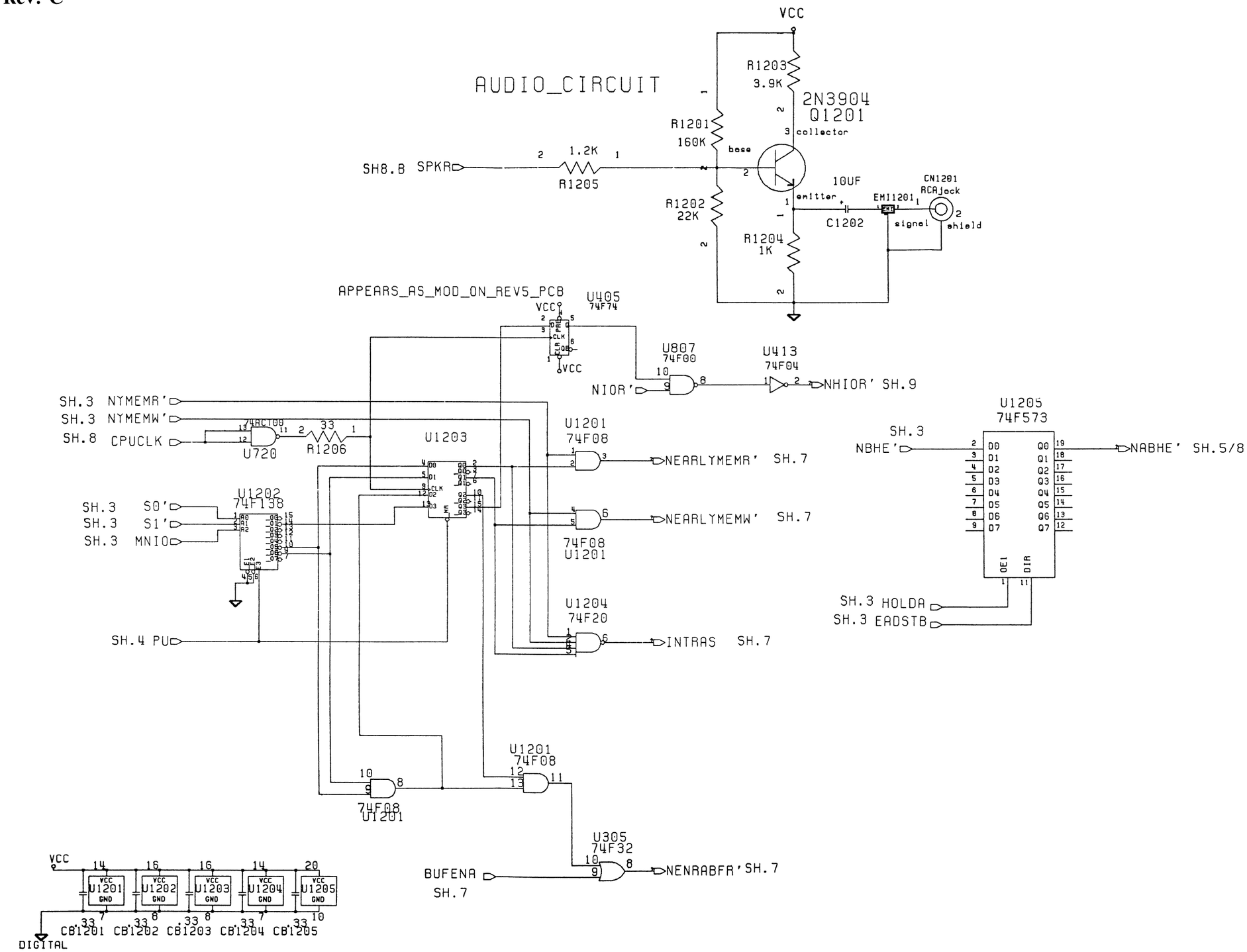


APPENDIX A

POWER SUPPLY SECTION

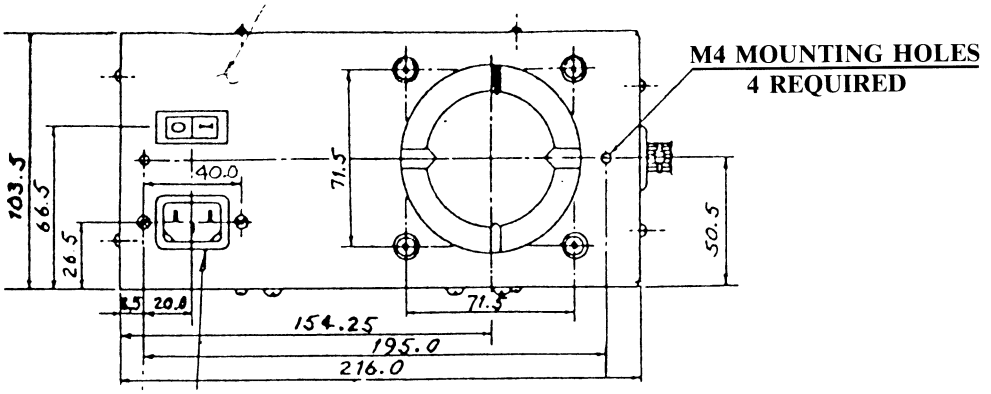
- **PC40-111 POWER SUPPLY SCHEMATIC (VDE, BS1, SEV, 5AA)**
- **PC40-111 POWER SUPPLY SCHEMATIC (CSA, UL)**

INFORMATION IN THIS SECTION IS FOR REFERENCE ONLY.

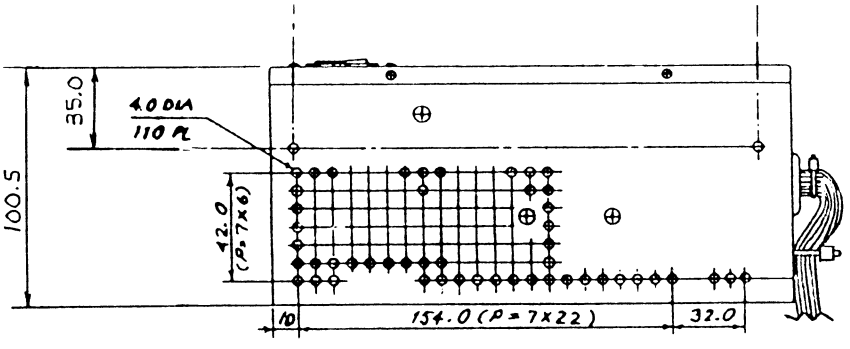
COMMODORE WILL NOT SUPPLY COMPONENT PARTS FOR OEM ASSEMBLIES.

PC40-111 POWER SUPPLY 390269

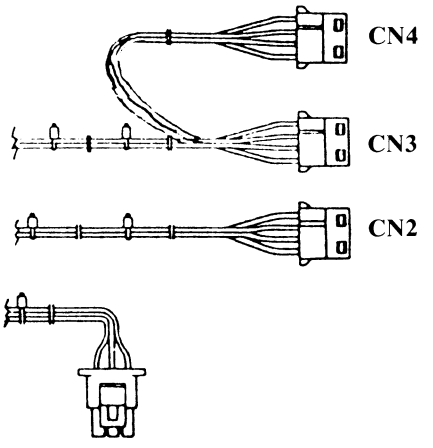
Input Requirements	VDE, BS1	CSA, UL
AC INPUT Parameter	**390269-01**	**390269-02**
Voltage Voltage Range Frequency (Hz) Surge Protection (maximum)	230 VAC 180 - 270 VAC 50 Hz 3 KV, 25 A for 30 usec	110 VAC 90 - 135 VAC 50 - 60 Hz 3 KV, 25 A for 30 usec
Inrush Current (maximum)		40 A for 30 usec



BACK VIEW



BOTTOM VIEW



NOTE: **FOR REFERENCE ONLY, —COLOR CODES AND SPECIFICATIONS MAY CHANGE.**

Connector CN1 : CPU

PIN	SIGNAL	AWG	COLOR	LENGTH (mm)
1	PWR GOOD	18	BRN	150.0 ±10%
2	−12V	18	RED	150.0 ±10%
3	+12V	18	ORG	150.0 ±10%
4	GND	16	BLU	150.0 ±10%
5	GND	16	BLU	150.0 ±10%
6	+5V	14	YEL	150.0 ±10%

Connector CN1 (Recommended)

Vendor	Housing	Pin	Remarks
AMP	350715-1	350552-1	MATE-n-LOK
BURNDY	UPH 600	UHM2200	—

Connector CN2 : HD 1

PIN	SIGNAL	AWG	COLOR	LENGTH (mm)
1	+12V	18	ORG	330.0 ±20%
2	GND	18	BLU	330.0 ±20%
3	GND	18	BLU	330.0 ±20%
4	+5V	18	YEL	330.0 ±20%

Connector CN2 (Recommended)

Vendor	Housing	Pin	Remarks
AMP	1-480424-0	611117-1	MATE-n-LOK
J.S. TERM	LCP-04	SLC21T2.0	—

NOTE: **FOR REFERENCE ONLY, — COLOR CODES AND SPECIFICATIONS MAY CHANGE.**

Connector CN3 : FDD 1

PIN	SIGNAL	AWG	COLOR	LENGTH (mm)
1	+12V	18	ORG	330.0 ±20%
2	GND	18	BLU	330.0 ±20%
3	GND	18	BLU	330.0 ±20%
4	+5V	18	YEL	330.0 ±20%

Connector CN3 (Recommended)

Vendor	Housing	Pin	Remarks
AMP	1-480424-0	611117-1	MATE-n-LOK
J.S. TERM	LCP-04	SLC21T2.0	—

Connector CN4 = FDD 2

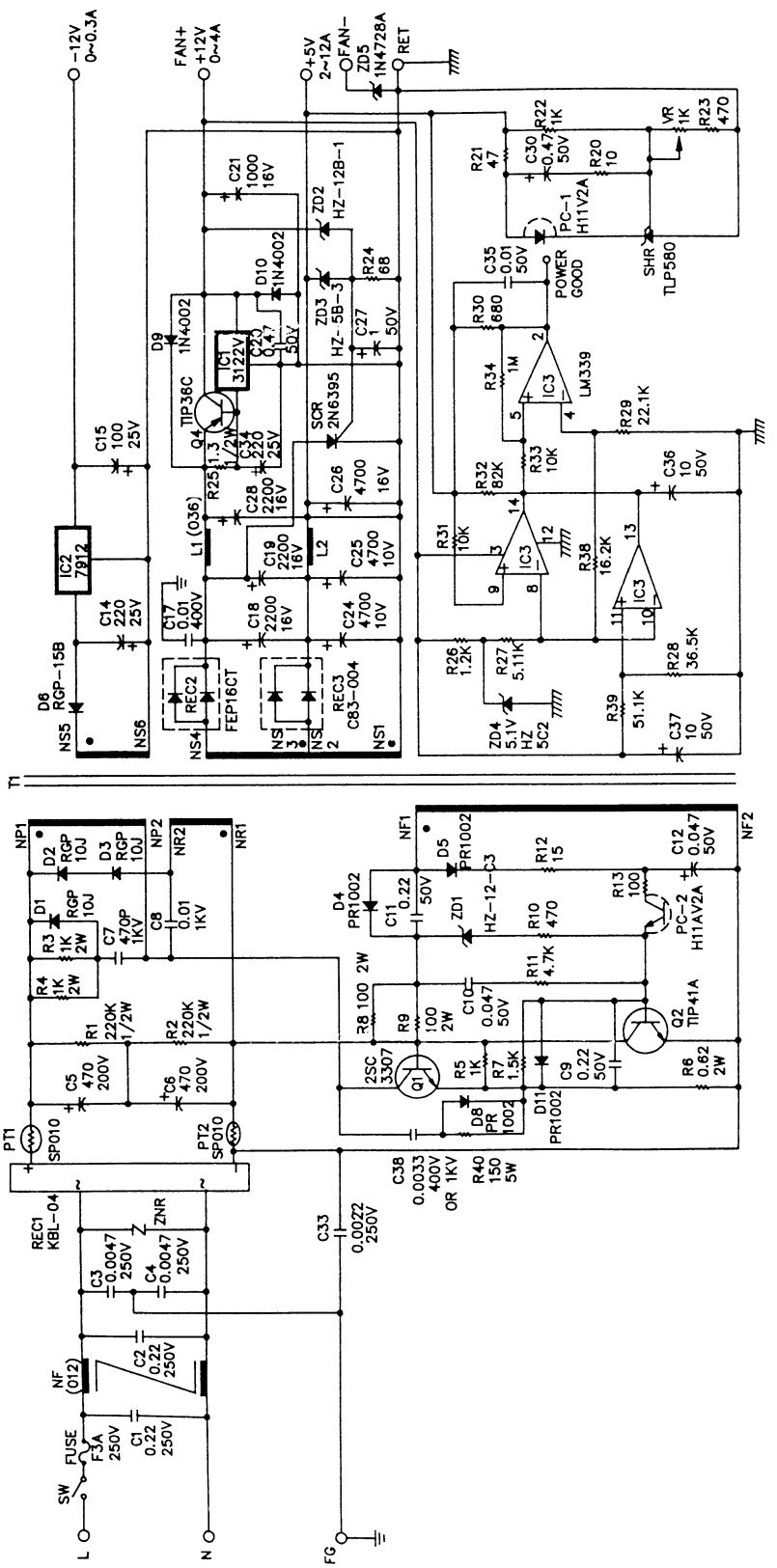
PIN	SIGNAL	AWG	COLOR	LENGTH (mm)
1	+12V	18	ORG	150.0 ±10%
2	GND	18	BLU	150.0 ±10%
3	GND	18	BLU	150.0 ±10%
4	+5V	18	YEL	150.0 ±10%

NOTE: Cable CN4 shall be daisy-chained from connector CN3.

Connector CN4 (Recommended)

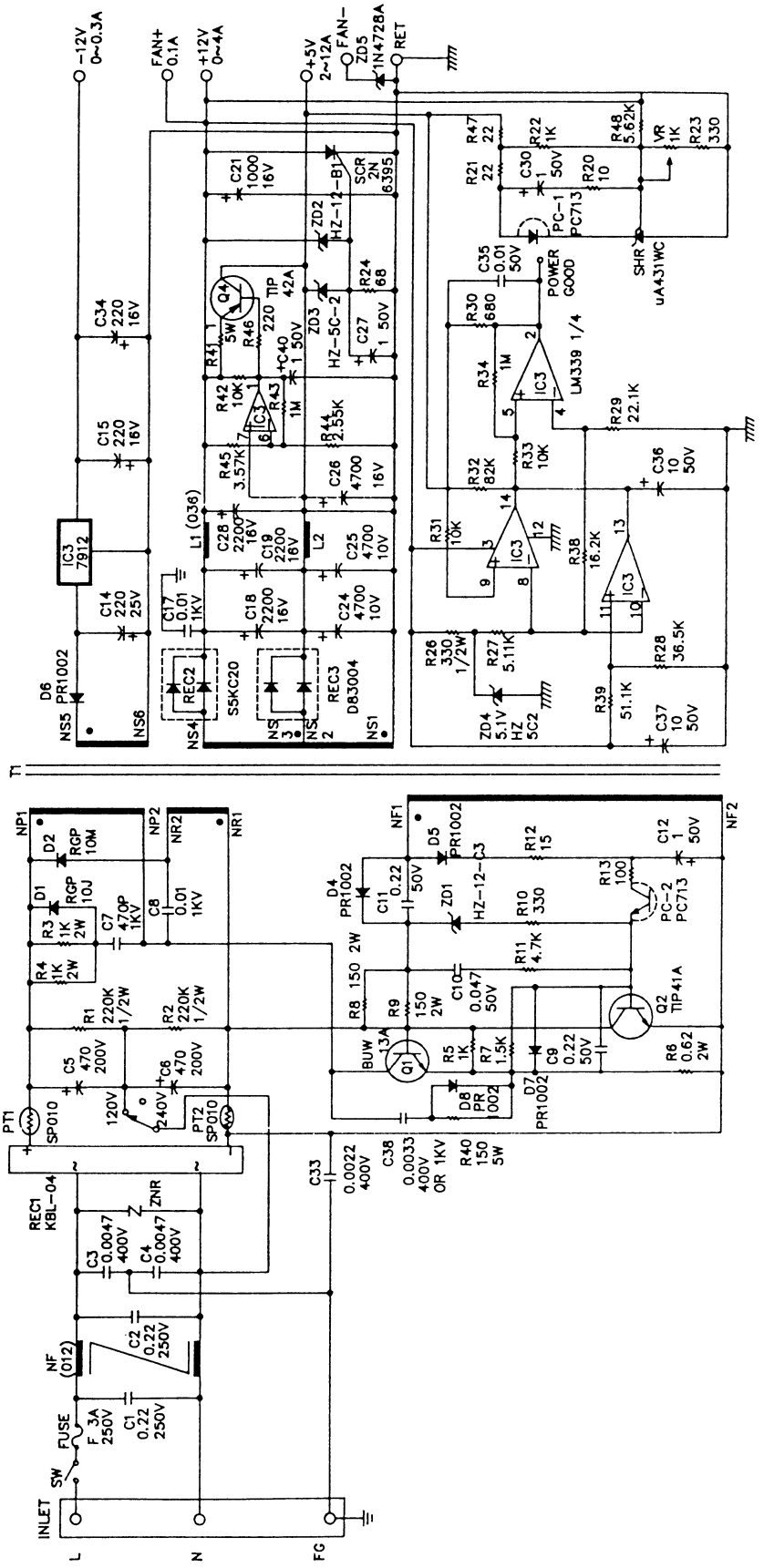
Vendor	Housing	Pin	Remarks
AMP	1-480424-0	611117-1	MATE-n-LOK
J.S. TERM	LCP-04	SLC21T2.0	—

FOR REFERENCE ONLY



PC40-III POWER SUPPLY (VDE, BSI, SEV, SAA)
PN #3902269-01

FOR REFERENCE ONLY



PC40-III POWER SUPPLY (CSA, UL)
PN#390269-02

APPENDIX B

DISK DRIVE SECTION

• PC40-III 40MB HARD DRIVE

• PC40-III Hard Drive PN #313065-01

Vendor : Quantum

Model : Prodrive 40AT

• PC40-III FLOPPY DISK DRIVE

• PC40-III Floppy Disk Drive PN #380825-02

Vendor : Chinon

Model : FZ506

• 910, 920 ADD ON NOTES

INFORMATION IN THIS SECTION IS FOR REFERENCE ONLY. COMMODORE WILL NOT SUPPLY COMPONENT PARTS FOR OEM ASSEMBLIES.

The information included in this section is for reference only. Vendors are subject to change without notice. Commodore service will provide alignment procedures and test diagnostics to authorized service centers for field repairs. The drive exchange program will be in effect and Commodore service will not provide discrete components for field replacement.

PC40-III HARD DRIVE 313065-01

GENERAL DESCRIPTION

The Quantum ***ProDrive Series***™ is a family of ten 3½-inch form factor hard disk drives using non-removable rigid disk platters as storage media. These drives feature formatted capacities ranging from 42 to 168 megabytes and a variety of interfaces. This manual covers the ***ProDrive***™ 40AT and ***ProDrive*** 80AT, which feature an IBM PC-AT® embedded controller and are available with or without an adapter board. With the adapter board, the ***ProDrive*** 40AT/80AT can plug directly into a 16-bit expansion slot in an IBM PC AT or compatible personal computer. Without the adapter board, the ***ProDrive*** 40AT/80AT is compatible with other AT-Bus architectures and can be plugged into an embedded AT adapter or into an existing adapter board in a PC AT compatible.

The ***ProDrive*** 40AT features 42 megabytes of formatted capacity on two disks with three movable heads; the ***ProDrive*** 80AT provides 84 megabytes of formatted capacity on three disks with six movable heads. Media defects and error recovery are efficiently managed within these products and can be fully transparent to the user. The ***ProDrive Series*** drives feature an innovative design using an integrated controller, minimum number of parts, and close control of product quality during manufacture, resulting in low cost, highly reliable products.

NOTE: Throughout this manual, ***ProDrive*** 40AT/80AT or ***ProDrive*** will refer to either the ***ProDrive*** 40AT or the ***ProDrive*** 80AT. ***ProDrive*** 40AT and ***ProDrive*** 80AT will be used to refer specifically to the 42 and 84 megabyte versions, respectively.

SPECIFICATIONS

Key features of the ***ProDrive*** 40AT/80AT include:

- Formatted storage capacity of 42 or 84 megabytes
- Industry standard 3½-inch form factor
- 19 millisecond average access time
- Data transfer rate up to 4.0 megabytes/second using programmed I/O
- 64K-byte look-ahead DisCache®
- 48-bit computer generated Error Correcting Code (ECC) with 11-bit burst correction capability
- Automatic retry for read disk errors
- Transparent defect mapping
- High-performance in-line defective sector skipping and reassignment of new defective sectors without need to reformat
- Patented AIRLOCK® automatic shipping lock and dedicated landing zone
- Read/Write with 1:1 interleave operation
- Emulation of IBM PC AT task file register and all AT fixed disk commands
- Ability to daisy-chain two drives on the interface

PHYSICAL SPECIFICATIONS

Environmental Limits

Ambient Temperature —	Non-Operating:	−40°F to 140°F (−40°C to 65°C) 42°F/hr (20°C/hr) gradient
	Operating:	39°F to 122°F (4°C to 50°C) 23°F/hr (10°C/hr) gradient
Ambient Relative Humidity —	Non-Operating:	5% to 95% without condensation Maximum wet bulb = 115°F (46°C)
	Operating:	8% to 85% without condensation Maximum wet bulb = 79°F (26°C)
Altitude (relative to sea level) —	Non-Operating:	−200 (−60M) to 40,000 ft. (12 km)
	Operating:	−200 (−60M) to 10,000 ft. (3 km)

Mechanical Dimensions (Exclusive of Faceplate)

Height = 1.625 in. (41.3 mm)
Width = 4.0 in. (101.6 mm)
Depth = 5.75 in. (144.9 mm)
Weight = 1.9 lb. (0.88 kg)

Heat Dissipation

Average Power Consumption (idle): 8 Watts (27.3 BTU/Hr)
Typical Power Consumption (30% Seeking): 9Watts (30.7 BTU/Hr)

Shock and Vibration

The table below lists specified levels for shock and vibration applied to any of the three mutually perpendicular axes (the principal drive base axes). The term "operating" implies that the drive will be fully functional while being subjected to the shock or vibration level listed during operation. "Non-operating" implies that there will be no change in performance once the drive is powered up after being subjected to the listed shock or vibration in the powered-down (non-operating) condition.

Vibration and Shock Specification

	Operating	Non-Operating
VIBRATION:		
5-500 Hz Sine Wave (Peak to Peak) 1 Oct/Min Sine Sweep	0.50 G	2.00 G
SHOCK: ½ Sine Wave of 11 msec Duration (10 hits maximum)	10 G (1 soft error/shock) (6 G No soft errors)	60 G

In addition, the ***ProDrive*** as packaged in the shipping container will withstand drops onto a concrete surface from 48 inches on all surfaces, six edges and three corners. It will withstand vibration applied to the container of 0.5 G, 5-100 Hz (0 to Peak) and 1.5 G, 100-500 Hz (0 to Peak).

PERFORMANCE SPECIFICATIONS

Capacity

	ProDrive 40AT	ProDrive 80AT
Formatted capacity (MB)	42*	84*
Number of 512 byte sectors	82,029	164,058

*40, and 80 megabytes, respectively when a megabyte is defined as 2^{20} bytes

Data Transfer Rates

Buffer to AT-Bus - Up to 4.0 Mbytes/second using programmed I/O
Disk to Buffer - Up to 1.25 Mbytes/second in bursts

Seek Times/Miscellaneous Times

DESCRIPTION	TYPICAL NOMINAL CONDITION	MAXIMUM NOMINAL CONDITION	MAXIMUM WORST CASE CONDITION
Single Track Seek (msec)	6	7	7
Average Seek (msec)	19	21	23
⅓ Stroke Seek (msec)	20	23	25
Full Stoke Seek (msec)	35	40	45
Average Rotational Latency (msec)	8.2	8.2	8.2
Sequential Head Switch (msec)	3.0	3.0	3.0
Power-Up Time (sec)	13	15	18

NOTES: Quoted seek times include head settling time but do not include command overhead or latency time. Seek time is the time required for the actuator to seek and settle on track.

Seek times are measured by averaging 1000 seeks of the indicated length. Average seek time is the average of 1000 random seeks. In the rare occurrence of a seek error, any individual seek may take up to 5 seconds for recovery.

Sequential head switch time is the time required for the head to move from the end of the last sector on a track to the beginning of the next sequential sector, located on the next track, same cylinder. This time is fixed by the track skewing feature of the drive. (See Appendix B.)

Power-up time is the time from the supply voltages reach operating range to the time the drive is able to accept all commands.

Nominal conditions are defined as 25°C ambient temperature, nominal supply voltages, and no applied shock or vibration. Worst case conditions are defined as worst case extremes of temperature and supply voltages.

Media Quality

The ***ProDrive*** features defect management, which eliminates the need to manually indentify defects. Defect management is completely transparent to the user. See Appendix C for a detailed description of the ***ProDrive's*** defect handling procedure and ECC capability.

Error Rates

Random Data Errors (2):	1 error per 10^{10} bits read (maximum)
Defect Data Errors (3):	1 error per 10^{12} bits read (maximum)
Unrecoverable Data Errors (4):	1 error per 10^{14} bits read (maximum)
Seek Errors (5):	1 error per 10^{6} seeks (maximum)

Error rates are defined as follows:

1) A data error is one (1) sector read incorrectly. Data error rates are defined as average rates measured over at least 1000 different sectors under any of the specified conditions **except** applied shock or vibration.
2) Random errors are those which do not exhibit a repeating error pattern, i.e, the error does not occur twice in a row within a specified number of retry reads; the default is eight. (Retries are terminated once data is read correctly.) The sectors will not be automatically reallocated since the errors are probably not due to media defects.
3) Defect errors are those which exhibit a repeating error pattern, i.e., the error occurs twice in a row within eight retry reads, and cannot be read without error up to that point. Such errors are likely due to media defects.
4) Unrecoverable errors are those whose final retry error pattern is uncorrectable using ECC: retry reads are terminated by either a repeating error pattern, or eight attempts without reading correctly.
5) A seek error is any seek in which the drive does not locate the desired cylinder, or any seek in which the drive must go through a full recalibration routine to locate the desired cylinder. A full recalibration takes approximately five seconds.

FUNCTIONAL SPECIFICATIONS

PHYSICAL FORMAT

	***ProDrive* 40AT**	***ProDrive* 80AT**
Nom Rotational Speed (RPM)	3,662 ±0.3%	3,662 ± 0.3%
Max Recording Density (bpi)	22,055	22,055
Max Flux Density (fci)	14,700	14,700
Track Density (tpi)	1,000	1,000
Data Cylinders	834	834
Data Tracks	2,502	5,004
R/W Heads	3	6
Disks	2	3
Encoding Scheme	RLL 2,7	RLL 2,7

LOGICAL FORMAT

The logical layout is how the drive appears to an AT-Bus system.

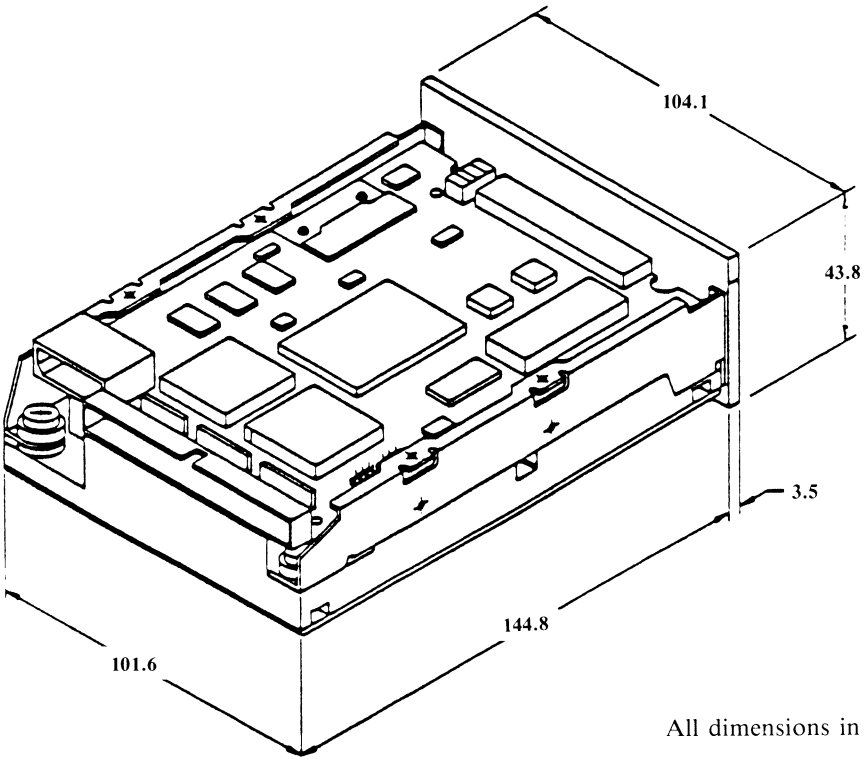
	ProDrive 40AT	*ProDrive* 80AT
Data Cylinders	965	965
Sectors/Track	17	17
R/W Heads	5	10

RELIABILITY SPECIFICATIONS

MTBF (Mean Time Between Failure): 50,000 POH (Power On Hours) typical usage
PM (Preventative Maintenance): Not required
MTTR (Mean Time To Repair): 30 minutes
Start/Stop: 10,000 cycles

ACOUSTICS

Idle Mode: 45 dBa maximum at 1 foot in any direction



All dimensions in millimeters

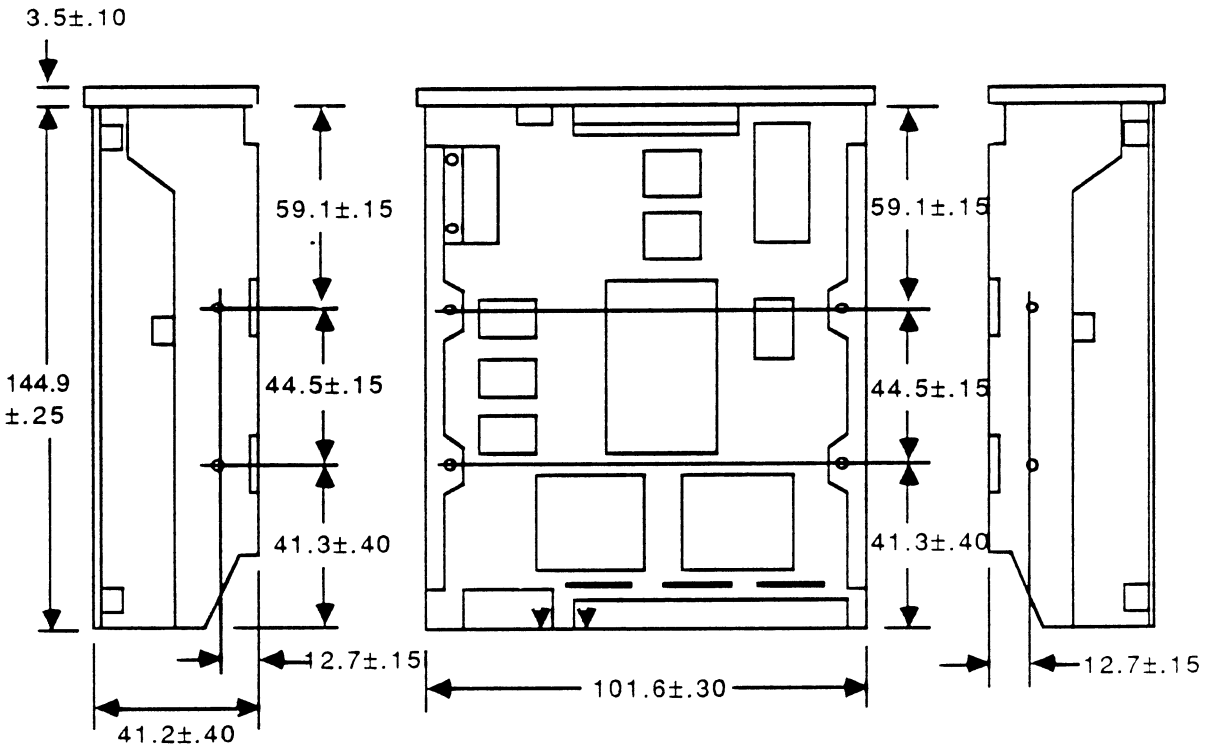
ProDrive Mechanical Dimensions

MOUNTING/DIMENSIONS (DIMENSIONS EXCLUSIVE OF FACEPLATE)

The drive may be mounted in any orientation.

Clearance from the drive to any other surface (except shock mount brackets or faceplate) should be 0.10 inch minimum.

HEIGHT	1.625 in.	41.3 mm
WIDTH	4.0 in.	101.6 mm
DEPTH	5.75 in.	146.1 mm
WEIGHT	1.9 lb.	0.88 kg



DIMENSIONS ARE IN MILLIMETERS; SCREW SIZE IS 6-32

PC40-III HARD DRIVE

POWER REQUIREMENTS

No damage or loss of data occurs if power is applied or removed in any order or manner, except that data may be lost in the sector being written to at the time of the power loss. This includes opening up or shorting out either voltage or return line, and transient voltages +10% to −100% from nominal, while powering up or down.

VOLTAGE	**+12V**	**+5V**
NOMINAL	+12V	+5V
TOLERANCE	±10%	±5%
CURRENT		
TYPICAL (IDLE)	0.5A	0.5A
TYPICAL (SEEKING)	0.8A	0.6A
MAXIMUM (POWER-UP)	1.6A	0.65A
RIPPLE AND NOISE (MAXIMUM)	100mVp-p	50mVp-p
AVERAGE POWER CONSUMPTION	8W	
TYPICAL POWER CONSUMPTION (30% SEEK)	9W	
MAXIMUM POWER	11W	

POWER RESET LIMITS

When powering up, the drive remains reset (inactive) until both supplies reach the upper threshold value. When powering down, the drive becomes reset when either supply voltage drops below the lower threshold value. Hysteresis is 50m V minimum.

5V	4.50V TO 4.20V
12V	10.4V TO 9.70V

PC40-III Power Connector - HD

PIN	Signal
1	+12 Volts
2	Ground
3	Ground
4	+5 Volts

DC POWER CONNECTOR

The DC power connector (J1) is a 4-pin DuPont Connector (SK 20055-000) mounted on the back edge of the Printed Circuit Board (PCB) near the AT-Bus connector. See Figure 1. The recommended mating connector (P2) (AMP P/N 1-480424-0) utilizes AMP pins [P/N 350078-4 (strip) or P/N 61173-4 (loose piece)]. J1 pins are labeled on the connector.

Pin 1 +12 volts DC
Pin 2 +12 volt return (ground)
Pin 3 +5 volt return (ground)
Pin 4 +5 volts DC

NOTE: Pins 2 and 3 are connected on the drive.

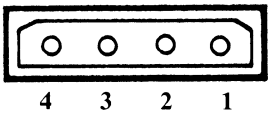


FIGURE 1 — DC POWER CONNECTOR (J1)

AT-BUS INTERFACE CONNECTOR

One AT-Bus interface cable connector (J2) is required for the ***ProDrive***. Details of the signals required can be found in AT-Bus Interface and Commands.

Connection to J2 is through a 40-pin Universal Header connector. A connector sketch is shown in Figure 2. A key slot is provided to prevent incorrect installation of the mating connector. The recommended mating connector for J2 is xxxxx.

NOTE: Unkeyed mating connectors should not be used due to the possibility of plugging the connector in backwards.

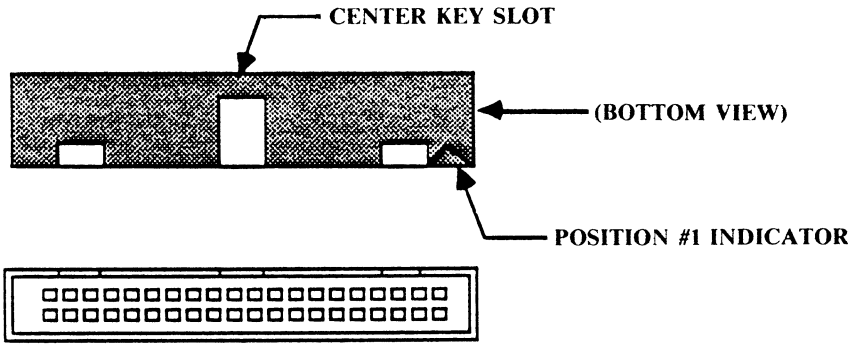


FIGURE 2 — AT-BUS INTERFACE CONNECTOR (J2)

JUMPER OPTIONS

Configuration of a ***ProDrive*** 40AT/80AT disk drive varies depending on the system in which it is to be installed. This section describes the user-selectable hardware options available on the disk drive PCB. These jumpers should be set prior to installation. Figure 3 identifies the location of the shorting plugs and terminators on the drive PCB.

NOTE: Additional jumper options are provided on the adapter board for systems in which the adapter board is used with the drive.

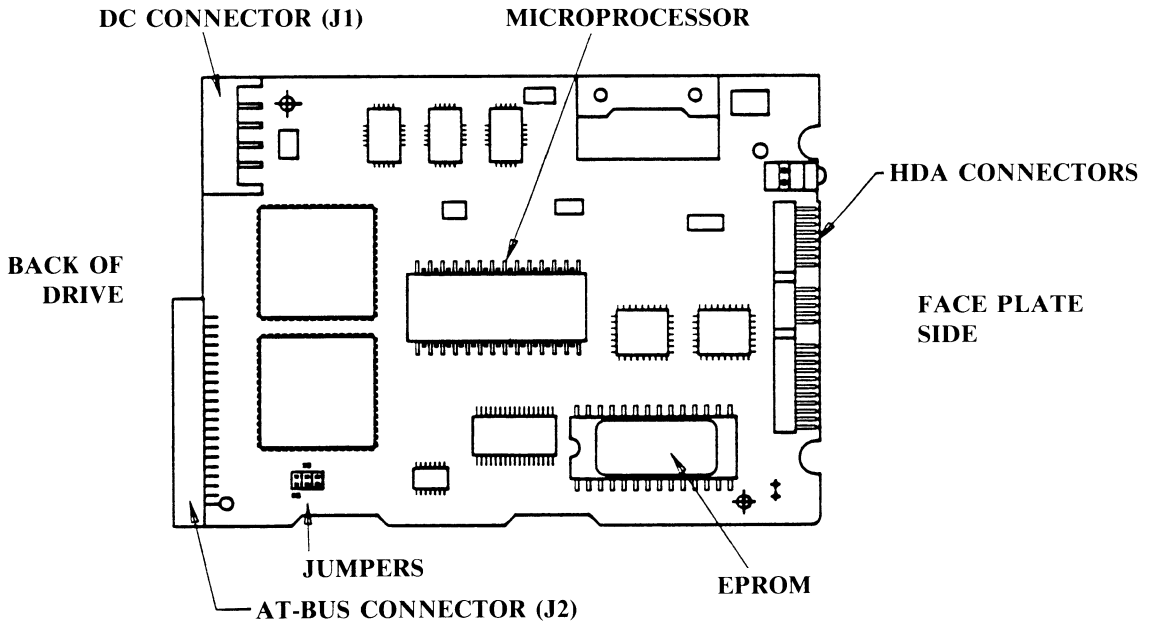


FIGURE 3 — Shorting Plug Locations on the Drive PCB

SELF SEEK TEST OPTION

The self seek test continuously exercises the actuator of the drive. When shorting plug option SS is installed, the drive will perform random seek patterns, verifying track IDs after every seek. The pattern will repeat as long as power is applied to the drive, until the shorting plug is removed, or until an error has occurred.

The ***ProDrive*** is sent from the factory with shorting plug SS not installed (Self Seek Test disabled).

DRIVE SELECT

Two drives can be daisy-chained on the AT-Bus interface. When two drives are attached, one must be configured as the primary drive, and the other as the secondary drive, using the Drive Select (DS) jumper. With the DS shorting plug installed, the drive is configured as the primary drive (Drive 0); with no shorting plug on jumper DS, the drive is configured as the secondary drive (Drive 1).

The ***ProDrive*** is sent from the factory with the DS shorting plug installed (Drive 0)

RESERVED JUMPER

The third jumper is reserved for future use.

FACEPLATE LED OPERATION

The green LED located on the faceplate illuminates when the drive is executing a command. It lights at the beginning of a command and does not go off until the command is completed or aborted.

ADAPTER BOARD

This section is relevant only for systems which implement the ***ProDrive*** AT-Bus drive with the adapter board.

ADAPTER BOARD JUMPER OPTIONS

Five jumpers labeled J2 through J6 are provided on the adapter board; the functions of these jumpers are described below. See Figure for the locations of the jumpers on the PCB.

J2 - Allows the drives interrupt logic to control IRQ14. This jumper is provided for compatibility with systems whose BIOS does not read the STATUS register when the drive issues an interrupt.
- for systems that do not read the STATUS register, jumper from the center pin of J2 to E4;
- for systems that do read the STATUS register, jumper from the center pin of J2 to E3.

J3 - Always open. Option for grounding pin #34 of the drive interface.

J4 - Forwards IO CH RDY to the drive for use with systems running Chips & Technologies chip set.

J5 - Secondary board enable.

J6 - For manufacturers use only; do not install a jumper.

INTRODUCTION

The ***ProDrive*** 40AT/80AT uses the standardized IBM PC AT Bus interface and is available with or without an Adapter Board. With the Adapter Board, the ProDrive can plug directly into a 16-bit expansion slot on an AT compatible computer. Without the Adapter Board, the drive is compatible with other AT-Bus architectures and can be plugged into an embedded AT Adapter or existing Adapter Board.

ADAPTER BOARD

The Adapter Board is an IBM PC AT I/O bus-compatible interface. The I/O extended bus connector is required for data bus D8-D15, IRQ14 and IO CS16. The Adapter Board buffers data and control signals between the drive and the host system, and performs address decoding of the Host Address Bus. The Task File Registers, which accept commands from the host system BIOS, are located on the drive itself.

NOTE: Some host systems will not read the STATUS register after the drive issues an interrupt. In such cases, the interrupt will not be acknowledged. A jumper option is provided on the Adapter Board to overcome this problem. This jumper allows interrupts to be controlled by the drive's interrupt logic. See jumper option J2.

AT-BUS INTERFACE CHARACTERISTICS

The AT-Bus interface supports one or two hard disk drives per adapter board, and will accomodate two adapter boards for a total of four drives. Regardless of the number of drives, there is a master/slave relationship between the host and the drive. The drive always maintains control of the bus; there is no arbitration.

ELECTRICAL CHARACTERISTICS

All signals are TTL compatible with a logic one being greater than 2.0 volts but less that 5.25 volts, and a logic zero being greater than 0.0 volts but less than 0.7 volts.

AT-BUS INTERFACE SIGNALS

The AT-Bus interface connector is a 40-pin shrouded connector with two rows of 20 male pins on 100 mil centers. The connecting cable is a 40-conductor flat ribbon with a maximum length of 18 inches. Table 1 describes each signal on the AT-Bus interface. Refer to Table 1 for the AT-Bus interface pinouts and their relationship with the AT system bus.

NOTE: The direction Table 1 is in reference to the drive, i.e., IN means to the drive. PINS are in reference to the 40-pin AT-Bus connector.

TABLE 1 — AT-Bus Interface Pin Assignments

SIGNAL NAME	DIR	PIN	DESCRIPTION
– HOST RESET	IN	1	Reset signal from the host system; active low during system power-up.
GROUND		2	Ground between host system and drive.
HOST DATA D0-D15	I/O	3-18	16-bit bi-directional data bus between the host and the drive. D0-D15 are used to transfer 8-bit information for register and ECC READ/WRITE. Data Bit D7 is disabled when the host reads the digital input register. These are tri-state lines with 24mA drivers.
GROUND		19	Ground between host system and drive.
KEY		20	Unused pin for keying ribbon cable to the drive.
– HOST IO CH RDY	OUT	21	Enables host wait state generation to lengthen the I/O read and write cycles. Driven low by the drive immediately upon detecting a valid I/) address select.
GROUND		22	Ground between host system and drive.
– HOST IOW	IN	23	Write strobe. Clocks data from the OF – HOST to the drive over data lines D0-D7 and/or D8-D15 on the rising edge of HOST IOW.
GROUND		24	Ground between host system and drive.
– HOST IOR	IN	25	Read strobe. Clocks data from the drive to host data lines D0-D7 and/or D8-D15 on the rising edge of – HOST IOR.
GROUND		26	Ground between host system and drive.
RESERVED		27	Reserved for future definition.
HOST ALE	IN	28	Address Latch Enable from the host. Not currently used, but provided to maintain compatibility.
RESERVED		29	Reserved for future definition.
GROUND		30	Ground between host system and drive.
HOST IRQ14	OUT	31	Interrupt signal to the host. Active only when the drive is selected and the drive interrupt enable bit is high. Goes to a high impedance state when the drive is not selected or the interrupt enable bit is low. The interrupt is cleared upon receiving the next command, when the status register is read or when the drive is reset.
– HOST IO CS16	OUT	32	Informs the host that one of the drive registers has been enabled and that the drive is prepared to perform a 16-bit I/O transer. Open collector output with 24mA driver.
HOST ADDR 1	IN	33	Address line from the host to the drive that is used to select a register on the drive.
GROUND		34	Ground between host system and drive.
HOST ADDR 0	IN	35	Address line from the host to the drive that is used to select a register on the drive.
HOST ADDR 2	IN	36	Address line from the host to the drive that is used to select a register on the drive.
– HOST CS0	IN	37	Decoded address select from the host indicating that access to one of the 8 task file registers is desired.
– HOST CS1	IN	38	Decoded address select from the host indicating that access to one of the 3 diskette function registers is desired.
– HOST SLAVE	OUT	39	Indicates the presence of a second drive. When this signal is low, a second drive is present. Open collector output with 24mA driver.
GROUND		40	Ground between host system and drive.

AT SYSTEM BUS SIGNALS

The table below presents the signals on the AT system bus that are used by the AT-Bus interface. You should refer to Figure for the AT-Bus interface pinouts and their relationship with the AT system bus.

NOTE: The direction in Table 2 is in reference to the host system, i.e., IN means to the host system. PINS are in reference to the 40-pin AT system bus connector.

TABLE 2 — AT System Bus Pin Assignments

SIGNAL NAME	DIR	PIN	DESCRIPTION
SA0-SA9	OUT	A22-A31	System address bus
SD0-SD15	I/O	A2-A9 & C11-C18	System address bus
AEN	OUT	All	Signal indicating a DMA address is on the system address bus. Active when high.
-IOW	OUT	B13	Signals that the enabled I/O device should read the data on the data bus. Active when low.
-IOR	OUT	B14	Signals that the enabled I/O device should gate data onto the system data bus. Active when low.
BALE	OUT	B28	Indicates a valid system address is available. Active when changing from high to low.
IRQ14	IN	D7	System interrupt request indicating an I/O device needs attention. Active when changing low to high.
RESET	OUT	B2	Used to reset or initialize system hardware at power up. Active when high.
-IO CH RDY	IN	A10	Pulled low during a bus transaction by an enabled I/O device to lengthen the read/write cycles. Open collector onto host bus.

AT-Bus Interface Pin Assignments

DISK CONNECTOR			AT BUS CONNECTOR	
PIN NO	SIGNAL NAME	DIRECTION	PIN NO	SIGNAL NAME
1	-HOST RESET	← INV	B2	RESET DRV
2	GROUND	---	---	GROUND
3	HOST DATA 7	↔	A2	SD7
4	HOST DATA 8	↔	C11	SD8
5	HOST DATA 6	↔	A3	SD6
6	HOST DATA 9	↔	C12	SD9
7	HOST DATA 5	↔	A4	SD5
8	HOST DATA 10	↔	C13	SD10
9	HOST DATA 4	↔	A5	SD4
10	HOST DATA 11	↔	C14	SD11
11	HOST DATA 3	↔	A6	SD3
12	HOST DATA 12	↔	C15	SD12
13	HOST DATA 2	↔	A7	SD2
14	HOST DATA 13	↔	C16	SD13
15	HOST DATA 1	↔	A8	SD1
16	HOST DATA 14	↔	C17	SD14
17	HOST DATA 0	↔	A9	SD0
18	HOST DATA 15	↔	C18	SD15

***AT-Bus Interface Pin Assignments** (continued)*

DISK CONNECTOR			AT BUS CONNECTOR	
PIN NO	**SIGNAL NAME**	**DIRECTION**	**PIN NO**	**SIGNAL NAME**
19	GROUND	---	---	GROUND
20	KEY			NO CONNECTION
21	-HOST IO CH RDY	→	A10	-IO CH RDY
22	GROUND	---	---	GROUND
23	-HOST IOW	←	B13	-IOW
24	GROUND	---	---	GROUND
25	-HOST IOR	←	B14	-IOR
26	GROUND	---	---	GROUND
27	RESERVED			NO CONNECTION
28	HOST ALE	←	B28	BALE
29	RESERVED			NO CONNECTION
30	GROUND	---	---	GROUND
31	HOST IRQ14	→	D7	IRQ14
32	-HOST IOCS16	→	D2	-IOCS16
33	HOST ADDR 1	←	A30	SA1
34	GROUND	---	---	GROUND
35	HOST ADDR0	←	A31	SA0
36	HOST ADDR2	←	A29	SA2
37	-HOST CS0			
38	-HOST CS1			
39	-HOST SLV			
40	GROUND	---	---	GROUND

NOTES: All grounds are connected together on the ground plane of the adapter board.

-HOST CS0, -HOST CS1 and -HOST SLV are generated on the adapter board; there are no directly related AT-Bus signals.

Recommended [1] Connectors

CABLE CONNECTOR DESCRIPTION	DISK DRIVE [2] CONNECTOR	HOST (CPU) [3] CONNECTOR
DC POWER PLUG	AMP 1-4807222-0	AMP 1-480424-0
DC POWER PIN	AMP 350079-4	AMP 350078-4
I/O CONNECTOR	BURNDY FRHL40R-2	BURNDY FRS40BD-8P

[1] THESE NUMBERS ARE FOR SIZE REFERENCE ONLY

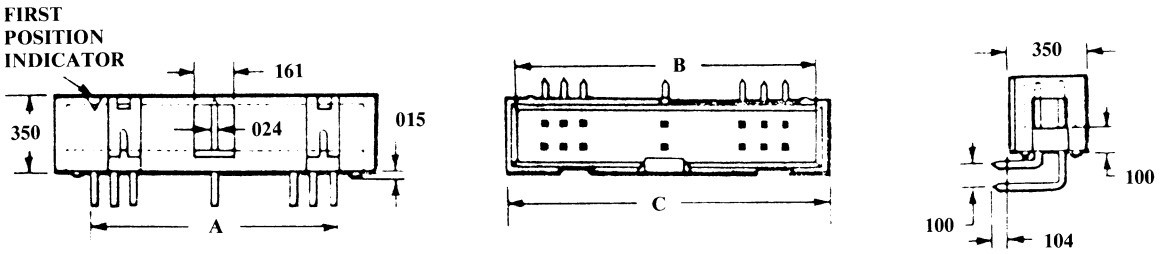
[2] PROVIDED BY DRIVE VENDOR

[3] PROVIDED BY COMMODORE

I/O INTERFACE CIRCUIT

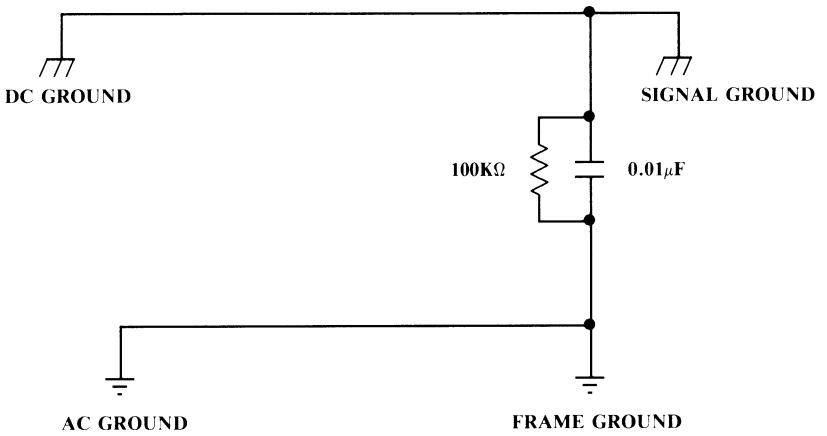
NOTE: Wiring shall be ribbon cable or twisted pair.

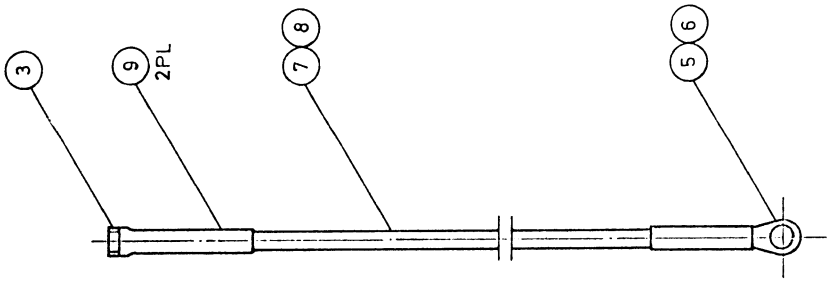
DIMENSIONS ARE IN INCHES



GROUND CIRCUIT

NOTE: Wiring shall be ribbon cable or twisted pair.





GROUND CABLE ASSY. — 380811-01

	CBM PART NUMBER	DESCRIPTION	VENDOR
03	324594-02	TERMINAL 4.6 X 0.3 DIN 46247	WEITKOWITZ 44113
05	903451-10	TERMINAL RING TONGUE ϕ 4.3 DIN 4623	MOLEX AA
06	905451-01	TERMINAL RING TONGUE ϕ 3.2 DIN 46234	
07	903733-10	LEAD WIRE	STRIPLENGTH 2 X 3 MM
08	903753-10	LEAD WIRE AWG 18 BLACK L = 60 MM	
09	906475-05	TUBEHEAT SHRINK	

PC40-III FLOPPY DISK DRIVE — 380825-01 (Dark Bezel); 380825-02 (Light Bezel)

SCOPE

This specification describes 5-¼ " double-sided 96-TPI minifloppy disk drive (hereafter abbreviated as FDD) CHINON FZ-506.

FEATURES

The features of the FZ-506 are as follows:

(1) Large Capacity Up-to 1.6M bytes
The FZ-506 is a double-sided, high-density, double-track type and its capacity is 1.6M bytes, in unformatted mode. The read/write selection of the high density 1.6M bytes, 96 TPI and double density 1M bytes, 96 TPI disk can be carried out by changing either the motor speed (360 rpm/300 rpm) or transfer rate (500K BPS/300K BPS). In addition, as the data retrieval from 250K bytes, 48 TPI disk to 500K bytes, 96 TPI disk is possible, the former software packages can be read.

(2) Pop-up Mechanism
With the newly employed pop-up mechanism, the disk can be loaded/unloaded with ease, preventing mischucking at disk insertion.

(3) Low Power Consumption
As a newly designed LSI (C-MOS chip) is employed in the read/write and control circuits, high performance and low power consumption are achieved. In stand-by mode, power consumption is only 1.59W, and in operation mode 3.81W, making system design easy.

(4) Built-in Disk-in sensor
With the built-in disk-in-sensor, when no disk is loaded, the motor is stopped. This extends the motor service life and reduces power consumption. When chucking the disk, the DD motor is rotated temporarily to assure the centering of the disk. DISK CHANGE signal will be output by the sensor, also.

(5) Various Disk Readings
With the FZ-506, the various disk readings shown below are possible, existing software written in 48 TPI format can be used without any conversion.

Disk Used	Normal Density				High Density
Track Density	48 TPI		96 TPI		96 TPI
Storage Capacity	250 KB	500 KB	500 KB	1 MB	1.6 MB
Rate of Data Transfer	250K/300K BPS	250K/300K BPS	250K/300K BPS	250K/300K BPS	500K BPS
Rotational Speed	300/360 rpm	300/360 rpm	300/360 rpm	300/360 rpm	360 rpm
Data Read	○	○	○	○	○
Data Write	*○	*○	○	○	○

* Data can be read by this drive, but data can not be read by a head made solely for 48 TPI use.

SPECIFICATIONS

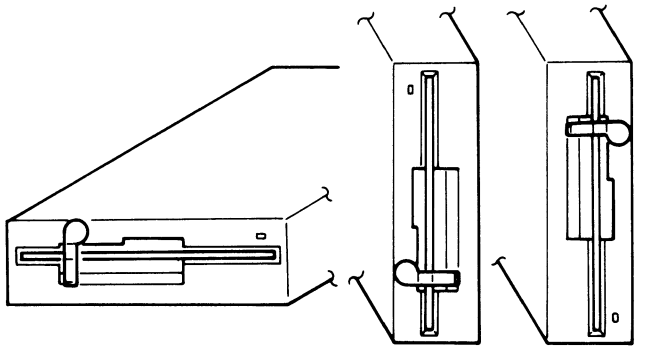
Specification (1)

Item			CHARACTERISTIC			
			HIGH DENSITY		NORMAL DENSITY	
Recording mode			FM	MFM	FM	MFM
Storage capacity	Unformatted	Per disk	833 KB	1666 KB	500 KB	1000 KB
		Per track	5.208 KB	10.416 KB	3.125 KB	6.25 KB
	Formatted	Per disk	615 KB	1229 KB	368.640 KB	737.280 KB
		Per track	3840 B	7680 B	2304 B	4608 B
		Number of sectors	15		16	
		Per sector	256 B	512 B	128 B	256 B
Recording density			4935 BPI	9870 BPI	2961 BPI	5922 BPI
Rate of data transfer			250K BPS	500K BPS	125K/150K BPS	250K/300K BPS
Access time	Power-on to ready time		0.5 sec or less			
	Single track seek time		3 msec			
	Average access time		94 msec			
	Settling time		15 msec			
	Average latency time		83.3 msec		100 msec/83.3 msec	
Rotation speed			360 rpm		300/360 rpm	
Number of tracks			160			
Number of cylinders			80			
Track density			96 TPI			
Number of heads			2			
Number of index			1			
Radius of track	Outer track	Side 0	57.150 mm			
		Side 1	55.033 mm			
	Inner track	Side 0	36.248 mm			
		Side 1	34.131 mm			

Specification (2)

Item	Specification			
Physical dimensions	146 (W) x 41 (H) x 193 (D) mm			
Weight	approx. 1 kg			
Power supply	DC +12 V ±5%			
	DC +5 V ±5%			
Power consumption		+5 V	+12 V	POWER
	Stand-by	290 mA TYP.	14 mA TYP.	1.62 W TYP.
	Read	330 mA TYP.	200 mA TYP.	4.05 W TYP.
	Write	330 mA TYP.	210 mA TYP.	4.17 W TYP.
	Seek	260 mA TYP.	440 mA TYP.	6.58 W TYP.
	Spindle Motor Starting current (0.5 sec. max.)		900 mA MAX.	
Ripple voltage allowance	DC +12 V	Less than 150 mVp-p (including spike noise)		
	DC +5 V	Less than 100 mVp-p (including spike noise)		
Noise	Less than 55 phons (class A) (separated from the drive by 1m)			
Cabinet specifications	Front panel	Material: ABS Color: Beige		
	Front lever	Material: ABS Color: Beige		

Installation Conditions

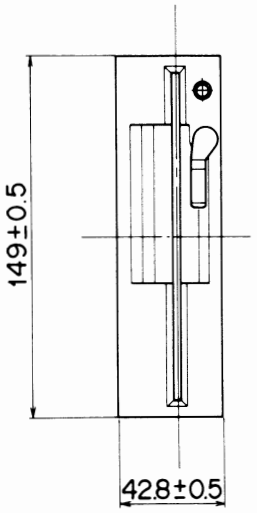
<table>
<tr><th>Item</th><th colspan="4">Specification</th></tr>
<tr><td>Mounting position</td><td colspan="4"> 
Horizontal Vertical
In horizontal position, the front panel can be raised a maximum of 15°.</td></tr>
<tr><td rowspan="6">Environment conditions</td><td rowspan="3">Temperature</td><td>During operation</td><td colspan="2">5 ~ 45°C</td></tr>
<tr><td>During non-operation</td><td colspan="2">0 ~ 50°C</td></tr>
<tr><td>During storage</td><td colspan="2">–20 ~ 60°C</td></tr>
<tr><td rowspan="3">Humidity</td><td>During operation</td><td colspan="2">20 ~ 80% RH Maximum wet bulb temperature 29°C</td></tr>
<tr><td>During non-operation</td><td colspan="2">5 ~ 90% RH No dew condensation</td></tr>
<tr><td>During storage</td><td colspan="2">8 ~ 90% RH No dew condensation</td></tr>
<tr><td colspan="2">Temperature change</td><td colspan="2">15°C/H</td></tr>
<tr><td rowspan="4">Vibration</td><td rowspan="2">During operation</td><td>Continuous vibration</td><td>Amplitude Less than 0.5 mm 5 ~ 25 Hz
0.25G 25 ~ 100 Hz</td></tr>
<tr><td>Single vibration</td><td>Less than 10G (10 ms)</td></tr>
<tr><td rowspan="2">During non-operation and storage (W/Protect sheet)</td><td>Continuous vibration</td><td>Amplitude Less than 7 mm 5 ~ 9 Hz
0.5G 9 ~ 100 Hz</td></tr>
<tr><td>Single vibration</td><td>Less than 30G (10 ms)</td></tr>
<tr><td>Drop shock</td><td colspan="4">Fall height in packing State: 70 cm
(corner: one time, sides: three times, flat surfaces: six times)</td></tr>
</table>

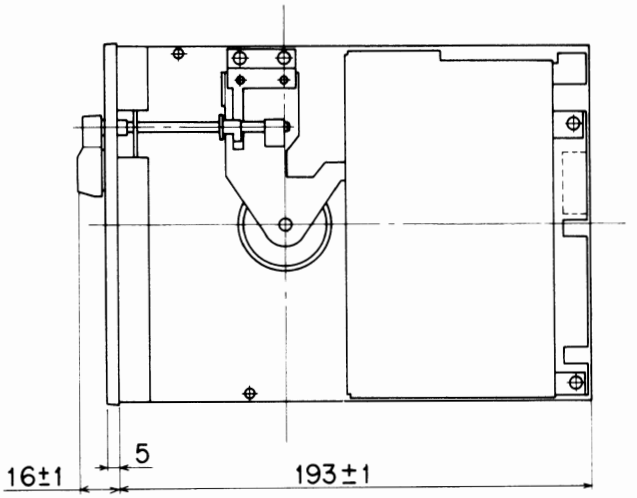
Reliability

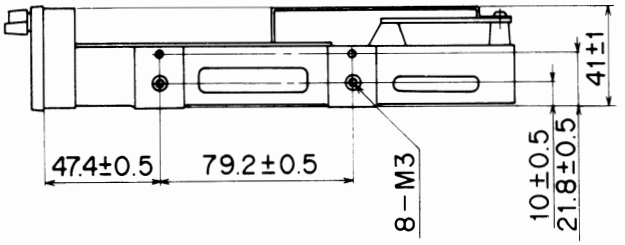
Item			Specification
Drive	MTBF		10,000 POH
	MTTR		0.5 H
	Drive life		Five years
Error rate	Software errors		10^{-9} times/bit
	Hardware errors		10^{-12} times/bit
	Seek errors		10^{-6} times/seek
Life	Drive	Number of mountings of the media	30,000 times or more
		Seek	10,000,000 seeks or more
		Head	10,000 H or more
	*1Media	Number of identical track passes	3,000,000 passes or more
		Number of mountings	10,000 times or more

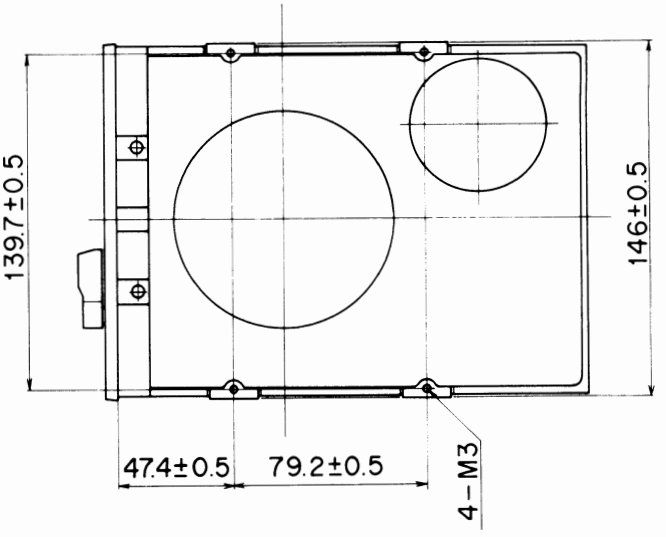
* Maintenance is not required under normal use conditions.
*1 Reference value

DIMENSIONS


149±0.5
42.8±0.5


16±1
5
193±1


41±1
47.4±0.5
79.2±0.5
8-M3
10±0.5
21.8±0.5


139.7±0.5
146±0.5
47.4±0.5
79.2±0.5
4-M3

INTERFACE SIGNALS

The interface signal has 12 input signal lines and 5 output signal lines.

Signal Voltage Levels

The interface signal interfaces with the controller at the TTL level. For all signals, low is true. The I/O signal level into the drives have the following specifications.

(1) Input level	0V to +0.40V
High level	+2.40V to +5.25V
Input impedance	150Ω
(2) Output signal	
Low level	0V to +0.40V
High level	+5.25V max. (by receiving the end terminator)
Output current (for low level)	48 mA (max.)
Output current (for high level)	250 μA (max.)

Input Signals

(1) DRIVE SELECT 0 to 3 signal lines
When one of these signal lines goes into low level, the drive corresponding to the signal line is selected and the I/O gate is opened. Up to four drives can be controlled using these four signal lines. The drive corresponding to one of the DRIVE SELECT 0 to 3 signal lines is determined by the position of the short plug in the drive.

(2) MOTOR ON signal line
This line controls the ON/OFF of the spindle motor. When this signal line is set to low level, the spindle motor revolves. When it is set to high level, it stops. 0.5 seconds is the required start up time of the spindle motor. The motor start operation is not executed when no disk is loaded.
This signal operates independently of the DRIVE SELECT signals.

(3) DIRECTION SELECT signal line
This signal determines the direction of movement of the head when a pulse is sent via the STEP signal line. When this signal line is set to low level and the STEP signal pulse is sent, the head moves towards the center of the disk. When it is set to high level and the STEP signal pulse is sent, the head moves away from the center.
The logic level of this signal should be held for at least 1 microsecond after the trailing edge of the STEP pulse.

(4) STEP signal line
This signal line moves the head. With the rise of a single low level pulse, this signal line changes from LOW level to HIGH level and the head moves one track in the direction determined by the DIRECTION SELECT signal.
However, this signal is not accepted when the FDD is in WRITE mode. The head is stabilized 20 ms after the trailing edge of the last STEP pulse, and the FDD is ready for data read/write operation.

(5) WRITE GATE signal line
This signal line specifies drive write and read status. When this signal line is set to low level, write enable status occurs and the data is stored on the disk surface by the WRITE DATA signal. When this signal line is set to high level, read status occurs.
After the writing operation, a period of 1.2 ms is necessary before a valid READ DATA signal appears on the interface.

(6) WRITE DATA signal line
Data written on the disk surface is transferred on the signal line. With the decline of the pulse sent to this signal line (when the signal line changes from the high level to the low level), data is written on the disk surface.

(7) SIDE SELECT signal line
This signal line selects the head.
When this signal line is set to high level, the side 0 head is selected; when it is set to low level, the side 1 head is selected. Side 0 stands for the one-sided medium recording surface.
The selection is completed 100 microseconds after the change of the SIDE SELECT signal line, and read/write becomes possible.

(8) MODE SELECT signal line
This signal status selects either 1.6M Byte mode or 1M Byte mode.
The line can be configured in positive or negative logic by position of short plug.

Output Signals

(1) INDEX signal line
Whenever the disk rotates once, this signal line outputs a low level pulse indicating the start of the track. A decline of the pulse signal (when this signal line changes from high level to low level) indicates the start of the track. However, the pulse is only output when the disk is inserted.

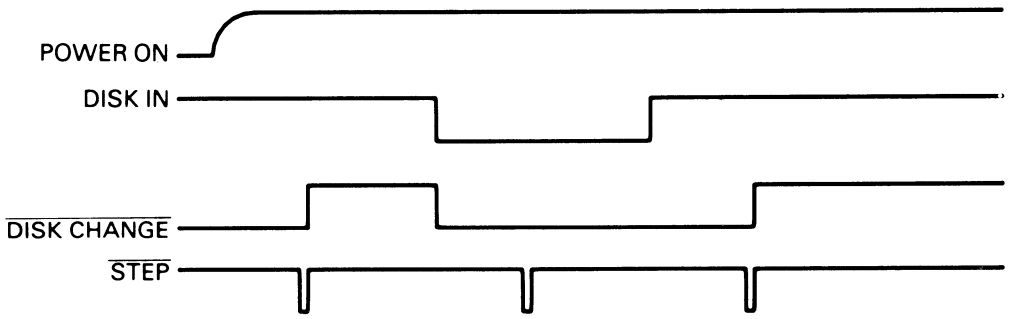
(2) TRACK 00 signal line
When this signal line is set to low level, the head is located at the track 00 position and the specific phase of the stepping motor is excited.

(3) WRITE PROTECT signal line
When this signal line is set to low level, the inserted disk cannot be written on. This signal line may also be set to low level even when no disk is inserted in the drive. The write function of the drive becomes inoperative when write-inhibited disk is inserted.

(4) READ DATA signal line
This signal line is used for the transfer of the pulse series read from the disk, in which clock pulses and data pulses are mixed. The negative-going edge (the moment of change from high level to low level) of the pulse output at this signal line indicates the readout data (clock and data pulses).

(5) READY signal line
When this output signal line is set to low level, the disk is inserted and the number of disk rotations is fixed.
When the READY signal is ON, read and write operations can be performed on the disk. Immediately after the MOTOR ON signal is turned ON, power is supplied. After the disk is inserted, check that the READY signal is ON before performing write and read operations.

(6) DISK CHANGE signal
This signal line is set to low level by power on or when a disk is ejected, and set to high level by STEP signal input when a disk is loaded.

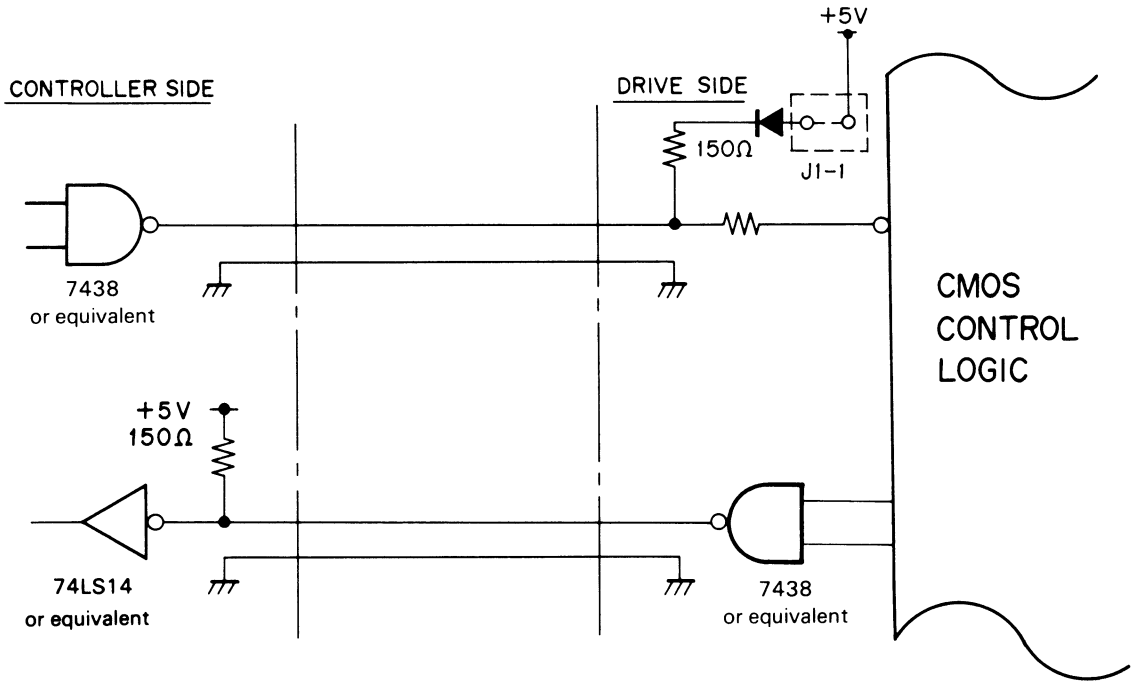


Input Signal Line Terminator

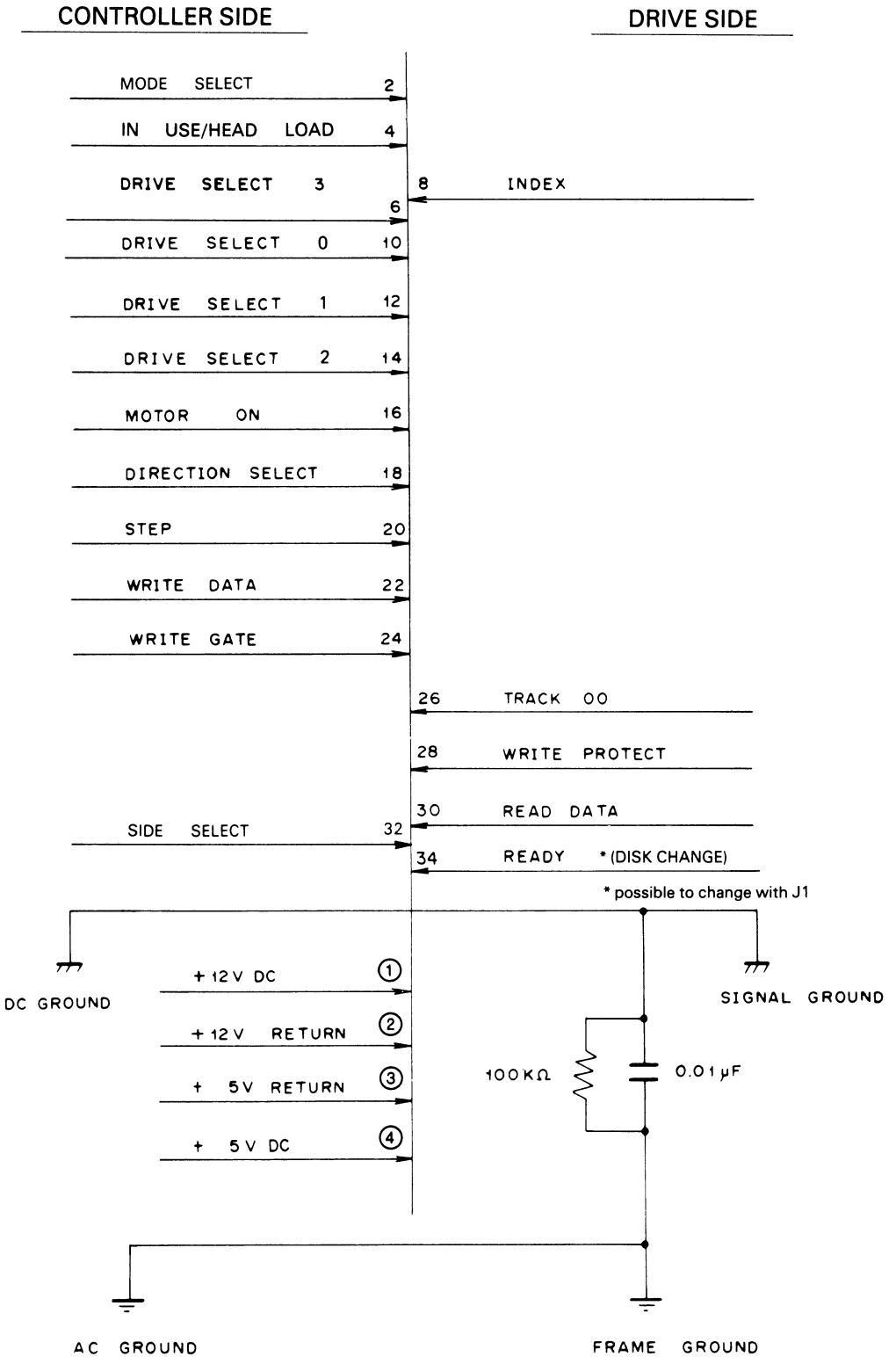
The FZ-506 is operable with either daisy chain or star chain systems. It is possible to use 4 pcs. Drives by daisy chain. When more than one drives are connected, termination resistors of all drives except the drive at the end of interface cable must be disconnected. (The termination resistors can be disconnected by taking away the short-plug at the connector J1-1) Each of the input signal lines has a 150Ω terminal resistor.

Interface Circuit

(1) Drives-receivers
When recommend the following drivers-receivers.

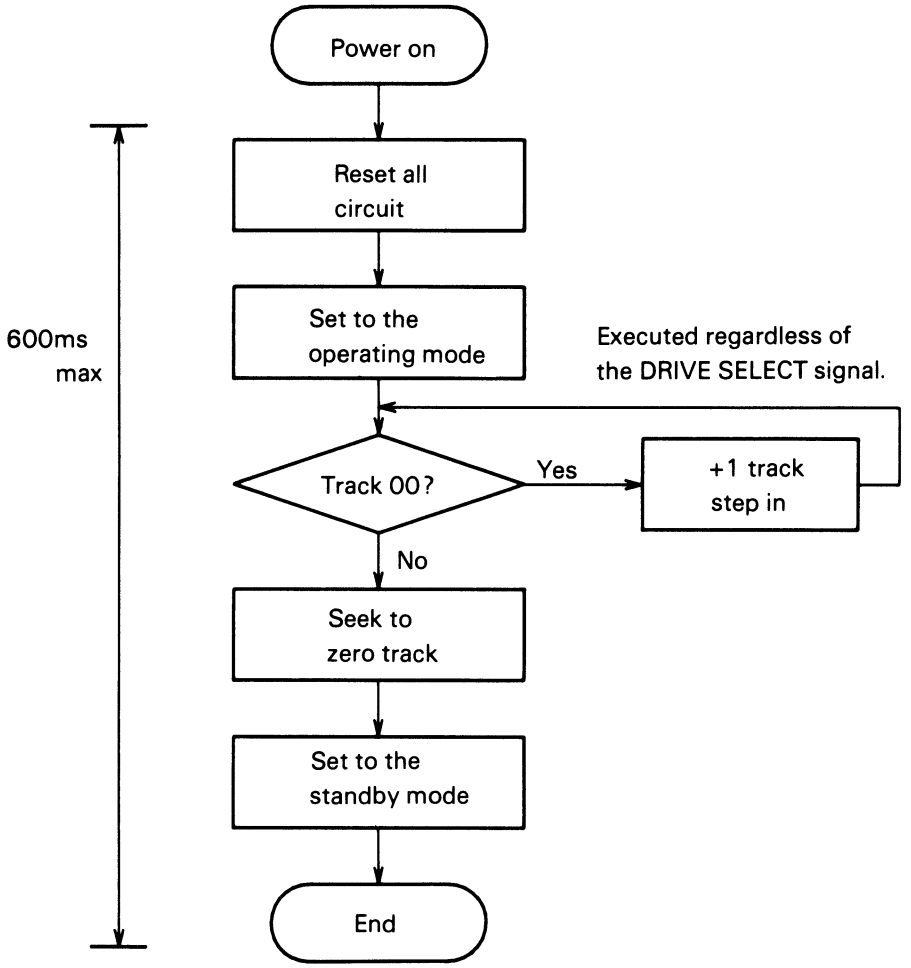


(2) Wire material
Flat cables or twisted pair wires


CONTROLLER SIDE
DRIVE SIDE
MODE SELECT 2
IN USE/HEAD LOAD 4
DRIVE SELECT 3 6
8 INDEX
DRIVE SELECT 0 10
DRIVE SELECT 1 12
DRIVE SELECT 2 14
MOTOR ON 16
DIRECTION SELECT 18
STEP 20
WRITE DATA 22
WRITE GATE 24
26 TRACK 00
28 WRITE PROTECT
30 READ DATA
SIDE SELECT 32
34 READY * (DISK CHANGE)
* possible to change with J1
DC GROUND
+12V DC ①
+12V RETURN ②
+ 5V RETURN ③
+ 5V DC ④
SIGNAL GROUND
100KΩ
0.01μF
AC GROUND
FRAME GROUND

POWER-ON SEQUENCE

Recalibration of the head position is performed during the power-sequence of the FDD. The figure below shows the power-on sequence.



POWER-ON SEQUENCE

POWER SUPPLY INTERFACE

Power Supply Specifications

The DC power (+12V, +5V) shown in Specification is required by the power supply. There are four power lines (+12V, +5V, and the two return lines).

Frame Ground

The frame ground and signal ground are connected through a capacitor and a resistor. The values are as follows:
R = 100 kΩ C = 0.01μF
Connect the frame ground where the AC ground and DC ground are one point connected in the host system.

Power Supply Sequence

(1) The power ON sequence is not specified. However, the time in which the supplied power voltage rises up to 90% of the specified value, should be set to 100 ms or less.

(2) If the drive is in a status other than write operation, and the DC power is disconnected, the disk and the data stored on the disk are not destroyed. However, its contents will be destroyed if the WRITE GATE is not set to high level.

INTERFACE CONNECTOR AND PIN ASSIGNMENT

Interface Connector

(1) DC power connector

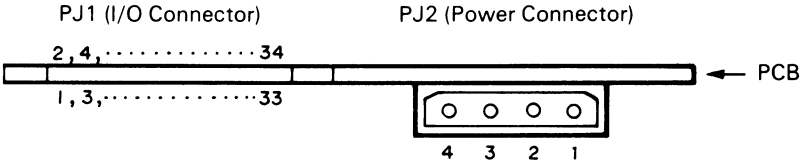
	Drive Side	Host Side
Connector/housing	AMP 172349-1 or equivalent	AMP 1-480424-0 or equivalent
Pin	—	AMP 60619-1 or equivalent

(2) Interface signal connector

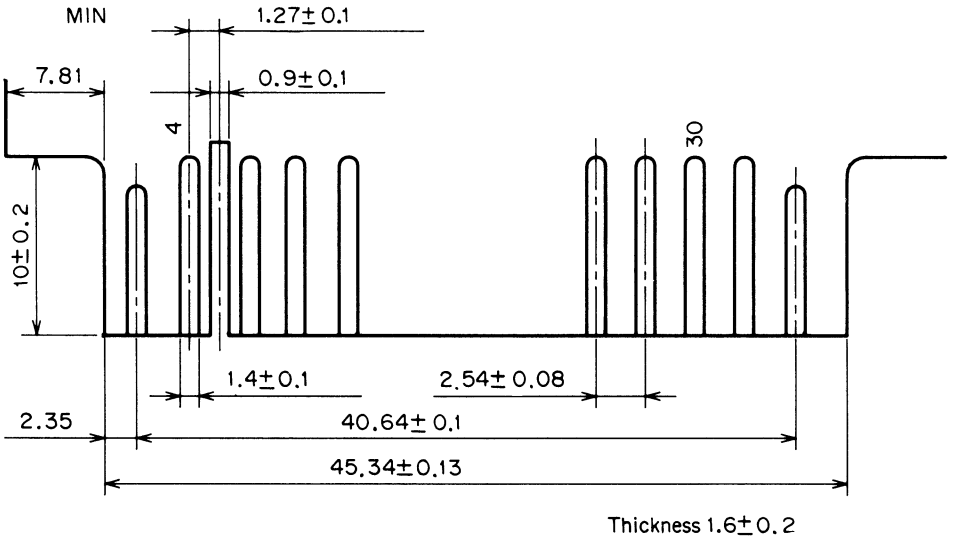
	Drive Side
Connector	Card Edge Connector

Pin Assignment

The assignment of each pin is shown. This diagram shows the back of the drive.



PIN ASSIGNMENT



CARD EDGE CONNECTOR

(1) DC Power connector

Pin number	Signal
1	+12V DC
2	+12V RETURN
3	+5V RETURN
4	+5V DC

(2) Interface signal connector

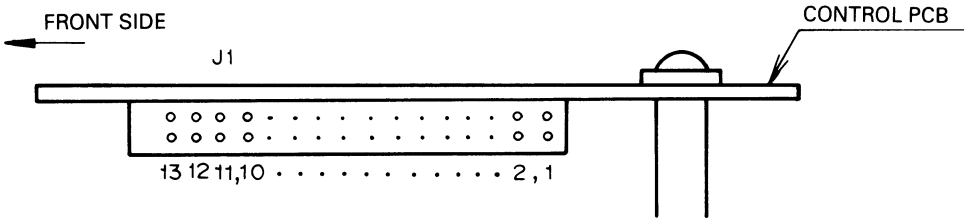
Pin number	Signal	Pin number	Signal
2	MODE SELECT	1	GND
*1 4	IN USE/HEAD LOAD	3	GND
6	DRIVE SELECT 3	5	GND
8	INDEX	7	GND
10	DRIVE SELECT 0	9	GND
12	DRIVE SELECT 1	11	GND
14	DRIVE SELECT 2	13	GND
16	MOTOR ON	15	GND
18	DIRECTION SELECT	17	GND
20	STEP	19	GND
22	WRITE DATA	21	GND
24	WRITE GATE	23	GND
26	TRACK 00	25	GND
28	WRITE PROTECT	27	GND
30	READ DATA	29	GND
32	SIDE SELECT	31	GND
*2 34	READY/DISK CHANGE	33	GND

GND: SIGNAL GROUND
*1: "HEAD LOAD" is optional.
*2: As for switching over between READY and DISK CHANGE, see paragraph 9; SHORT PLUG.

SHORT PLUG AND FRONT LED

Short Plug

The assignment of each pin is shown.



SHORT PLUG

This diagram shows the side of the drive.

CHINON FZ-506 high density 1.6 MB to 1 MB switchable floppy disk drive can be configured in several modes of operation using "SHORT-PLUGS" according to the table below.

Mode descriptions	Connector "J1"											
	1	2	3	4	5	6	7	8	9	10	11	12	13
1.6 MB to 1 MB variable speed switchable using Pin #2 as change-over signal input													
Pin #2: High = 1.6 MB (360 rpm)/Low = 1 MB (300 rpm)	o	o	—	—	—	o	—	o	—	o	—	o	—
*1 Pin #2: High = 1 MB (300 rpm)/Low = 1.6 MB (360 rpm)	o	o	—	—	—	o	—	o	—	—	o	o	—
1.6 MB to 1 MB switchable at 360 rpm, IBM PC/AT compatible, Pin #2 as change-over input	o	—	o	—	—	—	—	—	—	o	—	—	o
	o	—	—	o	—	—	—	—	—	o	—	—	o
Pin #2: High = 1.6 MB (360 rpm)/Low = 1 MB (360 rpm) *2	**o**	**—**	**o**	**—**	**—**	**o**	**—**	**—**	**—**	**o**	**—**	**—**	**o**
1.6 MB 360 rpm non-switchable (Disregards pin #2 signal	o	o	—	—	—	o	—	o	—	—	—	o	—

*1. The short-plug is factory set at this position.

***2. PC40-III Close 1, 3, 6, 10, 13**

12: READY
13: DISK CHANGE
"o" = Position closed
"—" = Position open

Note: Position 1 through 5 of the "J1" are designated as follows.

POS. 1: Connect the termination resistors when closed
POS. 2: Configure the drive as "DRIVE 0" when closed
POS. 3: Configure the drive as "DRIVE 1" when closed
POS. 4: Configure the drive as "DRIVE 2" when closed
POS. 5: Configure the drive as "DRIVE 3" when closed

Note: Only one of the positions 2 through 5 of "J1" can be closed. Above example demonstrates in the case of "DRIVE 0" and the termination resistors connected.

PIN #2: Card-Edge Connector (PJ1)-2

Front LED

The front LED lights when the DRIVE SELECT signal selected by the short plug is set to low level.

Handling of Connectors

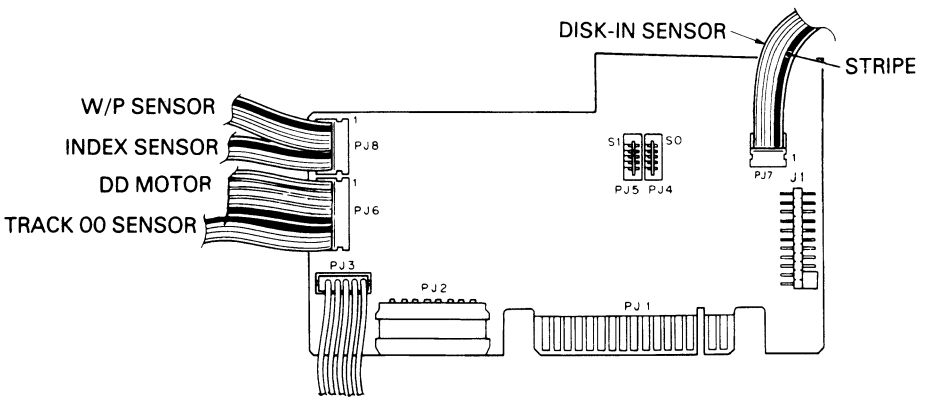
(1) Types of connectors

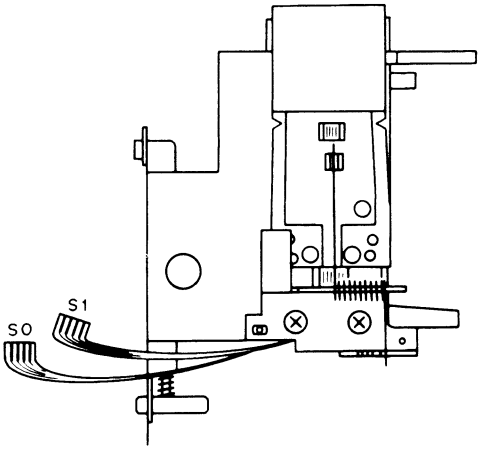
1. PJ1 : Interface connector (34-pin, card-edge type)
2. PJ2 : Power connector
3. PJ3 : Stepping motor connector
4. PJ4, 5 : Head connectors
5. PJ6 : DD motor connector and track 00 sensor connector
6. PJ7 : Disk-in sensor connector
7. PJ8 : Frond LED connector and index, write protect sensor connector
8. J1 : Short pin connector (13-pair) for drive selection

(2) Removal of connector wire
Be sure that power switch is turned off whenever inserting or removing the connector wire, etc. Pull out the connector wire can be removed from the connector on the PC board.

(3) Insertion of connector wire
Each connector wire should be set in a proper position as shown in Fig.
Also, as each wire has a stripe on one side make sure to insert so that the striped side is the same side as the pin no. 1 of the connector.

(4) Insertion of head FPC
Side 0 and side 1 of the head FPC are shown in Fig. Make sure to properly insert side 0 FPC into connector PJ4 of control PCB and side 1 FPC into connector PJ5.





Functions of Test Points

The following eight test points (with GND) are provided on the control board, each of which is used in observing the waveform for FDD adjustment or check.

(1) TP1, TP2 (pre-amp output) and TPC (analog GND)
These are the test points of the read amp output.
Amplified about 200 times by pre-amp, the signal from the head can be observed at TP1 and TP2 through LPF.
TP1 and TP2 are 180° phase off (inverted phase).
For accurate waveform observation, it is necessary to add the signals of both channels together (the signal of the one channel is inverted in phase) to observe these signals as one waveform using an oscilloscope with two channels. TP3 is used in grounding the oscilloscope.
TP1 and TP2 are used in checking the read/write head for its different characteristics or in checking and adjusting the tracking alignment, and the index burst timing.

(2) TP4 (read data signal)
This is the test point of the read data pulse. The READ DATA signal appears here.
In FM mode, a data signal with 2F or 1F period is observed, while MFM mode, a data signal with 2F, 1.5F or 1F period is observed. (See Table)
This test point is used in check of asymmetry.

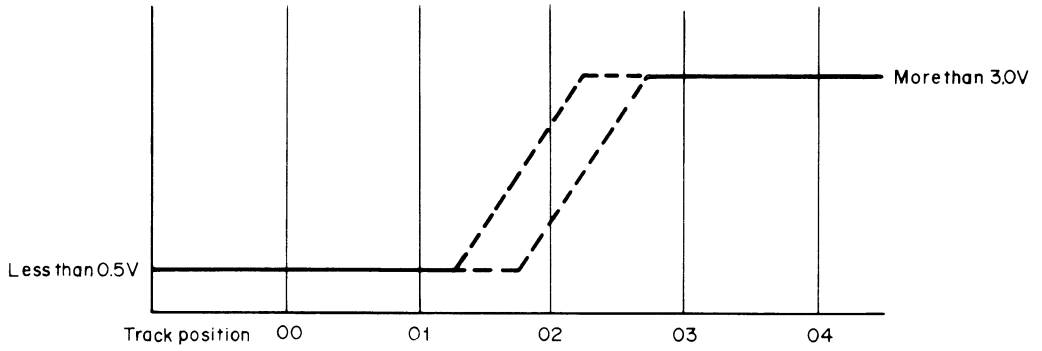
Mode / Frequency	1 MB	1.6 MB
2F	4 μs	2 μs
1.5F	6 μs	3 μs
1F	8 μs	4 μs

(3) TP5 (index sensor)
This is the test point of the index sensor photo-transistor output. A waveform with soft leading and trailing edges appears here, since the sensor output signal is taken out before flowing across the Schmitt inverter. Here it is necessary to check that the output voltage of the index sensor is normal (with no waveform split).

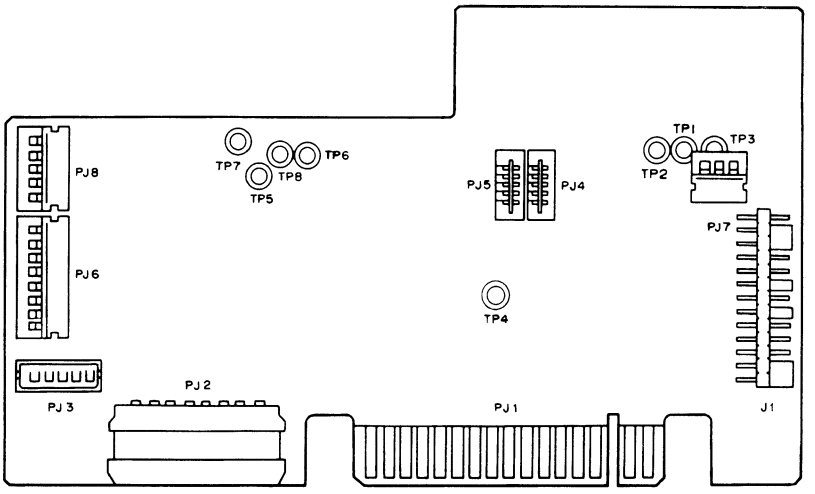
(4) TP6 (write protect sensor)
This is the test point of the write protect sensor photo-sensor photo-transistor output. The WRITE PROTECT output signal appears here. With a disk in which a measure for write protection is taken (its notches are masked), it becomes low level.
The voltage at this test point should be more than 3 V in the write enable state (the notches are open) and less than 0.5 V in the write protect state.
This test point is used in check of the write protect sensor.

(5) TP7 (Disk-in sensor)
This is the test point of the disk-in sensor photo-transistor output.
This signal becomes low level when a disk is inserted into the FDD.

(6) TP8 (track 00 sensor)
This is the test point of the tract 00 sensor photo-transistor output. The voltage at this test point should be within the range shown in the Figure on the following page.



Adjust so that the level of the sensor output changes between track 01 (Low level) and track 03 (High level)



TEST POINTS AND CONNECTORS ON THE CONTROL PC BOARD ASSY.

NOTE: When the various signals are extracted, proper test pin should be mounted at the test point since the test point is not equipped with the test pin.
Sufficient caution should be taken for the mounting of test pin and wiring of signal lines because it may cause damage if test pin and other places are short circuited.

INSTALLING THE OPTIONAL COMMODORE 910 and 920 FLOPPY DRIVES

In addition to following the general installation instructions given in the manuals for the Commodore 910 and 920 floppy drives the user must also perform the specific procedures for PC40-III installation described below.

Commodore 910 Floppy Drive

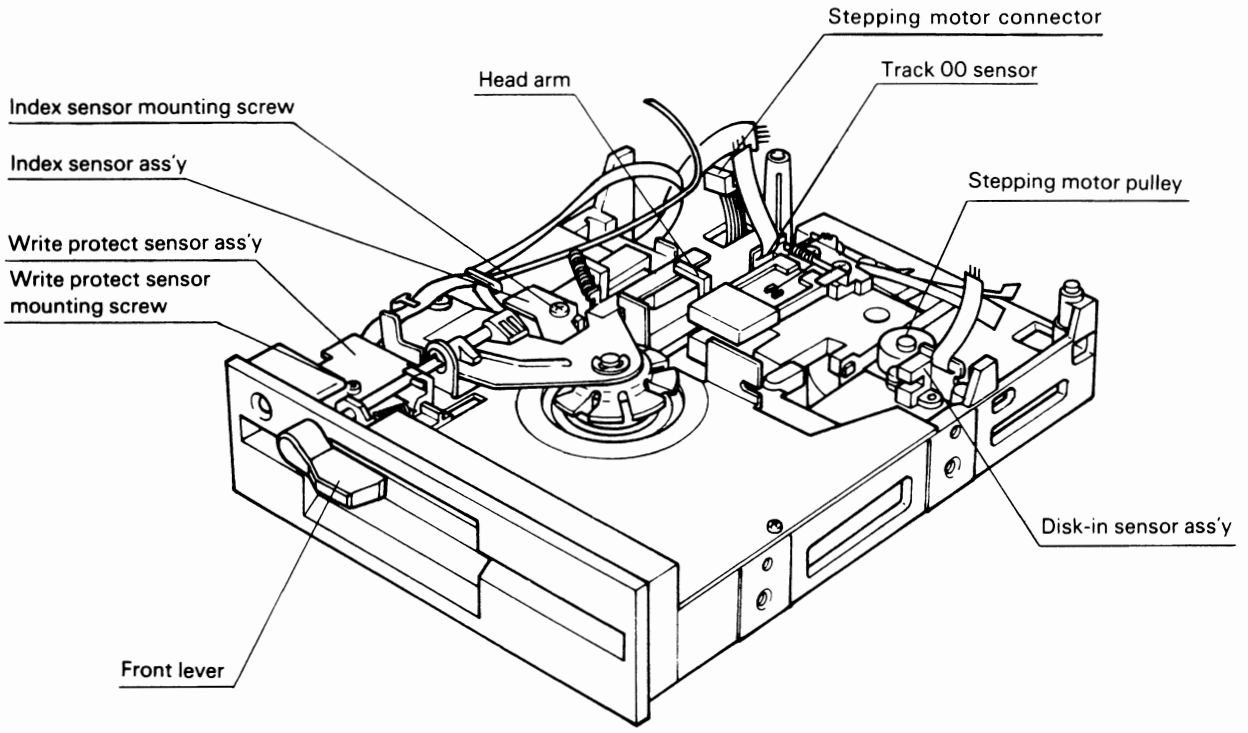
To install the Commodore 910 3.5 inch 720Kb drive as Drive B: in the PC40-III, the user must do the following:

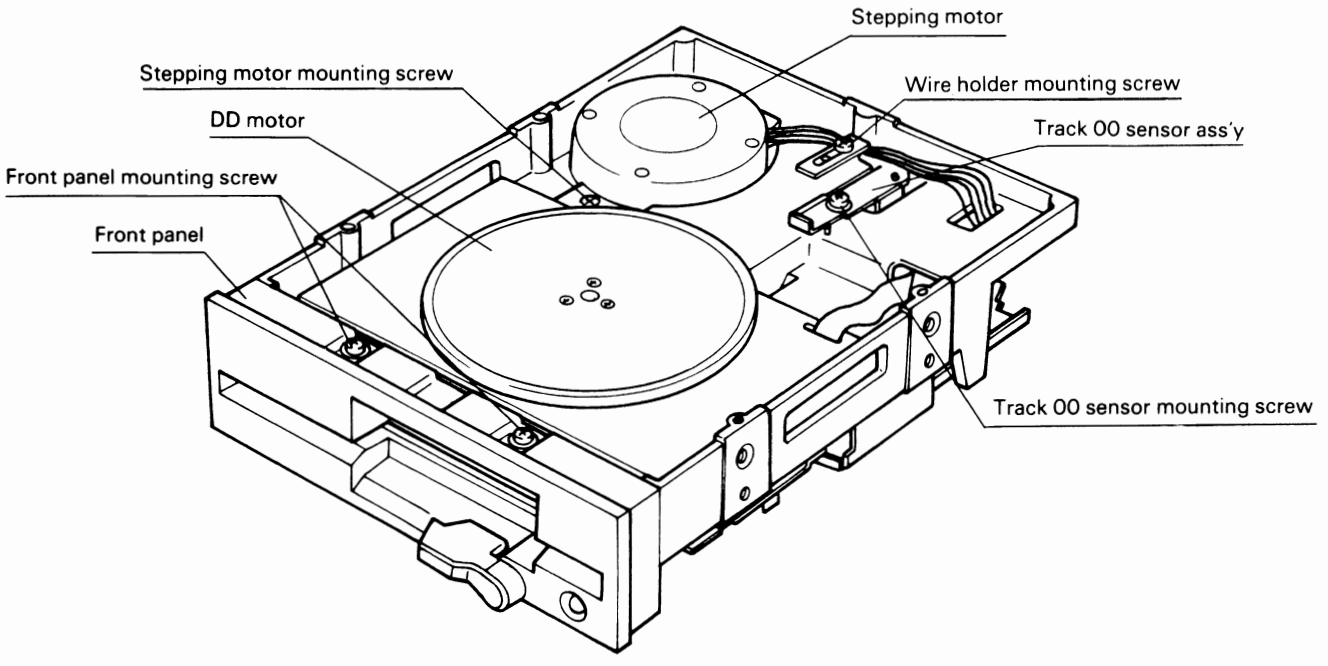
- Set the drive select jumper to position I.
- The M jumper should be in position 5.
- The R-D jumper should be in position 6.
- The first time you power up, use the Setup utility to identify your second drive (Diskette 2 on the menu) as a **720Kb 3.5** drive.

Commodore 920 Floppy Drive

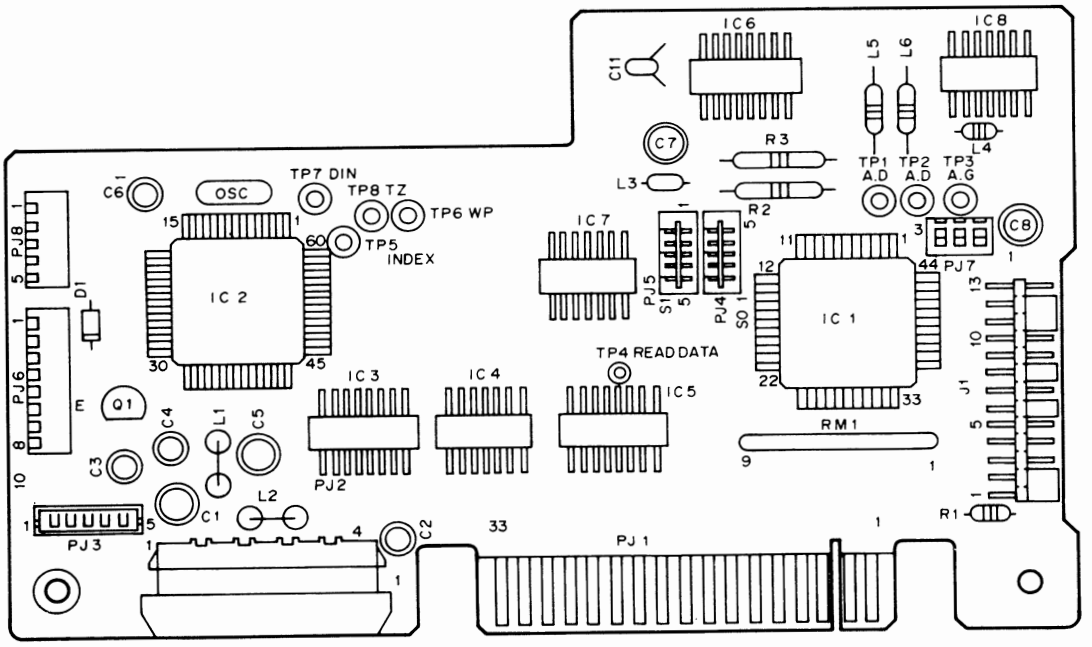
To install the Commodore 920 5.25 inch 360Kb floppy drive as Drive B: in the PC40-III, the user must do the following:

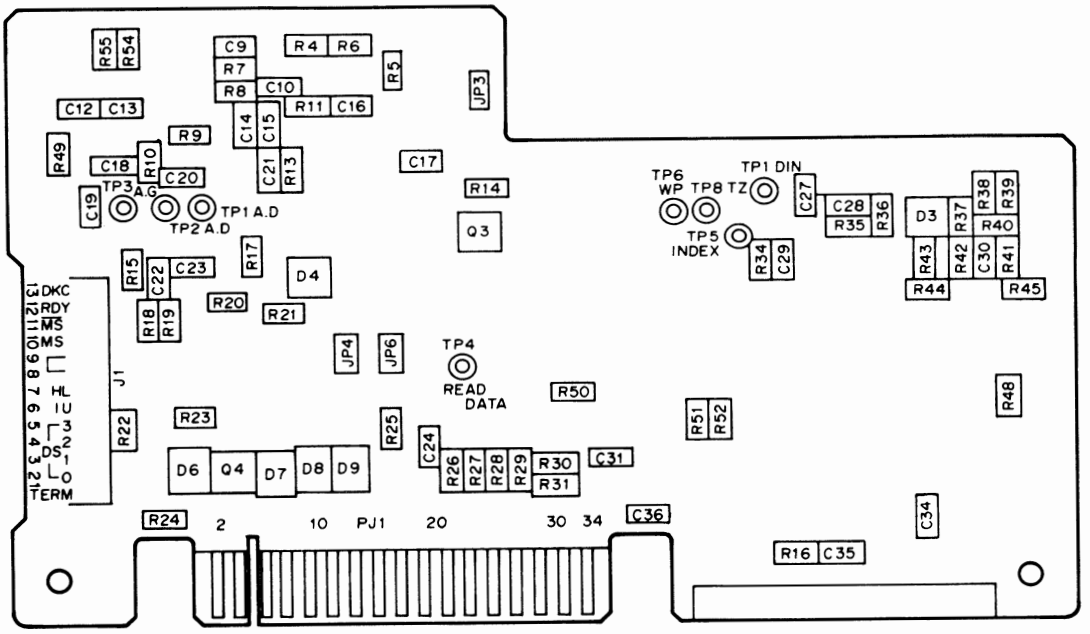
- Set the drive select jumper to position 1.
- Cut JP6 (located on the bottom side of JP1) in half.
- The first time you power up, use the Setup utility to identify your second drive as a **360Kb 5.25** drive.


Stepping motor connector
Track 00 sensor
Head arm
Index sensor mounting screw
Index sensor ass'y
Stepping motor pulley
Write protect sensor ass'y
Write protect sensor mounting screw
Disk-in sensor ass'y
Front lever


Stepping motor
Stepping motor mounting screw
Wire holder mounting screw
DD motor
Track 00 sensor ass'y
Front panel mounting screw
Front panel
Track 00 sensor mounting screw

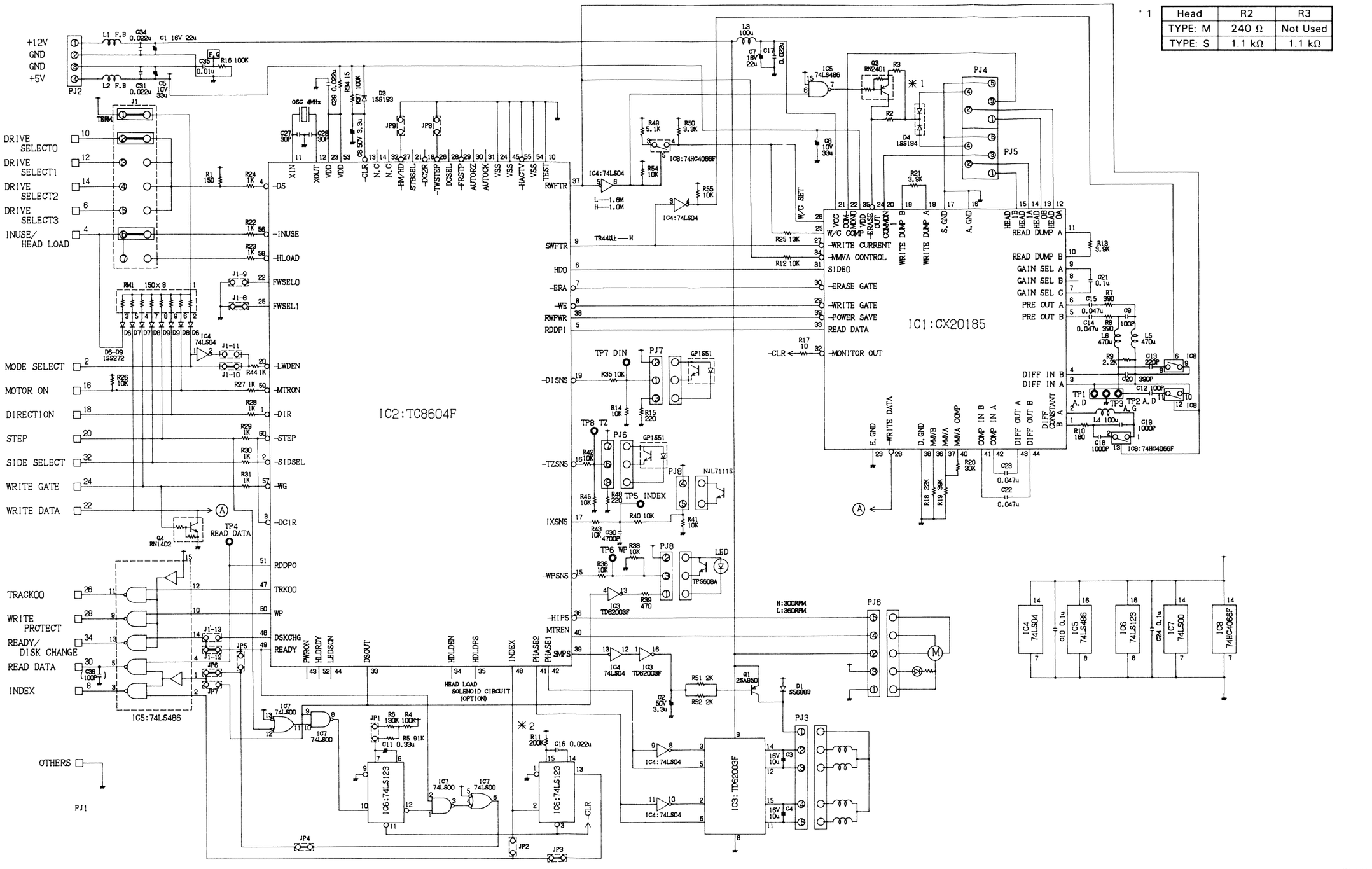
Location of Electrical Parts





SCHEMATIC DIAGRAM FOR CHINON FZ-506

Head	R2	R3
TYPE: M	240 Ω	Not Used
TYPE: S	1.1 kΩ	1.1 kΩ



APPENDIX C

KEYBOARD SECTION

INFORMATION IN THIS SECTION IS FOR REFERENCE ONLY.
COMMODORE WILL NOT SUPPLY COMPONENT PARTS FOR OEM ASSEMBLIES.

PC40-III KEYBOARD — OPERATIONS

THE COMMODORE PC40-III KEYBOARD

The Commodore PC40-III keyboard is divided into four sections:

— ***the Typewriter Area***
— ***the Special Key/Cursor Key area***
— ***the Numeric Keypad***
— ***the Function Keys***

In using the Commodore PC40-III keyboard, note that:

— *All the keys (except for the special keys) repeat as long as they are held down.*
— *You cannot interchange either the numeral zero (0) and the upper case letter O, or the numeral 1 and the lower case letter l.*
— *Keys may be program controlled. This means that their use is defined by the operating system, programming language or application software currently being used. The description of the specific function of these keys can be found in the* ***MS-DOS User's Guide/User's Reference*** *manual, or in the manual for the particular software being used.*

In this appendix, whenever combinations of keys are to be pressed, the names of the keys to be pressed are separated by a hyphen. For example, Ctrl-Alt-Del means hold the Ctrl and Alt keys down and then press the Del key at the same time. See Appendix C for a list of special key sequences used in MS-DOS.

The following pages describe each area of the keyboard, including definitions of the individual keys in each area. To make full use of your PC40-III computer, you should become familiar with the names, locations and functions of all the keys.

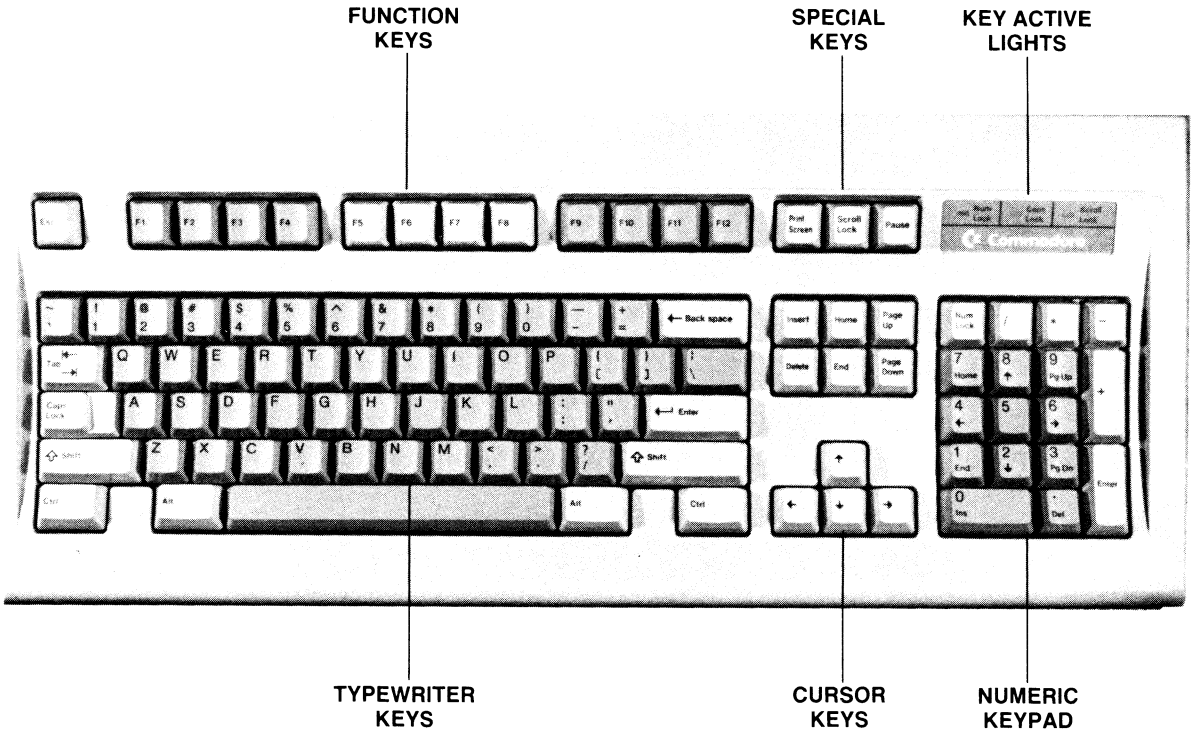


FIGURE D-1. THE COMMODORE PC40-III KEYBOARD
THE COMMODORE PC40-III KEYBOARD

THE NUMERIC KEYPAD

The Numeric Keypad is at the far right of the Commodore PC40-III keyboard. The keys in this section of the keyboard usually function as number and mathematical keys as long as the Num Lock light is on. With the Num Lock light off, you can use certain keys to control the position of the cursor on the screen and perform some special functions. Note that many of the functions of keys in the Special Key/Cursor Key area are available in the Numeric Keypad.

The NUM LOCK Key

When the computer is turned on, the Num Lock indicator light located above the Numeric Keypad goes on and the numeric keys 0 through 9 are locked into the numeric functions. To turn off Num Lock, press the Num Lock key and this light goes out.

The non-numeric functions on the Numeric Keypad keys (such as scrolling the cursor by using the 2, 4, 6 and 8 keys) can be obtained while Num Lock is on by holding down the Shift key and pressing the required key.

Controlling the Cursor from the Numeric Keypad

You can control cursor movement from the Numeric Keypad by using the 2, 4, 6 and 8 keys, as follows:

— *the 8 key moves the cursor up*
— *the 2 key moves the cursor down*
— *the 6 key moves the cursor to the right*
— *the 4 key moves the cursor to the left*

The cursor moves one line or one character position for each time a key is pressed. The cursor will move continuously as long as you are holding down a key.

The HOME key

This key (the 7 key) moves the cursor to the top left corner of the screen, which is known as the Home position.

The END key

This key (the 1 key) places the cursor one character position to the right of the last character on the line.

The PG UP key

The Pg Up (for "Page Up") key (the 9 key) is a program controlled key that moves the cursor to the previous page (a full page is 25 lines).

The PG DN key

The Pg Dn (for "Page Down") key (the 3 key) is a program controlled key that moves the cursor to the next page.

The INS key

Pressing the Ins (for "Insert") key (the 0 key) turns the Insert function on. Any characters typed while the Insert function is on are inserted at the cursor position. To turn the Insert function off, press the Ins key again. Any characters typed when Insert is off appear at the cursor position, overwriting (i.e., deleting) any character already at the cursor position.

The DEL key

Pressing the Del (for "Delete") key (the decimal point key) deletes the character at the cursor position. The cursor remains at that position and all the characters to the right of it move one position to the left.

*The +, −, * and / keys*

These keys are used for mathematical functions: + for addition, − for subtraction, * for multiplication and / for division. Pressing any one of these keys causes the selected sign to be displayed.

The ENTER key

You can press the Enter key on the Numeric Keypad to transmit a command or information to the computer. In other words, pressing this key has the same effect as pressing the Enter key on the main keyboard. This can be a program controlled key.

THE FUNCTION KEYS

The Function Keys are the keys located in the horizontal row of keys above the Typing Area, and marked F1 through F12. These keys are program controlled keys — that is, their use is controlled by whatever software you are currently using.

The DELETE key

Pressing the Delete key deletes the character at the cursor position. The cursor remains at the position and all the characters to the right of it move one position to the left.

The HOME key

This key moves the cursor to the top left corner of the screen, which is known as the Home position.

The END key

This key places the cursor one character position to the right of the last character on the line.

The PAGE UP key

The Page Up key is a program controlled key that moves the cursor to the previous page (a full page is usually 25 lines) in the program.

The PAGE DOWN key

The Page Down key is a program controlled key that moves the cursor to the next page in the program.

Controlling the Cursor from the Cursor Keypad

Cursor movement is program controlled — that is, cursor movement is defined and enabled by the operating system or application software currently being used. **Note that in MS-DOS only the left and right cursor keys are active.**
There are four cursor keys located in the Cursor Keypad located at the bottom of the keyboard, between the Typewriter Area and the Numeric Keypad. You can also move the cursor by using the 2, 4, 6, and 8 keys in the Numeric Keypad (see below). The cursor is controlled from the Cursor Keypad as follows:
— *the up arrow key moves the cursor up*
— *the down arrow key moves the cursor down*
— *the right arrow key moves the cursor to the right*
— *the left arrow key moves the cursor to the left*
The cursor moves one line or one character position for each time a key is pressed. The cursor will move continuously as long as you are holding down a key.

THE SPECIAL KEY/CURSOR KEY AREA

This area contains 13 keys, including a four key cursor keypad at the bottom and some special keys. Certain keys have dual functions (e.g., Pause/Break).

The PRINT SCREEN/SYSTEM REQUEST key

This is a dual function key. The Print Screen (PrtSc) function is used to give a printed copy of the information displayed on the screen. Alpha/numeric characters displayed on the screen, such as program listings, can be printed on any type of printer (daisy wheel, dotmatrix, laser, thermal, ink jet, etc.) printers. Graphics information cannot be reproduced on a daisy wheel printer and, depending on the software being run, may require a specific printer driver to be rendered fully. . .
The System Request (SysRq) function is program controlled.

The SCROLL LOCK Key

This is a program controlled key. It is used typically to halt the scrolling of information on the screen. Usually, to resume scrolling, you press the key again.

The PAUSE/BREAK key

This is a dual function key. The Pause function is used typically to halt program execution temporarily.
The Break function is program controlled. It is activated by pressing Shift and Pause together. Under MS-DOS, Ctrl-Break has the same function as Ctrl-C: that is, it aborts the command currently being executed. In GW-BASIC, the Break key is used with the Ctrl key (i.e., in a Ctrl-Break sequence) to stop a program when it is running.

The INSERT key

Pressing the Insert key turns the Insert function on. Any characters typed while the Insert function is on are inserted at the cursor position, without overwriting (i.e., deleting) any character already at the cursor position. To turn the Insert function off, press the Ins key again. Any character typed when Insert is off appears at the cursor position and overwrites any character already at the cursor position.

The ALT key

There are two Alt (for "Alternate") keys, located at either end of the Space Bar in the bottom row of typing keys.

The Alt key has a number of uses:

- Pressing the Alt key simultaneously with the Ctrl and Del keys restarts (or "reboots") MS-DOS.
- Within the GW-BASIC Interpreter, holding down the Alt key and pressing a single alphabetic key A through Z allows you to enter a GW-BASIC keyword automatically. This is fully described in the GW-BASIC Manual.
- Special characters can be entered using the Alt key and the number keys on the numeric keypad to the right of the main keyboard. Hold down the Alt key, type the three digit ASCII code for the required character and then release the Alt key. The character is then displayed. A list of ASCII character codes is shown in Appendix C of the *GW-BASIC User's Guide.*

The CTRL key

There are two Ctrl (for "Control") keys, located at either end of the bottom row of typing keys. The Ctrl key is a program controlled key. It is also used in conjunction with other keys to perform various control functions for MS-DOS.

The ESC key

The Esc (for "Escape") key, located at the far left of the top row of the keyboard, is a program controlled key.

The TAB key

This is the key with small horizontal arrows pointing left and right. The Tab key is located at the far left of the second from the top row of the typing keys. This key is used to set and remove tabs.

The Space Bar

This is the large key extending most of the way across the bottom of the main keyboard. This key is similar in location and function to the space bar on a typewriter. The Space Bar moves the cursor to the right, inserting spaces as it moves. If there are any characters in the path of the cursor movement, they are erased.

THE TYPEWRITER AREA

The Typewriter Area contains a standard (QWERTY) typing keyboard and some additional keys.

The SHIFT keys

There are two Shift keys in the Typewriter Area. They are oversized keys with an upward pointing arrow, and are located at each end of the row above the Space Bar. Holding down either Shift key and pressing any of the alphabetic keys causes the letter shown on that key to be displayed in upper case. In addition, the Shift keys are often used with other keys to perform special functions.

If the Caps Lock or Num Lock light is on, pressing the SHIFT key cancels the effect. For example, if Caps Lock is on and you hold down the SHIFT key and press the A key, then the lower case letter (i.e., a) is displayed.

The CAPS LOCK key

Pressing the Caps Lock key at the left side of the middle row of typing keys locks the characters A through Z into the upper case position. When you first press the Caps Lock key, an indicator light located above the Numeric Keypad goes on. To release the Caps Lock key, you press the key again and this light goes out.

Lower case characters can be obtained while the Caps Lock light is on by holding down the SHIFT key and pressing the required letter key.

The BACKSPACE key

This is an oversized key located on the far right side of the top row of the main keyboard, and having a small horizontal arrow pointing left. Pressing the Back space key causes the character to the LEFT of the cursor to be erased, while the cursor and any characters to the RIGHT of the cursor move one position to the left.

The ENTER key

There are two Enter keys: one on the main keyboard, and one in the Numeric Keypad. The Enter key on the main keyboard is located at the right side of the middle row. On the top of this key is a right-angled arrow that points left. You must press the Enter key to transmit a command or information to the computer. The Enter key (which can be program controlled) may be referred to as a Return key or as a CR (Carriage Return) key in some program documentation.

PC40-III KEYBOARD — HARDWARE

Commodore P/N	Country
312702-01	United Kingdom
312709-02	United States
312702-03	German
312702-04	Italian
312702-05	French
312702-06	Spain
312702-07	Dutch
312702-08	Denmark
312702-09	Norway
312702-10	Sweden/Finland

Key Scan Codes

All keys have two different 8 bits codes, a "Make" -code and a "Break" -code. (except ‡-marked keys)
These codes only differ in the MSB (bit 7).
Make-code : MSB = 0
Break-code : MSB = 1
A "Make"-code is transmitted once a key is depressed.
A "Break"-code is transmitted for any released key.
‡-marked keys have custom output codes.
See code table-4.

Clock and Data Signals

(1) Data — The transmitted serial data that consists of 1 start bit followed by 8 bits scan code. Data is transmitted LSB first.

(2) Clock — The synchronizing signal that gives timing to nine bits of transmitted data.

16 Characters FIF0 Buffer

The keyboard has a 16 characters FIF0 buffer for serial data transmission.
When a key is on or off, the corresponding code is once stored into FIF0 buffer in accordance with the regular sequence of switch-on or switch-off keys and then transmitted in the sequence. However, the keys after 16th keys are ignored on account of buffer full.

Auto repeat function

The keyboard has auto-repeat feature on all keys.
When a key is depressed, the corresponding "Make"-code is transmitted with clock. If the key is held down for more than 500 ms with any other keys off, the keyboard keeps on sending the code with clock at the rate of 10.89 characters per second until the data key is off or another new key is on.
In case of the plural key on, only the last on-key data code is transmitted like that.

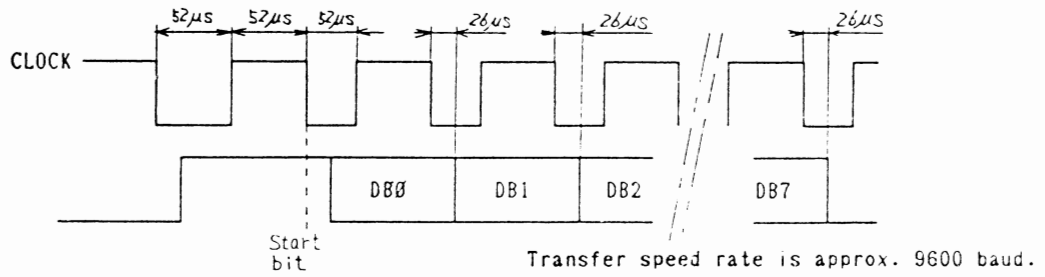
Handshake feature

The keyboard senses the clock line at intervals of approx. 10 ms during key scanning. On sensing the clock line low, resenses the line low or not for approx. 3.5 ms.
Confirming the line low, stops key-scanning and transmitting the data. After that the keyboard waits until the clock line high. The line high, sends status data "Hex AA". Then the keyboard clears FIF0 buffer and all LEDs get dark.

Caps Lock, Num Lock and Scroll Lock indication

Depressing the "Caps-Lock", "Num-Lock", and "Scroll-Lock" keys turn on each of their LED's indication.
The color of these LED's is green.
This state is latched until the key is depressed for the second time. Pressing the "Caps-Lock", "Num-Lock" and "Scroll-Lock" keys, in conjunction with the "Ctrl" key is not toggle each of their LED's status. If the clock line is tied low for more than 3.5 ms, these LEDs are turned off after the clock line high.

Data format



ELECTRICAL REQUIREMENT

Device Description	Parameter
Keyswitch Contact	12 Vdc with 200 micro-second pulse width 1/50 duty cycle 1 mA maximum rating.
Keyswitch Bounce	5 millisecond initial, 10 millisecond over lifetime.
Keyswitch Contact Resistance	1,000 ohms - maximum
Keyswitch Capacitance	500 pF - maximum
Withstanding Voltage (Dielectric)	250 Vac @ one (1) minute
Voltage - Vcc	+5 Vdc, ±0.25 Vdc
Current	300 mA - maximum
Output Logic	"1" = 2.4 Vdc - minimum; "0" = 0.4 Vdc - maximum
Rollover	N-Key rollover shall be provided on all keyswitches.
Reset	Keyboard circuitry shall allow for internal power on reset.

MECHANICAL PARAMETER

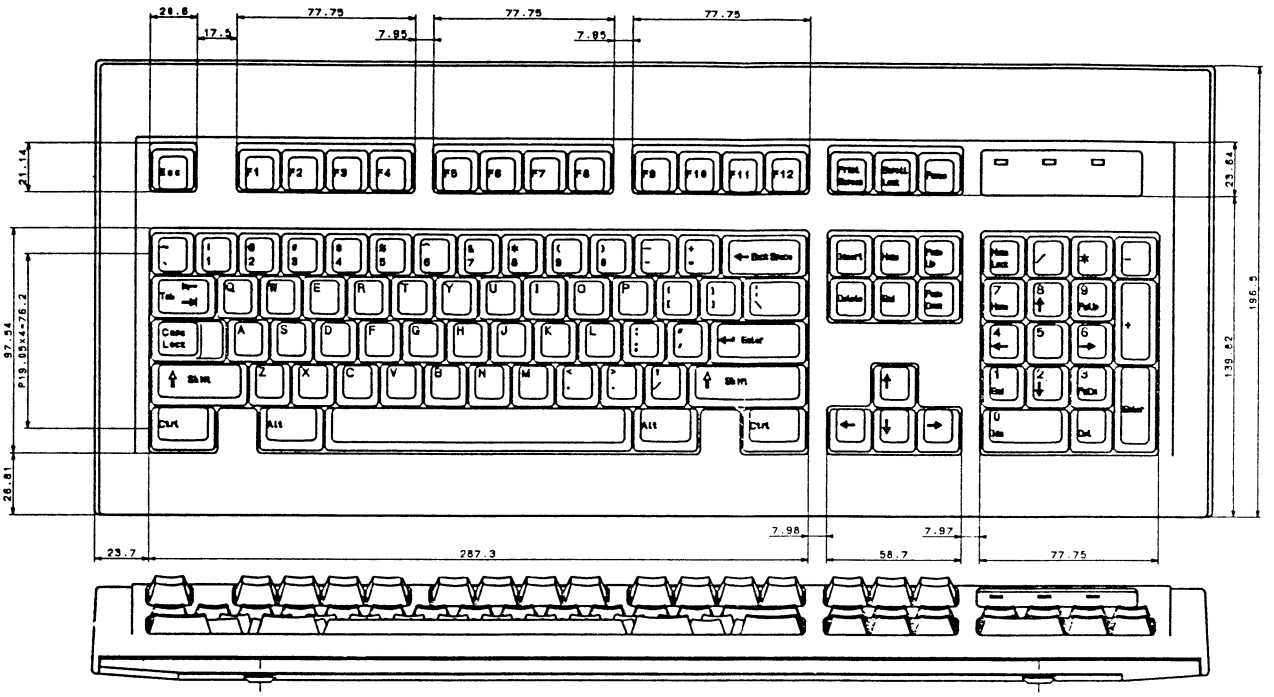
Keyswitches	Requirements
Operating Force	51 grams (Typical)
Zero Travel Force	15 ±10 grams at 0.5mm Travel
Full Travel Force	90 ±25 grams at 0.5mm Above Full Travel.
Key Travel	4.3 ±0.5mm; 4.0 ±0.5mm
Key Wobble	0.7mm, Maximum: (+) 300 grams Force Applied to Top of Key in any Direction.

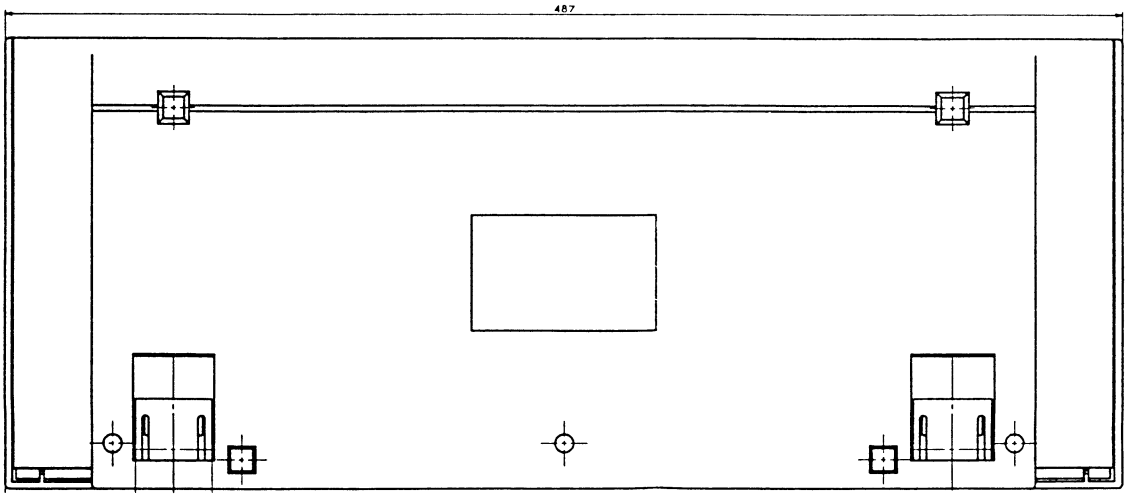
ENVIRONMENTAL SPECIFICATION

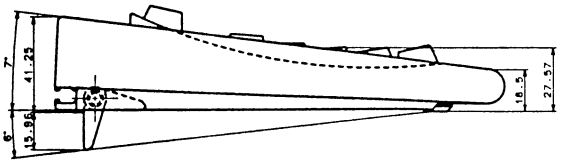
Description	Requirement
Operating Temperature	−5 deg C to +50 deg C
Operating Humidity	20% to 80% RH, non-condensing
Operating Altitude	0 to 3,000 meters
Storage Temperature	−20 deg C to +65 deg C
Storage Humidity	5% to 95% RH, non-condensing
Storage Altitude	0 to 15,000 meters
Shock (impact)	30-G @ 21 mseconds, 1/2 sine, two (2) shocks in each of six (6) planes (directions).

RELIABILITY REQUIREMENT

MTBF: 20,000 Hours MTTR: 0.5 Hour.
Switch Operating Life: Standard Key — Five (5) Million Cycles; Function Key — Three (3) Million Cycles.







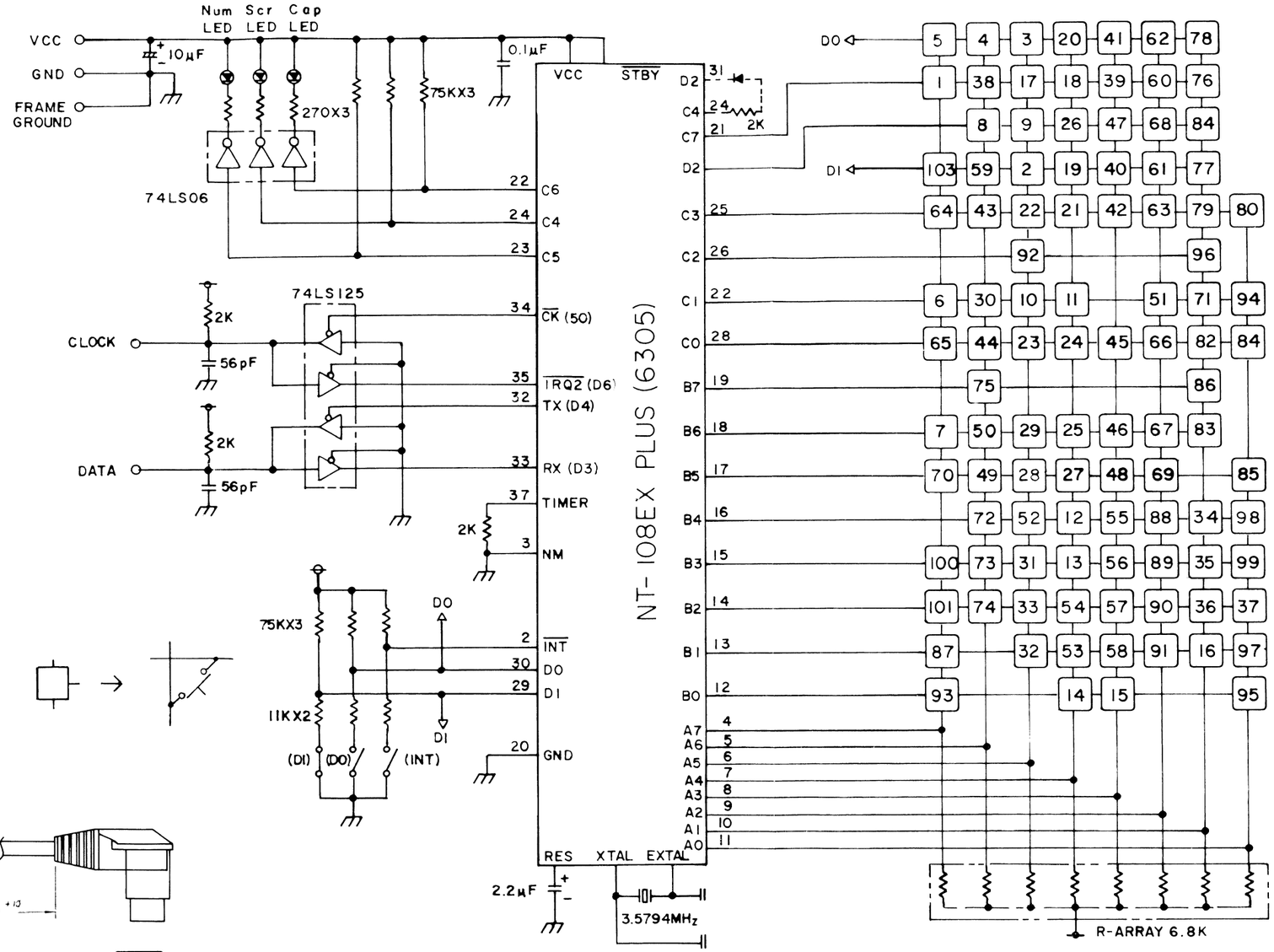
KEYBOARD ARRANGEMENT

FOR REFERENCE ONLY

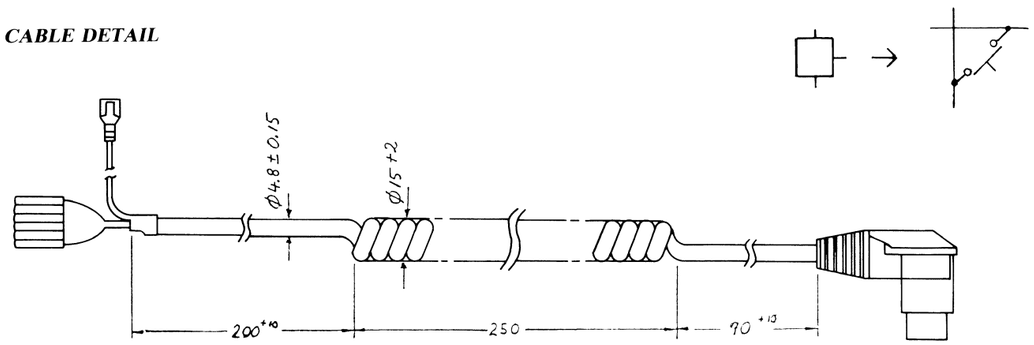
PARTS LIST

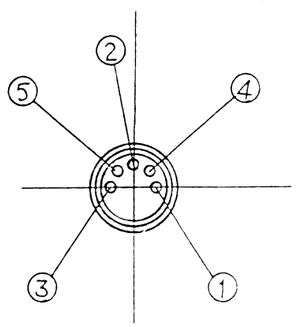
Symbol	Name
IC1	8049 CPU
IC2, 3	7406N
D1, D12	Diode 1S2473
	100kΩ ±5%1/8W
R1, R5	4.7kΩ ±5%1/4W
R6, R8	2kΩ ±5%1/4W
R9, R10	22kΩ ±5%1/4W
R11, R13	270Ω ±5%1/4W
C1	50V 1μF
C1	16V 47μF
C2	16V 4.7μF
C3, C6	12V 0.1μF
C7, C9	50V 1000pF
C10	CSC300
XT	CERA LOCK CSA 6.00MT
LED1, LED3	LED
L1, L2	Choke Coil

CIRCUIT DIAGRAM

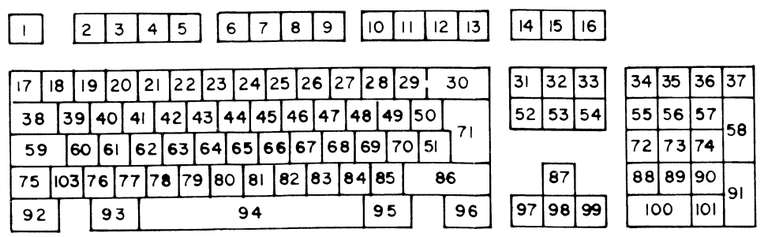


CABLE DETAIL





PIN	Signal
1	CLOCK
2	DATA
3	RESET
4	GROUND
5	Vcc = 5 V



APPENDIX D

OPTIONS SECTION

- **VIDEO PARAMETERS**
- **1403 MONITOR SPECS**
- **1352 MOUSE SPECS**

INFORMATION IN THIS SECTION IS FOR REFERENCE ONLY. COMMODORE WILL NOT SUPPLY COMPONENT PARTS FOR OEM ASSEMBLIES.

PC40-111 VIDEO MODES

VIDEO MODE NOTES

The Onboard Video Adapter is 100% IBM VGA compatible and can also be placed in CGA and MDA hardware compatible video modes. The Hardware MDA mode also is 100% Hercules compatible and will run all Hercules software. The Hardware CGA mode also includes Plantronics mode which can be exploited by any software which understands Plantronics special registers.

The PC40-III video output is always VGA compatible with a 31.5 KHz horizontal rate; vertical rate is either 60 or 70 Hz, depending on the VGA mode.

Dip switches 1, 2 and 3 in the CONFIG Control (located at the rear of the PC40-III) are used to set the default video mode. The switch settings are described clearly on the PC40-III's back label. The choices are as follows:

DISABLE VIDEO	— disables onboard video adapter
MDA/HERCULES	— sets hardware compatible MDA/Hercules mode.
CGA	— sets hardware compatible CGA/Plantronics mode.
VGA AUTO	— detects whether attached monitor is MONO or COLOR: If MONO is detected, VGA mode 7 is set. If COLOR is detected, VGA mode 2 is set. (See Video Mode Characteristics table in this appendix.)
VGA COLOR	— sets VGA color mode 2 by default regardless of monitor.
VGA MONO	— sets VGA mono mode 7 by default regardless of monitor.
132x43	— sets extended 132 column, 43 row text mode regardless of monitor.
132x25	— sets extended 132 column, 25 row text mode regardless of monitor

NOTE: EGA is a subset of VGA. EGA-based software will work when the system is configured as a VGA adapter.

USING THE VMODE UTILITY TO CHANGE VIDEO MODES

The VMODE utility provides a software method to change video modes. Just select the mode you want from the folllowing table: then type the corresponding command and press Enter.

Video Mode	*Command*
Hardware CGA	**Vmode – c**
Hardware MDA/HERC	**Vmode – m**
VGA Color	**Vmode – vc**
VGA Mono	**Vmode – vm**
132x25 Text	**Vmode – t1**
132x43 Text	**Vmode – t2**
Help	**Vmode – h**

Invoking VMODE with the Help key will display the information in the table above, so if you are not sure of a command just type *Vmode -h.*

IMPORTANT: If you change the video mode setting by the hardware method, you must reboot the system before the changes will take effect. Video mode changes made by the VMODE utility or the MS-DOS MODE command will take effect immediately.

VIDEO MODE CHARACTERISTICS

ALPHANUMERIC MODES

MODE #	*COL X ROW*	*CHAR MATRIX*	*RESOLUTION*	*COLORS*	*STANDARD*
0, 1	40 X 25	8 X 8	320 X 200	16	CGA (1)
		9 X 16	360 X 400	16 OF 256K	VGA (2)
2, 3	80 X 25	8 X 8	640 X 200	16	CGA (1)
		9 X 16	720 X 400	16 OF 256K	VGA (2)
7	80 X 25	9 X 14	720 X 350	MONOCHROME	MDA
		9 X 16	720 X 400	MONOCHROME	VGA (2)
54	132 X 43	7 X 9	924 X 387	COLOR	ENHANCED
55	132 X 25	7 X 16	924 X 400	COLOR	ENHANCED
56	132 X 43	7 X 9	924 X 387	MONOCHROME	ENHANCED
57	132 X 25	7 X 16	924 X 400	MONOCHROME	ENHANCED

GRAPHICS MODES:

4, 5	320 X 200	4	CGA (1)
		4 OF 256K	VGA (1 & 2)
6	640 X 200	2	CGA
		2 OF 256K	VGA (1 & 2)
D	320 X 200	16 OF 256K	VGA (1)
E	640 X 200	16 OF 256K	VGA (1)
F	640 X 350	MONOCHROME	VGA
10	640 X 350	16 OF 256K	VGA
11	640 X 480	2 OF 256K	VGA/MCGA
12	640 X 480	16 OF 256K	VGA
13	320 X 200	256 OF 256K	VGA/MCGA

NOTES:

(1) All 200 line modes are double scanned for 400 line resolution.

(2) The VGA implementation of these modes is the default.

VIDEO SIGNALS

Vertical	Horizontal sync		Vertical sync	
Resolution	**Frequency**	**Polarity**	**Frequency**	**Polarity**
350 lines	31.5 KHz	+	70.1 Hz	–
400 lines	31.5 KHz	–	70.1 Hz	+
480 lines	31.5 KHz	–	59.9 Hz	–
600 lines*	35.2 KHz	–	56.2 Hz	–

**Requires an Analog MultiSync® compatible monitor.*

HERCULES GRAPHICS MODE — PROGRAMMING NOTES

This mode is essentially a bitmapped version of the MDA. The video dot clock (16.257 Mhz) and the screen resolution (720x348 pixels) are identical. The memory requirement to hold one full display is just less than 32Kbytes: therefore, two display pages are available.

Page0: address b000:0000h to b000:7FFFh

Page1: address b000:8000h to b000:FFFFh

NOTE: Page 1 occupies address space used by CGA video memory. DO NOT switch to this page if an EXPANSION CGA adapter is installed. Hardware damage to the EXPANSION card or the motherboard may result!

The relevant registers are:

Hercules Enable Register - I/O addr 3bfh

bit0: 0 - disable setting graphics mode
1 - enable setting graphics mode

bit1: 0 - disable changing graphics pages
1 - enable changing graphics pages

Mode Register - I/O addr 3b8h

bit1: 0 - disable Hercules mode (default MDA)
1 - enable Hercules graphics

bit3: 0 - video disable
1 - video enable

bit5: 0 - blink disable
1 - blink enable

bit7: 0 - Hercules Page0
1 - Hercules Page1

Hercules 6845 CRTC parameters:

register #0	36h
#1	2dh
#2	2fh
#3	07h
#4	5bh
#5	00h
#6	57h
#7	53h
#8	02h
#9	03h
#a	00h
#b	00h
#c	00h
#d	00h

Locating specific pixels within the bitmap may be performed with the following equation:
byte offset = (8192* (Y mod 4)) + (90 * INT(Y mod 4)) + INT(X/8); bit position = 7 – (X mod 8):
where: 0 < = X < = 719
0 < = Y < = 347

PLANTRONICS COLOR PLUS MODE(S) — PROGRAMMING NOTES

This mode is an enhancement to the graphics modes of the CGA. The dot clock is 14.318 Mhz in the 640x200 mode and 7.16 Mhz in the 320x200 mode. The 640x200 mode offers a choice of 4 out of 16 colors per pixel vs. black & white in the CGA mode with the same resolution. The 320x200 mode offers 16 out of 16 colors vs. 4 out of 16 colors for the comparable CGA mode.

Plantronics 6845 CRTC parameters:
(actually the same as CGA 320x200 & 640x200)

register #0	38h
#1	28h
#2	2dh
#3	0ah
#4	7fh
#5	06h
#6	64h
#7	70h
#8	02h
#9	01h
#a	06h
#b	07h
#c	00h
#d	00h

The 32Kbytes of display RAM are divided into two bit planes.

Plane0 — Even scan lines @ addr b000:8000h to b000:9f3fh
Odd scan lines @ addr b000:a000h to b000:bf3fh

Plane1 — Even scan lines @ addr b000:c000h to b000:df3fh
Odd scan lines @ addr b000:e000h to b000:ff3fh

320x200 16 color BIT ORGANIZATION

bplane#	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
plane0	c1	c0	c1	c0	c1	c0	c1	c0
plane1	c3	c2	c3	c2	c3	c2	c3	c2
pixel#	pixel 0		pixel 1		pixel 2		pixel 3	

640x200 4 color BIT ORGANIZATION

bplane#	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
plane0	co	c0	co	c0	co	c0	co	c0
plane1	c1	c1	c1	c1	c1	c1	c1	c1
pixel#	pixel0	pixel1	pixel2	pixel3	pixel4	pixel5	pixel6	pixel7

c2/1	c1/R	c0/G	c3/B	COLOR
0	0	0	0	black
0	0	0	1	blue
0	0	1	0	green
0	0	1	1	cyan
0	1	0	0	red
0	1	0	1	magenta
0	1	1	0	brown
0	1	1	1	white
1	0	0	0	gray
1	0	0	1	lt. blue
1	0	1	0	lt. green
1	0	1	1	lt. cyan
1	1	0	0	lt. red
1	1	0	1	lt. magenta
1	1	1	0	yellow
1	1	1	1	bright white

Autoconfig examines the expansion bus for any expansion Advanced Video Adapter BIOS in the 0C0000h — 0C7FFFh memory range. If an expansion video BIOS is found, then an external VGA or EGA controller is assumed to be on the bus and the onboard VGA controller is disabled to avoid conflict. If an expansion video BIOS is not found, the video output is configured in accordance with the default CONFIG Control video setting (see Appendices F and H), as defined by the CONFIG dip switches 1, 2 and 3.

You can add an expansion MDA or CGA compatible controller in conjunction with the onboard VGA controller to provide two video screens. (This makes many CAD packages easier to use.)

NOTE: When using the PC40-III's onboard video controller, a VGA compatible monitor such as Commodore Models 1403 and 1450 (monochrome) or 1950 (color) must be connected to the 15 pin video output connector (no matter what video mode you have selected).

If you want to use two video screens, there are several things you should remember. First, you should use a CGA, MDA or compatible adapter — one that has no BIOS ROM of any kind.

Also, if you were to use an MDA/Herc adapter (monochrome) and you have the CONFIG switches set for VGA color, the PC40-III will boot using your VGA monitor and you will see a blinking cursor on your monochrome monitor, indicating that it has been initialized.

If, while using the MDA/Herc adapter in the expansion port, you have the CONFIG switches on the back of the System Unit set to MDA/Herc, your PC40-III will use the monochrome monitor as the boot monitor and the VGA monitor will be initialized with the blinking cursor.

In either case, you can switch between the VGA and the monochrome monitors by using the MS-DOS **MODE** command. The syntax for the MODE command is as follows:

- **MODE MONO** — sets the MDA as the default monitor
- **MODE co80** — places the onboard VGA adapter into 80 column mode and sets it as the default monitor
- **MODE co40** — places the onboard VGA adapter into 40 column mode and sets it as the default monitor

VIDEO DIP SWITCHES

Dip switches 1, 2 and 3 are set in combinations as shown below to enable the various video modes that the PC40-III supports.

DISABLE VIDEO
MDA/HERC.

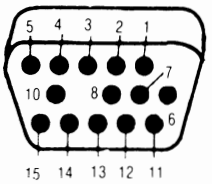
CGA
VGA AUTO.

VGA COLOR
VGA MONO.

132 COL. X 43 ROW
132 COL. X 25 ROW

***WARNING:* POWER OFF UNIT BEFORE CHANGING DIP SWITCHES**

PIN DEFINITIONS FOR VIDEO PORT

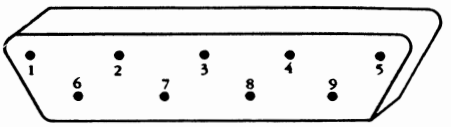


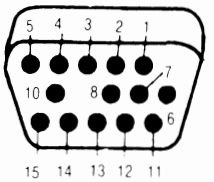
Pin	Function
1.	Red Video
2.	Green Video
3.	Blue Video
4.	Monitor ID Bit 2 (not used)
5.	ground
6.	Red Return (ground)
7.	Green Return (ground)
8.	Blue Return (ground)
9.	Key (no pin)
10.	Sync Return (ground)
11.	Monitor ID Bit 0 (not used)
12.	Monitor ID Bit 1 (not used)
13.	Horizontal Sync
14.	Vertical Sync
15.	not used

Monitor ID Bits are not used in VGA.

Monitor type is determined on power up by an automatic sensing circuit.

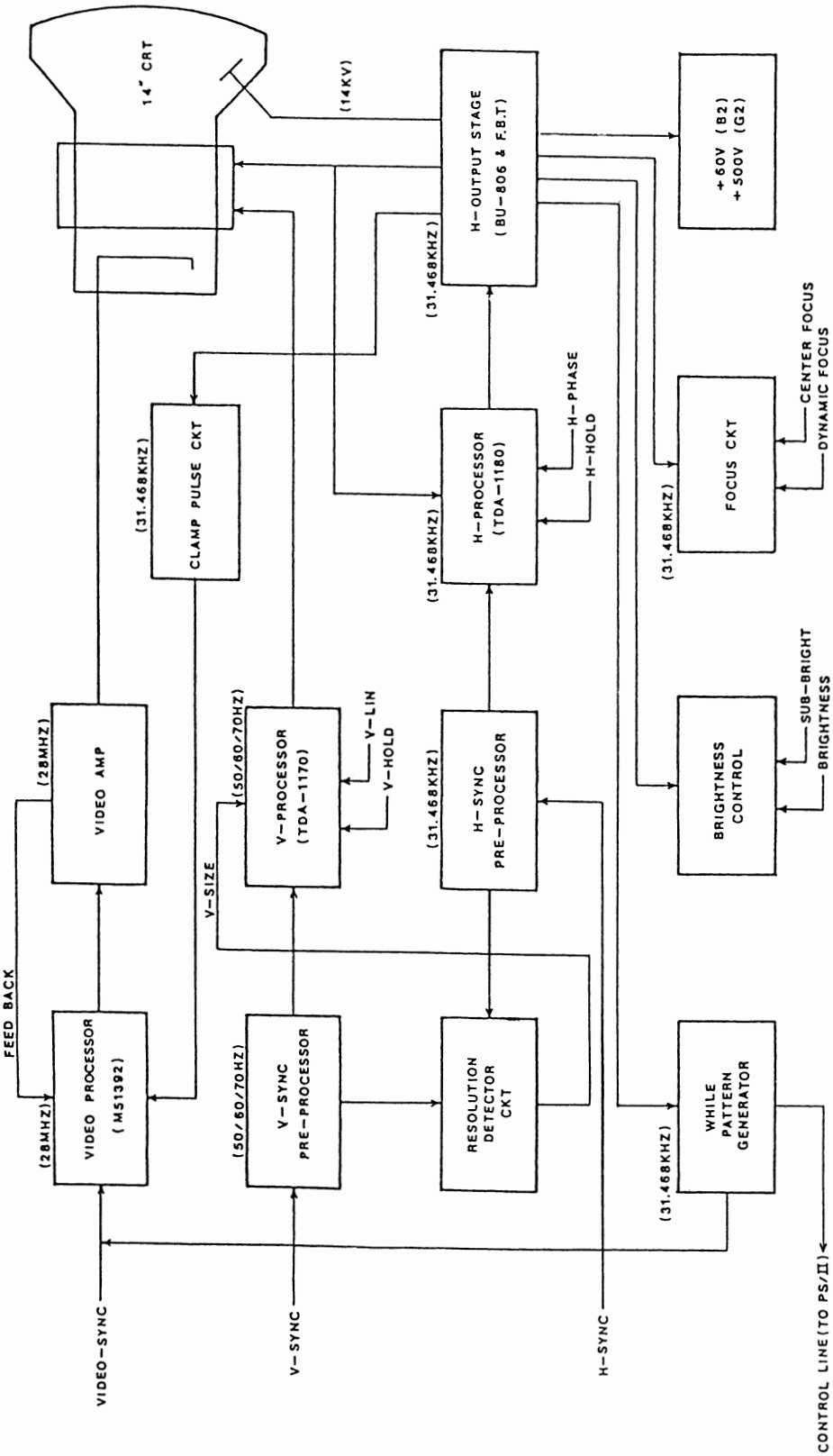
PIN DEFINITIONS FOR MULTISYNC ADAPTER CABLE



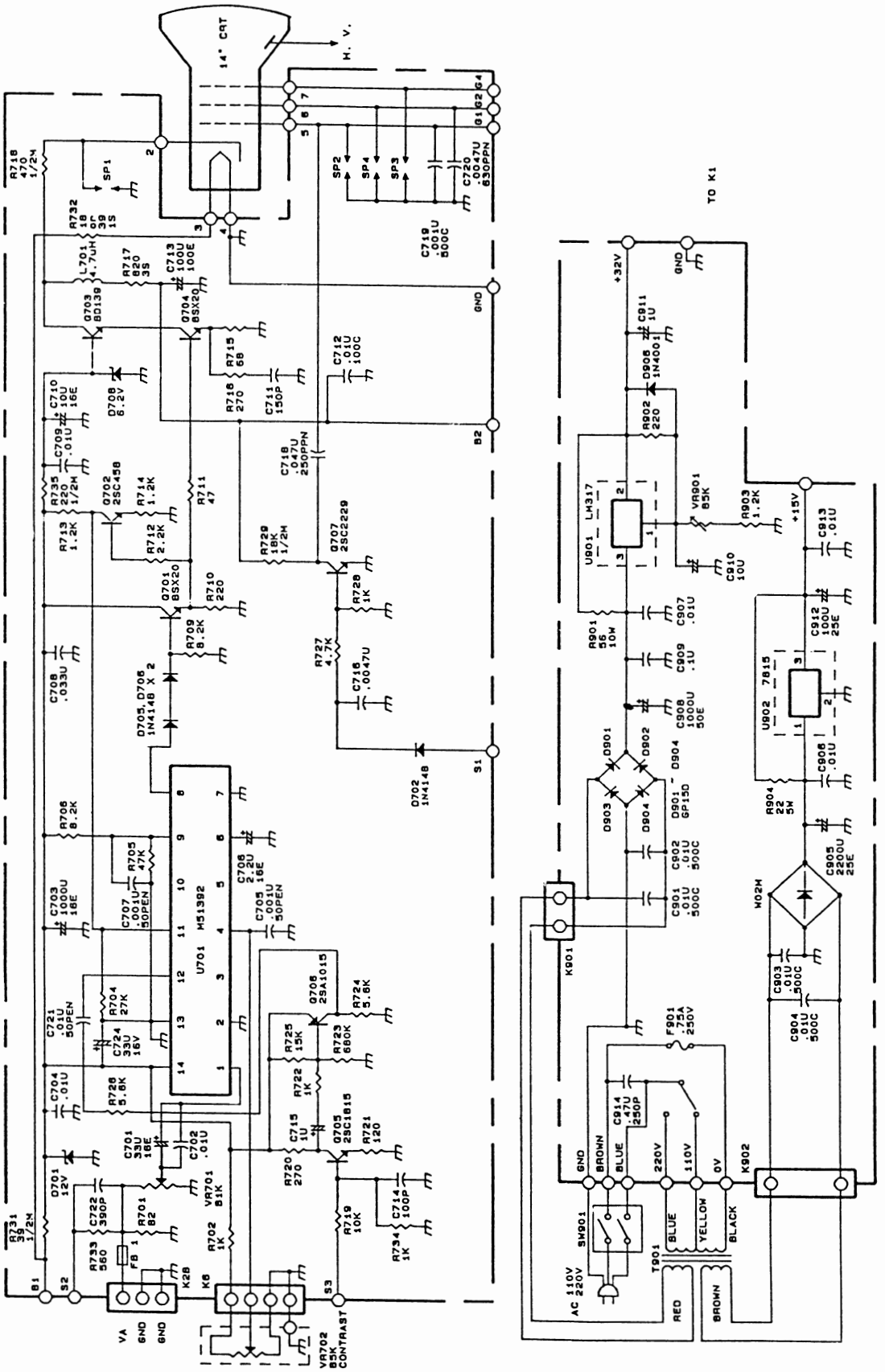


NEC Multisync DB9 Female		VGA DB 15 Male
1	RED	1
2	GREEN	2
3	BLUE	3
4	HORIZONTAL	13
5	VERTICAL	14
6	GROUND	6
7		—
8		8
9		10
		11

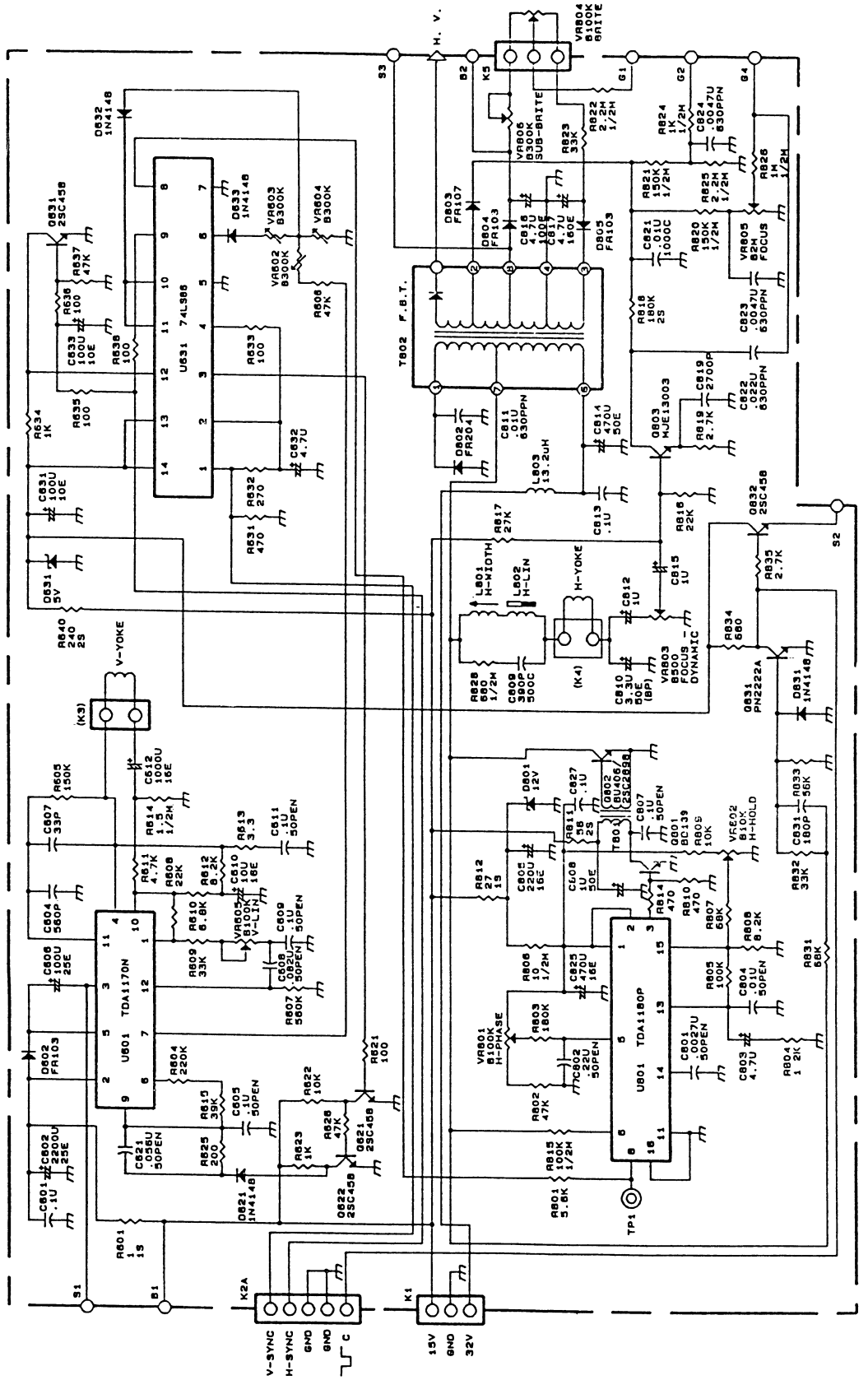
***NOTE:** Many Multisync monitors come equipped with a compatible adapter.*



1403 BLOCK DIAGRAM



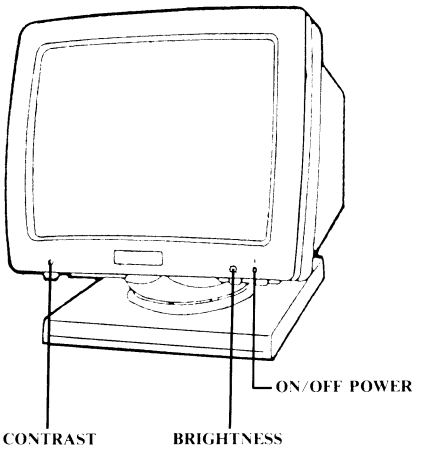
1403 VIDEO AND POWER UNIT



1403 DEFLECTOR UNIT

1403 MONOCHROME VGA COMPATIBLE MONITOR

SERVICE MANUAL AVAILABLE UNDER CBM PART NUMBER 314882-01



1. Cathode Ray Tube (CRT)

Size	: 14 inch diagonal (DM-3014)
	15 inch diagonal (DM-3015)
Deflection Angle	: 90 degrees
Neck Diameter	: 20 ϕ
Face Treatment	: dark glass, non-glare
Phosphor	: H192 or equivalent

2. Power Requirements

Power source	: 110 / 220 volts AC, 0.55 Amp.
Power consumption	: 50 watts

3. Deflection Characteristics

Horizontal	
Frequency	: 31.468 KHz
Blanking time	: 5.72 usec
Vertical	
Frequency	: 50 / 60 / 70 Hz
Vertical	
Blanking time	:
a. 50 Hz	
480 lines	: 4.236 msec
400 lines	: 6.844 msec
350 lines	: 8.496 msec
b. 60 Hz	
480 lines	: 0.905 msec
400 lines	: 3.511 msec
350 lines	: 5.163 msec
c. 70 Hz	
400 lines	: 1.130 msec
350 lines	: 2.728 msec

4. Video Response

Bandwidth	: 30 MHz (−3dB)
Rise time	: 15 nsec max.
Fall time	: 15 nsec max.
Characters	: Up to 64 gray shades
Horizontal resolution	: 640 / 720 pixels
Vertical resolution	: 350 / 400 / 480 lines

5. Display Format

Character format	: 8 x 14 matrix
	8 x 16
	9 x 16
Capacity	: 80 characters x 25 rows
	80 characters x 30 rows

6. Input Signal

Video signal	: 0 − 0.7 Vpp
Horizontal drive	: 3.5 Vpp
Vertical drive	: 3.5 Vpp

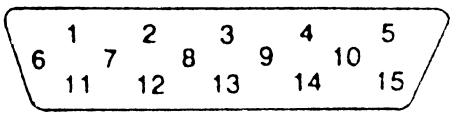
7. Display Performance

Picture	DM-3014	DM-3015
Horizontal	: 240 mm ± 3 mm	250 mm ± 3 mm
Vertical	: 180 mm ± 3 mm	190 mm ± 3 mm
Linearity	: Character height or width will not vary for more than 10% from the average character size.	

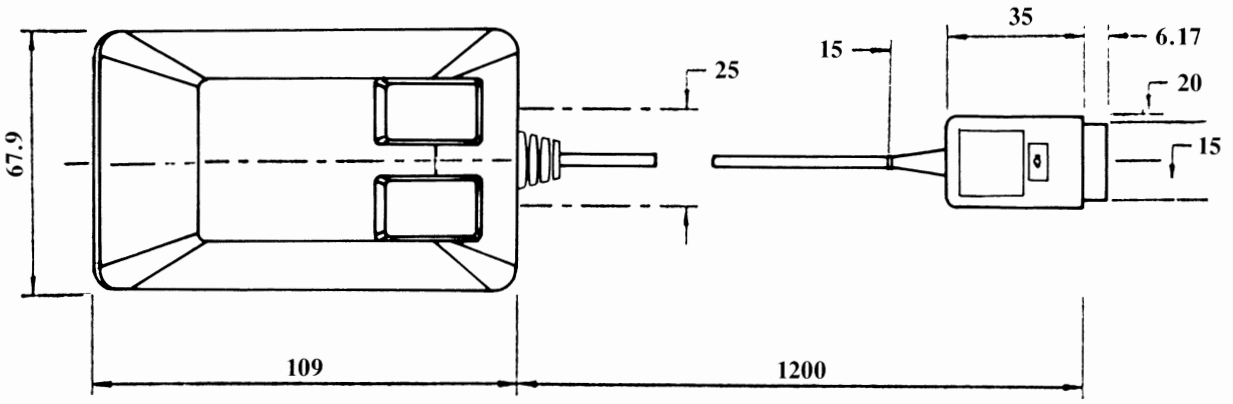
8. Geometric Distortion

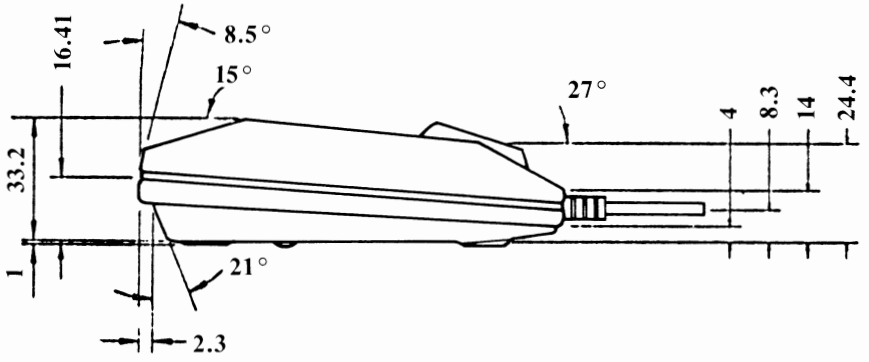
DM-3014 :	
Horizontal	: ±2 mm
Vertical	: ±2 mm
DM-3015 :	
Horizontal	: ±3 mm
Vertical	: ±3 mm

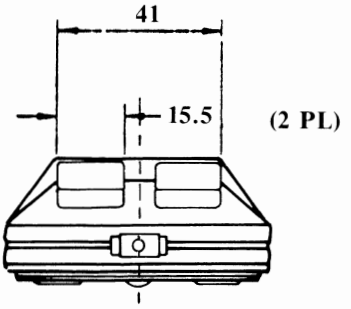
9. Video Cable Input Signal

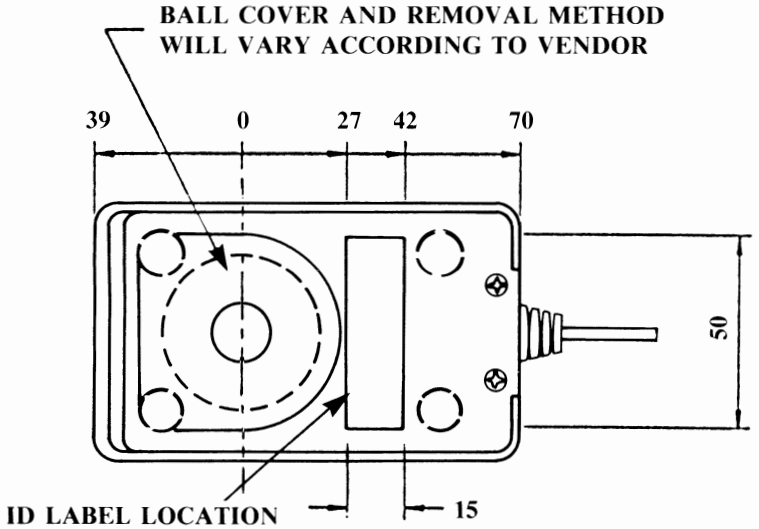


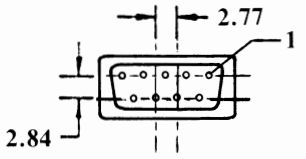
Pin 2 - Video
Pin 5 - Self test
Pin 7 - Ground
Pin 10 - Ground
Pin 13 - H-sync
Pin 14 - V-sync





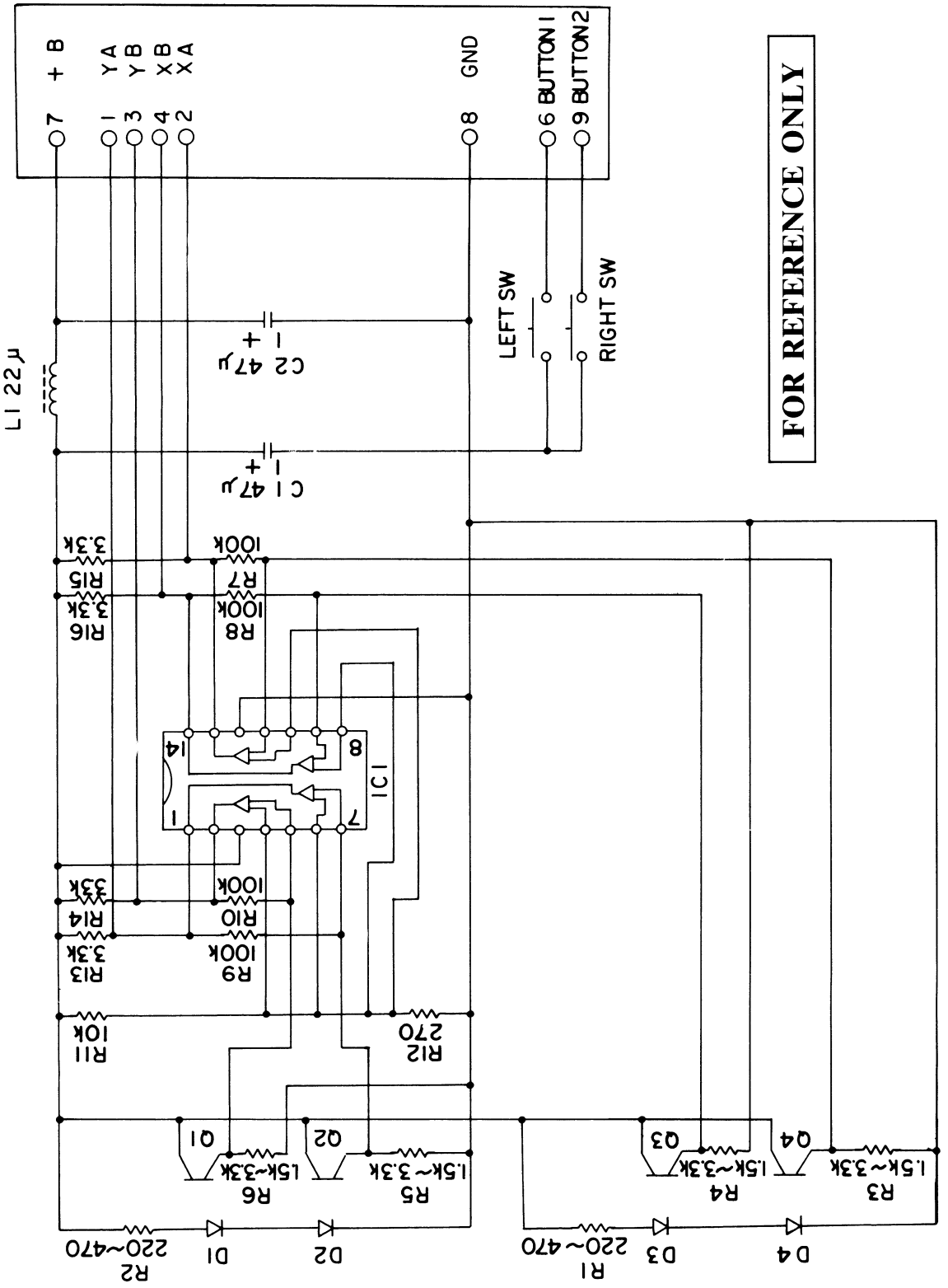






CONNECTION TABLE	
PIN NO.	FUNCTION
1	Y_B
2	X_A
3	Y_A
4	X_B
5	NC
6	BUTTON #1 (LEFT)
7	+5 V
8	GND
9	BUTTON #2 (RIGHT)

1352 MOUSE


FOR REFERENCE ONLY
7 +B
1 YA
3 YB
4 XB
2 XA
8 GND
6 BUTTON1
9 BUTTON2
LEFT SW
RIGHT SW
L1 22μ
C2 47μ
C1 47μ
3.3k
100k
R15
R7
R16
R8
IC1
R14
R10
R13
R9
R11
10k
R12
270
Q1
Q2
Q3
Q4
1.5k~3.3k
R6
R5
R4
R3
220~470
R2
R1
D1
D2
D3
D4
YB
YA
XB
XA

1352 MOUSE

APPENDIX E

TECHNICAL UPDATES

commodore

TECHTOPICS

********** FOR IMMEDIATE RELEASE **********

PC40-III VIDEO REPAIR TIP: IC/SOCKET CONTACT PROBLEMS.

THE PC40-III VIDEO CONTROLLER CHIP, PVGA-1A PN# 390302-01, LOCATED AT U101, CAN EXHIBIT A NUMBER OF DIFFERENT SYMPTOMS IF A POOR CONTACT EXISTS BETWEEN THE IC AND THE 100 PIN PLCC (PLASTIC LEADED CHIP CARRIER).

THE SYMPTOMS INCLUDE, BUT ARE NOT LIMITED TO THE FOLLOWING:

- NO VIDEO
- SCRAMBLED TEXT
- LOSS OF VIDEO SYNC
- CONTINUOUS SCROLLING OF SCREEN

NOTE: VIDEO MODE SWITCHES ON THE BACK OF UNIT SHOULD BE SET TO VGA COLOR (1 UP, 2 DOWN, 3 DOWN), SEE PAGE 64 IN PC40-III OPERATIONS GUIDE. THIS MODE INSURES THAT SOFTWARE USING COLOR MODES WILL RUN ON A MONOCHROME MONITOR.

IT WILL BE NECESSARY TO REMOVE THE DRIVE SUB-CHASSIS TO LOCATE U101.

1) TO INSURE PROPER CONTACT BETWEEN THE VIDEO CONTROLLER IC AND THE 100 PIN SOCKET (PLCC), INSERT THE IC ALL THE WAY DOWN INTO THE SOCKET BY APPLYING PRESSURE TO THE CORNERS OF THE IC WITH YOUR FINGERS.

   WARNING: DO NOT ATTEMPT TO REMOVE THE VIDEO CONTROLLER IC FROM THE SOCKET WITHOUT THE PROPER IC EXTRACTOR. THIS TOOL IS AVAILABLE FROM COMMODORE PARTS - PN# 314874-01, DEALER COST IS $20.00.

2) CHECK THAT GOOD CONTACT EXISTS WITH ALL SOCKETTED CHIPS.

3) USE STATIC-PROTECTION PROCEDURES, (SERVICER AND HARDWARE MUST BE AT THE SAME VOLTAGE POTENTIAL TO AVOID ELECTRO-STATIC DISCHARGE).

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commodore COMPUTERS

Computer Systems Division
1200 Wilson Drive
West Chester, PA 19380