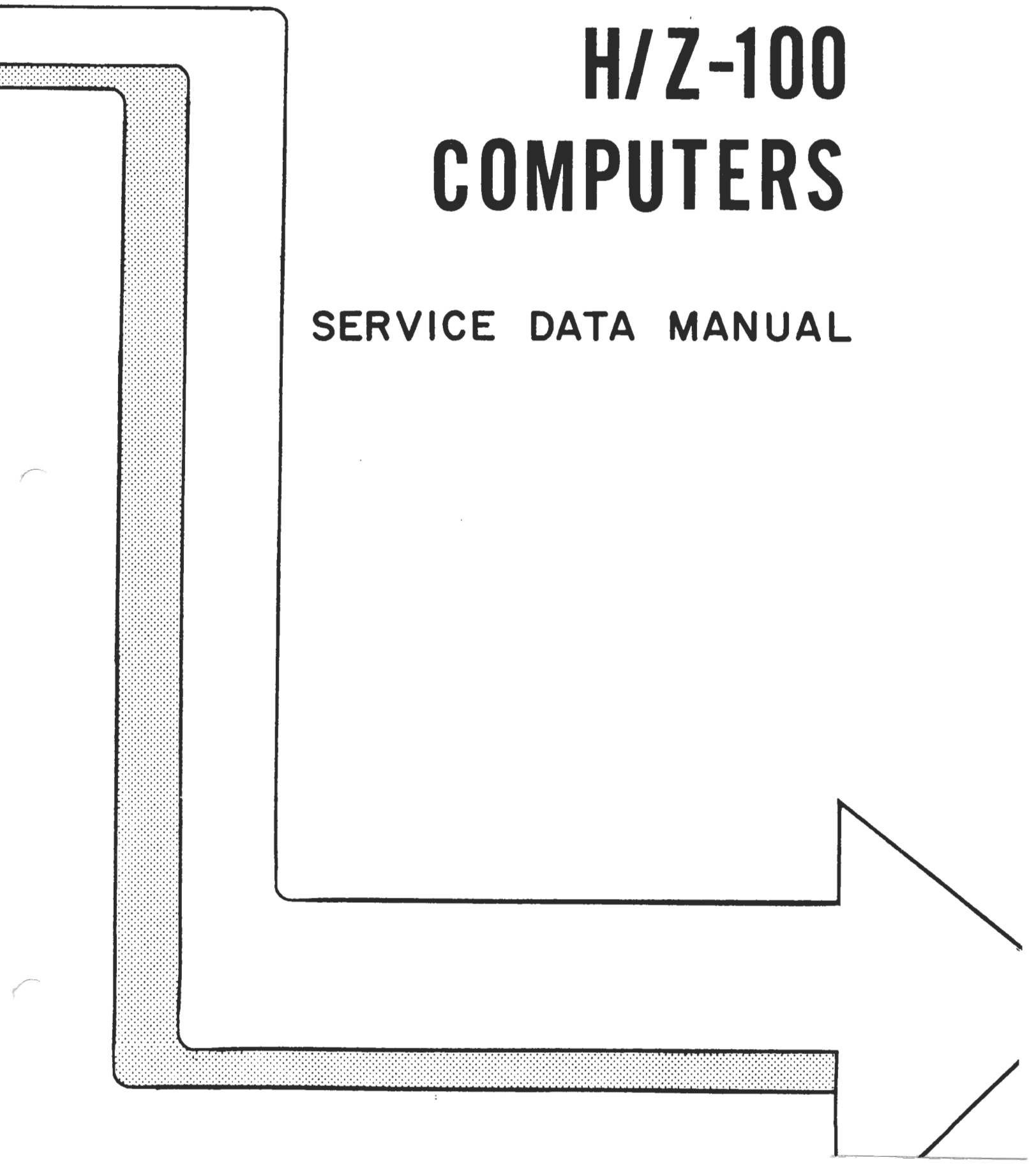
H/Z-100 COMPUTERS

SERVICE DATA MANUAL



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Prepared by Heath Company
Service Publications and Training
Benton Harbor, MI 49022

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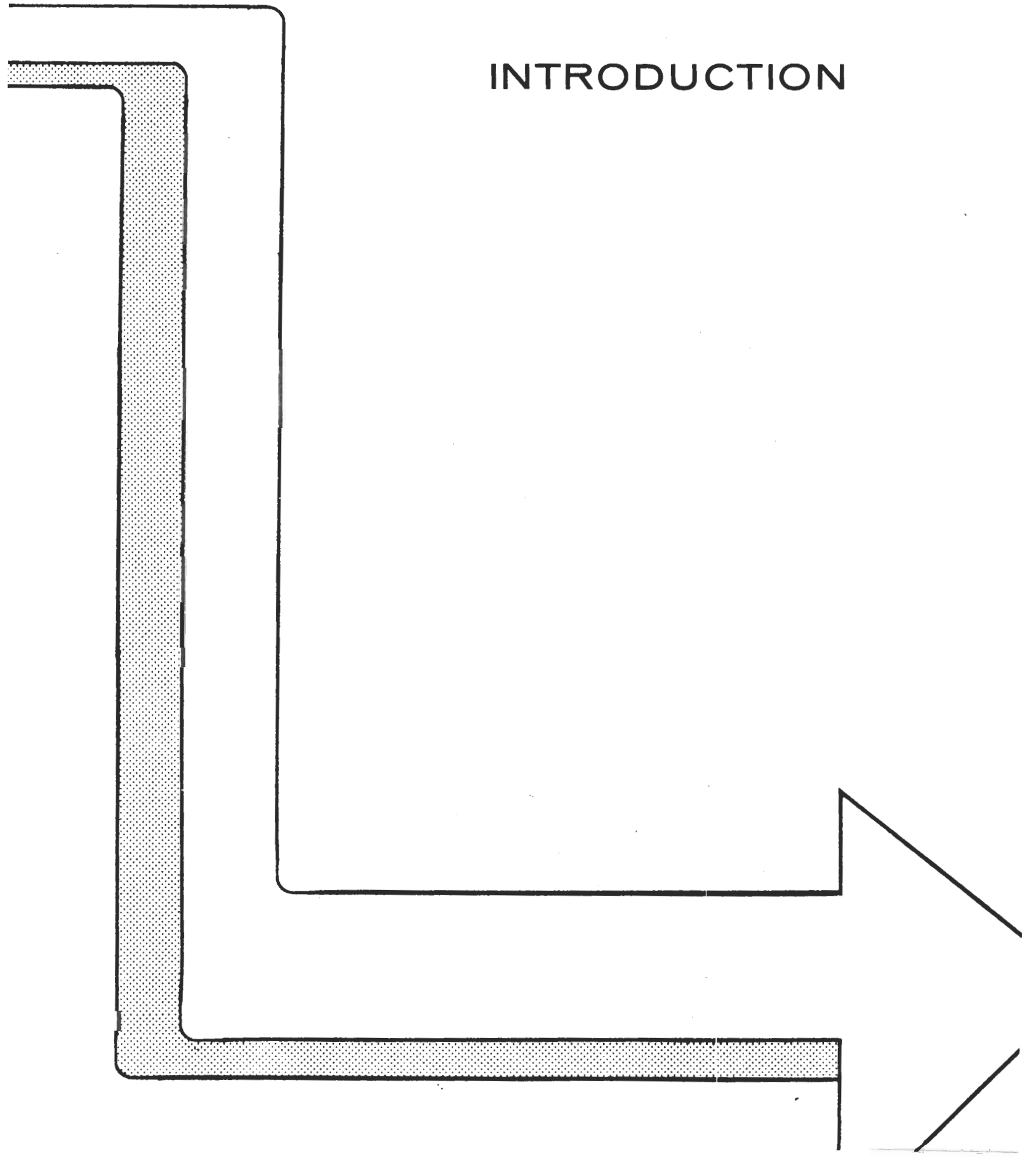


The H/Z-100 COMPUTER SERVICE DATA MANUAL (Blue Book) contains in-depth data about the new H/Z-100 Computers, both the All-In-One model and the Low-Profile model.

The information in this manual will help you efficiently troubleshoot and repair H/Z-100 Computers to either the module level or the component level.

There are thirteen sections in this manual. The first is a general introduction to the manual and an explanation of the model numbering system.

Section 2 introduces you to the Computer System and is presented in the familiar Blue Book format.

The following six sections, also laid out in the Blue Book format, contain detailed data on the:

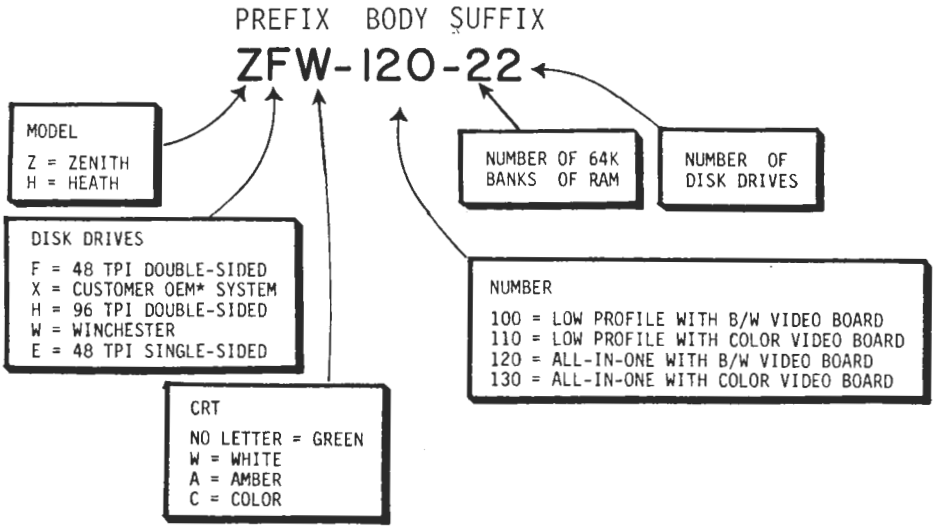
-- Motherboard,
-- Video Board,
-- Disk Controller and Drives,
-- Video Monitor,
-- Keyboard, and
-- Power Supply

The balance of the manual is set aside for your inclusion of material for Accessories, Service Bulletins, Data Sheets, and Diagnostics. Data on the S-100 bus has already been included in an Appendice section.

All thirteen sections are contained in an easy-to-use 3-ring binder...this will let you insert updates and new product information and will let you keep your H/Z-100 Computer Blue Book up to date.

And now for a look at the model number system...

Each model number lets you see at a glance the main features of that particular model. The illustration below shows what each portion of the model number means:



So, if the model number is ZF-120-22, it means:

Z *a Zenith wired model,*

F *with a 48 TPI,*

W *a white CRT,*

-120 *and it's an ALL-IN-ONE with a black and white video board*

-2 *with two banks of 64K of RAM (2 x 64 = 128K RAM), and*

2 *two disk drives!*

A couple of things to remember...

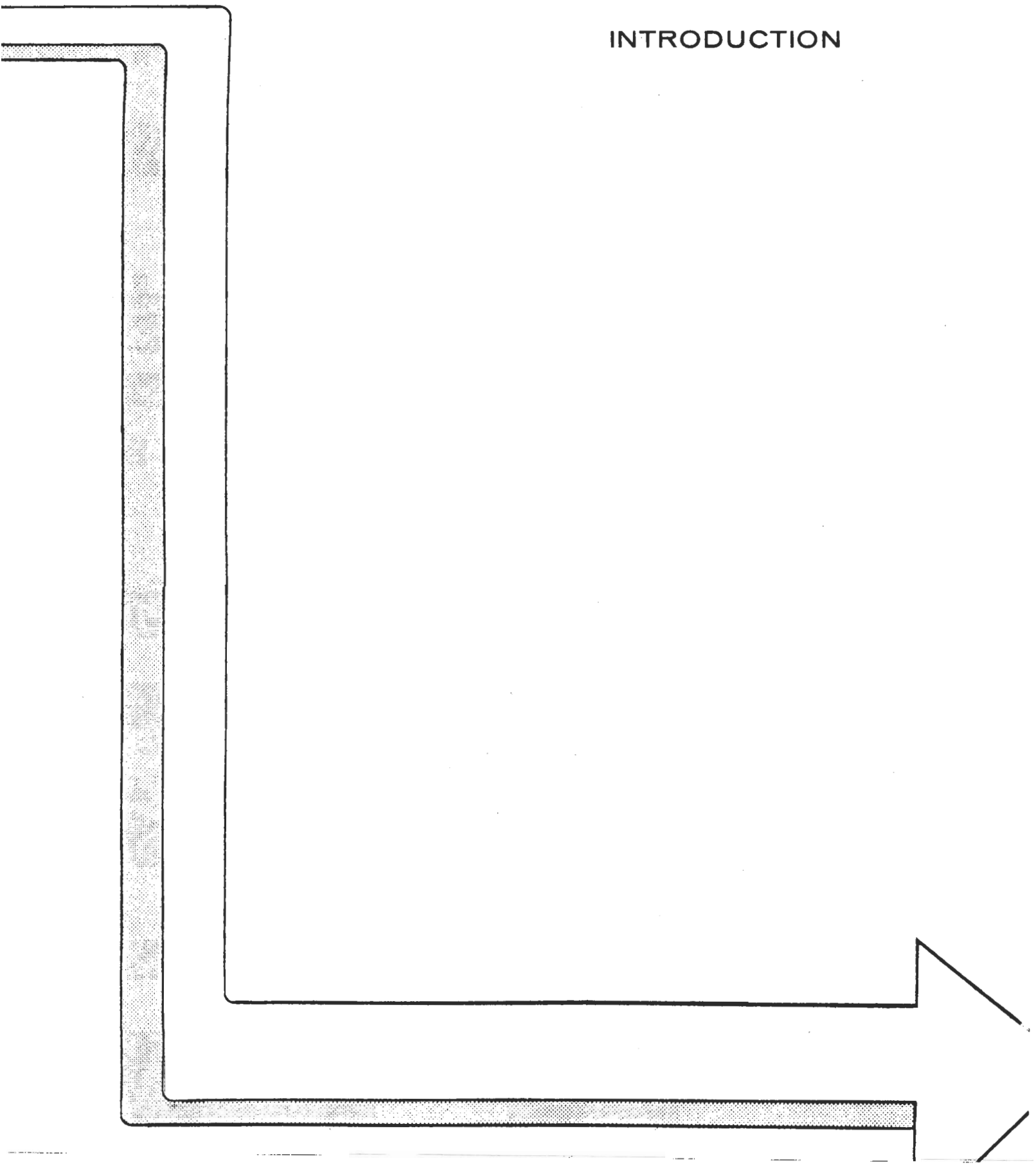
Note that in the body (or number), "Color Video Board" refers to the ability of the video board to produce color--not the nature of any CRT. Also, in the suffix portion of the model number, characters are alphanumeric for OEM models (and stand for a specific OEM); for all other models, the characters are numeric.

Carefully read each section in this Blue Book. After doing so, you'll not only become an expert on the H/Z-100, you will also be able to quickly locate the exact information that you need to service the unit.

Before learning how each module works in the Computer, you should know how the H/Z-100 works as a complete system. To gain this understanding, begin by reading section 2, "System."

SYSTEM

INTRODUCTION



The H/Z-100 is a versatile computer system. This computer is designed to be compatible with existing hardware and software products. The H/Z-100 offers an industry standard bus, a widely accepted operating system, high-resolution graphics, expandability, and high-speed computing to the prospective customer.

The computing functions of the H/Z-100 are controlled by two microprocessors; an 8088 and an 8085. The 8088 processor features 16-bit processing in an 8-bit environment. This gives the computer 16-bit speed and power, while still retaining an 8-bit bus. The 8085 processor is an 8-bit processor that is 8080 code compatible. This processor assures a large available software base. Thus, the computer buff with existing 8-bit software is supported.

The H/Z-100 computer is available in two models; the All-in-One and the Low Profile. The main difference between the two models is that the All-in-One contains a built-in video monitor, while the Low Profile does not. Both models include a mass-storage device, two processors, Dynamic RAM, and a professional keyboard.

Flexibility of the computer is assured by a 5-slot, S-100 compatible bus. The S-100 bus was designed to conform to the IEEE-696 definition of the S-100 bus. This definition was chosen since it is the widely accepted standard among computer manufacturers. This bus design provides an opportunity for the user to tailor a hardware environment to suit his needs. Additional I/O, slave processors, and special function S-100 boards from Heath Company and other sources will work within the H/Z-100.

To communicate with the outside world, the H/Z-100 motherboard contains on-board peripheral connections. These connections consist of two serial ports and a parallel port. The serial ports are configured to RS-232C standards. One is a DCE interface and the other is a DTE interface. The parallel port is configured as a Centronics compatable printer interface. Because these connections are built into the motherboard, a separate S-100 I/O card is not needed. Thus, space in the S-100 card cage is conserved.

In addition, the H/Z-100 contains many other features. These include:

- Two keyboard modes.
- Light pen input.
- Three timer outputs.
- H-19 graphic and escape code compatible.
- Wired and tested mother board.

These features, along with the stylish molded cabinet, make the H/Z-100 computer a powerful computing tool.

The information in this section of the manual enables you to service the H/Z-100 to the module level. If you require more information on an individual board, refer to the section entitled by the board name.

SPECIFICATIONS

CPU

Processor 1	Intel 8088.
Clock	5 MHz.
Type	16-bit CPU.
Wait State	Memory, Ø; I/O, 1.
Processor 2	Intel 8085.
Clock	5 MHz.
Type	8-bit CPU.
Wait State	Memory, 1; I/O, 2.
On-Board Memory	64K to 192K bytes in 64K increments. Parity checked.
Memory Space	1 megabyte.
Monitor Space	One 64K page.
Video RAM Space	Three 64K pages.
User Memory Space	3/4 megabyte.
Interrupts	
Controller	Dual 8259A.
System	15-level priority vector interrupt.

VIDEO DISPLAY

CRT (All-in-One)	12" diagonal, green non-glare or optional white or amber.
Display Format	25 lines of 80 characters.
Display Size	6.5" high x 8.5" wide.
Character Size	0.2" high x .1" wide (approximate).
Character Set	"Soft", dynamically redefinable.
Character Type	5 x 9 dot matrix.
Dot Resolution	640 x 225 pixels.
Colors (optional)	Eight: Red, green, blue, white, black, cyan, magenta, and yellow.
Gray Scale	Eight levels when a monochrome display is used and the color option is installed in the computer.

Options	
Interlace Mode	640 x 500 pixels.
Pages	Second page of display.
Light Pen	One pixel resolution.
Outputs	Red, green, blue, composite video, composite sync and separated horizontal and vertical sync.

BUS STRUCTURE

Type	Proposed IEEE-696 (S-100).
Number of Slots	Five.
Data Bus Width	Eight bits.
Address Bus Width	Twenty-four bits.
I/O Addressing	Eight bits.

TIMER

Type	Programmable.

KEYBOARD

Type	95 keys: 61-key alphanumeric and 16-key function and control section, plus an 18-key numeric and cursor control section.
Modes	Two: ASCII and Event Driven.
Processor	FIFO buffer (17 character).
Key Click	May be disabled.

DISK CONTROLLER

(May be omitted on S-100 Card)

Type	WD1797.
Drives Supported	Up to four each.
5-1/4"	Single/double-sided, 48 TPI, single/double density.
8"	Single/double-sided, single/ double density.
Data Separator	Phase-locked loop.
Precompensation	Variable independently for both 5-1/4" and 8" sizes.
Data Transfer	Programmed using wait states, interrupt or polling.

Internal Disk Drive	
Size	5-1/4".
Sides	Single or double.
Tracks per Inch	48.
Capacity (formatted)	80K, 160K, or 320K; depending on the number of sides and density.
Track Format	4K, eight sectors of 512 bytes each.
Stepping Speed	6 milliseconds per track or faster.

External Disk Drive	
Interface Type	Shugart 850 or equivalent.
Winchester Disk Drive (optional)	
Type	One internal 5" replacing one internal disk drive.

INPUT/OUTPUT

Serial I/O	Dual RS-232 ports, one DTE and one DCE.
Baud Rate	110 to 38,400.
Operation	Asynchronous RS-232 or synchronous.
Stop Bits	One, one and one half, or two.
Word Length	Five, six, seven, or eight bits.
Break Capability	Detection and generation.
Parity	Even, odd, or none.
Parallel I/O	Eight-bit output only.
Type	Centronics.

POWER SUPPLY

Input, Volts ..... 120 VAC or 240 VAC.
Input, Hertz ..... 50 Hz or 60 Hz.

TEMPERATURE AND HUMIDITY

Operating Temperature ... 15.6 to 32.2 degrees Celsius (60 to 90 degrees Fahrenheit).
Storage Temperature ..... 10 to 43 degrees Celsius (50 to 110 degrees Fahrenheit).
Operating Humidity ..... 8% to 80%, noncondensing.

DIMENSIONS

All-in-One ..... 19" W x 19.5" D x 13.5" H (47.5 x 48.75 x 33.75 cm).
Low-Profile w/o Monitor . 19" W x 19.5" D x 7.125" H (47.5 x 48.75 x 17.8 cm).

WEIGHT

All-in-One ..... 50 lbs (22.7 kg).
Low-Profile ..... 40 lbs (18.2 kg).

Heath Company and Zenith Data Systems reserves the right to discontinue products and to change specifications at any time without incurring obligation to incorporate new features in products previously sold.

OPERATION

In this section, operation of the H/Z-100 computer is discussed. This specifically covers power-up and reset, MTR-100 commands, and H-19 emulation. Information on hardware and peripheral applications can be found in the configuration section.

POWER-UP AND RESET

When shipped to the customer, the H/Z-100 is hardware set by S101 in auto-boot mode. This means that upon power-up or reset, MTR-100 will initialize the computer and automatically start the boot routine. If a disk is not found in the default drive within 30 seconds after power-up or reset, MTR-100 will print a boot error message and enter the monitor mode. The boot routine, however, may be averted in two different ways. The first way is to reset S101 (this is covered in Configuration). The second way is to use the delete key. By pressing the delete key during the boot routine, the routine is halted and the computer enters the monitor mode.

To power-up the computer, flip the switch on the right rear corner of the computer. To reset, the CTRL and RESET keys are simultaneously pressed. During the initialization process, MTR-100 selects the active processor, initializes the hardware devices, sizes RAM, and sets the stack segment. MTR-100 then times out 30 seconds and starts the boot routine.

There are two MTR-100 commands; Boot and Version. MTR-100 features command completion where only the first letter of the command is typed in and the computer will finish typing in the rest of the command. A detailed description of each command follows. Please note that these commands will be ignored if the computer is not in the monitor mode.

BOOT

The boot command will boot from the default drive specified by bits 0-2 of the configuration dip switch S101. MTR-100 contains all the code necessary to boot an operating system from the default drive. The command is initiated by pressing the B key after the hand prompt. The computer will respond with "oot". The pressing of the RETURN key will cause MTR-100 to jump to and start the boot-up routine. Pressing the DELETE or BACKSPACE keys will cause the boot routine to abort. An aborted boot returns the computer to the monitor mode, even if auto-boot is configured.

VERSION

The version command is intended to allow non-technical users of the H/Z-100 to identify which version of MTR-100 is installed in their machine. The command is implemented by pressing the V key after the hand prompt. The computer will respond with "ersion" and MTR-100 will identify itself.

H-19 EMULATION

To keep the H/Z-100 compatible with existing software, H-19 emulation of the keyboard and character display is necessary. This is accomplished through the use of subroutines within MTR-100. All of the H-19 escape sequences except the ANSI mode are supported. It is important to note that the H-19 escape sequences are supported during software control. Since there is no OFF LINE key, the terminal cannot be programmed directly from the keyboard. For further information on the keyboord, refer to the keyboard section of this manual.

SUMMARY OF H/Z-100 ESCAPE CODES

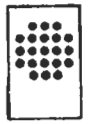
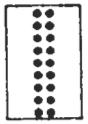
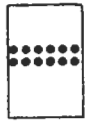
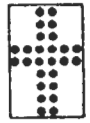
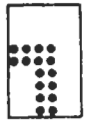
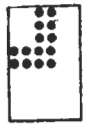
Escape Sequence	Definition
CURSOR FUNCTIONS	
ESC A	Cursor up
ESC B	Cursor down
ESC C	Cursor right
ESC D	Cursor left
ESC H	Cursor home
ESC I	Reverse index
ESC Y	Direct cursor addressing
ESC j	Save cursor position
ESC n	Cursor position report
ESC k	Set cursor to previously saved position
ERASING AND EDITING	
ESC E	Clear display and home cursor
ESC J	Erase to end of page
ESC K	Erase to end of line
ESC L	Insert line
ESC M	Delete line
ESC N	Delete character
ESC O	Exit insert character mode
ESC @	Enter insert character mode
ESC b	Erase to beginning of display
ESC l	Erase entire line
ESC o	Erase to beginning of line
CONFIGURATION	
ESC r*	Modify baud rate * A = 110 B = 150 C = 300 D = 600 E = 1200 F = 1800 G = 2000 H = 2400 I = 3600 J = 4800 K = 7200 L = 9600

Escape Sequence	Definition
Configuration (continued)	
ESC x*	Set mode(s) * 1 = Enable 25th line 2 = No key click 3 = Enter hold screen mode 4 = Block cursor 5 = Cursor off 6 = Keypad shifted 7 = Enter alternate keypad mode 8 = Auto line feed on receipt of CR 9 = Auto CR of receipt of line feed ; = Nonblinking cursor < = Disable keyboard auto repeat ? = Enable key expansion
ESC y*	Reset mode(s) * 1 = Disable 25th line 2 = Enable key click 3 = Exit hold screen mode 4 = Underscore cursor 5 = Cursor on 6 = Keypad unshifted 7 = Exit alternate keypad mode 8 = No auto line feed 9 = No auto CR ; = Blinking cursor < = Enable keyboard auto repeat ? = Disable key expansion
ESC z	Reset to power-up configuration
MODES OF OPERATION	
ESC F	Enter graphics mode
ESC G	Exit graphics mode
ESC =	Enter alternate keypad mode
ESC >	Exit alternate keypad mode
ESC p	Enter reverse video mode
ESC q	Exit reverse video mode
ESC t	Enter keypad shifted mode
ESC u	Exit keypad shifted mode

Escape Sequence	Definition
ALTERNATE KEYPAD SEQUENCE	
ESC ?M	Enter key
ESC ?n	Period (.) key
ESC ?p	0 key
ESC ?q	1 key
ESC ?r	2 key
ESC ?s	3 key
ESC ?t	4 key
ESC ?u	5 key
ESC ?v	6 key
ESC ?w	7 key
ESC ?x	8 key
ESC ?y	9 key
ADDITIONAL FUNCTIONS	
ESC Z	Identify as VT52(ESC /K)
ESC #	Transmit page
ESC]	Transmit 25th line
ESC ^	Transmit current line
ESC _	Transmit character at cursor
ESC ~	Zenith identify terminal type
ESC m*	Foreground and background colors * 0 = Black 1 = Blue 2 = Red 3 = Magenta 4 = Green 5 = Cyan 6 = Yellow 7 = White
ESC {	Keyboard enable
ESC }	Keyboard disable
ESC v	Wrap-around at end of line
ESC w	Discard at end of line

Octal ( )
Decimal [ ]
Hex

GRAPHIC SYMBOLS

(136) [94] 5E	(137) [95] 5F	(140) [96] 60	(141) [97] 61 a	(142) [98] 62 b	(143) [99] 63 c	(144) [100] 64 d
						
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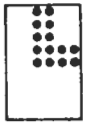
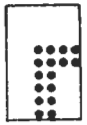
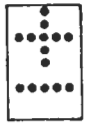
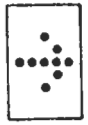
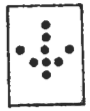
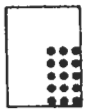
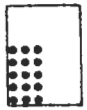
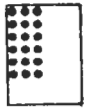
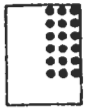
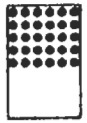
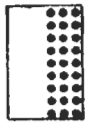
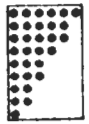
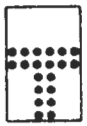
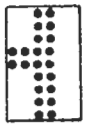
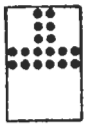
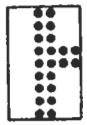
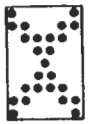
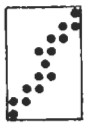
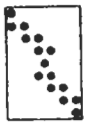
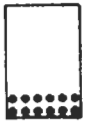
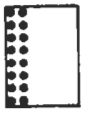
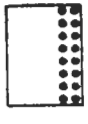
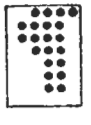
						
(154) [108] 6C l	(155) [109] 6D m	(156) [110] 6E n	(157) [111] 6F o	(160) [112] 70 p	(161) [113] 71 q	(162) [114] 72 r
						
(163) [115] 73 s	(164) [116] 74 t	(165) [117] 75 u	(166) [118] 76 v	(167) [119] 77 w	(170) [120] 78 x	(171) [121] 79 y
						
(172) [122] 7A z	(173) [123] 7B {	(174) [124] 7C |	(175) [125] 7D }	(176) [126] 7E ~		
						

CONFIGURATION

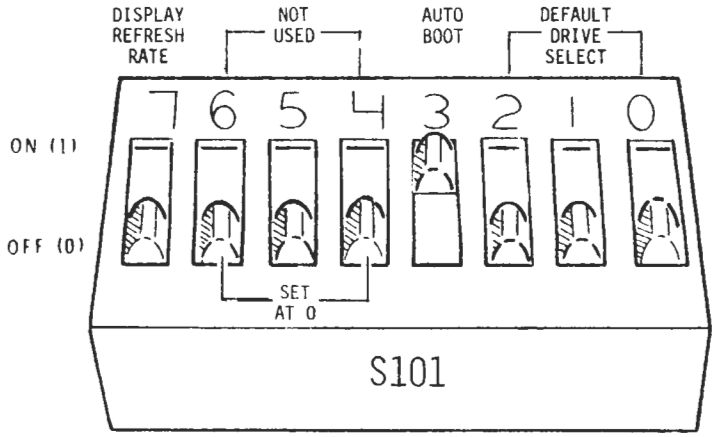
INTRODUCTION

The H/Z-100 is a versatile computer. Due to this versatility, many different configurations are possible. This section provides the basic information on how the computer may be configured.

MOTHERBOARD CONFIGURATION

S-101

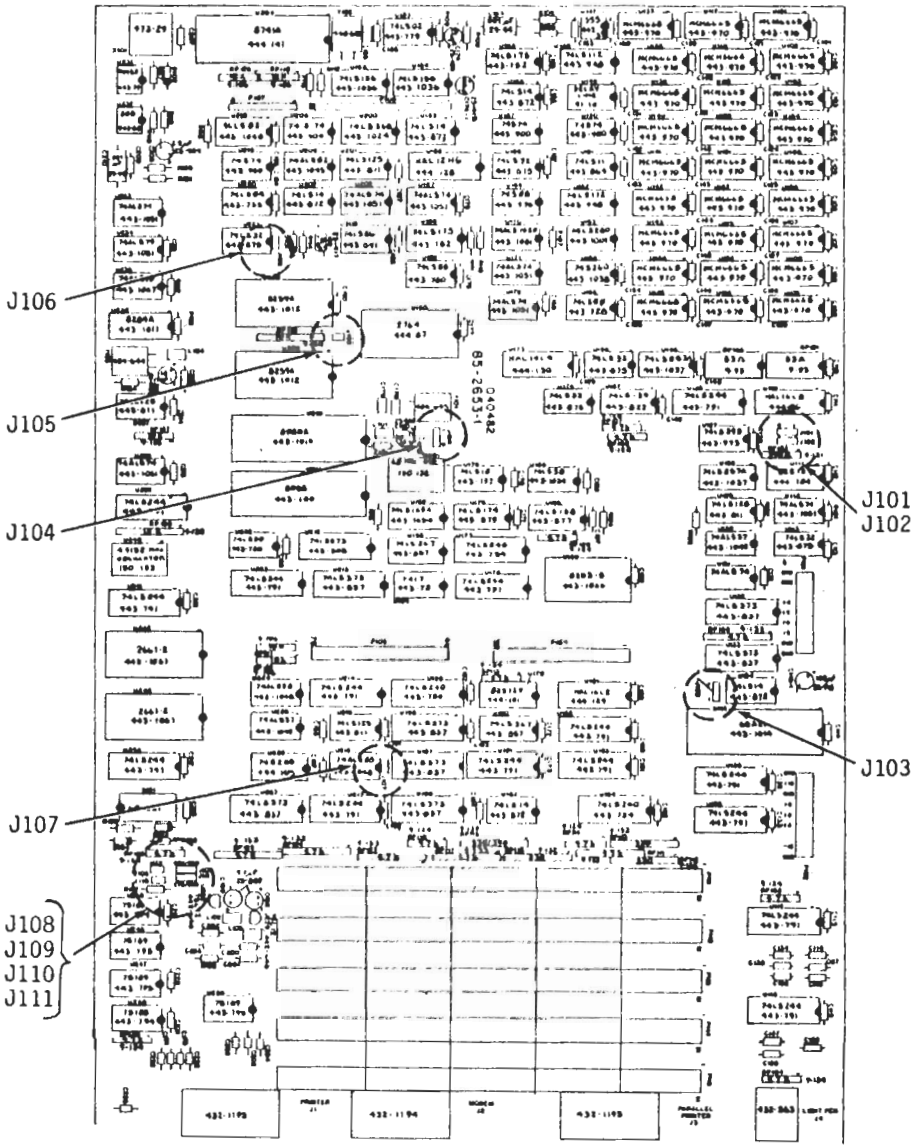
The 8-section slide switch (S101) on the motherboard determines the condition of the computer upon power-up or reset. The sections of S101 are defined as follows:



Section	Definition
0-1-2	The positions of these bits determine the default drive. 000 = 5-1/4". 100 = 8". 010 = Winchester.
3	This bit determines auto-boot. 0 = manual booting. 1 = Auto-boot.
4	Not used. Leave at 0.
5	Not used. Leave at 0.
6	Not used. Leave at 0.
7	This bit determines refresh rate of the display RAM. 0 = 60 Hz. 1 = 50 Hz.

JUMPERS J101 THROUGH J111

Refer to the pictorial below when reading through the jumper descriptions.



J101 and J102 determine the size of ROM that may be installed.

ROM	J101	J102
2764 (8K)	0	0
27128 (16K)	1	0
27256 (32K)	0	1

The 27128 and 27256 ROMs are not used in the H/Z-100 at this time, but may be supported in the future.

J103 determines the polarity of the light pen. The markings on the PC board are self-explanatory. The light pen is not supported at this time.

J104 is jumpered by a foil run on the motherboard to the 1 position. This connection jumpers the NMI line to ground.

J105 when jumpered, grounds the test pin of the 8088 microprocessor. J105 is not used at this time.

J106 is not used at this time. This position is normally unjumpered.

J107 is jumpered by a foil run on the motherboard. This position will be shorted regardless of a jumper.

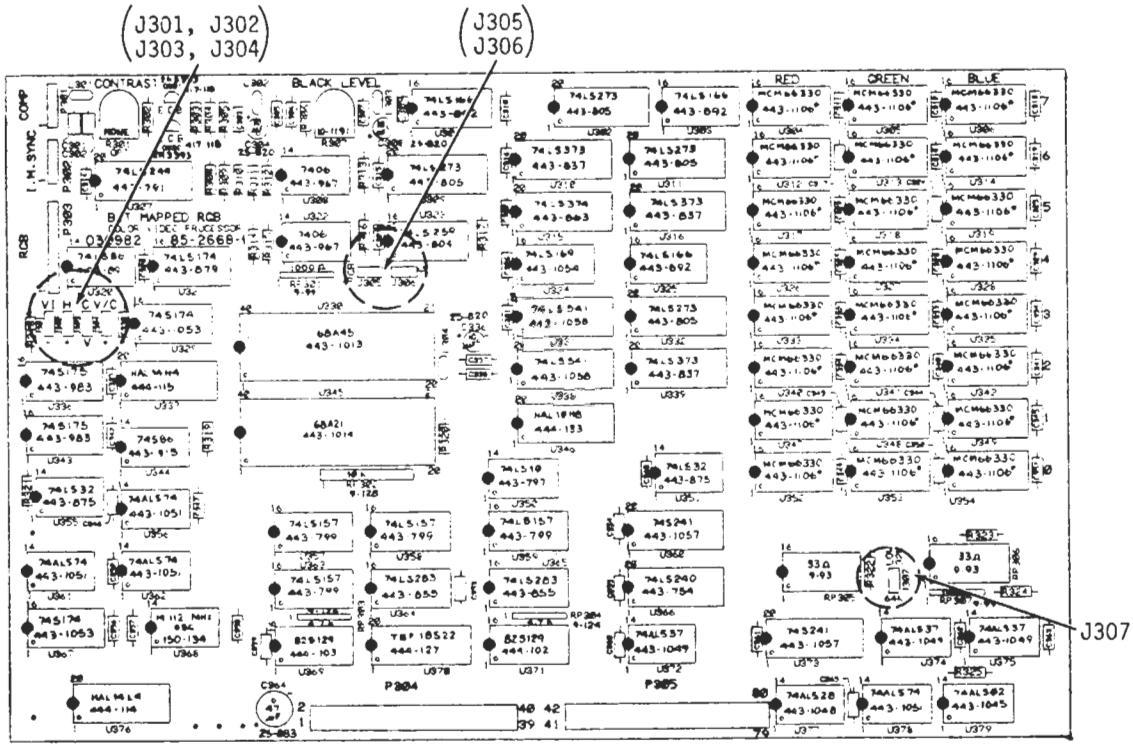
J108 determines whether or not pin 18 ($\overline{\text{TxEMP}}$) of U242 is connected to the serial interrupt line (EPCIBINT). When using Heath peripherals, this jumper location is normally unjumpered.

J109 and J111 determine the handshaking protocol of IC U243. This port will support many different printers through the positioning of these jumpers. J109 determines whether pin 16 ($\overline{\text{DCD}}$) of U243 is connected to the RTS line or ground. J111 determines whether pin 17 ($\overline{\text{CTS}}$) of U243 is connected to the RTS line or ground. Using Heath peripherals, J109 connects $\overline{\text{DCD}}$ to RTS and J111 connects $\overline{\text{CTS}}$ to ground. If the H/Z-100 you are servicing is not set up in the Heath configuration, the jumpers may be connected to support another manufacturer's peripheral. Consult the peripheral manual for proper jumpering.

J110 determines whether or not pin 18 ($\overline{\text{TxEMP}}$) of U243 is connected to the serial interrupt line (EPCIAINT). The position of this jumper is determined by the peripherial used on this port. When using Heath peripherals, this jumper location is normally unjumpered.

VIDEO BOARD CONFIGURATION

Refer to the pictorial below when reading through the jumper descriptions.



J301 determines the polarity of the vertical sync as connected to the internal monitor. The markings on the PC board are self-explanatory. In the Heath mode, this jumper is set for negative vertical sync.

J302 determines the polarity of the horizontal sync. The markings on the PC board are self-explanatory. In the Heath mode, this jumper is set for negative horizontal sync.

J303 determines whether the signal at pin 9 of the RGB cable assembly is composite sync or vertical sync. When the jumper is in the CV position, the signal at pin 9 of the RGB cable assembly is composite sync. When the jumper is in the V position, the signal at pin 9 of the RGB cable assembly is vertical sync.

J304 determines the polarity of the vertical sync as connected to the RGB cable assembly. The markings on the PC board are self-explanatory. In the Heath mode, this jumper is set for negative vertical sync.

J305 and J306 determine the type of video signal that is to be available. When the jumpers are in the RGB position, the output video signal will support a color or an 8-level gray scale output. When the jumpers are in the G position, the video output will be a monochrome signal. If the video board contains only one bank of RAM, these jumpers must be set at G.

J307 determines how the individual 64K RAM banks will be addressed. When no jumper is installed, the video board will address the high 32K end of the 64K bank. When the jumper is installed in the 32K position, the video board will address the lower 32K end of the 64K bank. When the jumper is installed in the 64K position, the video board will address a 32K section within the 64K bank. NOTE: An advanced programmer may address the whole 64K bank of RAM if he alters the operation of the CRTC. This, however, is not supported at this time. To further explain the jumpering of these two jumpers, the RAM chips that may be installed in the banks must be discussed.

There may be two primary RAM chips installed on the video board; 64K or 32K chips. The 32K RAM chips are further divided in two categories; high end 32K or low end 32K chips. Because 32K RAM chips are actually 64K chips that failed in either the high or low section of the 64K memory area, the 32K and 64K chips are pin for pin compatible. To tell the difference between the two types of 32K chips, you must first identify the manufacturer.

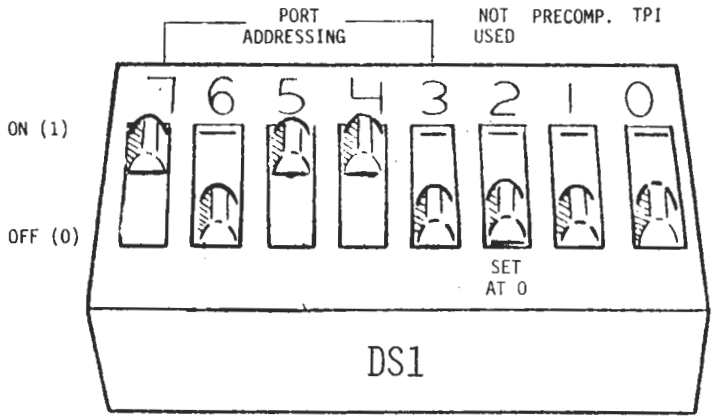
There are two approved manufacturers at this time, Motorola and Okie. Use the chart below to identify high-end or low-end chips.

Manufacturer	Generic Number	Type
Okie	MSM3732L-20AS	low end (HE 443-1106)
Okie	MSM3732H-20AS	high end (HE 443-1107)
Motorola	MCM66330	low end (HE 443-1106)
Motorola	MCM66331	high end (HE 443-1107)

Once you have the chips identified, you can set the jumper J307. Remember, you cannot mix low end and high end 32K chips on the video board. You may, however, mix manufacturers. If the majority of chips are high end chips, then all chips must be high end and J307 set accordingly. If the majority of the chips are low end chips, then all chips must be low end and J307 set accordingly. If the chips are 64K RAMs, you must set J307 to the 64K position.

DISK CONTROLLER (H/Z-207)

The 8-section slide switch (DS1) on the disk controller board determines the configuration of the board. The sections of DS1 are defined as follows:



Section	Definition
0	This bit determines the TPI of the 5-1/4" disk drive. 0 = 48 TPI. 1 = 96 TPI.
1	This bit determines whether precomp is on or off. 0 = precomp off. 1 = precomp on.
2	Not used. Leave at 0.
3-4-5-6-7	Port addressing. A port I/O map is shown below:

I/O ADDR. (Binary)	READ	WRITE	PORT DESIGNATION
SSSSS000 *	X		1797 Status Register
SSSSS000		X	1797 Command Register
SSSSS001	X	X	1797 Track Register
SSSSS010	X	X	1797 Sector Register
SSSSS011	X	X	1797 Data Register
SSSSS100		X	Control Latch
SSSSS101	X		Status Port

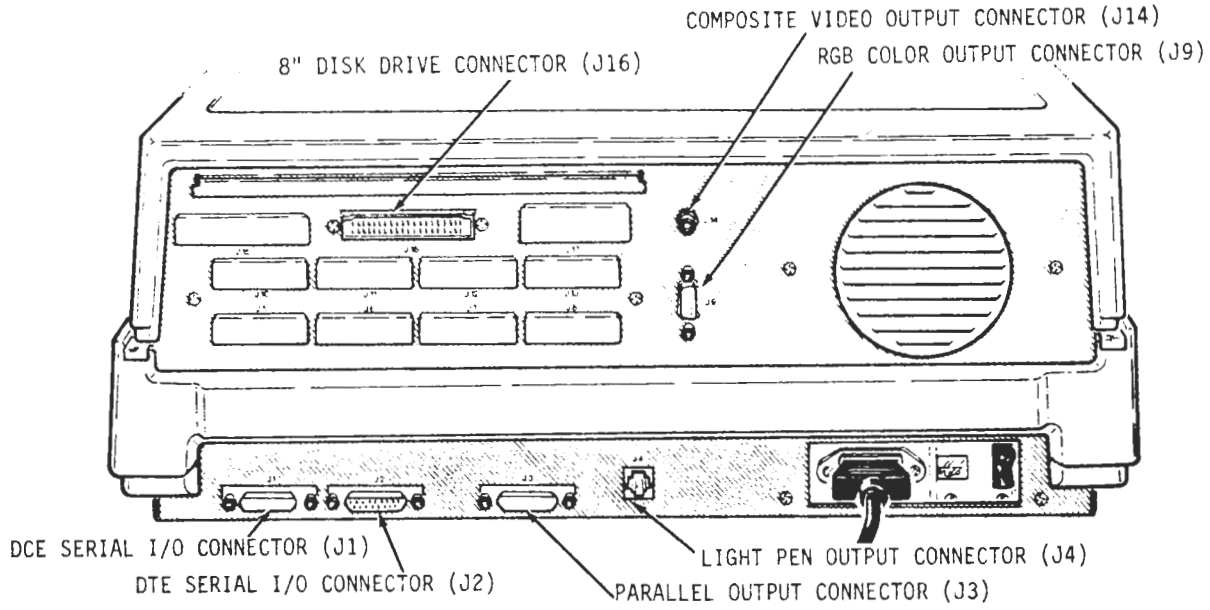
* S = dip switch bit

The dip switch bits are simply defined from the binary equivalent of the switches. An example, port addressing for the H/Z-100, is shown below.

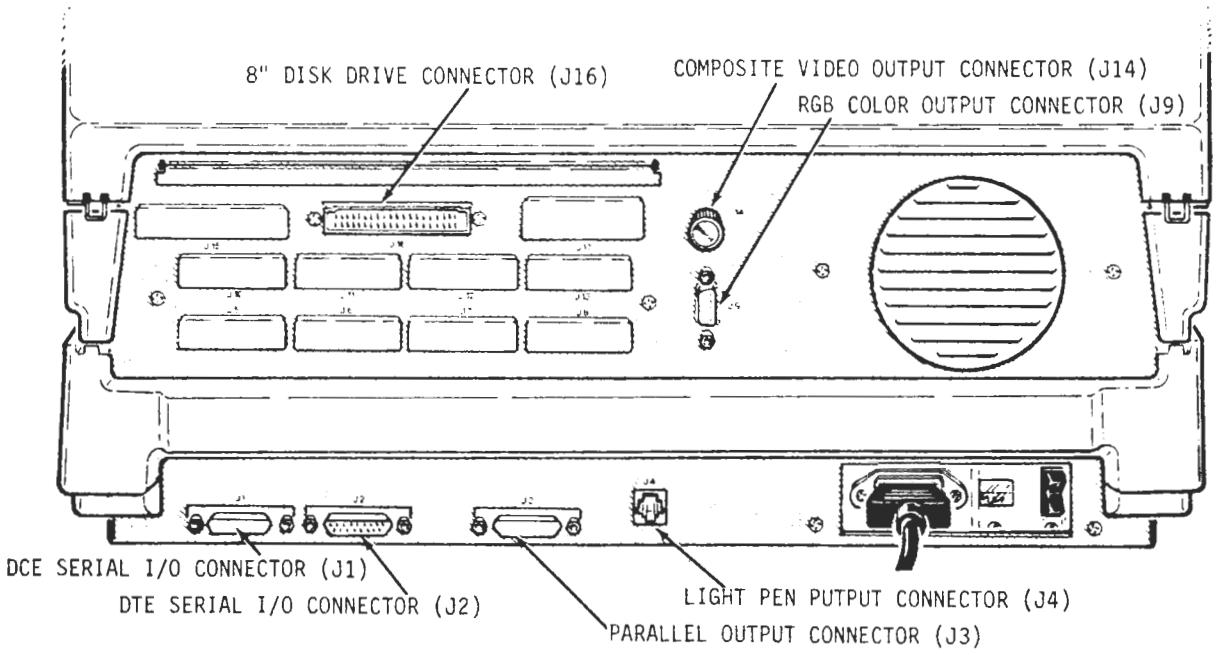
SSSSSXXX * = 10110XXX = H/Z-100 port B0 - B7.

* X = 1797 register, control latch, or status port.

OUTPUT CONNECTORS



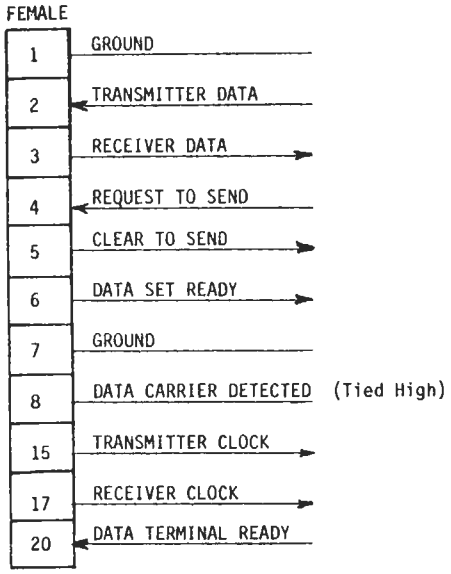
LOW PROFILE



ALL-IN-ONE

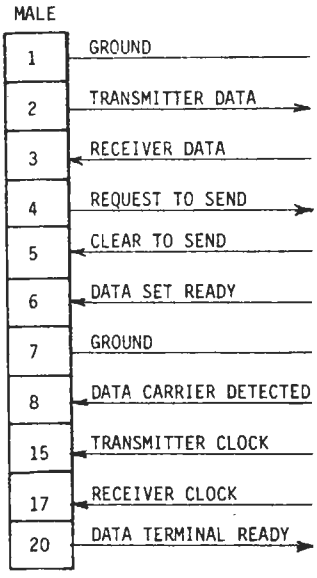
SERIAL I/O CONNECTOR (J1)

The 25-pin D connector at this location is a RS-232C DCE connector. Its location on the I/O map is port E8 (Hex). The primary use of this connector is for printer operation. For Heath supported printers, refer to "Printer Configuration" (elsewhere in this section) for recommended hardware set-up. Other peripherals and non-Heath printers may require special set up procedures. Use the pinout description and the peripheral's manual for recommended set-up.



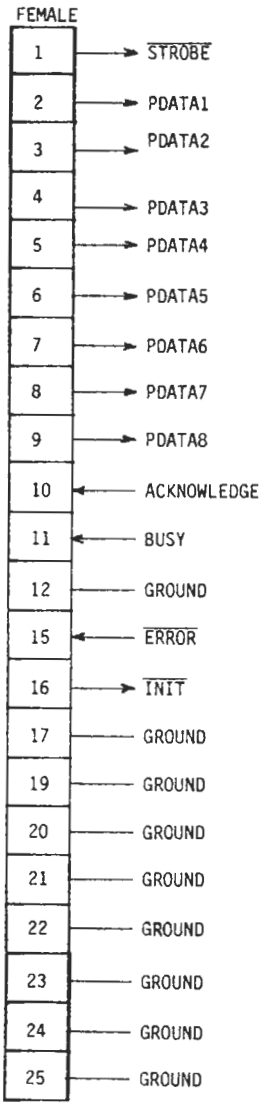
SERIAL I/O CONNECTOR (J2)

The 25-pin D connector at this location is an RS-232C DTE connector. Its location the I/O map is port EC (Hex). The primary use of this connector is for modem operation. Refer to the pictorial below for a description of the pinouts of this connector.



PARALLEL OUTPUT CONNECTOR (J3)

The 25-pin D connector at this location is a Centronics compatible printer port. Its location on the I/O map is E0 (Hex). The primary use of this connector is for parallel printer hookup. Refer to the pictorial below for a description of the pinouts of this connector.



LIGHT PEN OUTPUT CONNECTOR (J4)

This connector provides the necessary signals to operate a light pen.

COLOR OUTPUT CONNECTOR (J9)

When the video board has the color option installed, this connector provides the necessary signal to drive an RGB video monitor. Refer to the pictorial below for a description of the pinouts of this connector. Also refer to the video monitor's manual for hookup instructions.

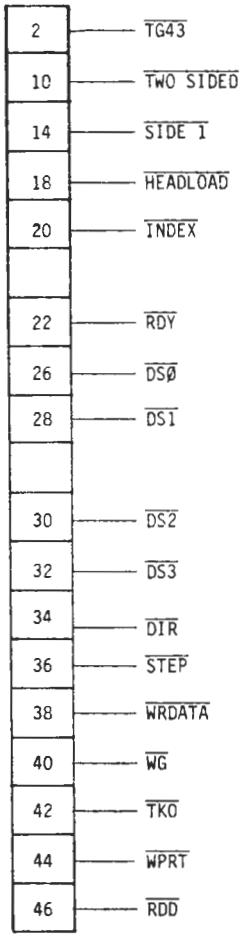
Pin	Signal
1	Ground
2	Ground
3	Red
4	Green
5	Blue
6	Not connected
7	Not connected
8	Horizontal Sync
9	Vertical or Composite Sync

COMPOSITE VIDEO OUTPUT CONNECTOR (J14, LOW PROFILE ONLY)

This connector is located on the Low Profile model. This connector provides the necessary signals to drive a monochrome video monitor. Refer to the manual of the video monitor for instructions on hookup.

8″ DISK DRIVE CONNECTOR (J16)

This 50-pin connector provides the necessary signals to drive an 8" Shugart compatible disk drive. Refer to the pictorial below for a description of the pinouts of this connector.



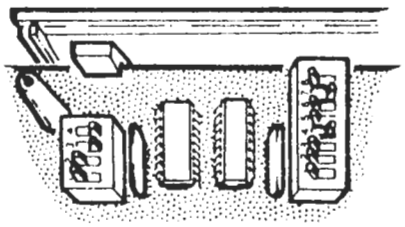
*All odd numbered pins grounded

PRINTER CONFIGURATIONS

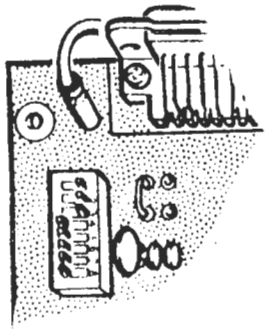
Refer to the following pictorials for information on how to set the configuration switches within the following Heath supported printers. Handshaking for each of the printers is software supported in Z-DOS using the program "CONFIGUR". For information on the Configur program, refer to the Z-DOS manual or the H/Z-100 User's Manual.

MX-80 PRINTER

The MX-80 may be connected to the H/Z-100 using either the parallel or serial modes. To use the MX-80 in the parallel mode, set the switches within the MX-80 case as follows:

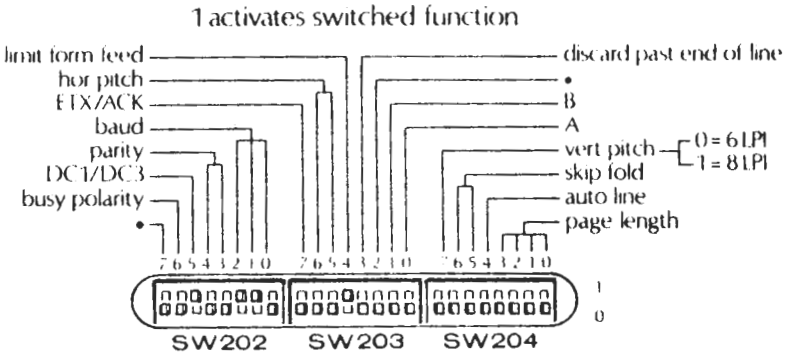


Remember, the interface cable must be attached to the parallel output connector J3 for the MX-80 to operate in the parallel mode. To use the MX-80 in the serial mode set the switch on the serial board within the MX-80 as follows:



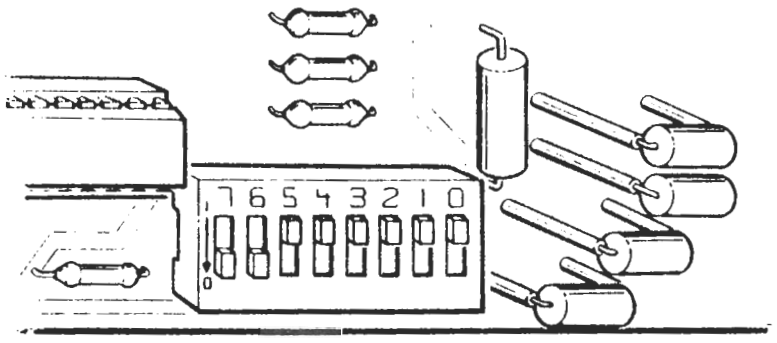
H/Z-25 PRINTER

To use the H/Z-25 with the H/Z-100, set switches SW202, SW203, and SW204 as shown below:



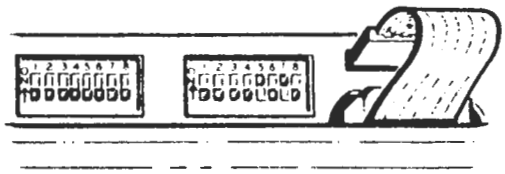
H/WH-14 PRINTER

To use an H/WH-14 with the H/Z-100, set switch SW102 as shown below:



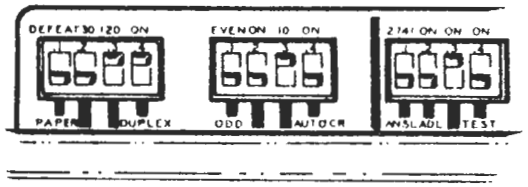
DIABLO 630 PRINTER

To use a Diablo 630 with the H/Z-100, set the internal switches as shown below:



DIABLO 1640 PRINTER

To use a Diablo 1640 with the H/Z-100, set the internal switches as shown below:



If other manufacturer's printers are being used, refer to its manual to determine proper configuration for that printer.

NEC VIDEO MONITOR CONFIGURATION

Follow the instructions below to configure the NEC Video Monitor cable for use with the H/Z-100.

-- Remove the DIN-type connector from the NEC Video Monitor cable (P/N PC-8091A).

-- Obtain a subminature 9-pin male D connector (Amp P/N 205204-1) and cable clamp assembly (Amp P/N 207908-1).

-- Remove 3/4" of outer insulation material from the NEC cable.

-- Remove 1/4" of insulation from each end of the exposed conductors. Pre-tin each wire.

-- Connect each of the wires from the NEC cable to the 9-pin connector as follows:

Quantity	NEC Cable	D Connector Pinout	Signal
1	BR/WHT	5	Blue Video
1	BR/BLK	4	Green Video
1	BR/Red	3	Red Video
3	Solid Yellow	2	Ground
2	Solid Yellow	1	Ground
1	Solid Gray	1	Ground
1	YEL/WHT	9	V Sync
1	YEL/BLK	8	H Sync

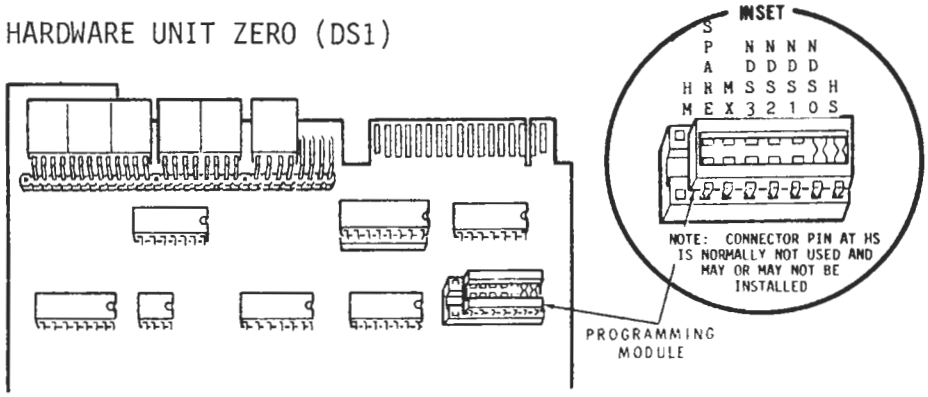
-- Assemble the cable clamp assembly.

INTERNAL DISK DRIVE CONFIGURATION

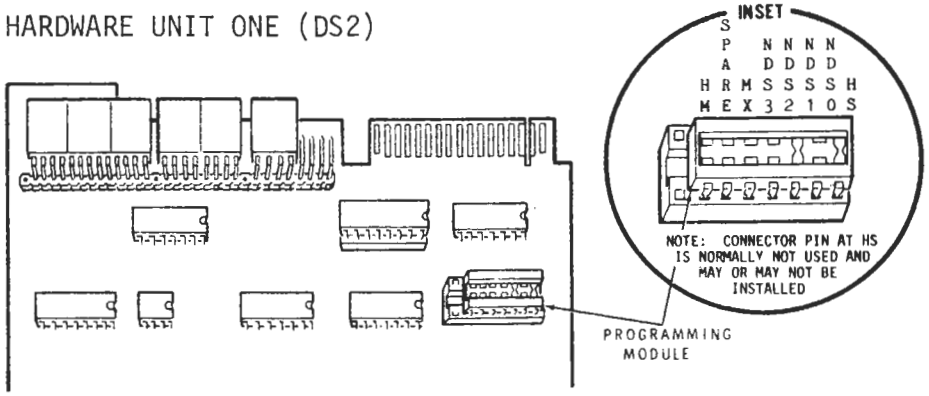
Drive programming for the internal 5-1/4", 48 TPI Tandon disk drives is shown below. On some disk drives the jumper pack shown below may be replaced with a single jumper wire at NDS0 or NDS1. This configuration is considered normal since connection across HS is not necessary. If you encounter one of these drives, do not replace the jumper wire with the jumper pack (HE 432-1068). The leads on this jumper pack are too thin and may not make proper contact in the socket. If you do not have a Tandon jumper pack, carefully insert a piece of bare wire (HE 340-8) into the proper location.

The location of the resistor pack is the same as in other Heath or Zenith Data Systems disk drive systems. That is, the resistor pack(s) are removed from all drives except the last hardware unit.

HARDWARE UNIT ZERO (DS1)

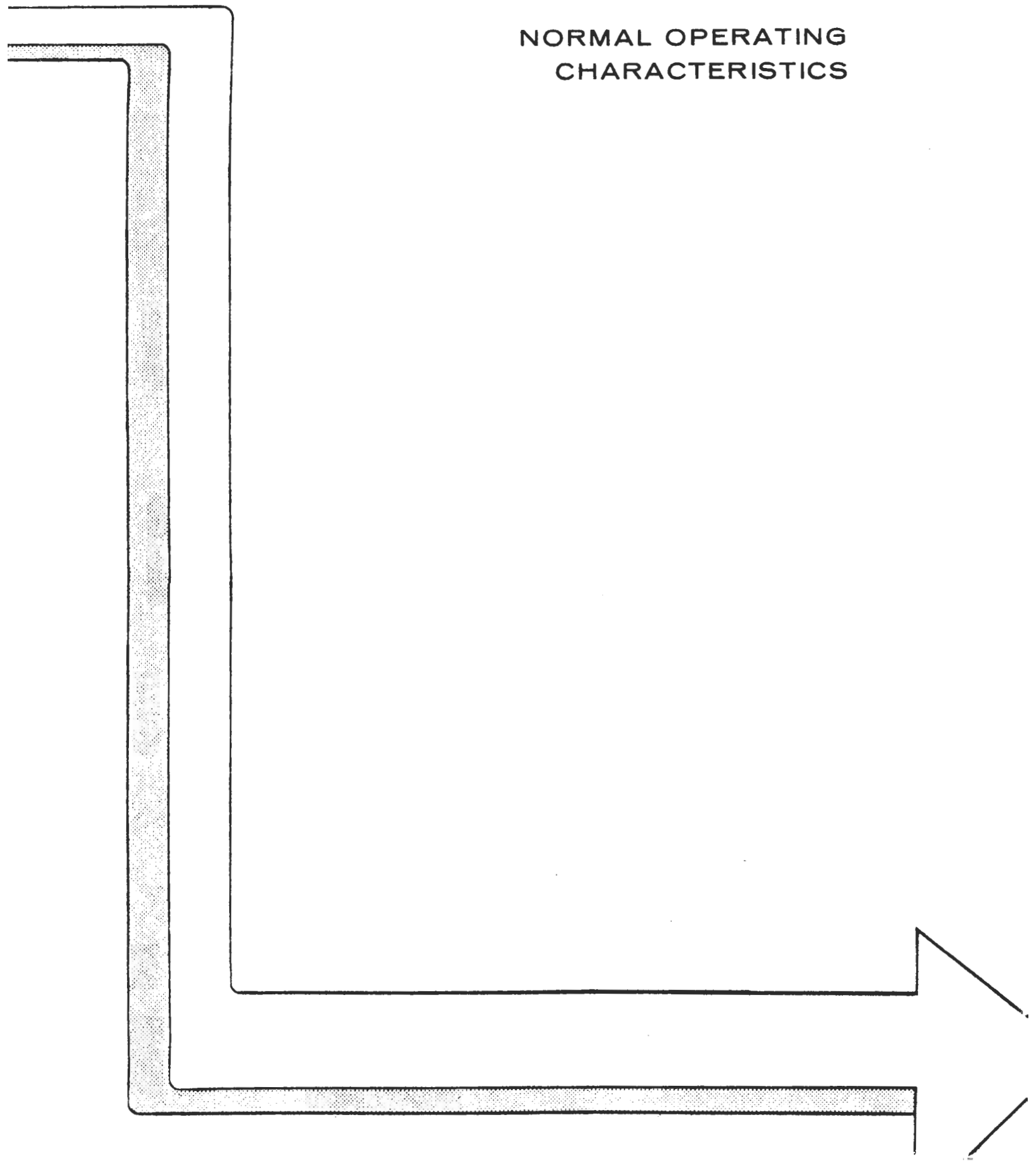


HARDWARE UNIT ONE (DS2)



TECHNICIAN NOTES:

NORMAL OPERATING CHARACTERISTICS



The following characteristics of the H/Z-100 Computer are considered normal. Become familiar with these characteristics. It can save you time by preventing any servicing of the computer for a condition that is considered normal operation.

-- During the boot process, the cursor will move to a random position in the line "Read Completed". The position of the cursor may change with each boot-up.

-- The internal 5-1/4" disk drives will not turn off until they time out 18 seconds after the last deselection. Even if a master reset is initiated, the drive motors will stay on until they are timed out.

-- The computer is sent to the customer in the auto-boot mode. If a disk is not installed within 30 seconds after power-up, the display will show a disk error message and the computer will go into the monitor mode.

BLOCK DESCRIPTION

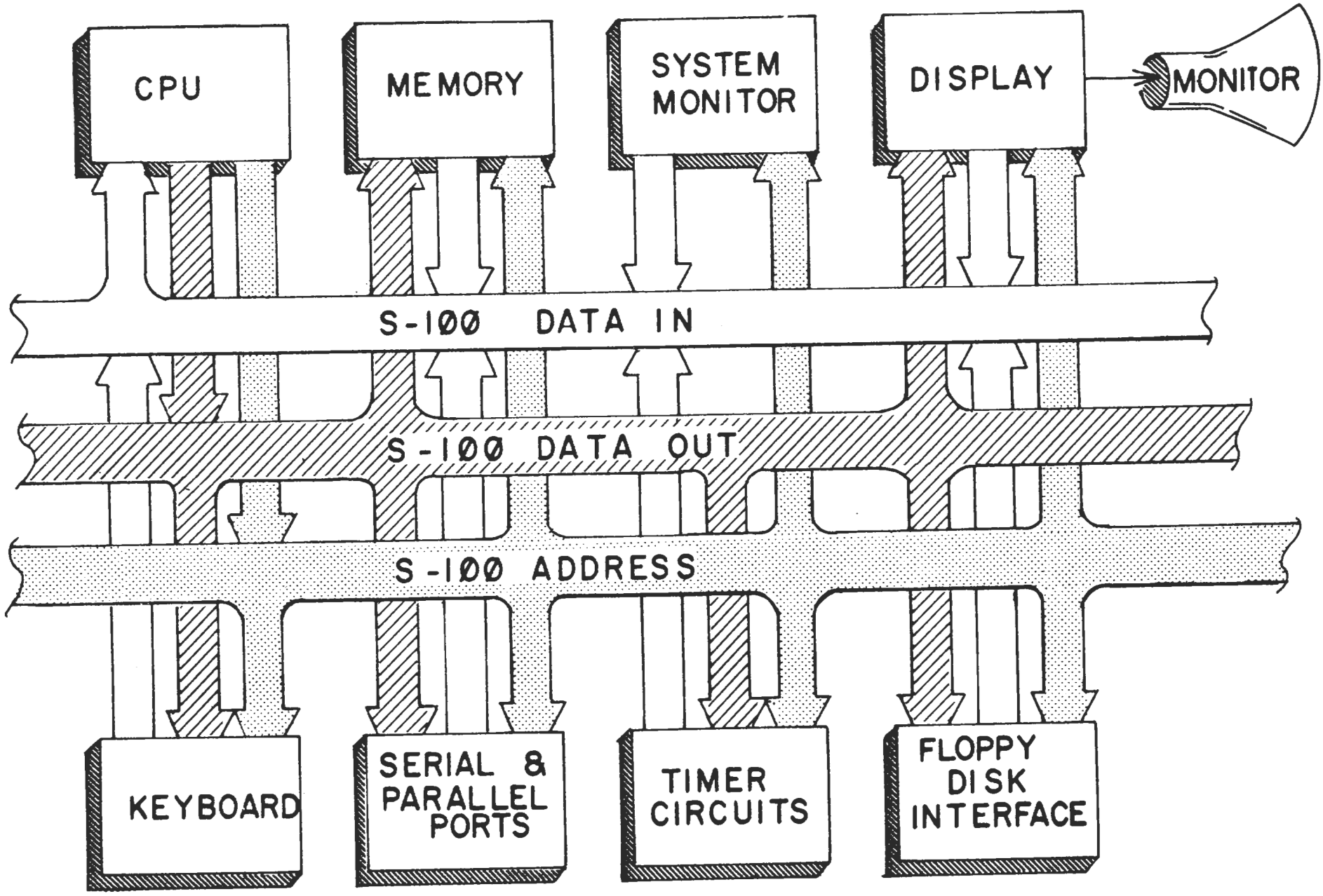
INTRODUCTION

This block diagram description will show you how the H/Z-100 operates as a system. It starts with the basic blocks and then analyzes what goes on in each block. Once you understand the operation on this level, go on to the circuit descriptions located in the appropriate section of the Blue Book.

The circuit descriptions are written on the level of the experienced microcomputer technician. If you're new to computers, we recommend that you study one of the computer courses available from Heath Company.

Even if you are an experienced computer technician, you may want to review the IC data sheets in the Data Sheets section of this book. The description explains the important features of the more complex ICs affecting circuit operation, but assumes that you know how the ICs work. This is necessary to keep the circuit description from drifting off its intended subject -- the H/Z-100.

Likewise, you should become familiar with the S-100 bus (IEEE-696). The description explains how and why certain lines are developed, but assumes that you're familiar with the bus pin-out and understand the mnemonics used. You can find a description of the S-100 bus in the Appendices section of this manual.



H/Z-100 COMPUTER

SYSTEM OVERVIEW

In this block diagram description, we'll cover the major circuits of the H/Z-100 Digital Computer. Though some of these block diagrams appear detailed, several buffers and gates have been left out to keep the illustrations from getting cluttered. As a result, you will see several circuits that appear to connect to the S-100 bus when they may actually be separated from the bus by an octal buffer. The block diagrams do show the buffers where the bus must be multiplexed or demultiplexed.

Basically, the H/Z-100 Digital Computer can be broken down to eight major blocks: The CPU, memory, system monitor, display, keyboard, serial & parallel ports, timer circuits, and the floppy disk interface board.

The CPU block consists of two microprocessors; an 8085 8-bit processor and an 8088 16-bit processor. The 8085 permits software compatibility with the existing body of 8080/8085 software while the 8088 provides greater computing power for new applications. Either CPU is software selectable. The 8088 CPU, however, is the active processor after power up or reset.

The memory block contains up to three 64-kilobyte banks of RAM for 192K of read/write memory. The memory circuits provide refresh to prevent data loss when the CPU isn't accessing memory. This block also has an arbitration circuit to ensure that refresh doesn't occur when the CPU is accessing RAM, and that the CPU won't access RAM while a refresh operation is taking place.

The system monitor takes control of the CPU after power up or reset. Through it, the CPU programs the I/O circuits to allow communicating with the user.

The display circuits provide a video graphics output from the computer. This can be monochrome or color. The display circuits can contain up to 192K of RAM; 64K for each primary color (red, green, blue). After reset, the system monitor programs the display circuits to print alphanumeric characters when the appropriate keyboard key is pressed. However, the display memory can be directly addressed by the CPU, permitting graphics.

The keyboard circuits are built around a dedicated microprocessor that interfaces the matrix keyboard to the CPU. Through software control, the keyboard can output either the normal ASCII character set, or a special event-driven character set for real-time applications. The keyboard circuits also contain oscillators for bell and key-click sounds.

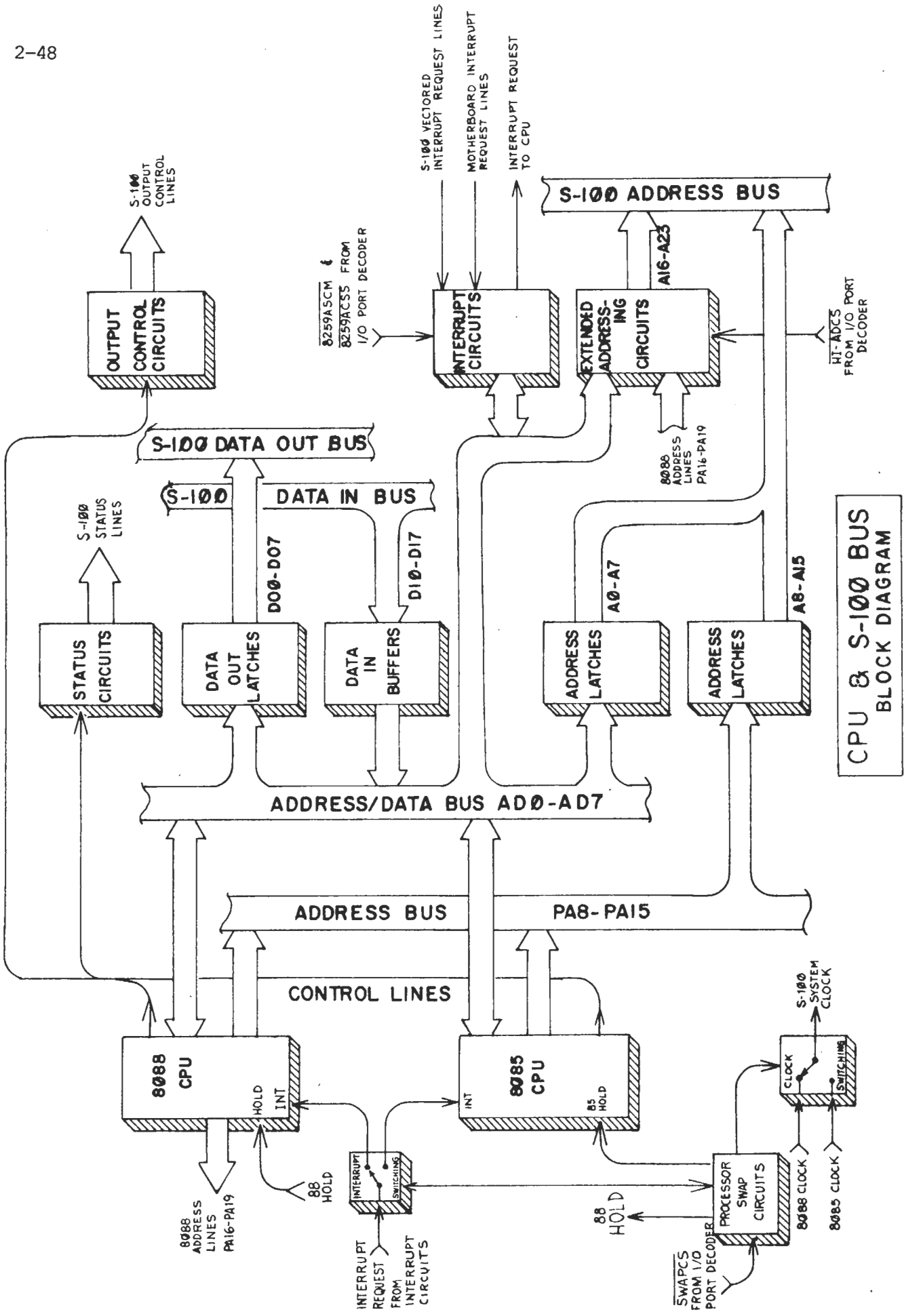
The serial and parallel ports permit the H/Z-100 to communicate with outside devices such as MODEMs, printers, and voice synthesizers.

The timer circuits contain programmable counters that the CPU can use for a real-time clock, a calendar, or for other events-related functions. This circuit has its own oscillator, so the CPU doesn't need to spend any time periodically updating the count.

The floppy disk interface permits connecting up to four 8" and four 5" floppy disk drives to the H/Z-100. This is the only circuit in this block diagram that plugs into the S-100 bus. Though the other circuits communicate through the S-100 bus, they are all located on either the motherboard or the video board. See the Disk Controller and Drives section of this Blue Book for more information on the interface board.

The block diagram also shows three of the major S-100 buses; data in, data out, and address. Both data buses are 8 bits wide; if the CPU fetches a 16-bit instruction, it transfers it a byte at a time. The address bus is 24 bits wide, allowing the CPU to directly address up to 16 megabytes of memory.

Note that the data directions are referenced to the CPU. Data from the top bus goes IN to the CPU. Data from the CPU goes OUT to memory or a port through the middle bus.


S-100 VECTORED INTERRUPT REQUEST LINES
MOTHERBOARD INTERRUPT REQUEST LINES
INTERRUPT REQUEST TO CPU
S-100 ADDRESS BUS
S-100 OUTPUT CONTROL LINES
8259ASCM & 8259ACSS FROM I/O PORT DECODER
A16-A23
HT-ADCS FROM I/O PORT DECODER
OUTPUT CONTROL CIRCUITS
INTERRUPT CIRCUITS
EXTENDED ADDRESSING CIRCUITS
8088 ADDRESS LINES PA16-PA19
S-100 DATA OUT BUS
S-100 DATA IN BUS
S-100 STATUS LINES
D00-D07
D10-D17
A0-A7
A8-A15
STATUS CIRCUITS
DATA OUT LATCHES
DATA IN BUFFERS
ADDRESS LATCHES
ADDRESS LATCHES
CPU & S-100 BUS BLOCK DIAGRAM
ADDRESS/DATA BUS AD0-AD7
ADDRESS BUS
PA8-PA15
CONTROL LINES
S-100 SYSTEM CLOCK
8088 CPU
HOLD
INT
8085 CPU
INT
85 HOLD
CLOCK
SWITCHING
INTERRUPT
SWITCHING
8088 ADDRESS LINES PA16-PA19
88 HOLD
INTERRUPT REQUEST FROM INTERRUPT CIRCUITS
88 HOLD
PROCESSOR SWAP CIRCUITS
8088 CLOCK
8085 CLOCK
SWAPCS FROM I/O PORT DECODER

DETAILED LOOK

CPU AND S-100 BUS

READING AND WRITING DATA

The 8085 CPU is an 8-bit internal, 8-bit external processor. It is software compatible with the 8080 CPU and can directly address up to 64 kilobytes of memory. The 8088 CPU is a 16-bit internal, 8-bit external processor. It is software compatible with the 8086 CPU and can directly address up to 1 megabyte of memory. This is due to the extended-address lines, PA16-PA19.

Except for lines PA16-PA19, the 8088 address, data, and control lines function in the same manner as those of the 8085. The lower 8 bits of the address bus is multiplexed with the data bus. Whenever either CPU accesses memory, it first places the address on lines AD0-AD7 and PA8-PA15. This information is latched into the address latches shown in the lower center of the block diagram. The outputs of these latches connect to lines A0-A15 of the S-100 bus.

Next, if writing data, the CPU places the data onto lines AD0-AD7 and latches it into the data-out latch. The output of the latches connects to lines D00-D07 of the S-100 data output bus. When the data and address lines are stable, the CPU control lines activate certain lines in the status circuits and the output control circuits to write the data into the addressed memory location.

The operation is almost the same for reading from memory. In this case, however, once the address lines are stable, the status and output control lines will cause the addressed memory location to place the data byte onto the S-100 data-in bus. It is then coupled through the data-in buffers and loaded into the CPU.

EXTENDED ADDRESSING

The extended addressing circuits provide up to 16-megabyte addressing capability, in accordance with the IEEE-696 standards. It does this by latching data onto address lines A16-A23.

When the 8088 is active, the extended address lines couple the 8088 extended address lines, PA16-PA19, to A16-A19 of the S-100 bus. Thus the 8088 is able to access its normal 1-megabyte address space.

If the 8088 needs to address a location above 1 megabyte, it places the extended address values onto lines AD0-AD7 and asserts HI-ADCS from the I/O port decoder. The extended address circuits disconnect the PA16-PA19 lines and latch the value on AD0-AD7 onto A16-A23 of the S-100 bus.

When the 8085 is active, the extended addressing circuits are normally disabled; lines A16-A23 are zero so the 8085 is operating within the first 64K bank of memory.

If the 8085 needs to address a location above 64 kilobytes, it places the extended address values onto lines AD0-AD7. It then asserts HI-ADCS to latch this value onto A16-A23 of the S-100 bus.

PROCESSOR SWAP CIRCUITS

The processor swap circuits handle all the switching necessary to disable one CPU and enable the other. It is activated by asserting SWAPCS from the I/O port decoder and sending a control word from the active CPU to the swap circuits.

The swap circuits switch CPUs by asserting the proper HOLD line. For example, if switching from the 8085 to the 8088, the 85HOLD line will go high to disable the 8085, and the 88HOLD line will go low to enable the 8088.

The swap circuits also determine whether the 8088 clock or the 8085 clock is coupled to the S-100 system clock line. Although these 5-MHz clocks are crystal controlled, they aren't in phase. To ensure that a spike doesn't occur, the clock switching circuits hold the system clock line at its previously-valid logic state until the incoming signal matches it.

For example, if the system clock is logic one when the H/Z-100 swaps from the 8085 to the 8088, it will remain high until the 8088 clock is logic one. Once this occurs, the 8088 clock is allowed to pass to the S-100 system clock line.

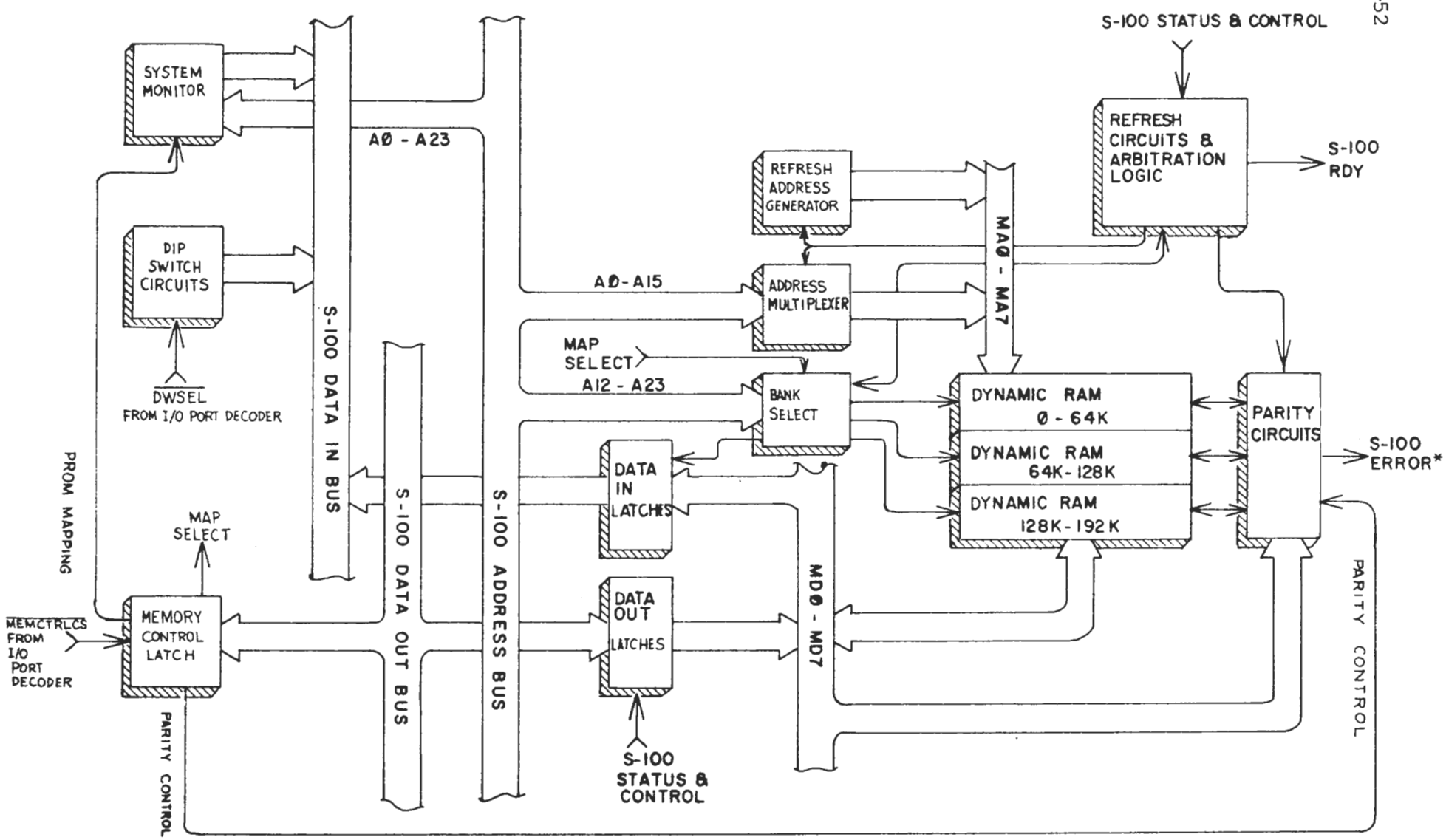
The processor swap circuits also control the interrupt switching circuits. These circuits ensure that any interrupt request is routed to the currently-selected processor. These circuits also have a masking feature that forces the 8088 to handle all interrupts.

If, for example, the 8085 is active and the mask mode is selected, the 8085 will continue to operate until an interrupt request occurs. The interrupt switching circuits cause the processor swap circuits to disable the 8085 and enable the 8088. The interrupt switching circuits then route the interrupt request to the 8088. After the interrupt is processed, it is up to the interrupt-handler program to return control to the 8085.

INTERRUPT CIRCUITS

The interrupt circuits monitor various circuits on the motherboard and notify the CPU if any of the circuits have data that requires immediate attention. These circuits include the various I/O ports, the timer, and memory parity. Also, the interrupt circuits monitor the vectored interrupt lines which are used by S-100 boards, such as the Z-207 floppy disk interface board.

The interrupt circuits are programmable through the address/data bus and the chip-select lines, 8259ACSM and 8259ACSS. Programming options include: masking out unwanted interrupts, selecting the interrupt priority, and setting up the pointer to the interrupt-handling routine.



MEMORY CIRCUITS
BLOCK DIAGRAM

MEMORY CIRCUITS

SYSTEM MONITOR

The system monitor is an 8K ROM that can be relocated in memory through software control. This is done by the PROM mapping signal from the memory control latch. The memory control latch is programmed by sending it a control word from the CPU and asserting the MEMCTRLCS line from the I/O port decoder.

There are four relocating options available to the system monitor:

Option 0 makes the ROM appear to be in all memory locations whenever a memory read is performed. Memory writes still take place normally. This is the option selected immediately after power-up/reset. The 8085 is in control of the H/Z-100, switches to the 8088, and then selects Option 2 for the system monitor.

Option 1 puts the ROM at the top 8K of every 64K page of memory. This is useful for the 8085, which has only a 64K natural address space.

Option 2 gates the ROM to appear in the top 8K of the 8088's natural 1 megabyte address space. This is the normal operating option when the 8088 has control of the H/Z-100.

Option 3 disables the ROM. The ROM is not accessible when this mode is selected.

When the ROM is selected, all other memory (except video RAM) is disabled. This allows other memory to share the ROM's address space using the S-100 PHANTOM line.

After reset, the monitor tests the status of the dip-switch circuits to set up the H/Z-100 default operating modes. See the Configuration section of this Manual for the various configurations.

DYNAMIC RAM

Read/write memory consists of three 64K banks of dynamic RAM. This permits a total of 192K of onboard memory.

The proper memory location is selected by the combination of the address multiplexer and the bank select circuits. The S-100 address bus couples lines A0-A15 to the address multiplexer and lines A12-A23 to the bank select.

The bank select tests to see if the address is within the 192K address range. If so, it selects one of the three 64K banks. It does this by first asserting the appropriate row address strobe (RAS), followed by asserting the column address strobe (CAS).

When RAS asserts, the address multiplexer places lines A0-A7 onto memory address lines MA0-MA7, which are then latched into the row address registers in memory. When CAS asserts, the address multiplexer places lines A8-A15 onto MA0-MA7. This, plus the row address, points to the correct location in memory.

If the CPU is reading data from memory, the memory circuits will place the addressed byte on the memory data bus, MD0-MD7. Next, the bank select circuits enable the data-in latch to couple the data to the S-100 data-in bus.

If the CPU is writing data to memory, the appropriate S-100 status and control lines enable the data out latches to couple the data to MD0-MD7. From there, the data is written into the correct memory location.

Like the system monitor, portions of the dynamic memory can be relocated to different addresses. There are four options available, these include:

Option 0 is the normal configuration. This mode provides contiguous addressing to all of the memory.

Option 1 swaps the 0-48K segment with the segment between 64K-112K. This could be used for MP/M when running the 8085 processor.

Option 2 swaps the 0-48K segment with the segment between 128K-176K. This could also be used with MP/M and the 8085.

Option 3 swaps a 56K segment located between 4K-60K with a segment located between 68K-124K. This can be used to build an advanced disk operating system for CP/M-85.

REFRESH AND ARBITRATION LOGIC

The refresh circuits keep the dynamic RAM from losing its contents when the CPU isn't accessing a specific location. When the refresh circuits have control of memory, it disables the address multiplexer and enables the refresh address generator. The refresh address generator, a binary counter, places an 8-bit refresh address onto MA0-MA7.

At the same time, the refresh circuits send a control signal to the bank select circuit that forces it to enable all three memory banks. Subsequently, the same relative memory address is refreshed in each bank. When finished, the refresh circuits disable the refresh generator, increment its address count, and restore the address multiplexer and bank select circuits to normal operation.

The arbitration circuits determine if the refresh circuits or the CPU is to have control of the dynamic memory circuits. If the CPU is accessing memory when the refresh circuits attempt to refresh the RAM, the arbitration circuits will halt the refresh operation until the CPU is done.

Likewise, if the CPU attempts to access memory during the middle of a refresh operation, the arbitration circuits will stop CPU operation until refresh is completed. It does this by placing a logic zero on the S-100 RDY line. This line couples back to the active CPU to place the CPU into a wait state. While in a wait state, all of the CPUs register and signal lines do not change states; thus maintaining the processor's last valid status.

When the refresh circuit is finished refreshing the RAM, it brings the RDY to logic one. The CPU continues where it left off.

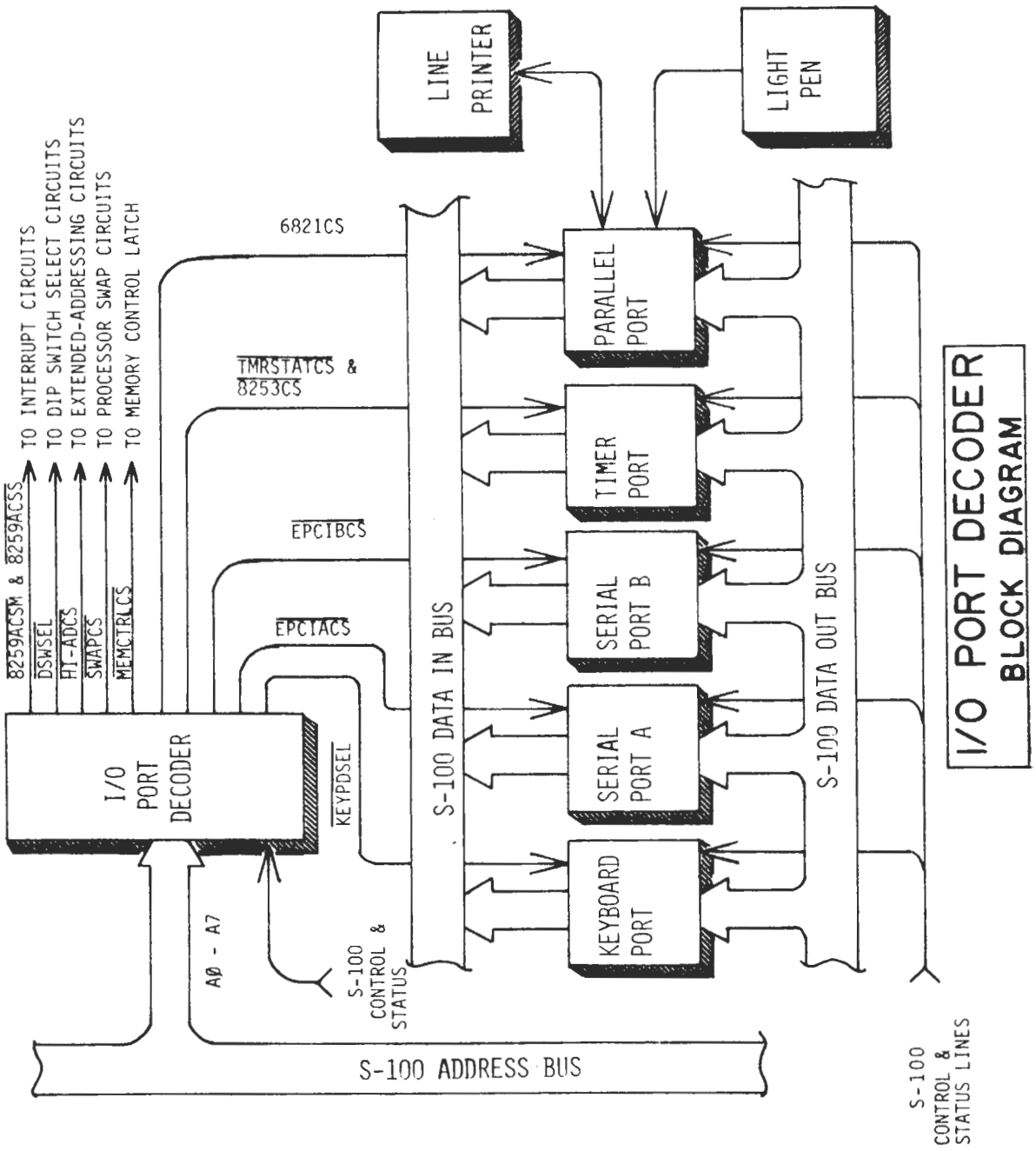
PARITY CIRCUITS

The parity circuits monitor the number of bits written into each byte of memory. If the number of bits are odd, the parity circuits adds a logic one to the count and stores it in parity RAM. Otherwise, it stores a logic zero in parity RAM. Parity RAM consists of a 64K x 1-bit RAM IC for each 64K x 8 memory bank.

When the CPU reads a memory location, the parity circuits count the number of bits in the 8-bit RAM location and adds it to the bit in the equivalent location in parity RAM. If the result is still even, everything is okay. However, if the total number of bits are odd, due to a bad memory chip for example, the parity circuits will assert the S-100 ERROR* line.

In turn, the ERROR* signal will send an interrupt request to the CPU. It is up to the user's program to process the interrupt.

The parity control line, from the memory control latch, allows you to disable the parity circuits, or to force a parity error for test purposes. In addition, a control line from the refresh circuits ensures that a parity error isn't generated during a memory write or a refresh.


I/O PORT DECODER
8259ACSM & 8259ACSS
DSWSEL
HI-ADCS
SWAPCS
MEMCTRLCS
TO INTERRUPT CIRCUITS
TO DIP SWITCH SELECT CIRCUITS
TO EXTENDED-ADDRESSING CIRCUITS
TO PROCESSOR SWAP CIRCUITS
TO MEMORY CONTROL LATCH
6821CS
TMRSTATCS & 8253CS
EPCIBCS
EPCIACS
KEYPDSEL
A0 - A7
S-100 CONTROL & STATUS
S-100 ADDRESS BUS
S-100 DATA IN BUS
S-100 DATA OUT BUS
KEYBOARD PORT
SERIAL PORT A
SERIAL PORT B
TIMER PORT
PARALLEL PORT
LINE PRINTER
LIGHT PEN
S-100 CONTROL & STATUS LINES
I/O PORT DECODER
BLOCK DIAGRAM

I/O PORT DECODER

GENERAL

The I/O port decoder provides enable lines to the data and control ports on the H/Z-100 motherboard. Each enable line is asserted by placing an address on A0-A7 of the address bus and asserting the appropriate S-100 control and status lines. The I/O port decoder responds by asserting the correct enable line.

The following lines have been discussed previously: 8259ACSM & 8259ACSS, DSWSEL, HI-ADCS, SWAPCS, and MEMCTRLCS. Refer to the appropriate block diagram description to see how these work.

The remaining lines control data transfer ports. This is done in conjunction with control and status signal from the S-100 bus.

KEYBOARD

The keyboard port contains an 8041A UPI, a dedicated microprocessor that handles all keyboard processing. When a key is pressed, the UPI determines which key it was, and sends the appropriate ASCII code to the computer. The UPI can also send an interrupt to the computer to tell it that it has a character ready. The program must provide the software to process this interrupt.

Through program control, you can change the ASCII code to a special code that sends out one byte pattern when the key is pressed, and another byte pattern when the key is released. This permits real-time applications. Other programming options include disabling the key-click, disabling the beep, and clearing the UPI's buffer.

To program the program processor, the CPU places the programming byte onto the S-100 data out bus and asserts KEYBDSEL. The appropriate S-100 control and status lines write the programming data into the keyboard circuits.

SERIAL PORTS A AND B

Serial ports A and B provide RS-232 communications between the computer and the outside world. These ports feature programmable baud rate, synchronous or asynchronous operation, optional parity testing, and character transmission length.

Serial port A uses a DCE connector and can be used for an asynchronous device such as a printer.

Serial port B uses a DTE connector to connect to external devices. This port can be used for synchronous devices such as a MODEM.

Both ports can be polled or interrupt-driven. In a polled operation, for example, the CPU constantly checks the port's status register to see if it has received a data byte. If interrupt-driven, the CPU can be performing other tasks until the port has a character ready for transfer. When it does, the port sends an interrupt request to the CPU. If programmed to do so, the CPU finishes its current instruction and responds to the interrupt request.

TIMER PORT

The timer port contains an 8-bit counter and a 16-bit counter. These are driven by a 250-kHz crystal-controlled clock that is independent of the system clock. The timer circuits allow the CPU to perform other tasks, instead of spending time counting through a loop.

The CPU can load a starting count through the S-100 data out bus and, through software control, check the count through the S-100 data in bus. One application would be to translate the count into time-of-day or the date.

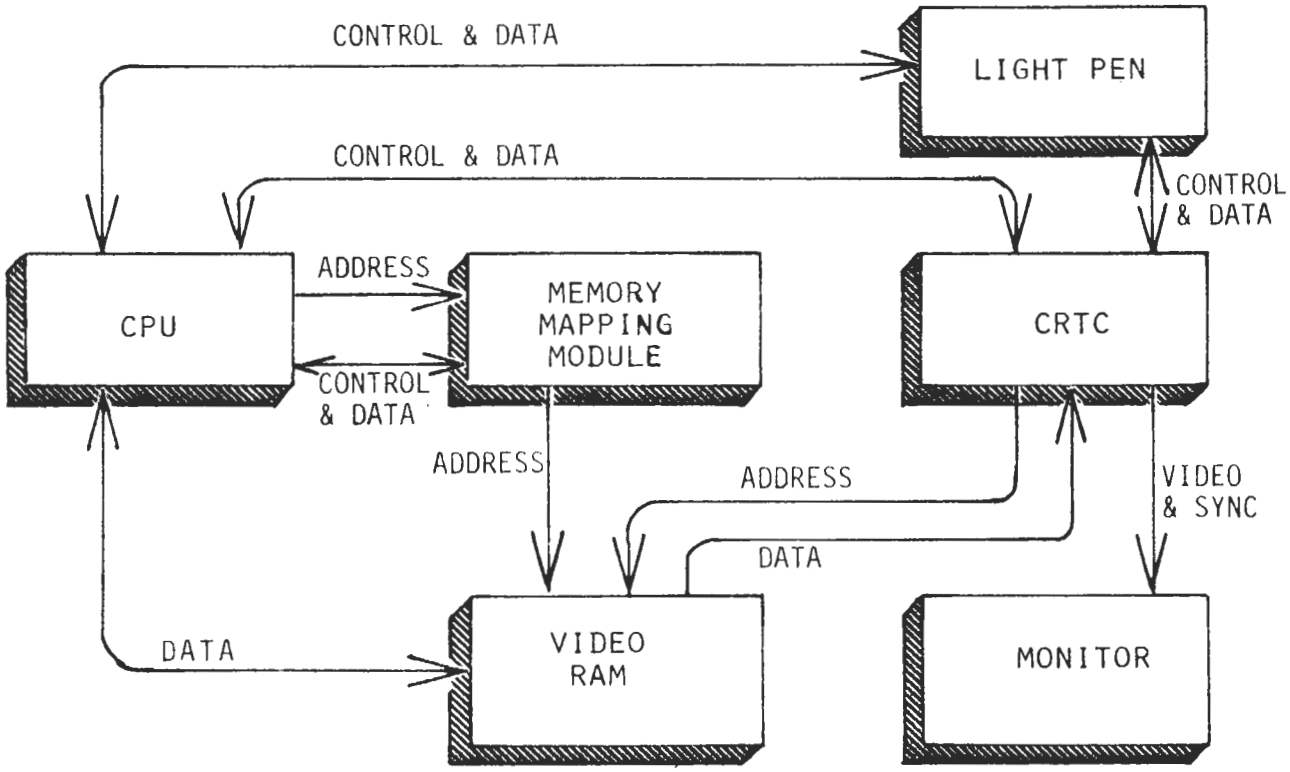
The timer will also generate an interrupt when it counts down from the preloaded number to zero. The CPU can use this for real-time applications such as displaying the total time on line, at one-second intervals, when running a MODEM program.

PARALLEL PORT

The parallel port processes two major I/O circuits: a line printer port and a light pen port. Not shown is an interrupt line from the video board.

The line printer port provides 8-bit parallel data output plus full handshaking. This port allows interfacing to some of the more popular line printers without having to buy a serial-to-parallel converter.

The light pen port permits using a light pen with the H/Z-100. When the light pen is placed near the CRT and detects a pixel, it strobes the CPU and the video board. Circuits on the video board store the location of the detected pixel. The user must supply the software to process this information (such as moving the pixel or drawing a picture).



BASIC VIDEO CIRCUITS

BLOCK DIAGRAM

BASIC VIDEO CIRCUITS

The CPU can access the video circuits as either a port or as a memory location. The CPU accesses the video circuits as a port to program the CRTC, and as a memory location to set up the character font or perform high-density graphics.

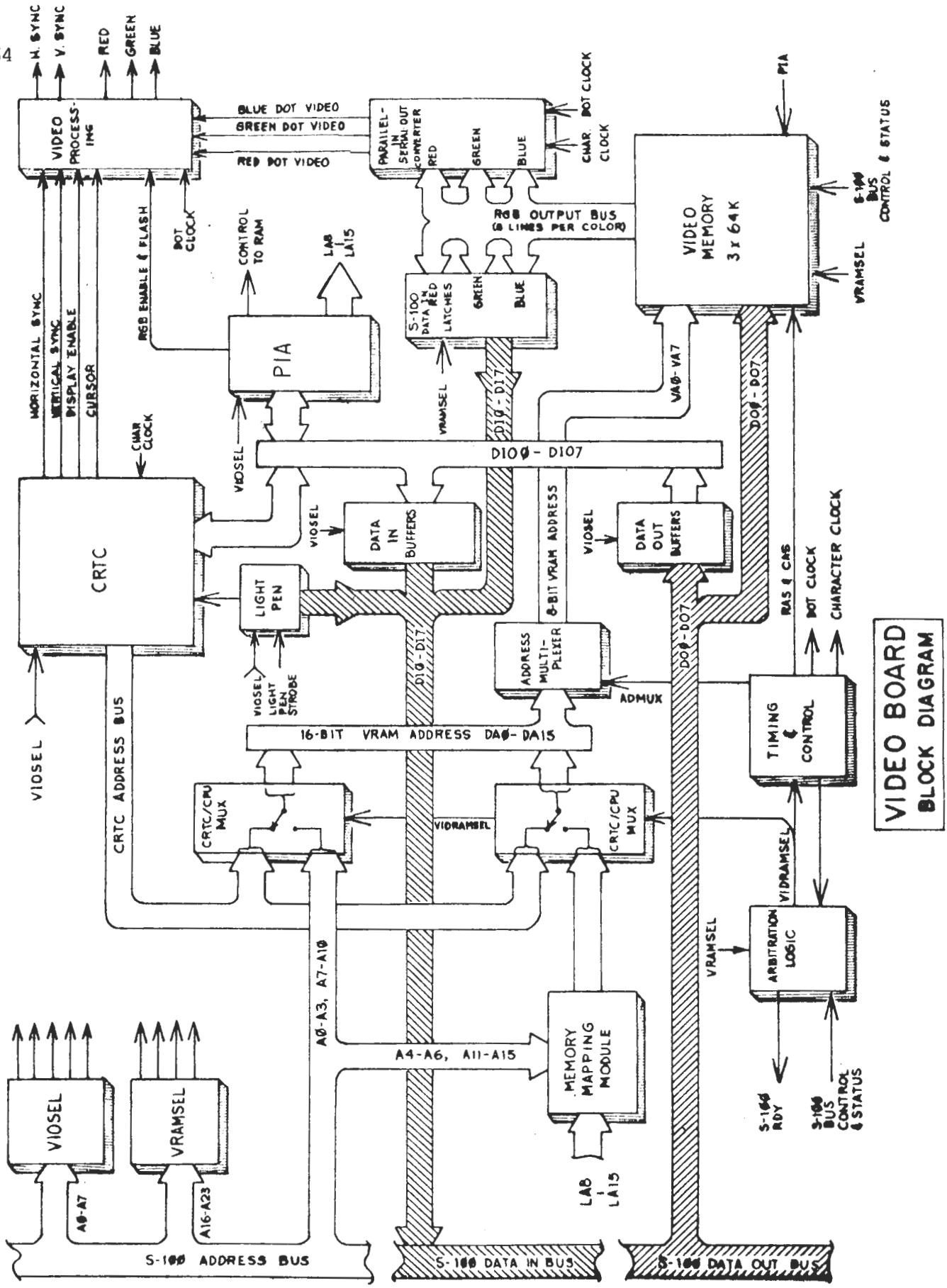
The CPU sends programming information to the CRTC along the control and data signal path. This information includes the number of characters and lines to be displayed, the scan rate, and cursor location.

Once programmed, the CRTC sequentially addresses the video RAM to fetch a character, convert it to serial, and send it to the monitor. The address counter increments, fetches the next character data, and the cycle repeats.

To write or read video memory, the CPU first programs the memory mapping module through the address and the control & data lines. The mapping module is necessary because the CRTC sees the VRAM address starting at zero and going to 64K, while the CPU sees the VRAM address starting at 744K and going to 936K. Once the mapping module is set up, the CPU can, for example, write a byte to 744K and the mapping module will send it to the same location that the CRTC sees as address 0.

The light pen circuits consist of the interface circuits discussed earlier and some counters on the video board. These registers hold the exact location of the pixel pointed to by the light pen.

Because of the complexity of the video board, we will discuss it in more detail.



VIDEO BOARD BLOCK DIAGRAM

VIDEO BOARD

PROGRAMMING THE CRTC

The CPU programs the CRTC by asserting the appropriate VIOSEL line. VIOSEL is a port decoder that selects the right video port by monitoring address lines A0-A7. Programming data couples through the S-100 data out bus, the data out buffers, bus DIO0-DIO7, to the CRTC.

Similarly, the CPU can read certain CRTC registers through the S-100 data in bus and the data in buffers.

CRTC OPERATION

Once programmed, the CRTC sends the video RAM address to the CRTC/CPU address multiplexers. These multiplexers are normally in the address shown; that is, they couple the CRTC address to the 16-bit VRAM address bus, DA0-DA15.

The 16-bit VRAM address bus connects the CRTC address to the address multiplexer. This circuit, under control of the ADMUX line, places the address onto the VRAM address bus, VA0-VA7, 8 bits at a time. At the same time, the timing & control block sends a RAS and CAS signal to the video memory to load each half of the 16-bit address into the row and column latches.

The video RAM is made up of three 32K x 8 banks located 64K apart. These banks can be expanded to 64K; however, this isn't supported at this time. There is one bank for each primary color; red, green, and blue. The minimum configuration for monochrome only has memory in the green bank. Otherwise, all three banks are filled.

The CRTC can only read video RAM, and it addresses all three banks at once. When the address lines are stable, the byte(s) are placed on the RGB output bus. There are 8 bus lines for each color.

The RGB buses connect to the CPU data-in latches, which are disabled, and to the parallel-to-serial converters. This circuit loads the parallel data in at the character clock rate and serially shifts it out at the dot clock rate (dot clock = 8 x character clock). The three serial dot video lines enter the video processing circuits.

At the same time the CRTC is addressing memory, it is also generating horizontal and vertical sync, blanking, and cursor information. These signals are also coupled to the video processing circuits where they are retimed to match the dot video data.

From here, these signals go through buffers to an RGB color monitor for display. Also, there are circuits to combine these pulses into a composite signal for output to a monochrome monitor.

A set of control lines also go to the video processing circuits. These are the RGB enable and flash lines. The RGB enable lines allow selectively turning off a particular color, while the flash line forces the screen to become a solid color. The exact color depends on what primary colors are enabled by the RGB enable line.

These enable lines are controlled by the PIA. In turn, the PIA is controlled by the CPU in the same manner that the CPU programs the CRTC. That is, one of the VIOSEL lines selects the PIA and the CPU reads or writes data through the DIO0-DIO7 bus.

ACCESSING THE VRAM WITH THE CPU

When the CPU reads or writes video RAM, it asserts the lines from the VRAMSEL block. This block activates the appropriate gates and enables the desired color bank in memory. VRAMSEL does this by monitoring address lines A16-A23, which ensures that the address will always be an even 64-kilobyte boundary between 744K and 936K.

The CPU first programs lines LA8-LA15 of the PIA for a specific mapping pattern. The mapping pattern is fed to the memory mapping module where it is compared to address lines A4-A6 and A11-A15. The memory mapping module connects to one of the CRTC/CPU multiplexers. Address lines A0-A3 and A7-A10 connect directly to the other multiplexer.

When the CPU attempts to read or write memory, one of the VRAMSEL lines sends a request to the arbitration logic. The CRTC has top priority, so if the CRTC is accessing memory, the arbitration logic puts the CPU into a wait state by bringing S-100 RDY low.

When the CRTC is done, the arbitration logic activates VIDRAMSEL to switch the CRTC/CPU multiplexers to the CPU position. The mapped address couples through the address multiplexer to the RAM in the same manner as described for the CRTC.

If the CPU is writing data, it couples the data through DO0-DO7 to the memory circuits. It selects the correct bank with VRAMSEL. If reading data, the addressed byte(s) are placed on the RGB output bus and the CPU selects one of the three groups of CPU latches. The VRAM data couples to DI0-DI7 of the S-100 data in bus.

TIMING AND CONTROL

The ADMUX, RAS, and CAS timing was previously explained. The timing and control circuits also provide dot clock and character clock timing. The dot clock, at 14.112 MHz, is the basic timing frequency for the video board.

The timing circuits also provide a control signal to the arbitration logic. The video circuits are designed to let the CRTC have control of the video board for two RAS cycles, and let the CPU have control for the third cycle. The line from the timing block to the arbitration block tells the arbitration block when it can give the CPU control of the video circuits.

If the CPU isn't requesting control at this time, then nothing happens until the next RAS cycle, at which time the CRTC again has control of the board.

If the CPU is requesting control of the video board, indicated by VRAMSEL and signals on the S-100 bus control and status lines, the CPU will get control of the video board as described previously.

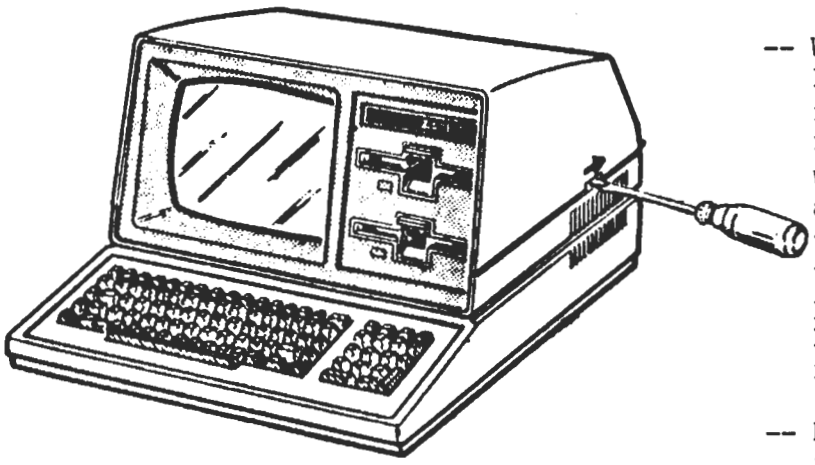
DISASSEMBLY

Since there are two models of the H/Z-100, the All-In-One and the Low Profile, a separate disassembly procedure for each model is contained within this section. On the following pages, you will find the procedure for the model you are servicing. Read through the procedure, so you'll know what to expect when you start disassembling the computer.

Each procedure contains instructions on how to completely disassemble each model of the H/Z-100. In most cases you will not have to completely disassemble the computer to reach the area in which you need to service. Therefore, follow the instructions in order until you reach the area you wish to access. When you are finished servicing the particular circuit board or assembly, reverse the procedure to reassemble the computer.

ALL-IN-ONE COMPUTER

CABINET TOP REMOVAL



-- With a flat-blade screwdriver, slide the latch bracket to the center of the slot in the cabinet top. The latch bracket is spring loaded, so you will have to work with one side of the cabinet top at a time. While holding the latch in the center position, lift that side of the cabinet top. After one side is freed, perform the procedure on the other side. Be sure to hold the freed side up, so it will not snap back down.

-- Remove the cabinet top and set it aside in a safe place.

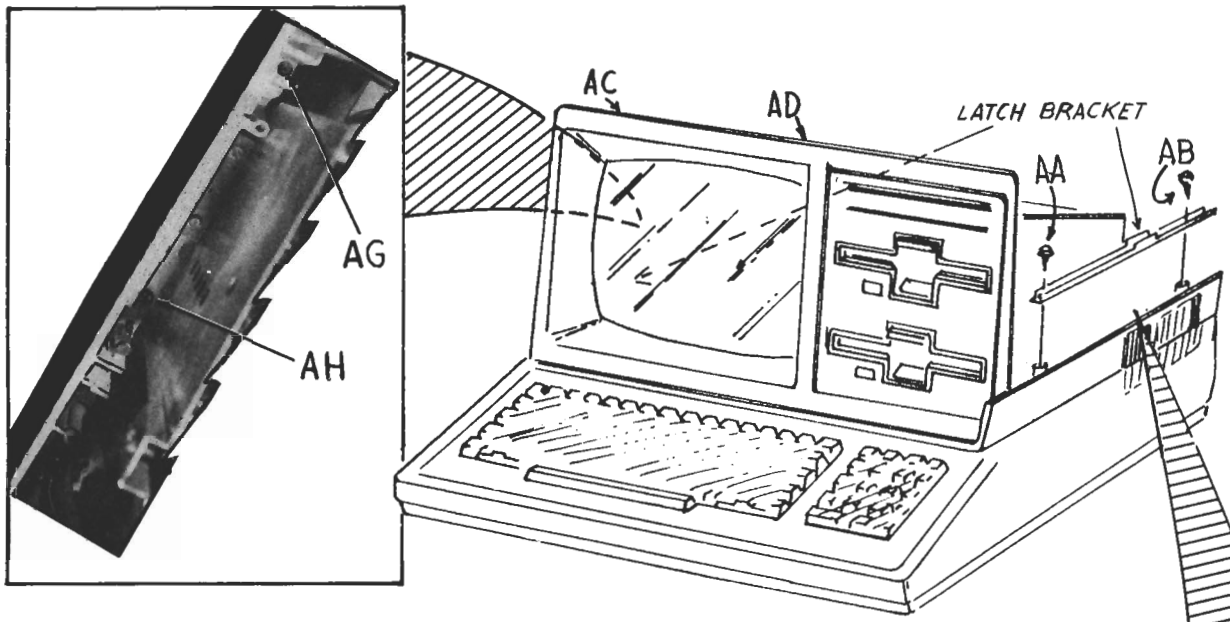
At this point, access to the drives, sweep board, and accessory boards may be obtained without any further disassembly.

CRT/DISK DRIVE REMOVAL (VIDEO MONITOR)

-- Remove the 6-32 x 3/8" screws at AA, AB, AC, and AD that hold the two latch brackets in place.

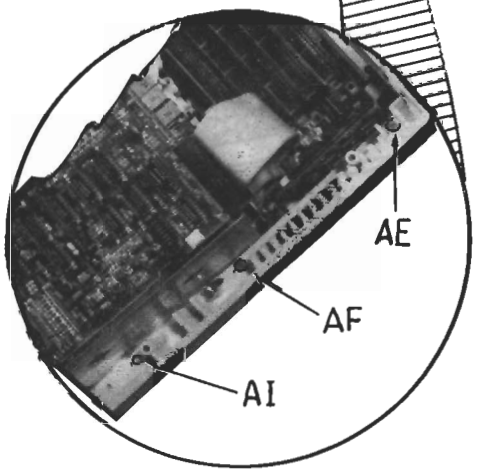
-- Carefully disconnect the spring holding each latch bracket to the cabinet base.

-- Remove the latch brackets.

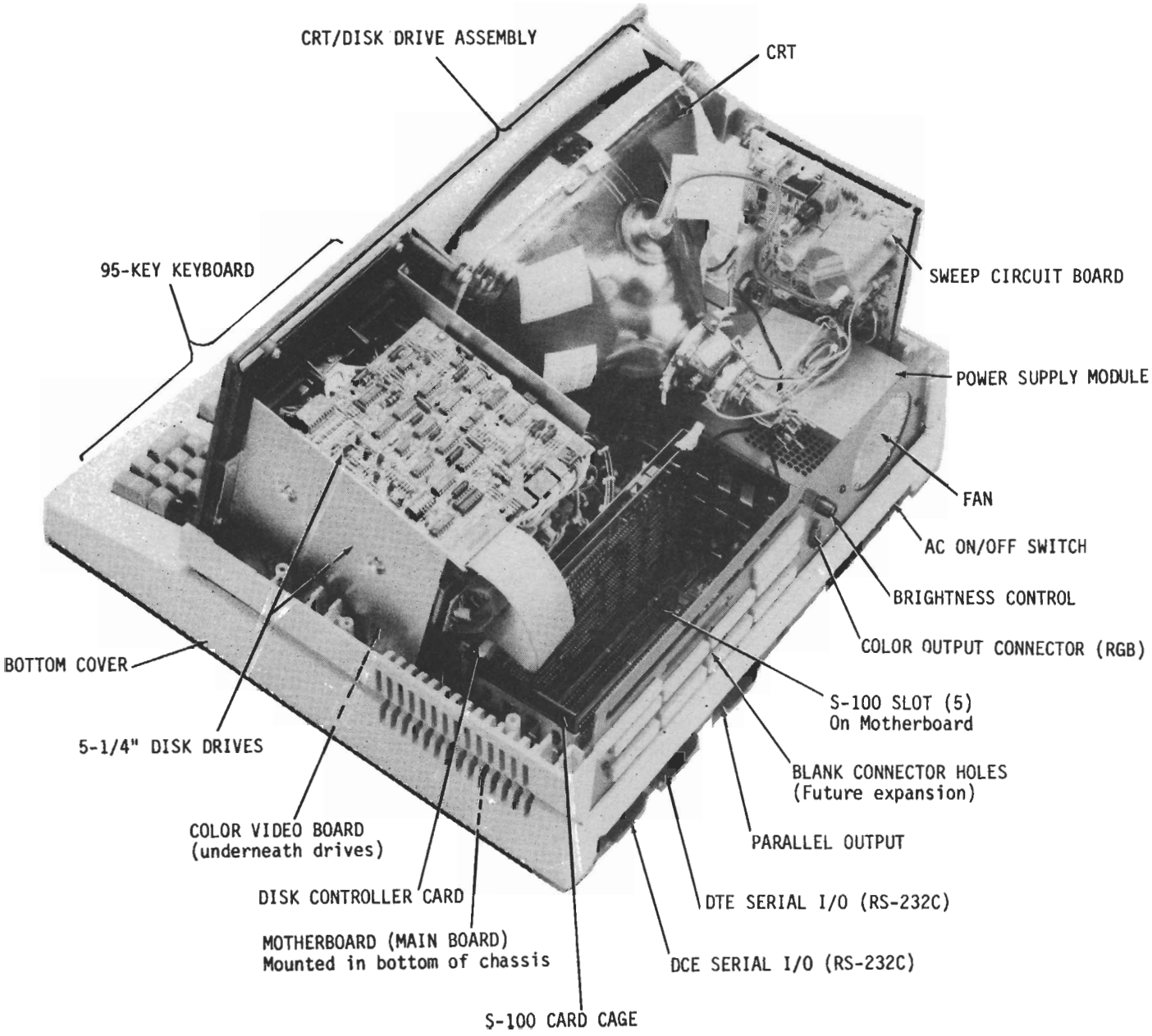


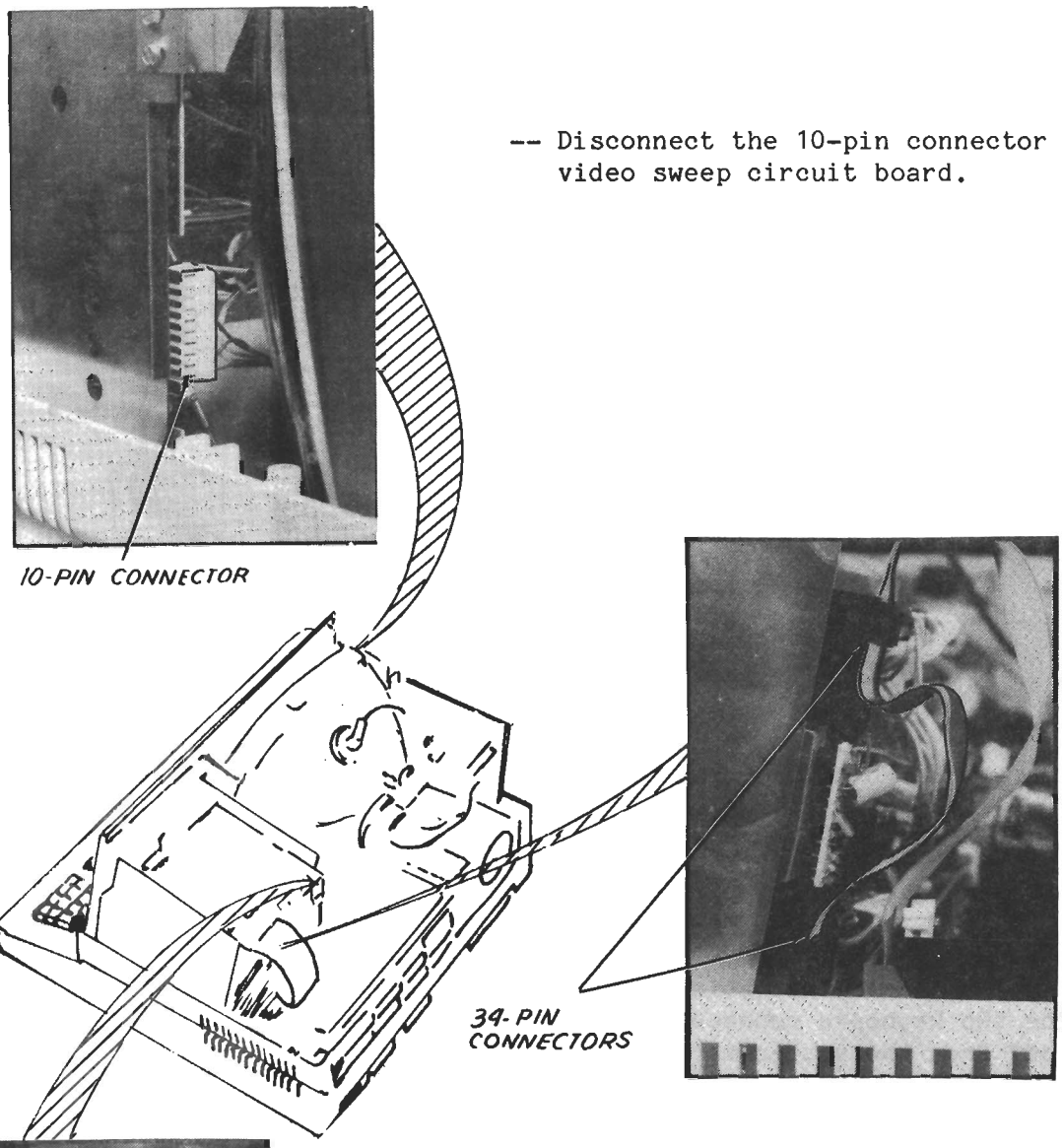
-- Remove the four 6-32 x 1-3/4" screws at AE, AF, AG, and AH.

-- Remove the #8 x 1-1/2" screw at AI.



VIEW OF ALL-IN-ONE COMPUTER





-- Disconnect the 10-pin connector from the video sweep circuit board.

-- Disconnect the 34-pin ribbon cable connector from each disk drive unit.

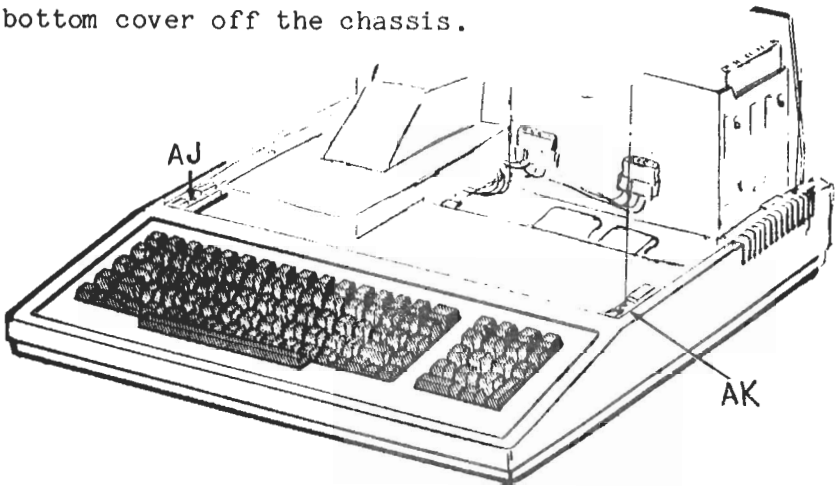
-- Disconnect the 4-pin power supply connector from each disk drive unit.

-- Lift the CRT/disk drive assembly off the lower portion of the cabinet and set this assembly aside.

BOTTOM COVER REMOVAL

-- Remove the two #8 x 5/8" screws at AJ and AK.

-- Lift the bottom cover off the chassis.

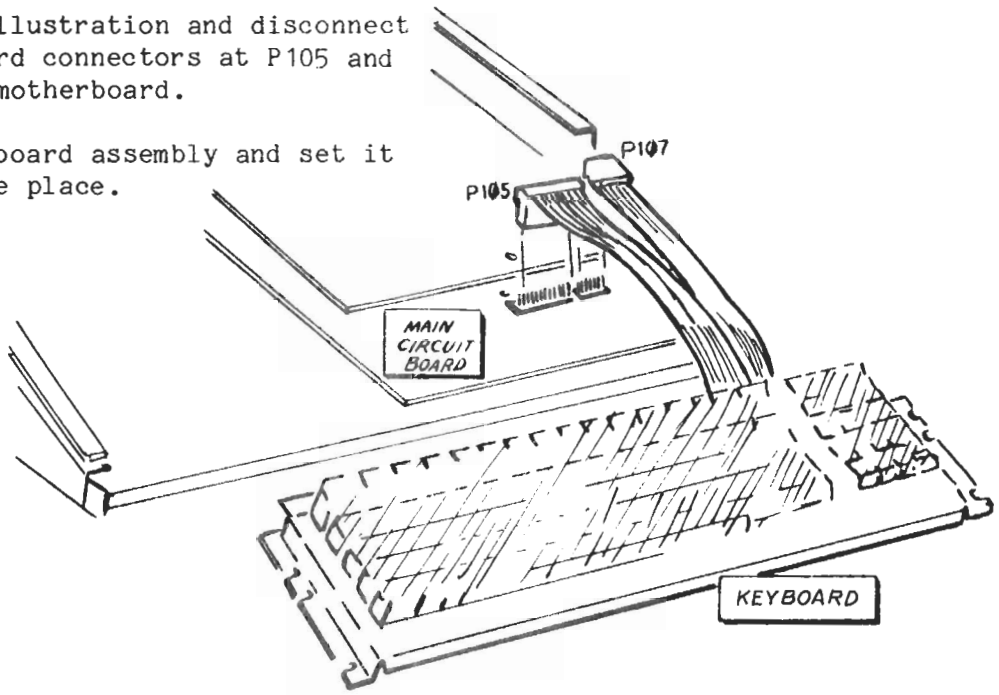


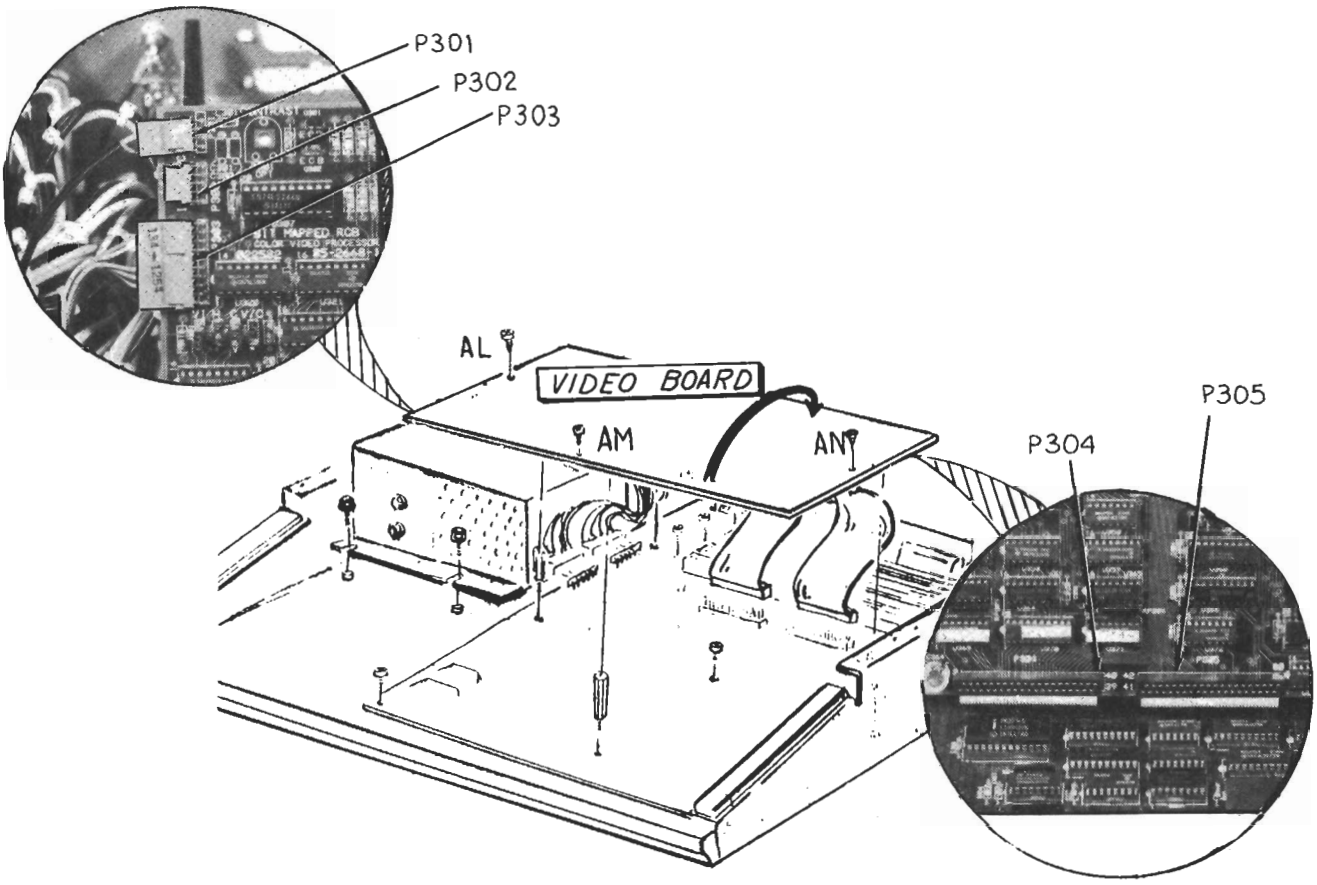
KEYBOARD REMOVAL

-- Place the keyboard in front of the chassis.

-- Refer to the illustration and disconnect the two keyboard connectors at P105 and P107 from the motherboard.

-- Remove the keyboard assembly and set it aside in a safe place.





VIDEO BOARD REMOVAL

-- Remove the three 4-40 x 1/4" phillips screws at AL, AM, and AN on the video board.

-- Carefully lift the video board by the front edge to a vertical position.

-- Disconnect the three cable connectors at P301, P302, and P303.

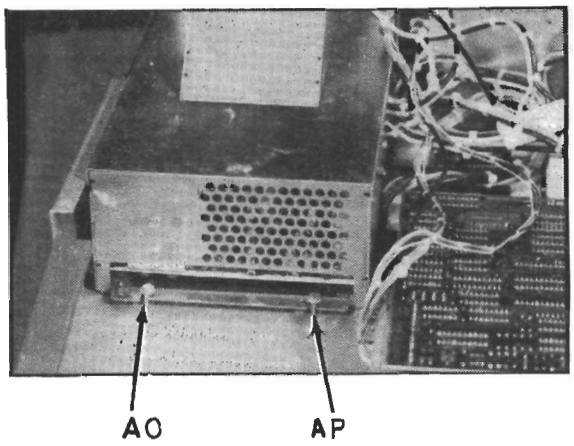
-- Disconnect the two 40-pin cable connectors at P304 and P305 on the video board.

-- Carefully lift the video board from the chassis.

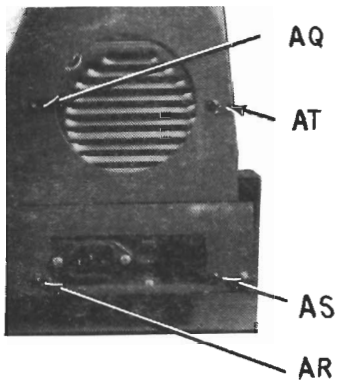
Depending on your servicing needs, the power supply and/or the motherboard may be removed from the chassis. Find the appropriate procedure and follow the instructions.

POWER SUPPLY REMOVAL

-- Remove the two 6-32 x 3/8" hex-head screws from the front of the power supply at AO and AP.



-- Remove the four #6 x 1/4" screws at AQ, AR, AS and AT that secure the power supply to the back panel.



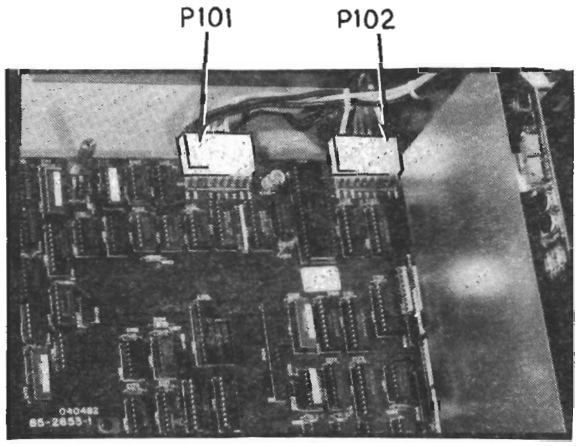
-- Lift the power supply until you are able to disconnect the two power supply connectors P101 and P102 from the motherboard.

-- Remove the knob on the brightness control by pulling it straight off the control shaft.

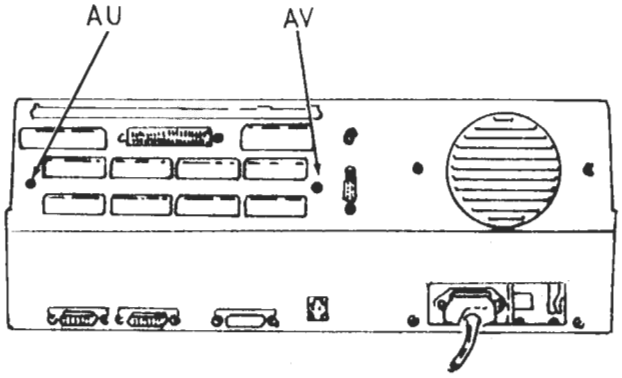
-- Remove the control nut from the brightness control.

-- Find the large toothed washer on the brightness control and set it aside in a safe place.

-- Carefully remove the power supply from the chassis.

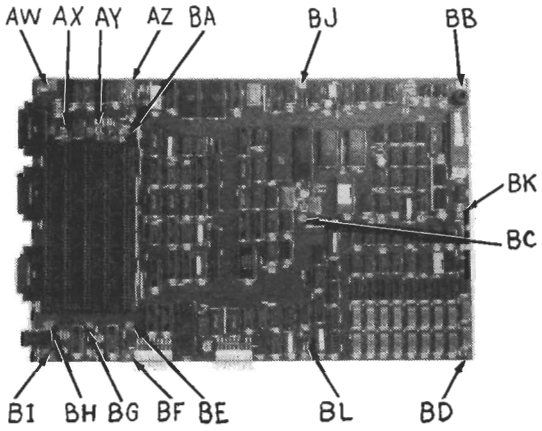


MOTHERBOARD REMOVAL



-- Remove any accessory boards from the S-100 card cage.

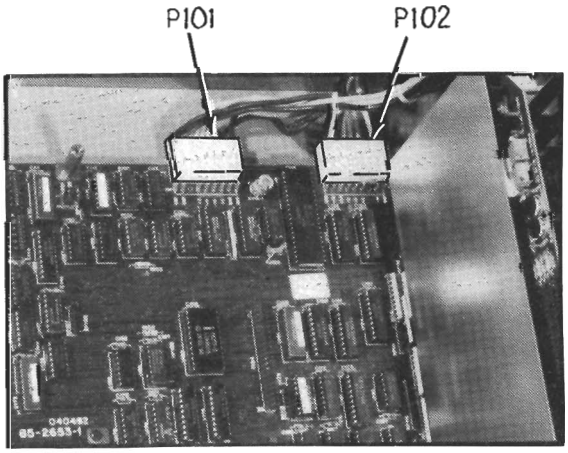
-- Remove the two #6 x 1/4" screws at AU and AV that secure the card cage to the back panel.



-- With a phillips screwdriver, remove the thirteen 4-40 x 1/4" screws at AW through BI from the motherboard.

-- Lift the card cage from the motherboard.

-- Remove the three 4-40 x 1" hex spacers at BJ, BK, and BL from the motherboard.



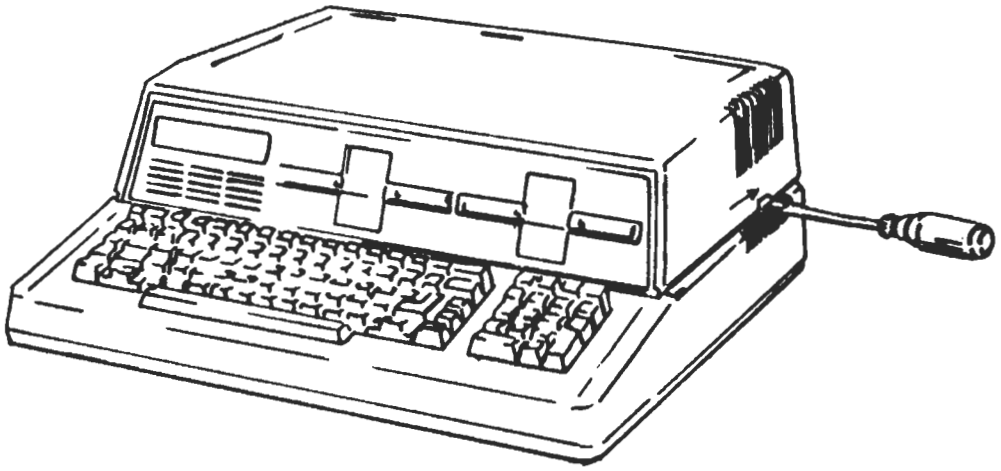
-- Lift the motherboard until you are able to disconnect the two power supply connectors P101 and P102 from the motherboard.

-- Carefully lift the motherboard from the chassis.

This completes the disassembly of the All-In-One Computer. Reverse the procedure to reassemble the computer. Be careful not to pinch any wires.

LOW-PROFILE COMPUTER

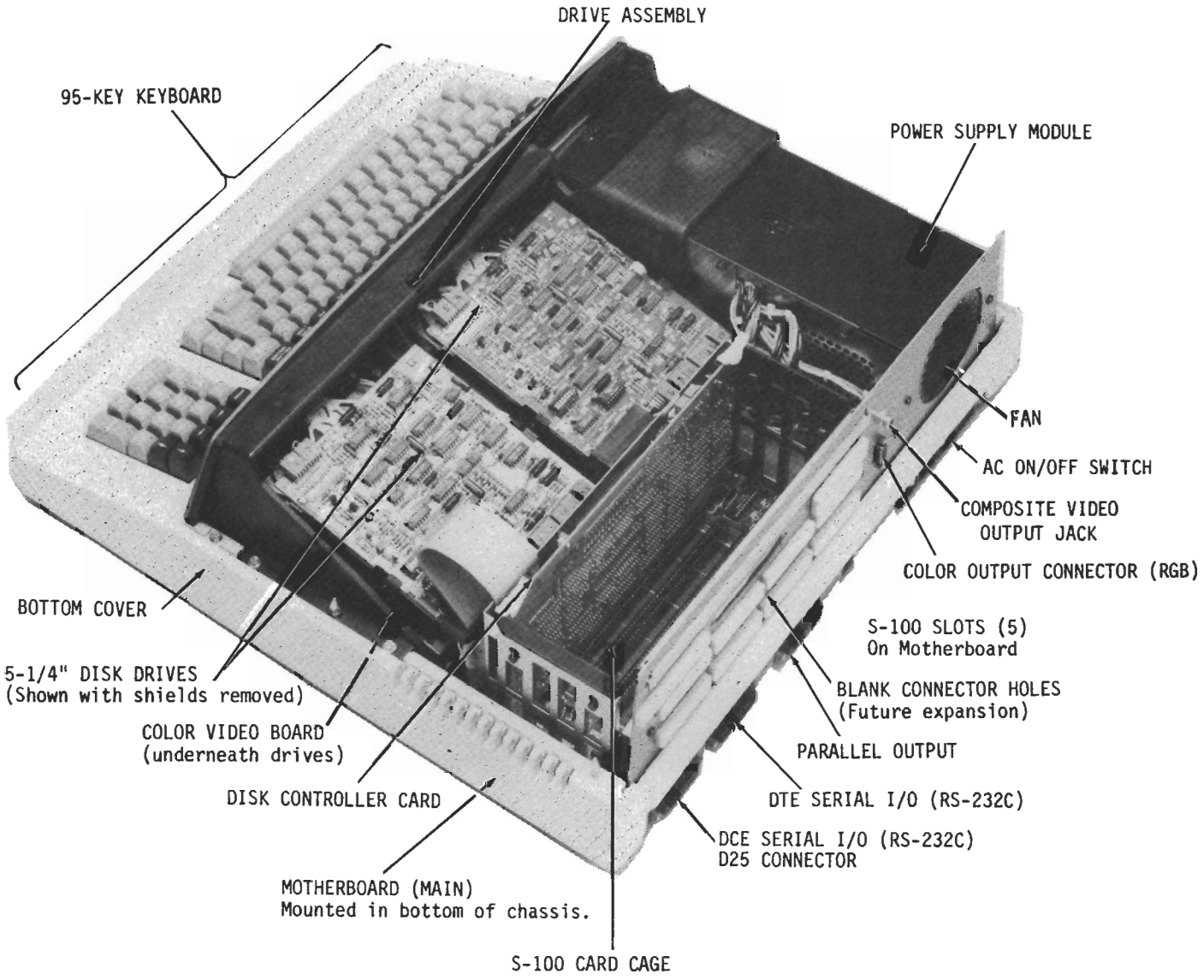
CABINET TOP REMOVAL



-- With a flat-blade screwdriver, slide the latch bracket to the center of the slot in the cabinet top. The latch is spring loaded, so you will have to work with one side of the cabinet top at a time. While holding the latch in the center position, lift that side of the cabinet top. After one side is freed, perform the procedure on the other side. Be sure to hold the freed side up, so it will not snap back down.

-- Remove the cabinet top and set it aside in a safe place.

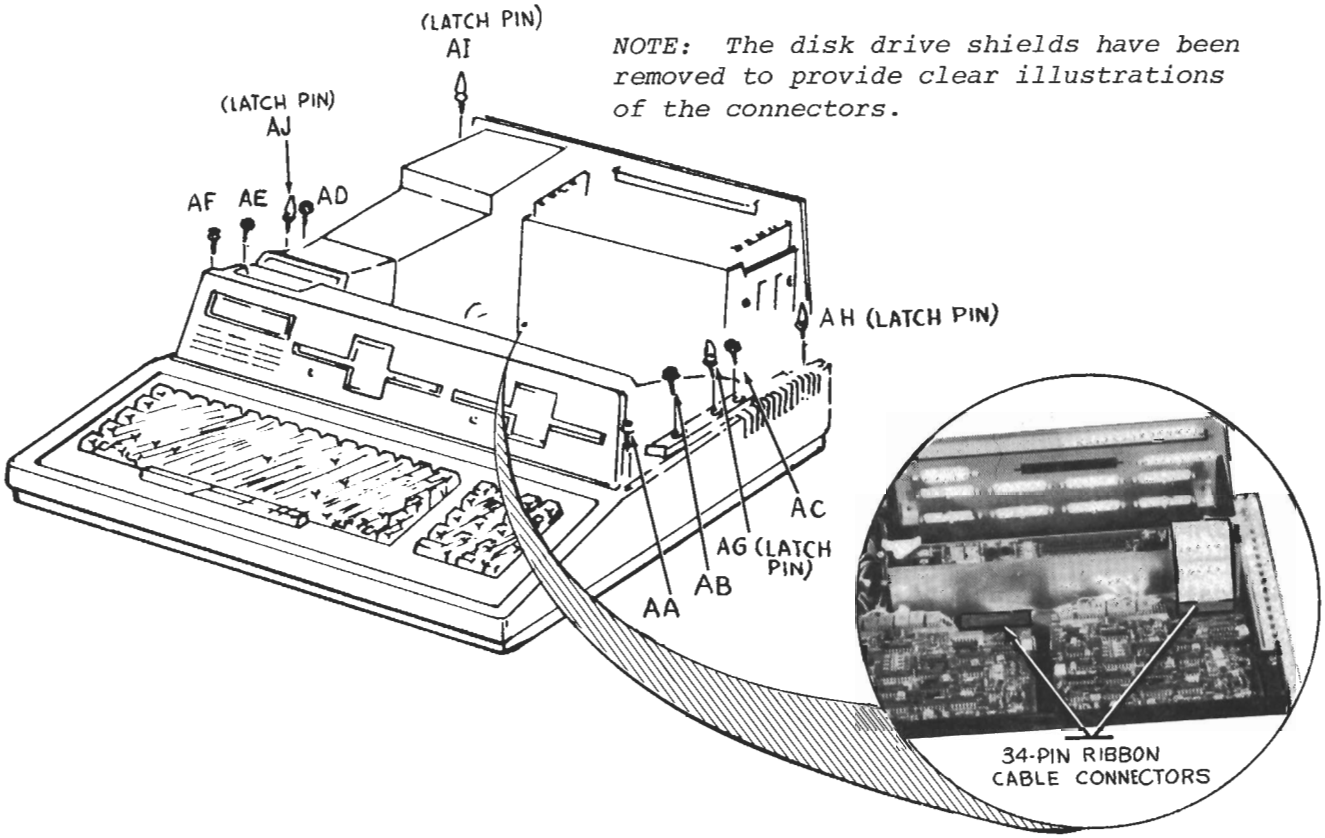
At this point, access to the accessory boards may be obtained without further disassembly.

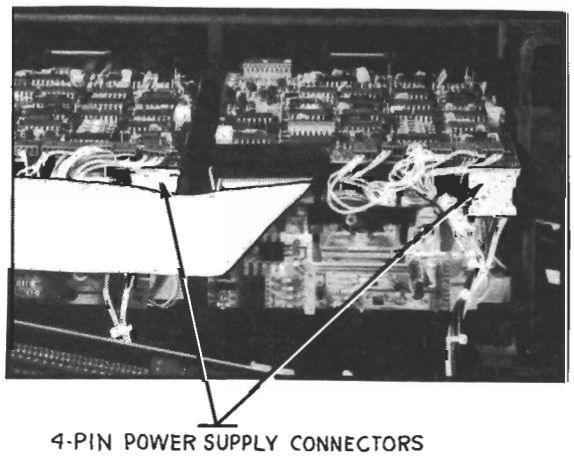


VIEW OF LOW-PROFILE COMPUTER

DISK DRIVE ASSEMBLY/ BOTTOM COVER REMOVAL

NOTE: The disk drive shields have been removed to provide clear illustrations of the connectors.





-- Remove the six #8 x 3/4" screws at AA, AB, AC, AD, AE, and AF.

-- Remove the four latch pins at AG, AH, AI, and AJ.

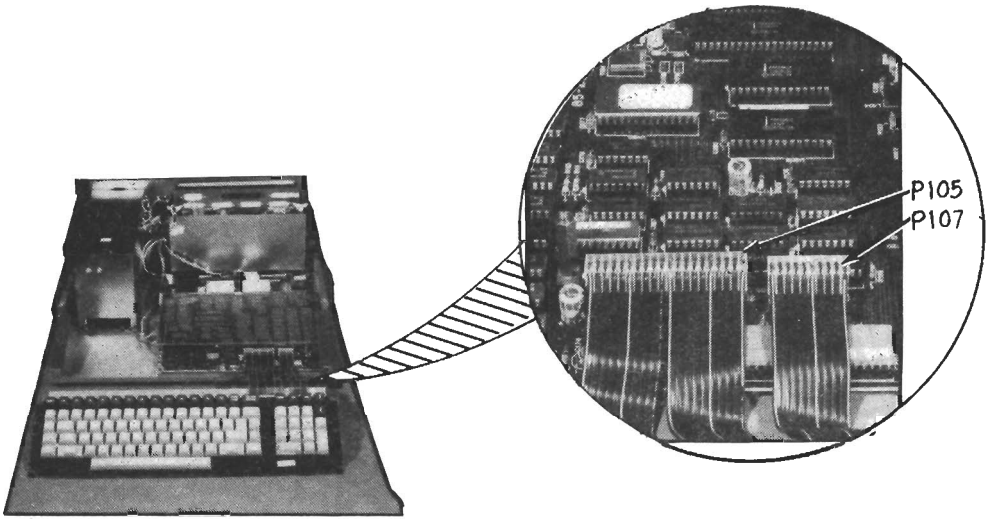
-- Disconnect the 34-pin ribbon cable connectors from the disk drive units.

-- Disconnect the 4-pin power supply connectors from the disk drive units.

-- Lift the disk drive assembly off the lower portion of the cabinet.

-- Lift the bottom cover off the chassis.

To further disassemble the disk drive assembly, refer to the Disasembly section of "Disk Controller and Drives."

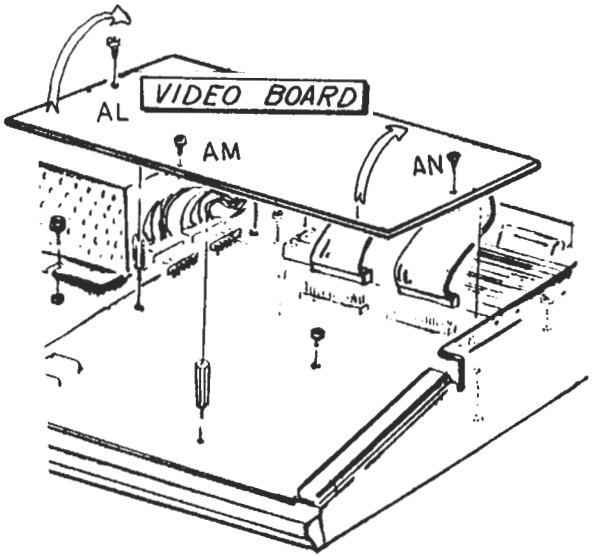


KEYBOARD REMOVAL

-- Position the keyboard in front of the chassis as shown in the illustration.

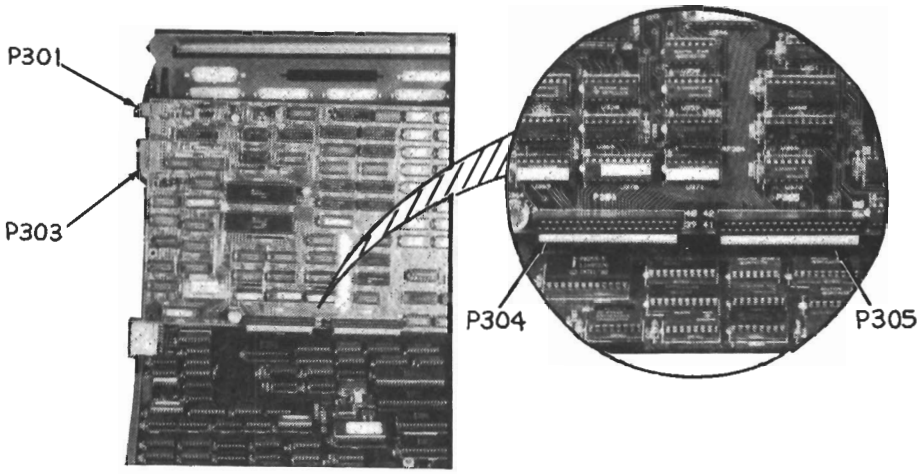
-- Refer to the inset, and disconnect the two keyboard connectors at P105 and P107 from the motherboard.

-- Remove the keyboard assembly and set it aside in a safe place.



VIDEO BOARD REMOVAL

-- Remove the three 4-40 x 1/4" phillips screws at AL, AM, and AN from the video board.



-- Carefully lift the front edge of the video board so the board is in a vertical position.

-- Disconnect the two cable assemblies at P301 and P303.

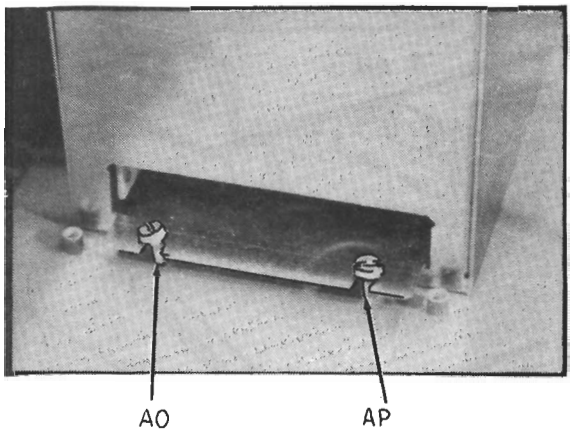
-- Disconnect the two 40-pin cable connectors at P304 and P305 on the video board.

-- Carefully lift the video board from the chassis.

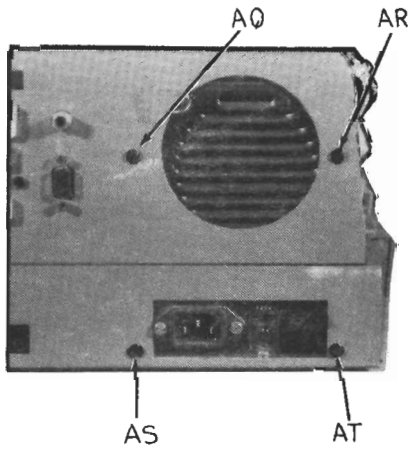
Depending on your servicing needs, the power supply and/or the motherboard may be removed from the chassis. Find the appropriate procedure and follow the instructions.

POWER SUPPLY REMOVAL

-- Remove the two 6-32 x 3/8" hex-head screws at AO and AP from the front of the power supply.

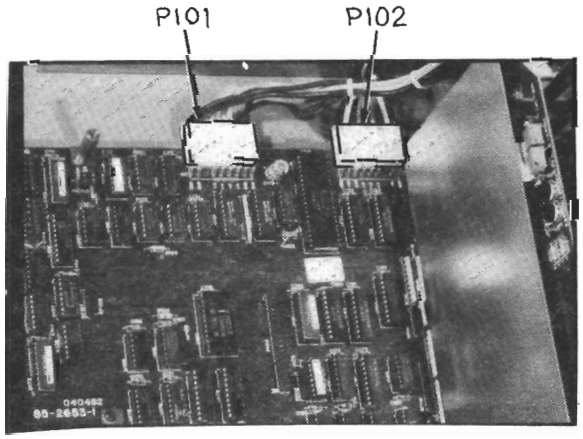


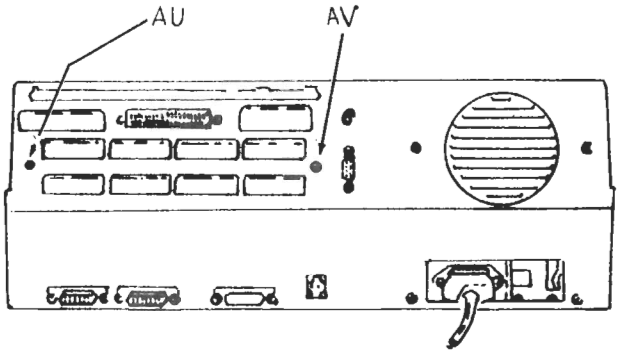
-- Remove the four #6 x 1/4" screws at AQ, AR, AS, and AT that secure the power supply to the back panel.



-- Lift the power supply until you are able to disconnect the two power supply connectors P101 and P102 from the motherboard.

-- Carefully remove the power supply from the chassis.

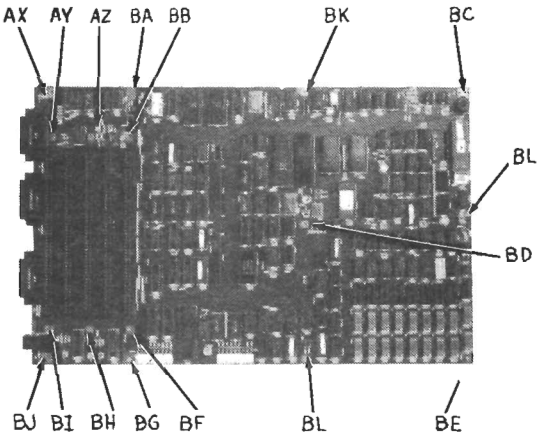




MOTHERBOARD REMOVAL

-- Remove any accessory from the S-100 card cage.

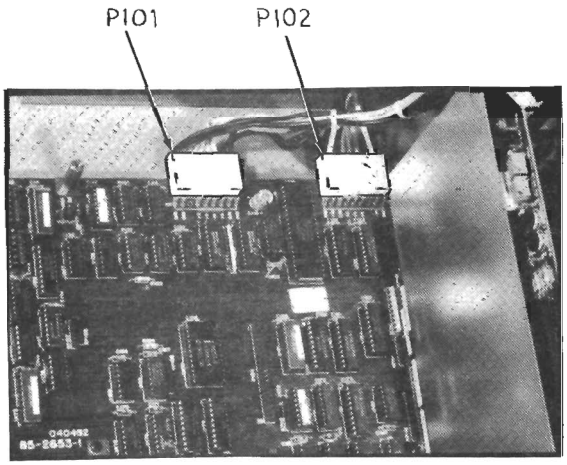
-- Remove the two #6 x 1/4" screws at AU and AV that secure the card cage to the back panel.



-- With a phillips screwdriver, remove the thirteen 4-40 x 1/4" screws at AX through BJ from the motherboard.

-- Lift the card cage from the motherboard.

-- Remove the three 4-40 x 1" hex spacers at BK, BL, and BM from the motherboard.

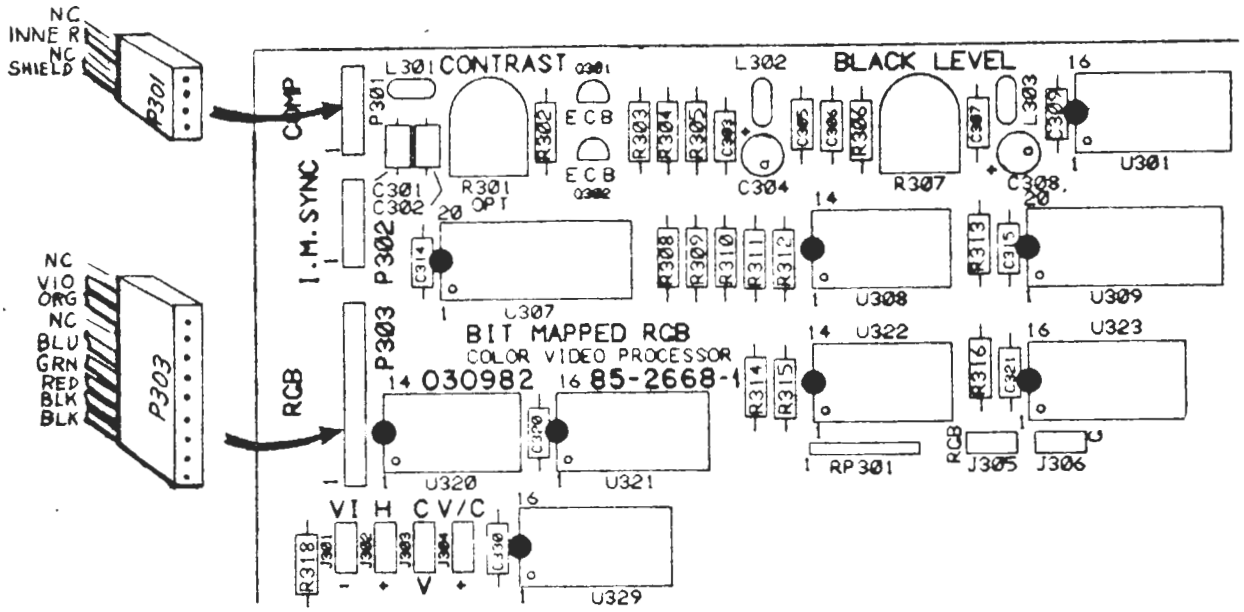


-- Lift the motherboard until you are able to disconnect the two power supply connectors P101 and P102 from the motherboard.

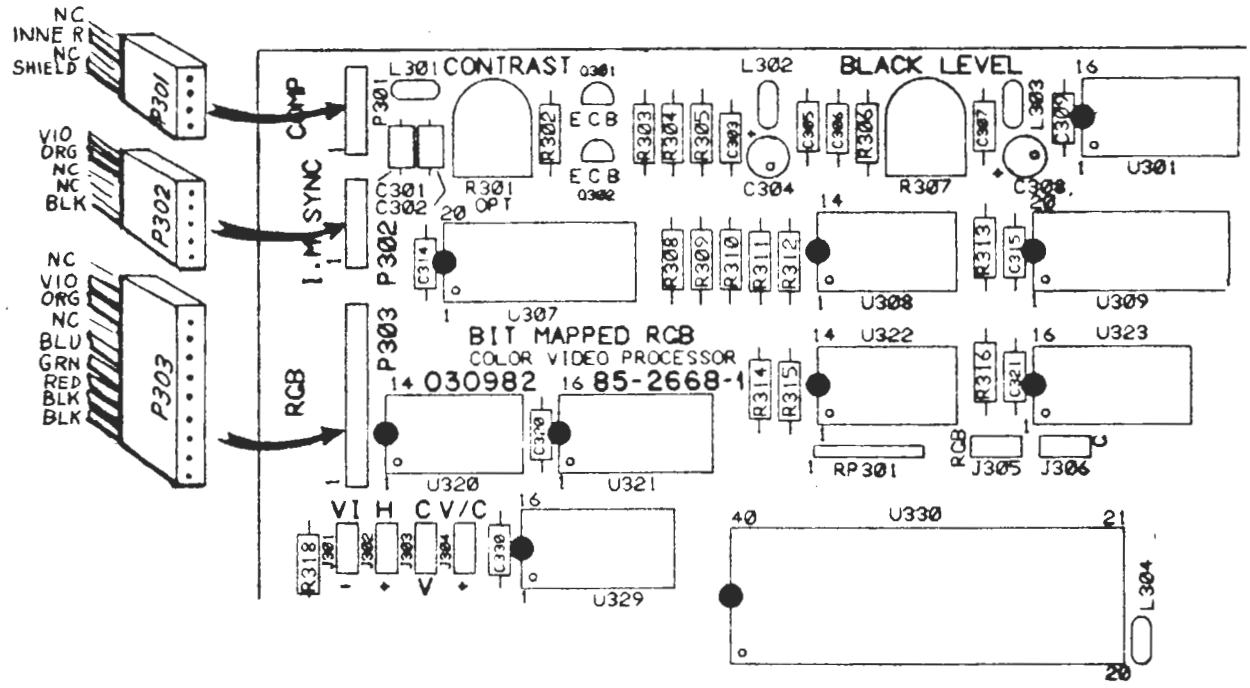
-- Carefully lift the motherboard from the chassis.

This completes the disassembly of the Low Profile Computer. Reverse the procedure to reassemble the computer. Be careful not to pinch any wires.

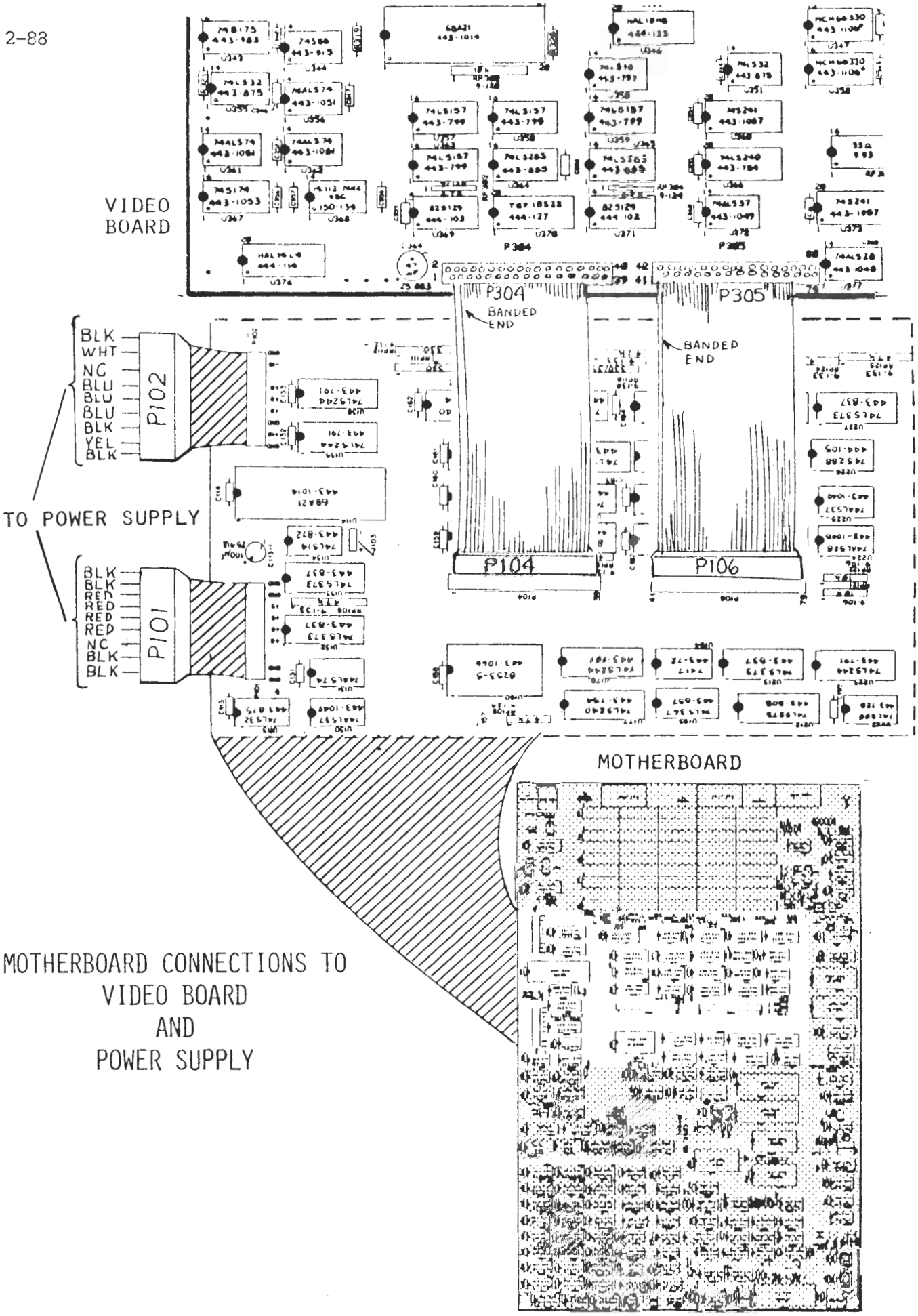
VISUAL CHECKS



LOW-PROFILE VIDEO BOARD CONNECTIONS

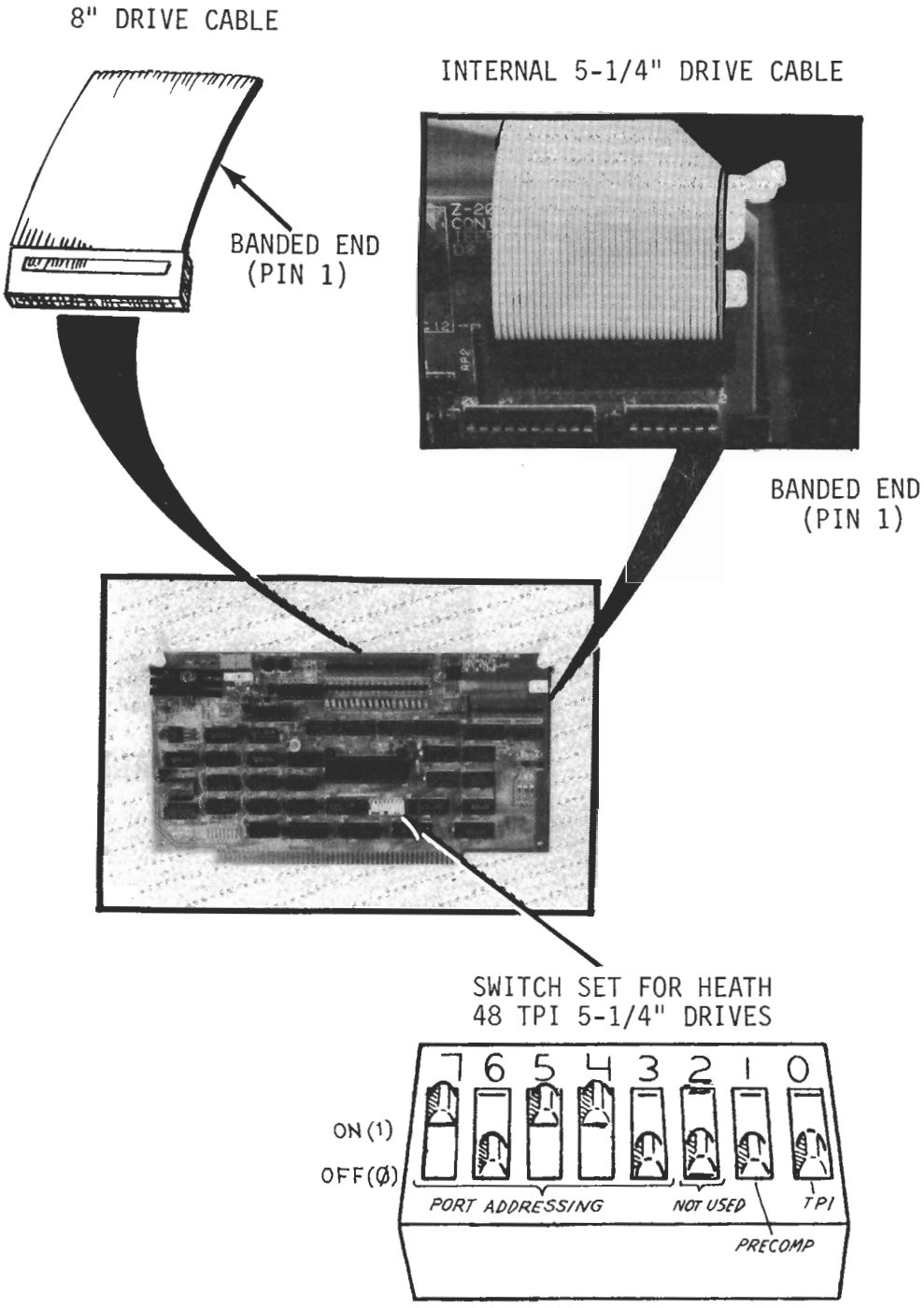


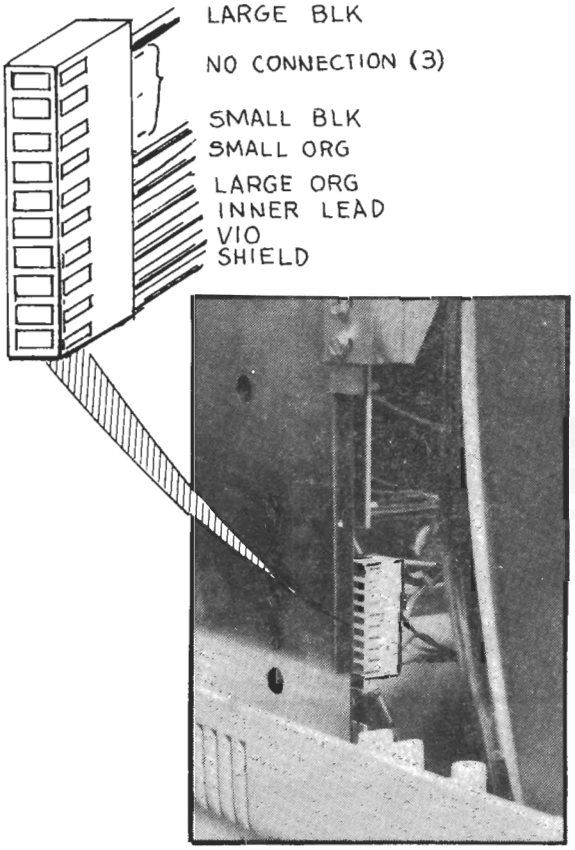
ALL-IN-ONE VIDEO BOARD CONNECTIONS



MOTHERBOARD CONNECTIONS TO VIDEO BOARD AND POWER SUPPLY

DISK CONTROLLER BOARD CABLE CONNECTIONS AND SWITCH POSITIONS



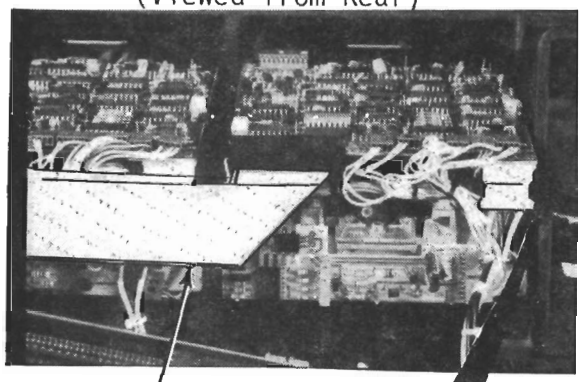


ALL-IN-ONE SWEEP BOARD CONNECTIONS

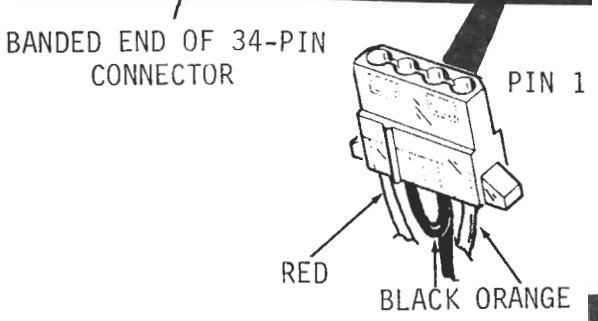
DISK CONTROLLER BOARD
5-1/4" DISK DRIVE CONNECTIONS

LOW PROFILE COMPUTER (SHOWN WITH DRIVE SHIELDS REMOVED)

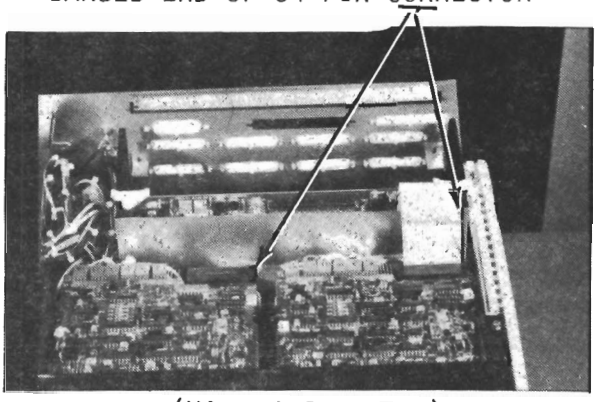
(Viewed from Rear)



BANDED END OF 34-PIN CONNECTOR



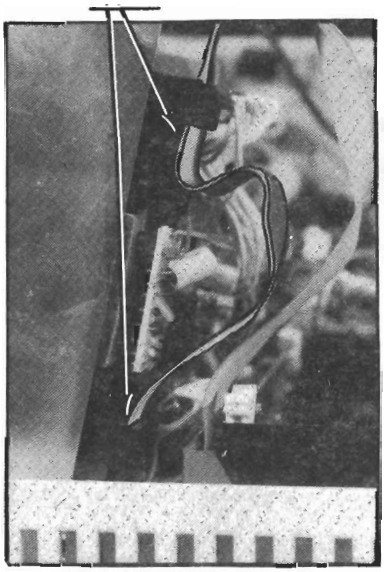
BANDED END OF 34-PIN CONNECTOR



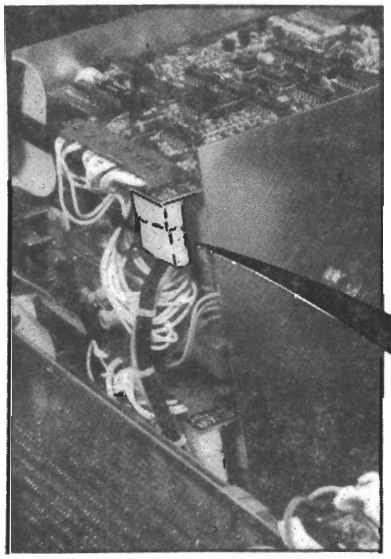
(Viewed from Top)

ALL-IN-ONE COMPUTER

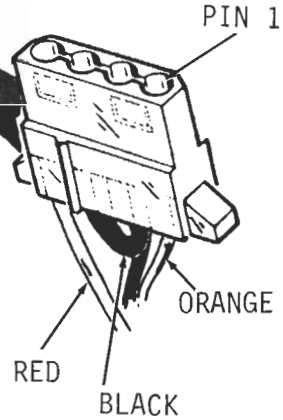
BANDED END OF 34-PIN CONNECTOR



(Viewed from Right Side)



(Viewed from Left Top)



TROUBLESHOOTING

INTRODUCTION

GENERAL

These troubleshooting procedures provide guidelines on what modules and components to check when troubleshooting a particular problem. Due to the complexity of the H/Z-100, however, these tests will not always lead you to the exact component causing the problem.

To service to the component level, you must be familiar with the H/Z-100 circuitry. Study the Circuit Descriptions, IC Data Sheets of the more complex ICs, Operation, and Specifications sections of this Manual. But, once you understand how the computer works, you will be able to quickly repair the unit and have fewer tough-dogs to contend with.

TROUBLESHOOTING PROCEDURE

This section, System Troubleshooting, will help you narrow the problem down to a board/module level. What you do next depends on whether you're servicing to the module level or to the component level.

If you're doing module-level repair, replace the defective board and proceed to Final Checks in this section.

If you're repairing the unit to the component level, perform the procedure outlined in this section to narrow the problem down to a board or module. Once you've determined which module is defective, go to the appropriate section in this manual (such as the Motherboard or Video Board) for detailed troubleshooting information.

When you've repaired the problem, return to this section and perform the final checks.

DIAGNOSTICS

The diagnostic programs make it easier to service the H/Z-100. These routines will show which circuit is bad and, in some cases, will locate the component causing the failure. Some of the diagnostic programs will continually exercise a suspected defective circuit, allowing you to test the circuit with a logic probe or oscilloscope. See the Diagnostics section of this Manual for the available programs and operating instructions.

From time to time, new diagnostic programs will be added to this Manual. Depending on what the program is for, it will be supplied as a printed source listing, or on a disk, or in ROM.

EQUIPMENT NEEDED

To troubleshoot the H/Z-100, you need the following test equipment. The test equipment specifications should meet or exceed those listed after the underlined item. The suggested model numbers, at the end of each item, will fulfill these recommendations.

Oscilloscope DC to 20-MHz, dual trace, triggered sweep. Heath SO-3220, or equivalent. Note: This oscilloscope is suitable for most of your troubleshooting needs. However, for critical pulse measurements, use a 35-MHz, delayed-sweep oscilloscope such as the Heath SO-4235.

Logic Probe DC to 20-MHz, capable of detecting 10-nS single pulses. Indicates logic one, logic zero, and high-impedance states. Heath IT-7410, Hewlett-Packard HP-545A, or equivalent.

DVM High-impedance input. 0-1000 volts, 0-1 megohm. Heath SM-2215 DVM or equivalent.

Voltage-Variable AC Power Supply Zero to 120 Vac RMS, 3 amperes. Heath SP-5220 or equivalent.

Variable DC Power Supply Voltage adjustable to 1 volt, current-limiting adjustable to 100 mA. Heath IP-2728 or equivalent.

Low-Capacitance Oscilloscope Probe Input capacitance adjustable between 15-50 pF, 4-nS rise time. Heath PKW-105 or equivalent.

High-Voltage Probe Capable of measuring up to 40 kV in color video monitors. Heath IM-5210 or equivalent.

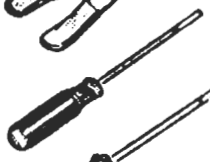
Video Monitor RGB wide-band color monitor. Nippon Electric Co. JC-1202DH or equivalent. If a color monitor is not available, use a wide-band (15 MHz) monochrome monitor. Zenith ZVM-121 or equivalent.

USEFUL TOOLS

Long-Nose Pliers

Diagonal Cutters

Wire Strippers



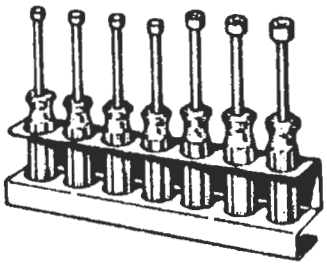
1/8" Blade Screwdriver

1/4" Blade Screwdriver

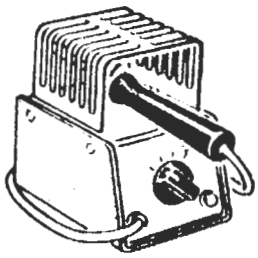
Phillips Screwdriver

Desoldering Bulb

Desoldering Braid
(#HE490-185)



Nut Drivers

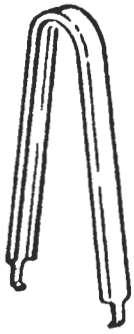


Soldering Iron
(Model GH-17A)

1/4" & 5/16" Open-End Wrench
(#HE490-168)

Nut Starter
(#HE490-5)

IC Puller
(#HE490-111)



IC Puller
(#HE490-189)

INITIAL SETUP

INTRODUCTION

The H/Z-100 is easy to disassemble; even an all-in-one unit requires only about 15 minutes to remove the motherboard.

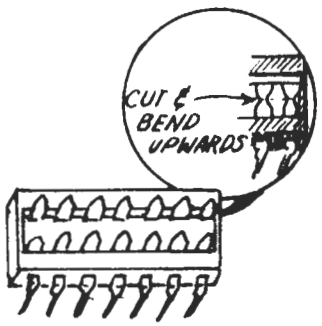
However, due to the way the unit is packaged, there are very few test points that you can reach while the unit is assembled and operating. To get around this, you should build the following extender cables.

These extender cables allow you to spread out the H/Z-100 over a 29" x 46" surface. This permits you to easily reach every IC while the unit is operating.

PARTS REQUIRED

Qty.	Description	Part No.
2	40-pin ribbon cable w/connectors	HE 134-1108
1	34-pin ribbon cable w/connectors	HE 134-1025
4	Small alligator clips for jumper wire construction	HE 260-16
20 ft.	#18 stranded wire	HE 344-155
20	Large spring connector	HE 432-753
1	10-pin adapter plug	HE 432-788
2	10-hole socket shell	HE 432-1061
1	Programming plug	HE 969-18

PROGRAMMING PLUG CONSTRUCTION

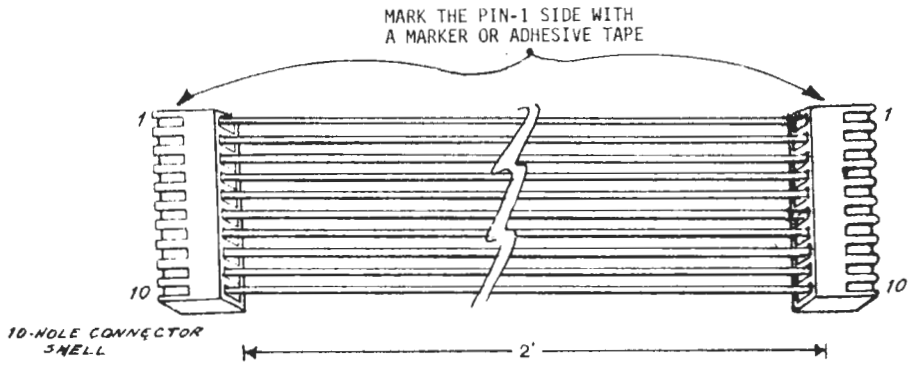


In some of these tests you'll be required to remove an IC and short one of the socket pins to ground or to +5 volts. If you use a resistor lead to make the socket connection, you may bend the spring connector of the socket out of place. This could cause intermittent operation when the IC is reinstalled. Since replacing an IC socket on a four-layer board is a time-consuming task, build and use the following test jig.

-- Locate the programming plug and cut all jumpers along their centers.

-- Bend every other lead up so you can connect an alligator clip to any one of them without shorting to another lead.

VIDEO BOARD EXTENDER CABLE CONSTRUCTION



NOTE: The video board circuits do not use all ten leads of the following extender cable. However, you should install all ten leads into the extender cable to allow for future modifications.

-- Cut the stranded wire into 10 two-foot lengths and solder a spring connector to both ends of each wire.

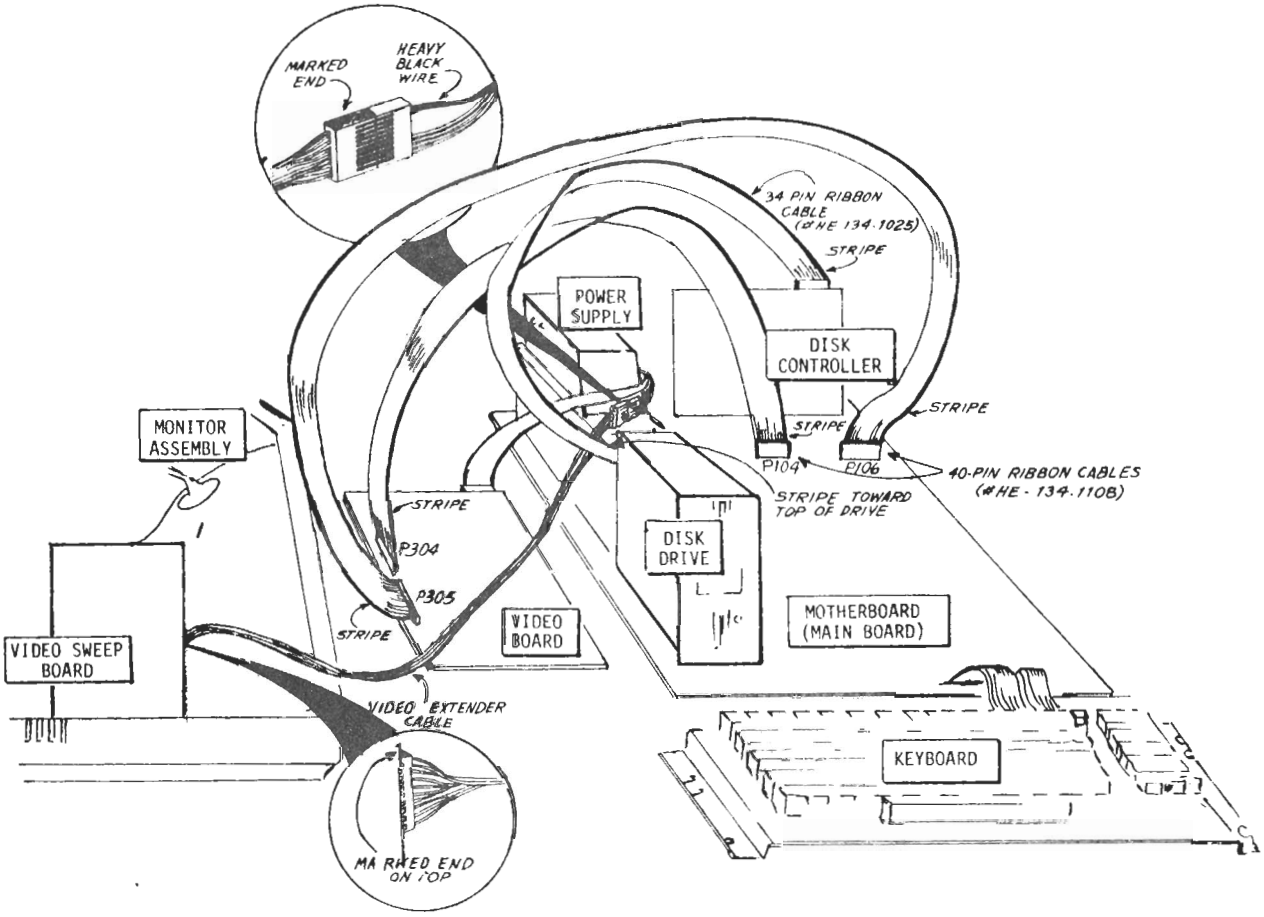
-- Position the 10-hole socket shells so that the slotted sides are facing toward you and install the wires as shown in the previous illustration.

-- Refer to the illustration and mark the pin-1 side of each shell with a marker or adhesive tape.

-- Locate the 10-pin adapter plug and install it into one end of the extension cable.

-- Locate the two 40-pin ribbon cables and inspect the connectors. If there are any pin plugs present, remove them with a pair of long-nosed pliers.

PIN PLUGS



H/Z-100 TEST SETUP

-- Refer to the Disassembly section and disassemble the H/Z-100 down to the motherboard. Leave the motherboard and power supply mounted on the base.

-- Remove the S-100 card cage assembly so you can reach the ICs that it covers.

If you're working on the low-profile H/Z-100, skip the next step.

-- Refer to the accompanying illustration and install the video sweep board extender cable as shown. Make sure that the slots are facing the same way at the 10-pin adapter plug end.

If you're working on the all-in-one H/Z-100, skip the next step.

-- Connect the unit under test to your video monitor. Use 75-ohm coaxial cable.

-- Connect the disk drives to the floppy disk controller board with the 34-pin ribbon connector cable. The cable stripe should face the same direction at both the board and the drives.

-- With the 40-pin ribbon cable, connect P304 on the video board to P104 on the motherboard. Make sure that the striped edge of the cable is facing the same direction on both boards (see the inset in the accompanying illustration).

-- In the same manner, connect P305 to P105.

-- Set up S101 for 5-1/4" drives (primary boot), and auto-boot defeated (see the Configuration section).

DISK DRIVE SETUP

Currently, the male pins needed to build an extension cable for the disk drive power supply are not available from stock. To test a disk drive, you'll have to remove it from its mounting bracket and place it closer to the main chassis. A convenient location is the open area to the left of the motherboard and in front of the power supply module.

-- Position the disk drive as described and install the power cable.

The H/Z-100 is ready for servicing.

GENERAL TROUBLESHOOTING INFORMATION

REPAIRING MULTILAYER BOARDS

The H/Z-100 contains two 4-layer circuit boards: the motherboard and the bit-mapped video board. These boards contain foil runs on the two outer surfaces and a +5 volt plane and ground plane on the inside of the board.

Although a 4-layer board is more complex than a double-sided board, you can replace components on the board by being careful and using tools similar to the following:

1. Heath GH-17A 25-watt soldering iron with the temperature control set to medium.

2. #2 solder wick (G.C. Electronics catalog no. 684).

3. A desoldering bulb. Do not use a spring-action solder sucker; it could damage the foil runs.

4. Solder, long-nose pliers, diagonal pliers, and small screwdriver.

There are two problems you should watch out for when replacing a component on the motherboard or video board: (1) A sleeve connecting one layer to another may open when you remove a component. (2) A solder bridge may short together two foil runs, which are closely spaced.

Since most of the circuit board foils are solder-masked, solder bridges should not be a problem. However, be careful around IC sockets; you'll quite often find conductors running between the socket pins.

If a sleeve opens, you can repair it by using wire-wrap wire to jumper the component lead to its destination. Note, however, that this may make the circuit board incompatible with the automated board-testing equipment at the factory.

To prevent opening a sleeve, or causing other damage to the multilayer board, observe the following guidelines:

1. AXIAL-LEAD COMPONENTS (SUCH AS RESISTORS)

   Removal

   Completely remove the solder from the leads with solder wick.

   Straighten the resistor leads so they won't pull against the sleeves when you remove the resistor.

   Heat one lead with the soldering iron until the solder melts, then gently pull that lead away from the board.

   In the same manner, remove the remaining lead.

   Replacement

   Make sure that the holes where the resistor leads are to be installed are clear. Use solder wick, if necessary, to remove excess solder.

   Install the resistor, solder it, and clip off the excess lead lengths as you normally do for any circuit board.

2. VERTICALLY-MOUNTED COMPONENTS (SUCH AS ELECTROLYTIC CANS)

   Removal

   Remove the solder with solder wick. This may take longer than removing solder from a resistor lead. Most of the electrolytics connect to the +5 volt and ground planes of the circuit board, which act as heat-sinks.

   Straighten the component leads so they won't drag against the sleeves when you remove the component.

Generally, solder wick will not completely remove all the solder between the leads and the sleeves; causing the leads to stick to the sleeves. Since, in vertically mounted components, you usually can't pull one lead out at a time, you must use a rocking technique. Here's how...

Heat one lead with the soldering iron and tilt the capacitor so that the lead starts to move out of its hole.

Then heat the other lead and tilt the component in the opposite direction so that lead starts to move out of its hole.

Continue the previous two steps until the capacitor pulls free of the circuit board.

The above is a common procedure for removing vertically mounted components from any circuit board. The only difference here is that you must be more careful.

Replacement

Use the same technique described in the section on resistor replacement. Do not apply too much solder, since you won't be able to tell if a solder blob is forming between the capacitor and circuit board.

3. IC Sockets

Removal

Pry off the plastic portion of the socket with a small screwdriver.

Remove the socket spring connectors, one at a time, using the following technique:

Position the board on its edge so that you can reach both sides of the board.

Grip the spring connector with a pair of long-nose pliers.

Heat the spring connector solder connection from the foil-side of the board.

When the solder melts, gently pull the spring connector from the board.

Replacing

Remove any excess solder from the IC socket holes. Use the desoldering bulb if the solder wick won't remove all of the solder.

Install and solder the IC socket. Apply the solder sparingly to prevent solder blobs from forming beneath the IC socket.

4. OTHER COMPONENTS

Board Connector Pins

Generally, you would remove these in the same manner as described under "IC Sockets." That is, grip one pin with the pliers, heat the solder connection, and gently pull the pin out. Repeat until all pins have been removed.

Resistor Packs

You will probably never have to replace a resistor pack. However, if the situation arises, review the following.

Like other rigid, multi-pin components, resistor packs have to be destroyed in order to be removed -- unless you have special desoldering tools. The leads of some resistor packs are accessible to diagonal pliers; allowing you to clip the pack away from the leads and then removing each lead from the board.

Other resistor packs are mounted flush to the board; preventing you from reaching the leads. In cases like this, use a slightly heavier pair of diagonal pliers and cut up the resistor pack to get to the leads.

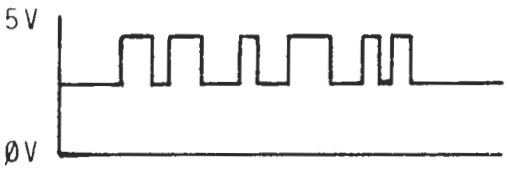
Be careful and don't apply any stress to the board.

S-100 Bus Connectors

You will not be able to efficiently replace the S-100 connectors without special desoldering tools. If you discover a bad S-100 socket that can't easily be fixed, you may be better off if you replace the entire motherboard. If this situation arises, first check with the technical consultants and your store manager or service supervisor.

CHECKING SHORTED FOIL RUNS

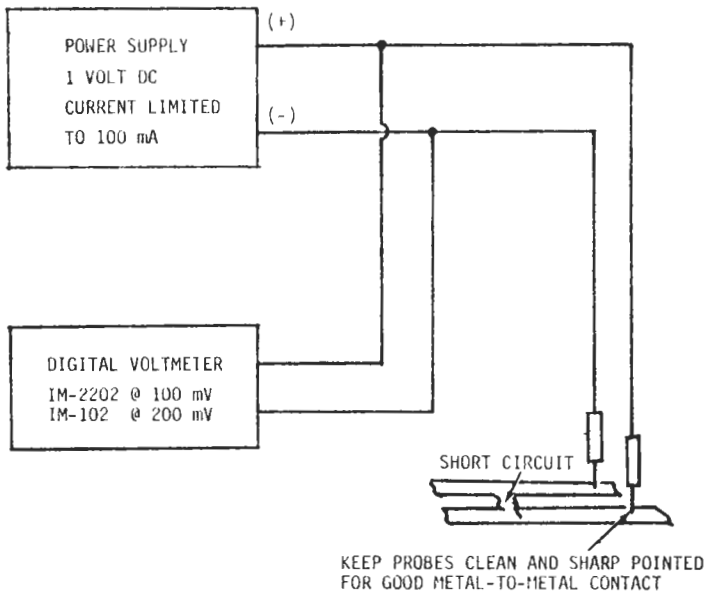
Occasionally the input or output of a TTL logic circuit can partially short inside the IC, causing a high-resistance path to the +5 volt supply. The resulting logic level on that bus line may be an undefined state of about +1.5 volts. If this line is shared by other ICs, their outputs will override this level to give a waveform similar to the one shown below:



Measuring this line with a logic probe may indicate normal operation. Although most logic probes will show pulses going from a high-impedance state to logic one, this can be easily overlooked. In this case, an oscilloscope will give a quick and definite indication of a faulty line.

A direct short, on the other hand, can cause zero ohms between a bus line and +5 volts, ground, or another bus line. If this should occur, the most likely cause is a shorted IC rather than a solder bridge, since most of the H/Z-100 boards are factory assembled and tested. Since the ICs are installed in plug-in sockets, it is perhaps quickest to place an ohmmeter across the shorted lines and start pulling ICs connected to those lines until the reading jumps up from zero ohms.

If removing the ICs doesn't correct the problem, you can use the following technique:



-- Unplug all ICs and lift (if possible) all components connected to the shorted line.

-- Adjust the DC power supply to 1.0 volt and set the current limiting to 100 mA.

-- Set the DVM to its 200-mV range and connect it in parallel with the DC power supply.

-- Connect two sharp-pointed test probes (for good metal-to-metal contact) to the two shorted lines. Test various sections of the line until you locate the area where the displayed voltage is lowest. The short circuit should be at this point.

   When the short is beneath an IC socket, the voltage along the lines will drop as the pair of probes enters the socket area, and rise again as measurements are made further away from the socket on the other side.

Depending on line length, maximum voltage will be about 10 to 15 mV furthest away from the short.

NOISE PROBLEMS

The H/Z-100 contains six RF-frequency crystal oscillators and dozens of circuits generating fast rise-time pulses. These all contribute noise to the power supply lines and ground returns, even when filtered. This can cause erroneous readings if you do not properly connect your test probe. If you don't maintain an awareness of this noise, you can waste a lot of time trying to track down a symptom that doesn't exist.

When testing the H/Z-100, connect the ground return of your logic probe or oscilloscope probe as close as possible to the component that you're measuring. If there's a long distance between the point you're measuring and the ground connection, the ground run may pick up noise which could give you false readings. A good place to ground your test lead is one of the diode-shaped ceramic capacitors near the IC under test.

Another type of noise problem can occur if the power supply isn't regulating or filtering properly. In this case, for example, a surge of current, such as when a disk drive turns on, may generate a large enough spike into the line to affect some of the logic circuits. This could result in intermittant crashes, and, in this example, cause you to waste time troubleshooting the drive circuits instead of the power supply. So, when troubleshooting H/Z-100 -- or any electronic circuit for that matter -- check the power supply first.

SERVICE HINTS

DEAD UNIT

OPEN FUSE OR CIRCUIT BREAKER

Unplug the power supply from the circuit boards. Then connect the power supply to a voltage-variable AC supply and adjust the primary voltage from 0 Vac to 120 Vac. If the primary current should suddenly increase above 2 amperes, then replace the power supply module. (The average primary current is about 1.5 amperes.)

If the current is okay, then check the DC output voltages. If any of the voltages or peak-to-peak ripple is incorrect, then replace the power supply module.

If the voltages are okay, then one of the circuit boards is defective.

To find out which one, make resistance readings. If you find a shorted foil run, locate the short by using the techniques described earlier.

If you can't find an obvious short circuit, then plug in boards, one at a time, and slowly adjust the variable AC supply from 0 to 120 Vac each time. When the current rises too fast, you've found the bad board.

Inspect the suspected board for heat-damaged components and improperly installed components (see Visual Checks for the board you're inspecting). Check the on-board regulators for short circuits between their inputs and outputs.

If necessary, replace the suspected board with a known-good one.

INCORRECT VOLTAGES

Use the same procedure described under "Opens Fuse or Circuit Breaker." That is, unplug the power supply module from all the circuit boards and check the supply voltages. If any of these are incorrect, then replace the power supply.

Otherwise, a circuit board is causing the problem. For example, if it's pulling a voltage line down, you probably won't find the cause by taking ohmmeter measurements.

In this case, use the visual checks section and make sure that each component is in the right place. Make sure that none of the ICs are installed backwards. Touch each IC and make sure that none of them are hot -- indicating an internal short. (Note that the larger ICs will be warm, but not so hot that you can't keep your finger on it.)

If necessary, replace the circuit board.

DISPLAY PROBLEMS

If an all-in-one unit, check the 12-volt power supply to the video sweep board. If missing, check the power supply cables and, if necessary, replace the power supply module.

Connect your shop monitor to the appropriate video output (RGB or composite). If the display is okay on your monitor, then the customer's video sweep board or monitor is bad.

If the video sweep board or monitor is okay, then substitute a known-good bit-mapped video board. If this corrects the problem, go to the video board troubleshooting section, or replace the video board.

If the video sweep board and the bit-mapped video board test okay, then proceed to the motherboard troubleshooting section.

DEFECTIVE KEYBOARD

Is the LED on the RESET key lit? If not, then check the 5-volt supply to the motherboard. If missing, refer to the suggestions under "Dead Unit." If 5 volts is present, then check for open foil runs on the motherboard.

Substitute a known-good keyboard assembly. If this corrects the problem, then replace the keyboard. Otherwise, replace the motherboard; or, if you're troubleshooting to the component level, perform the tests in the Motherboard Troubleshooting section.

WON'T BOOT

Attempt to boot up with known-good software. If you can, then try the customer's software. Also, make sure the customer is correctly following the boot-up procedure. If the software is okay, then perform the following hardware checks.

Check the power cables to the drives. Make sure that the drives are getting both +12 volts and +5 volts.

Make sure that the 34-pin ribbon cable between the drives and controller board is installed properly.

Check the configuration section and make sure that the slide switches are correctly positioned and jumper plugs properly installed. This includes the motherboard, disk controller board, and disk drives.

Substitute a known-good disk controller board. If this corrects the problem, then replace the board or refer to "Troubleshooting" in the Disk Controller section of this Manual for more service information.

Substitute a known-good disk drive. Though it's unlikely for both drives in a dual-drive system to go bad, it can happen.

If the above modules test okay, then replace the motherboard. Or, for in-depth troubleshooting, refer to "Troubleshooting" in the Motherboard section of this Manual.

OTHER PROBLEMS

SERIAL PORT A DEFECTIVE (ASYNCHRONOUS PRINTER)

Check this port with a known-good printer (such as the H/Z-25), connecting cables, and software. If the system works properly, then the problem is likely in the customer's peripheral equipment. Otherwise, perform the following tests.

Check the +5 volt and ±16 volt supplies to the motherboard. If missing, replace the power supply module.

Replace the motherboard; or, for in-depth troubleshooting, refer to "Troubleshooting" in the Motherboard section of this manual.

SERIAL PORT B DEFECTIVE (MODEM)

Check this port with a known-good MODEM (such as the Heath WH-43 {Hayes Stack Smartmodem}), connecting cables, and software. If the system works properly, then the problem is likely in the customer's peripheral equipment. Otherwise, perform the following tests.

Check the +5 volt and ±16 volt supplies to the motherboard. If missing, replace the power supply module.

Replace the motherboard; or, for in-depth troubleshooting, refer to "Troubleshooting" in the Motherboard section of this manual.

PARALLEL PORT DEFECTIVE

Check this port with a known-good line printer (such as the Epson MX-80), connecting cables, and software. If the system works properly, then the problem is likely in the customer's peripheral equipment. Otherwise, perform the following tests.

Check the +5 volt power supply to the motherboard. If missing, replace the power supply module.

Replace the motherboard; or, for in-depth troubleshooting, refer to "Troubleshooting" in the Motherboard section of this manual.

FINAL CHECKS

Before returning the H/Z-100 to the customer, ensure that the computer is operating properly by performing the following final checks:

-- All circuit boards, plugs, and other connectors securely installed.

-- All hardware installed and tightened.

-- All switches and jumper options configured for the customer's system; or configured to the customer's specifications. (Unless requested otherwise, the auto-boot feature should be enabled.)

-- Unit powers up properly.

-- Unit loads and runs Z-DOS, CP/M-85, and other programs properly.

-- Keyboard echos all printable characters to the CRT under Z-DOS.

-- Display is properly calibrated for height, width, and linearity.

-- Display is uniformly focused across the CRT.

-- Unit passes the system and video memory tests on the Z-DOS disk (see the Diagnostics section in this manual).

-- Let the H/Z-100 operate for an hour and again test the memory for thermal problem.

   If the customer has complained of a thermal or intermittent problem (or you suspect one), let the unit run overnight and again perform the diagnostics in the morning.

-- Paperwork is in order.

-- The customer has been notified.

TECHNICIAN NOTES:

PARTS LISTS

PARTS LIST - ALL-IN-ONE CABINET AND ASSEMBLIES

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
ASSEMBLIES		
	CRT monitor assembly consisting of:	HE 234-202
	1) CRT (green)	100-724-03
	2) Yoke	A-8337
	3) Video sweep p/c bd	A-10520
	Disk drive 5-1/4", 48TPI	HE 150-142
	Keyboard	HE 64-899
	Power supply	HE 234-201
	Wired floppy control board	HE 181-3763
	Wired mother board	HE 181-3630
	Wired video board (B/W)	HE 181-3631
	(Color)	HE 181-3267
CABINET - CHASSIS		
	Bottom cover	HE 92-759
	CRT support bracket	HE 204-2606
	CRT support panel	HE 203-2116
	Cabinet center	HE 92-762
	Cabinet top	HE 92-761
	Cable clamp	HE 204-2638-1
	Chassis	HE 200-1418-1
	Drive mounting plate	HE 200-1419
	Dual drive support panel	HE 203-2129
	Dual drive front panel	HE 203-2131
	Front bezel	HE 92-763
	Latch bracket	HE 204-2632
	Nut holding plate	HE 205-8199
	Rear panel	HE 203-2139-1
	S-100 card cage	HE 206-1416
	S-100 panel guide	HE 94-631
CABLES		
	34-conductor flat ribbon cable assembly	HE 134-1247
	50-conductor flat ribbon cable assembly	HE 134-1264
	Composite video cable assembly	HE 134-1265
	Internal video cable assembly	HE 134-1273
	RGB cable assembly	HE 134-1254
	Video interface cable assembly	HE 134-1257

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
HARDWARE		
#4 and #6 Hardware		
	#4 lockwasher	HE 254-9
	#4 nut (large)	HE 252-2
	#4 nut (small)	HE 252-15
	4-40 x 1/4" black phillips-head screw	HE 250-1411
	4-40 x 1/2" screw	HE 250-1413
	4-40 x 3/16" hex "D" spacer	HE 255-757
	4-40 x 1" hex spacer	HE 255-804
	#6 flat washer	HE 253-60
	#6 lockwasher (internal-toothed)	HE 254-1
	#6 lockwasher (external toothed)	HE 254-6
	#6 solder lug	HE 259-1
	#6 x 5/8" hex-head screw	HE 250-1199
	#6 x 1/4" black phillips-head self-tapping screw	HE 250-1307
	6-32 nut	HE 252-3
	6-32 x 3/4" black phillips-head screw	HE 250-1240
	6-32 x 1/2" screw	HE 250-1430
	6-32 x 1/4" phillips-head screw	HE 250-1325
	6-32 x 3/8" hex-head screw	HE 250-1264
	6-32 x 1-3/4" screw	HE 250-1315
OTHER HARDWARE		
	#8 x 1/2" black phillips-head screw	HE 250-1265
	#8 x 1-1/2" hex-head screw	HE 250-1405
	#8 x 3/4" hex-head screw	HE 250-512
	#8 x 5/8" hex-head screw	HE 250-1138
	#10 flat washer	HE 253-98
	#10 x 1-1/2" hex-head screw	HE 250-1318
	Control lockwasher	HE 254-14
	Latch pin	HE 262-56
	Small control nut	HE 252-39
	Spring	HE 258-749

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
MISCELLANEOUS		
	100 ohm 1/4 watt, 5%	HE 6-101-12
	500 ohm control	HE 10-1192
	Braid	HE 345-1
	Foam tape 3/4"W x 5/16"T	HE 74-41
	Insulating paper 5-1/2" x 6-1/2"	HE 75-826
	Knob	HE 462-952
	Label: Class A FCC	HE 390-2331
	Label: Power rating	HE 390-2334
	Label: Serial set	HE 390-2036
	Label: Warning	HE 390-2325
	Line cord	HE 89-60
	Name plate	HE 391-653
	Rubber grommet	HE 73-6
	Rubber foot	HE 261-29
	2-1/8" brown hole cover	HE 485-42
	2-3/8" brown hole cover	HE 485-43
	2-7/8" brown hole cover	HE 485-44
	Manual set consisting of:	HE 172-8284
	1) Binder	HE 701-140
	2) Slip-in cover	HE 597-2802-1
	3) Spine cover	HE 597-2803-1
	4) Document holder	HE 597-2914
	5) Diskette holder	HE 703-73
	6) Demonstration disk	HE 891-342
	7) Publisher's package consisting of:	HE 593-0037
	1) User's manual	HE 595-2892
	2) Tab set	HE 597-2768
	3) Fly sheet	HE 597-2907

PARTS LIST - LOW PROFILE CABINET AND ASSEMBLIES

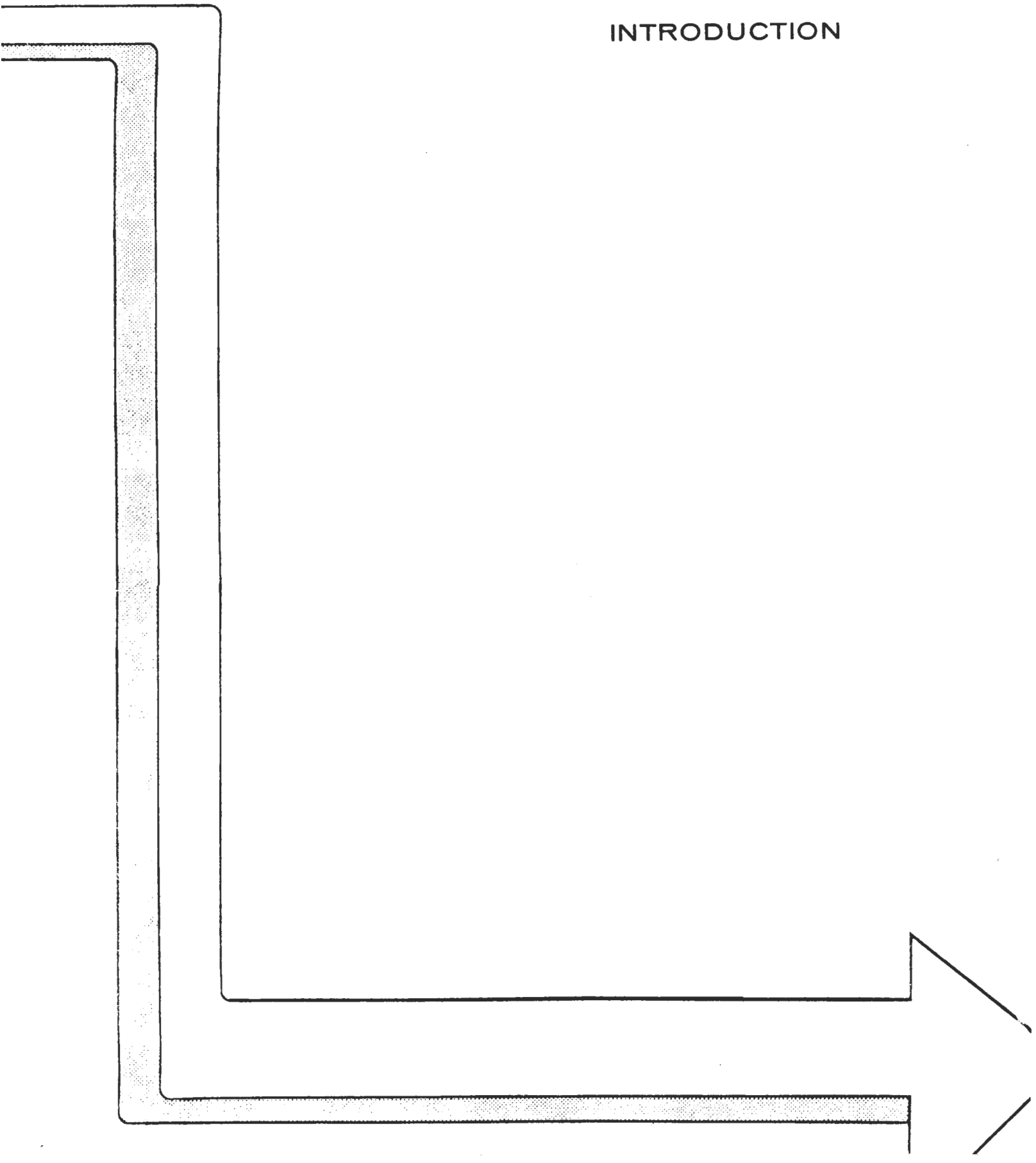
CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
ASSEMBLIES		
	Disk drive 5-1/4", 48 TPI	HE 150-142
	Keyboard	HE 64-899
	Power supply	HE 234-200
	Wired floppy control board	HE 181-3763
	Wired mother board	HE 181-3630
	Wired video board (B/W)	HE 181-3631
	(Color)	HE 181-3267
CABINET - CHASSIS		
	Bottom cover	HE 92-759
	Cabinet cover	HE 92-758
	Cable clamp	HE 204-2638-1
	Chassis	HE 200-1418-1
	Drive shelf	HE 92-760
	Drive shield	HE 206-1441
	Front panel	HE 203-2125
	Rear panel	HE 203-2139-1
	S-100 card cage	HE 206-1416
	S-100 panel guide	HE 94-631
	Slide bracket	HE 204-2605
CABLES		
	34-conductor flat ribbon cable assembly	HE 134-1246
	50-conductor flat ribbon cable assembly	HE 134-1264
	Composite video cable assembly	HE 134-1265
	RGB cable assembly	HE 134-1254
	Video interface cable assembly	HE 134-1257

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
HARDWARE		
#4 and #6 Hardware		
	#4 lockwasher	HE 254-9
	#4 nut (large)	HE 252-2
	#4 nut (small)	HE 252-15
	4-40 x 1/4" black phillips-head screw	HE 250-1411
	4-40 x 1/2" screw	HE 250-1413
	4-40 x 3/16" hex "D" spacer	HE 255-757
	4-40 x 1" hex spacer	HE 255-804
	#6 lockwasher (internal-toothed)	HE 254-1
	#6 lockwasher (external-toothed)	HE 254-6
	#6 x 5/8" hex-head screw	HE 250-1199
	#6 x 1/4" black phillips-head self-tapping screw	HE 250-1307
	6-32 nut	HE 252-3
	6-32 x 1/4" screw	HE 250-1422
	6-32 x 1/8" phillips-head screw	HE 250-1325
	6-32 x 3/8" hex-head screw	HE 250-1264
OTHER HARDWARE		
	#8 x 3/4" hex-head screw	HE 250-512
	Latch pin	HE 262-56
MISCELLANEOUS		
	Foam tape 3/4"W x 5/16"T	HE 74-41
	Label: Class A FCC	HE 390-2331
	Label: Power rating	HE 390-2334
	Label: Serial set	HE 390-2036
	Label: Warning	HE 390-2325
	Line cord	HE 89-60
	Name plate	HE 391-658
	Phono socket	HE 434-107
	Rubber foot	HE 261-27
	Spring	HE 758-750
	2-1/8" brown hole cover	HE 485-42
	2-3/8" brown hole cover	HE 485-43
	2-7/8" brown hole cover	HE 485-44

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
MISCELLANEOUS (CONTINUED)		
	Manual set consisting of:	HE 172-8263
	1) Binder	HE 701-140
	2) Slip-in cover	HE 597-2802-1
	3) Spine cover	HE 597-2803-1
	4) Document holder	HE 597-2914
	5) Diskette holder	HE 703-73
	6) Demonstration disk	HE 891-342
	7) Publisher's package consisting of:	HE 593-0037
	1) User's manual	HE 595-2892
	2) Tab set	HE 597-2768
	3) Fly sheet	HE 597-2907

MOTHERBOARD

INTRODUCTION



The motherboard is the primary component of the H/Z-100. This is the large four-layer circuit board located on the chassis floor. This board is factory wired and tested to be 100% operational. The motherboard contains the processors, I/O, and memory facilities for the computer.

The processors for the H/Z-100 are the 8088 and the 8085. The 8088 is a 16-bit processor that operates in an 8-bit environment. This processor gives the computer its power and speed. The 8085 is an 8-bit processor that is code compatible with the popular 8080 microprocessor. The use of the 8085 microprocessor assures the user a large software base. Both processors run at a clock speed of 5 MHz. By using the advantages of both processors, the H/Z-100 is a powerful and versatile machine.

I/O communication to the outside world is located on the motherboard. It contains two serial ports, a parallel port, and a keyboard. The two serial ports are RS-232C compatible; the parallel port is a Centronics compatible printer interface. A 95-key keyboard provides user input to the computer through a dedicated microprocessor.

Also located on the motherboard are the memory facilities for the computer. This consists of on-board RAM and ROM. MTR-100, an 8K ROM, contains all the code necessary to initialize the computer and emulate H-19 functions. The standard RAM configuration for the H/Z-100 is 128K bytes. This may be expanded to 192K bytes of on-board RAM. These features make the H/Z-100 the most powerful Heath computer available.

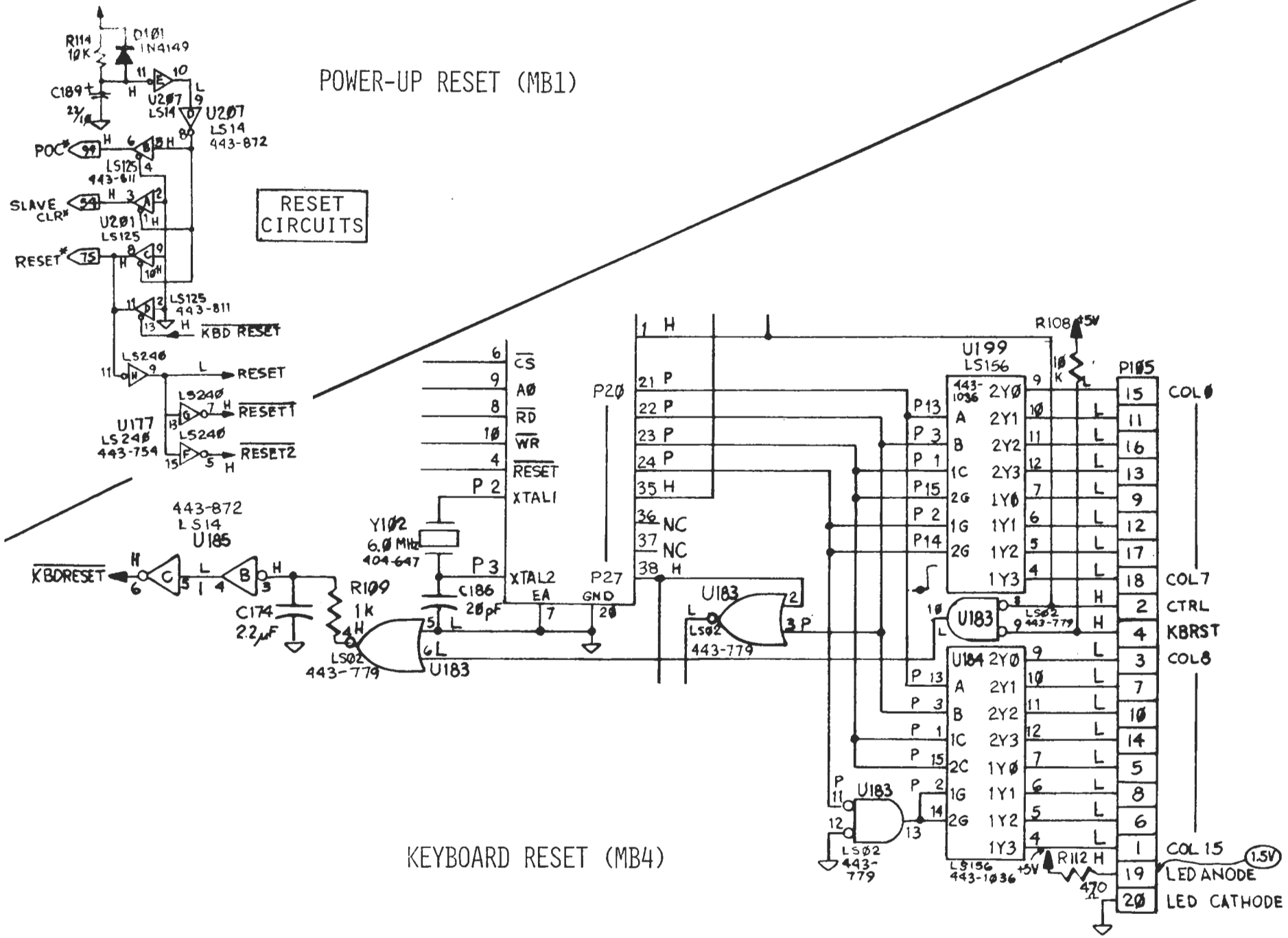
In addition, a 5-slot, S-100 bus is located on the motherboard. It is defined by the IEE-696 definition for a S-100 bus. This allows the H/Z-100 flexibility in hardware configurations. The motherboard is configured to be the controller for the bus; however, the memory and I/O facilities may be accessed by slave processors. The only areas on the motherboard that are not accessible by slave processors are the interrupt controllers for the 8088 and the 8085, the high order address latch, and the processor swap port.

The information located in this section of the manual will aid you in troubleshooting the motherboard to the component level. Contained in this section are: Circuit Description, Visual Checks, Troubleshooting, Parts List, and X-Ray Views. If additional information on a particular IC is required, refer to the IC Data section in the back of this manual.

CIRCUIT DESCRIPTION

(continued)

CIRCUIT DESCRIPTION (continued)


POWER-UP RESET (MB1)
RESET CIRCUITS
KEYBOARD RESET (MB4)
R114 10K
D101 IN4149
C189 2.2µF
U207 LS14 443-872
POC*
LS125 443-611
SLAVE CLR*
U201 LS125
RESET*
LS125 443-811
KBD RESET
LS240
RESET
RESET1
RESET2
U177 LS240 443-754
443-872 LS14 U185
KBDRESET
C174 2.2µF
R109 1k
LS02 443-779
U183
Y102 6.0 MHz 404-647
C186 20pF
P2Ø
P27
CS
AØ
RD
WR
RESET
XTAL1
XTAL2
EA
GND
NC
U199 LS156
R108 10K
U184
P105
COLØ
COL7
CTRL
KBRST
COL8
COL 15
LED ANODE
LED CATHODE
1.5V
R112 470Ω

RESET CIRCUITS

POWER-UP RESET

Refer to schematic MB1.

R114 and C189 provide the power-up reset pulse for the H/Z-100. Upon turn-on, C189 charges through R114, holding U207-8 low for about 200 mS. This pulse connects to several buffers to provide the proper reset levels to the rest of the computer:

U201B buffers the reset pulse to provide the S-100 power-up clear (POC*) signal. This signal is logic zero for reset and logic one otherwise. POC* resets the video board through U215D and P106-64 on schematic MB2.

U201A buffers the reset pulse to provide the S-100 SLAVE CLR* signal. Because U207-8 controls U201A through its gate line (pin 1), SLAVE CLR* is logic zero to clear and open-collector otherwise. This signal is present only to maintain IEEE-696 (S-100) standards. Currently, it's not used in the H/Z-100.

U210C is also wired to provide a logic zero for reset and a high-impedance state otherwise. This is because several circuits may share the S-100 RESET* line. This line drives U177H and, through the S-100 bus, resets the floppy disk controller board.

U177H inverts the reset signal, which can be the power-up reset or a keyboard reset, to drive the RESET line high. This line is again inverted by U177G and U177F to provide $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$; all three lines go to several places on the motherboard and video board to provide the proper reset signals.

KEYBOARD RESET

Refer to the keyboard circuits on schematic MB4.

When you press the CRTL key and the RESET key at the same time, pins 8 and 9 of U183 will go low and force U183-10 to logic one. This is inverted at U183-4 and to U185A through the filter network, R109 and C174.

U185B and U185C double inverts the signal to provide the active-low $\overline{\text{KBDRESET}}$ pulse that couples to U201-13 (see schematic MB1). The output, U201-11, is logic zero for reset and high-impedance otherwise.

From U201-11, the reset signal is processed as described under "Power-Up Reset."

8085 CPU

PIN-OUT DESCRIPTION

The 8085 CPU, U210 on schematic MB1, is the H/Z-100 8-bit processor. Because it uses the same instruction set as the Intel 8080, the H/Z-100 maintains software compatibility with previous Heath computers.

However, this IC has some hardware differences from the 8080, so we will briefly discuss the pin-out and basic timing. If you need to know more about the 8085, see the IC data sheets elsewhere in this manual.

A8-A15 (Output, Tri-State) These are multiplexed lines. During a memory access they contain the upper 8-bits of the memory address; during an I/O operation these lines contain the port address. These lines are tri-stated during Hold, Halt, and RESET.

AD0-AD7 (Input/Output, Tri-State) These are multiplexed lines. During a memory access they first contain the lower 8 bits of the memory address. This address is then stored in external latches. The CPU next places on AD0-AD7 the input or output data associated with that address. During an I/O operation these lines first contain the port address, then the data (either input or output) associated with that port.

ALE (Output) This is the address latch enable line. This line pulses high, then low, when either the memory or I/O address is on lines A0-A7. The external circuits use the negative-going transition to latch the address information. The falling edge of ALE is also used to strobe CPU status information.

S0, S1, IO/$\overline{M}$ (Output) These lines are used in conjunction with ALE to develop the S-100 machine cycle status lines at U227. See the section "Bus Status Circuits" for more detail.

$\overline{RD}$ (Output, Tri-State) The read control line goes to logic zero to indicate that the data bus is ready to transfer data from memory or I/O to the CPU. Tri-stated during Hold, Halt, and RESET.

$\overline{WR}$ (Output, Tri-State) The write control line goes to logic zero to indicate that the data bus is ready to transfer data from the CPU to memory or I/O. Data is set up on the trailing edge of the pulse. Tri-stated during Hold, Halt, and RESET.

READY (Input) If logic zero, the CPU will enter a wait state until READY is brought to logic one again. This allows using the 8085 with slow memories or peripherals.

HOLD (Input) If logic zero, the CPU will halt operation, raise the hold-acknowledge line (HLDA), and place the following lines into a high-impedance state: Address/Data, $\overline{WR}$, $\overline{RD}$, and IO/$\overline{M}$. This allows other processors, such as the 8088, to gain control of the H/Z-100.

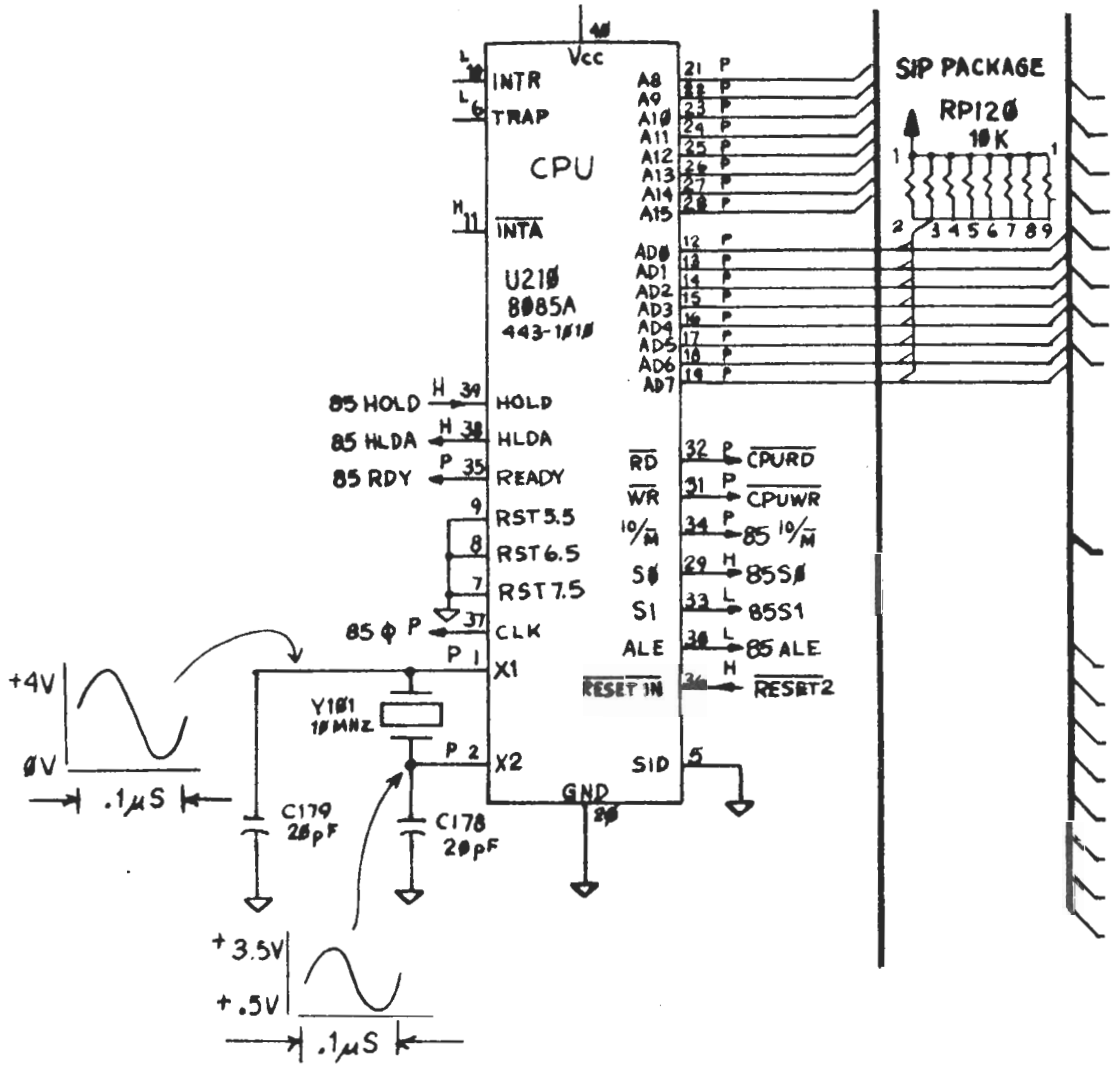
HLDA (Output) The hold acknowledge goes high to indicate that the CPU received the HOLD request and will release control of the bus in the next cycle. HLDA goes low again after the HOLD request is removed.

INTR (Input) This is the interrupt request line. If brought high, and the interrupts aren't disabled through software, the CPU will complete its current cycle and then process the interrupt. See the section "Interrupt Circuits" for more detail.

$\overline{INTA}$ (Output) The interrupt acknowledge goes low to indicate that the CPU has accepted the interrupt.

TRAP (Input) This is the nonmaskable interrupt input line. It is the highest priority interrupt and can't be disabled.

$\overline{RESETIN}$ (Input) Bringing this line low resets the computer. It sets the program counter to zero, disables interrupts, and resets the HLDA flip-flop.

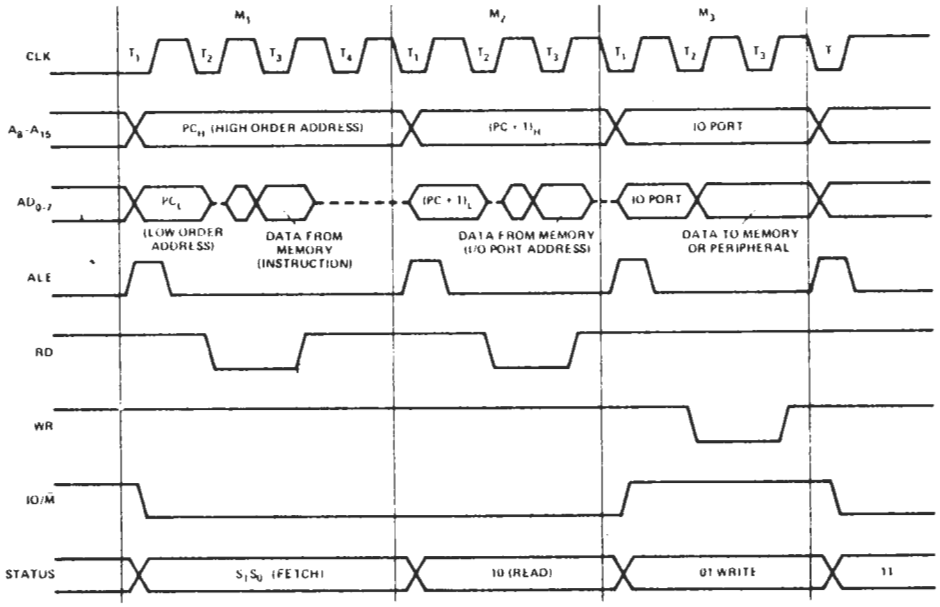


U210, 8085 CPU (MB1)

X1, X2 (Input) The clock input. The 10-MHz signal from Y101 is internally divided down to 5 MHz.

CLK (Output) The clock output. This provides 5-MHz timing to the H/Z-100 when the 8085 has control of the computer.

BASIC SYSTEM TIMING



To better understand how the H/Z-100 works, you should become familiar with the 8085 timing. The above illustration shows the waveforms that occur when the 8085 processes the OUT instruction. Though there are seven possible types of machine cycles (see the data sheets), these waveforms are typical.

During the M1 cycle, the computer fetches the op-code; in this example, the OUT instruction. The M1 cycle lasts for four clock states (T-states). During this time, A8 through A15 contain the upper 8 bits of the memory address of the instruction to be fetched.

From time T1 to T2, lines AD0-AD7 contain the lower 8 bits of memory address data. The ALE line goes low to strobe this information into the external address latches. The the IO/M line goes low to indicate that this is a

memory-read operation. The signals on the status lines, S0 and S1, indicate that the op-code fetch cycle is taking place. The status circuitry will be covered in more detail later.

From time T2 to T3, $\overline{RD}$ goes low and the instruction in the memory location pointed to by the address latches is placed on lines AD0-AD7, which are now acting as data lines. This data, the OUT instruction, is loaded into the computer for internal processing during time T3 to T4.

From time T3 to T4, RD goes high and AD0-AD7 goes to a high-impedance state.

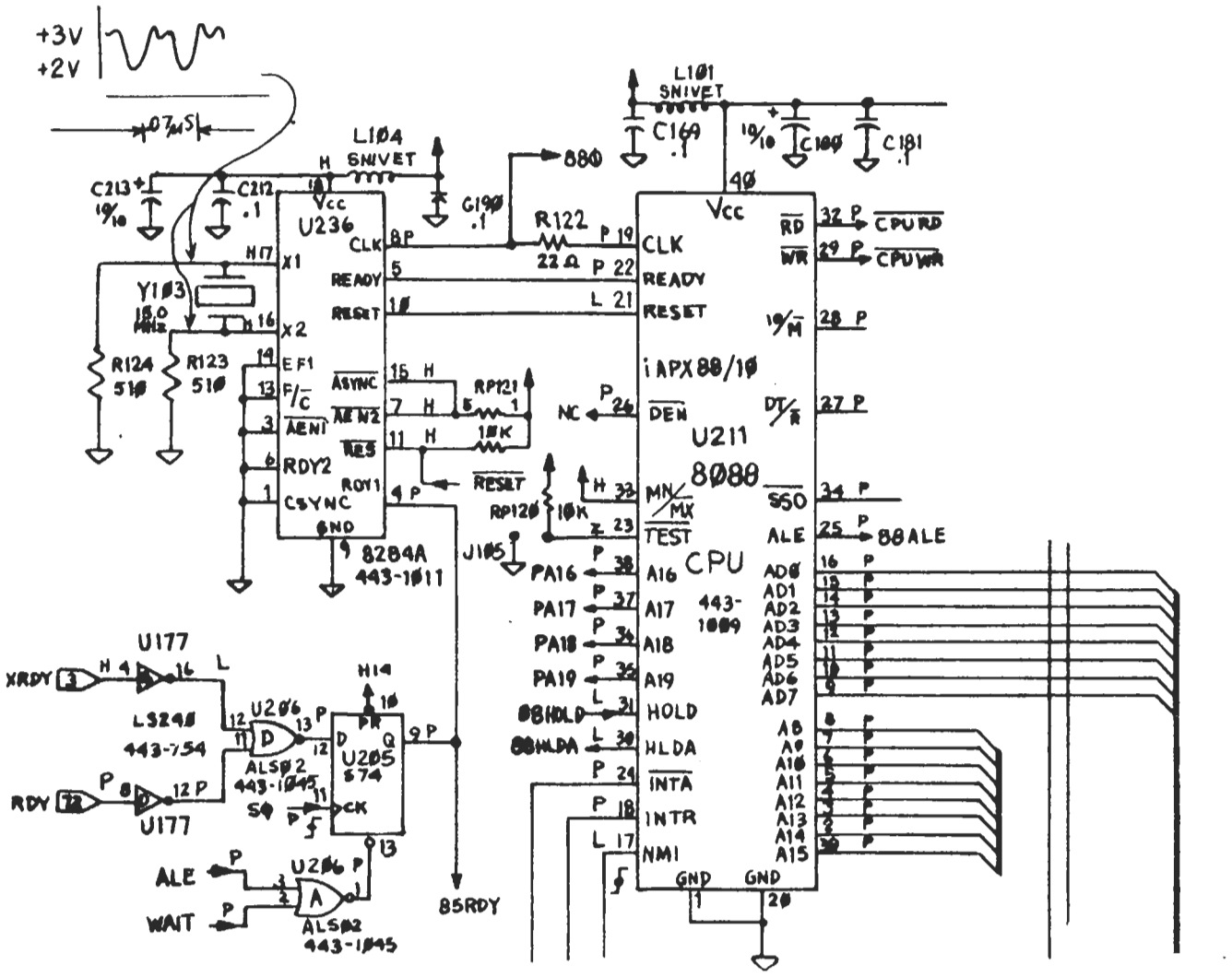
During the M2 cycle, the computer reads the data in the next memory location, which is the I/O port address the computer is to OUTput the data to. At time T1, lines A0-A15 contain the address of the memory location that holds the I/O port address. The ALE line strobes this address into the external address latches. Line IO/$\overline{M}$ is still low to indicate that the M2 cycle is a memory read cycle. This is also indicated by the logic states on status lines S1 and S0.

At time T2 to T3, $\overline{RD}$ goes low to read the memory location pointed to by the address latches. This location contains the address of the I/O port to be accessed.

During the M3 cycle, the computer transfers the data in its accumulator to the port address specified by the M2 cycle. This time, during T1-T2, lines AD0-AD7 contain the port address fetched during the M2 cycle. Line ALE strobes this information into the external address latches. Lines AD8-AD15 also contain the port address, but aren't used in the H/Z-100. The IO/$\overline{M}$ line goes high to indicate that this cycle is an I/O cycle, rather than a memory cycle. The logic states of the status lines, S0 and S1, will indicate that this cycle is an I/O write cycle.

During time T2 to T3, the data in the accumulator of the 8085 is placed on the data bus and WR goes low to write it to the port pointed to by the address latches.

After T3, the 8085 generates another M1 cycle and fetches the next instruction in the program.



U211, 8088 CPU (MB1)

8088 CPU

OVERVIEW

The 8088 CPU is located at U211 on schematic MB1. This IC combines the powerful resources of a 16-bit microprocessor internal architecture with the easy-to-use 8-bit bus interface. In fact, most of the functions of the bus lines are identical to the 8085 at U210, making it easy to interface both CPUs to the H/Z-100 motherboard.

The 8088 is completely software compatible with the 8086, the 16-bit bus CPU in this family. Other features are:

-- Seventy basic instructions and 24 different addressing modes.

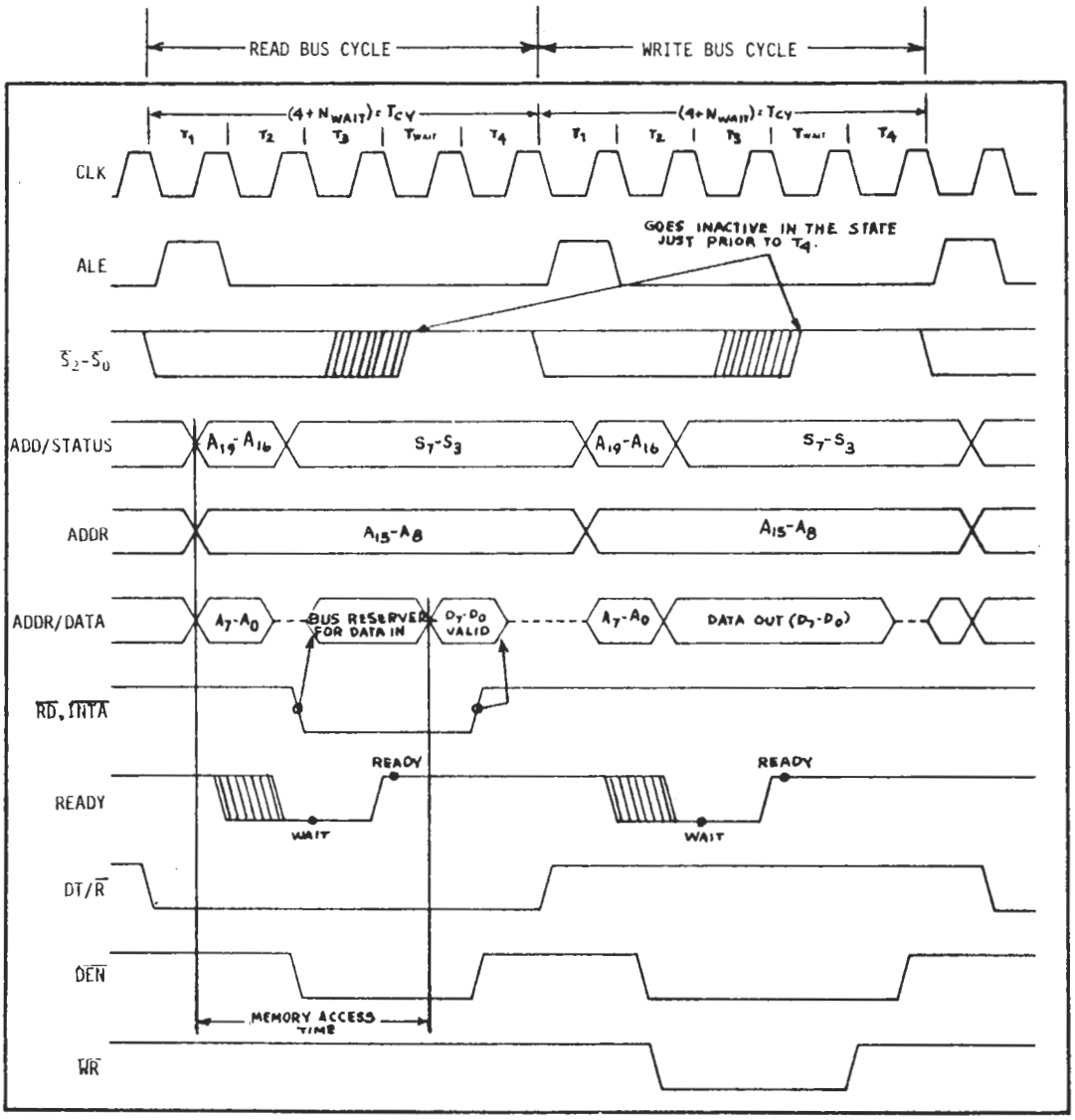
-- 20-bit address bus, allowing the 8088 to directly address up to 1 megabyte of memory.

-- 16-bit input/output port address range, allowing the 8088 to select up to 65536 port addresses.

-- Thirteen 16-bit registers; consisting of four segment registers, four pointer and index registers, one flag register (9 bits used), and four data registers. The four data registers can also be used as eight 8-bit registers.

-- Pipelined architecture to allow fetching instructions and processing previously-fetched instructions at the same time. (Understanding the instruction pipeline isn't critical for hardware troubleshooting; so it won't be discussed here. However, if you'd like to learn more about the 8088, order the "iAPX 88 Book" from Intel Corporation, Literature Department SV3-3, 3065 Bowers Avenue, Santa Clara, CA 95051. This book is also available from Heath Company Parts Department; part number 500-68.)

8088 CPU PIN FUNCTIONS



Refer to the accompanying set of waveforms and U211 on schematic MB1 as you read this.

$\overline{RD}$, Pin 32 Read Strobe: This line goes low at time T2 when the CPU reads from memory or an I/O port. This signal goes to a high-impedance state during hold acknowledge.

$\overline{WR}$, Pin 29 Write Strobe: This line goes low when the CPU writes to memory or an I/O port. This signal goes to a high-impedance state during hold acknowledge.

IO/$\overline{M}$, Pin 28 Status Line: This line goes low during a memory read or write ($\overline{RD}$ or $\overline{WR}$ asserted). It goes to logic one for an I/O read or write. It's tri-stated during hold acknowledge. (Also see the description on the S-100 bus status circuits.)

DT/$\overline{R}$, Pin 27 Data Transmit/Receive: This line is similar to IO/$\overline{M}$. It's used in the H/Z-100 to develop the S-100 bus status circuits. It goes low during a read operation and high for write. It is tri-stated during hold acknowledge.

$\overline{SSO}$, Pin 34 Status Line: This line is used with DT/$\overline{R}$ and IO/$\overline{M}$ to develop the S-100 status circuit signals. The logic levels on this line depend on what type of instruction the CPU is processing. See the status circuit description elsewhere in this manual. This line is brought to a high-impedance state during hold acknowledge.

ALE, Pin 25 Address Latch Enable: This line pulses high when the CPU places the address information on the address/data bus. In the H/Z-100, this line clocks the address into external latches on the negative-going edge of ALE.

AD0-AD7, Pins 16-9 Address/Data Bus: When ALE is asserted, these lines contain the lower 8 bits of the 20-bit address. This can be a memory address or an I/O port address. From time T3 to T4, these lines contain the input or output data. Demultiplexing circuits in the H/Z-100 are used to separate the data and address information. These lines are tri-stated during hold acknowledge.

A8-A15, Pins 2-8 & 39 Address Bus: These lines carry the next 8 bits of the address. This is memory address during a memory access and I/O address during a port access. These lines hold the address during the entire bus cycle. They're tri-stated during hold acknowledge.

NMI, Pin 17 Non-maskable Interrupt: A positive-going transition on this line will interrupt the CPU. It can't be blocked with software. The CPU will complete its current instruction and then service the interrupt.

INTR, Pin 18 Interrupt Request: The CPU tests this line during the last clock cycle of each instruction to see if some device is requesting an interrupt. If pin 18 is logic one, then an interrupt request is taking place. The CPU will process the interrupt unless the interrupt is masked by software.

$\overline{\text{INTA}}$, Pin 24 Interrupt Acknowledge: The CPU brings this line to logic zero to inform the interrupting device that it's processing the interrupt. It's used as a read strobe to get vector information from the interrupt circuits (see the interrupt circuit description for more details).

HLDA, Pin 30 Hold Acknowledge: Goes high to indicate that the CPU has acknowledged a hold request at pin 31. See the description of the processor swap port for more details.

HOLD, Pin 31 Hold Request: This line goes high when another device requests control of the H/Z-100; such as when the 8085 is the active processor. The CPU will assert the HLDA line and suspend operation. See the description of the processor swap port for more details.

A19-A16, Pins 31 & 35-38 Address/Status Bus: From time T1 to T2, these lines hold the top 4 bits of the 20-bit address bus. ALE clocks this value into external latches when it returns to zero. The CPU then places the bus cycle status information on these lines. This feature isn't used in the H/Z-100 since the status information is developed in a different manner. See the description on the status circuits. These lines are tri-stated during hold acknowledge.

$\overline{\text{TEST}}$, Pin 23 Test Input: This input is examined by the "wait for test" software instruction. If pin 23 is low, execution continues, otherwise the processor waits in an idle state.

MN/$\overline{\text{MX}}$, Pin 33 Minimum/Maximum: Logic one on this pin places the 8088 in the minimum mode, the mode used by the H/Z-100. When placed in the maximum mode, some of the pin functions change. Usually, the maximum mode is used for larger systems and multi-processing systems.

RESET, Pin 21 Reset: Goes high to reset the 8088. The interrupts are disabled, certain registers in the 8088 are set or cleared, and the instruction pointer (program counter) points to the memory address 16 bytes below the top end of the 1 megabyte range (FFFF0H).

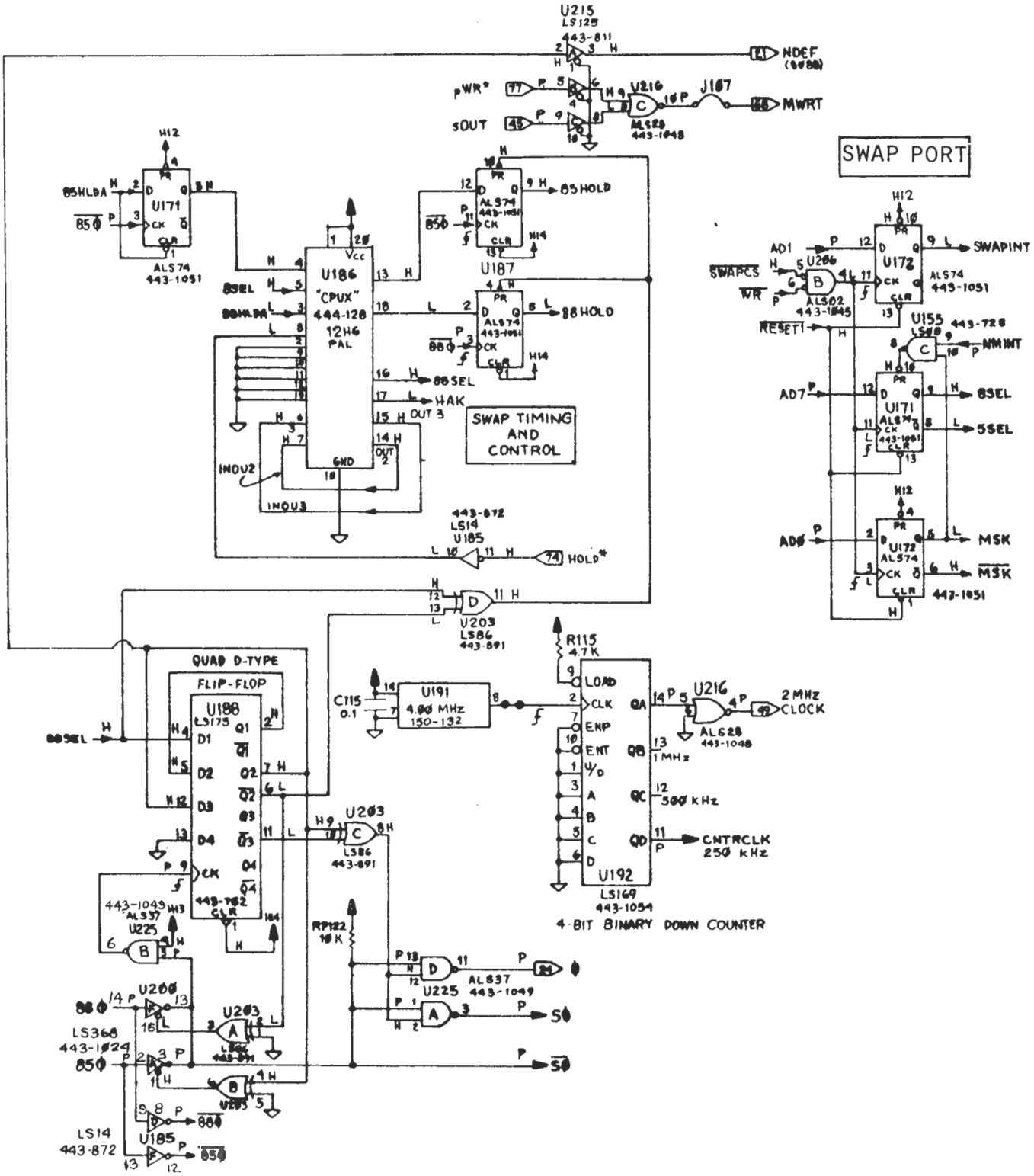
This line is asserted when the $\overline{\text{RESET}}$ line at U236-11 is pulled low. A Schmitt trigger shapes this signal and the clock circuits retimes it before applying it to the 8088.

READY, Pin 22 Ready: This is an acknowledgement signal from the addressed memory or I/O port that it is ready to transfer data. When this line is low, the CPU goes into a wait state until the addressed device brings it high. This allows using the 8088 with slow memory or I/O devices.

The READY signal is generated when U205-9 places a logic one on U236-4. U236 synchronizes this signal with the 8088 clock to ensure correct set up and hold times.

CLK, Pin 19 8088 Clock Input. Five-megahertz clock to provide timing to the 8088.

This signal comes from U236-8 which derives it from the 15-MHz crystal at Y103. Duty cycle is about 33% for optimized timing inside the 8088. When the 8088 is the active processor, this line also goes to the processor swap port as 880 to provide system timing.



PROCESSOR SWAP PORT (MB1)

PROCESSOR SWAP PORT

OVERVIEW

The processor swap port controls which CPU is to be active, handles interrupt routing, and ensures proper timing of the clock circuits during the swap. To access the swap port, the CPU writes a control byte to port 0FEH. Only three bits of the byte are used: AD0 controls the interrupt mask, AD1 controls the swap interrupt line, and AD7 performs the processor swap.

PROCESSOR SWAP

Refer to schematic MB1 as you read the following.

At power up, the reset circuits clear U171-9 to logic zero. This pin, 8SEL, connects to U186-5, a 12H6 PAL. This IC responds by placing a logic zero on U187-12 and a logic one on U187-2. On the first positive transition of $\overline{85\phi}$, the 85HOLD line will go low, enabling the 8085 CPU. On the first positive transition of $\overline{88\phi}$, the 88HOLD line will go high, disabling the 8088 CPU.

The 8085, while executing the code in the monitor ROM, soon transfers control to the 8088. It does this by setting bit 7 of the processor swap port control byte to logic one. Here's how...

The CPU addresses port 0FEH to assert $\overline{\text{SWAPCS}}$ (from the I/O decoder) at U206-5. It then sets AD7 to logic one at U171-12. Finally, it asserts the write line at U206-6. As a result, U171-11 goes high and latches U171-9 to logic one. The 8SEL line is now asserted.

The values at U172-12 and U172-2 are also latched to their respective outputs, but these will be covered later.

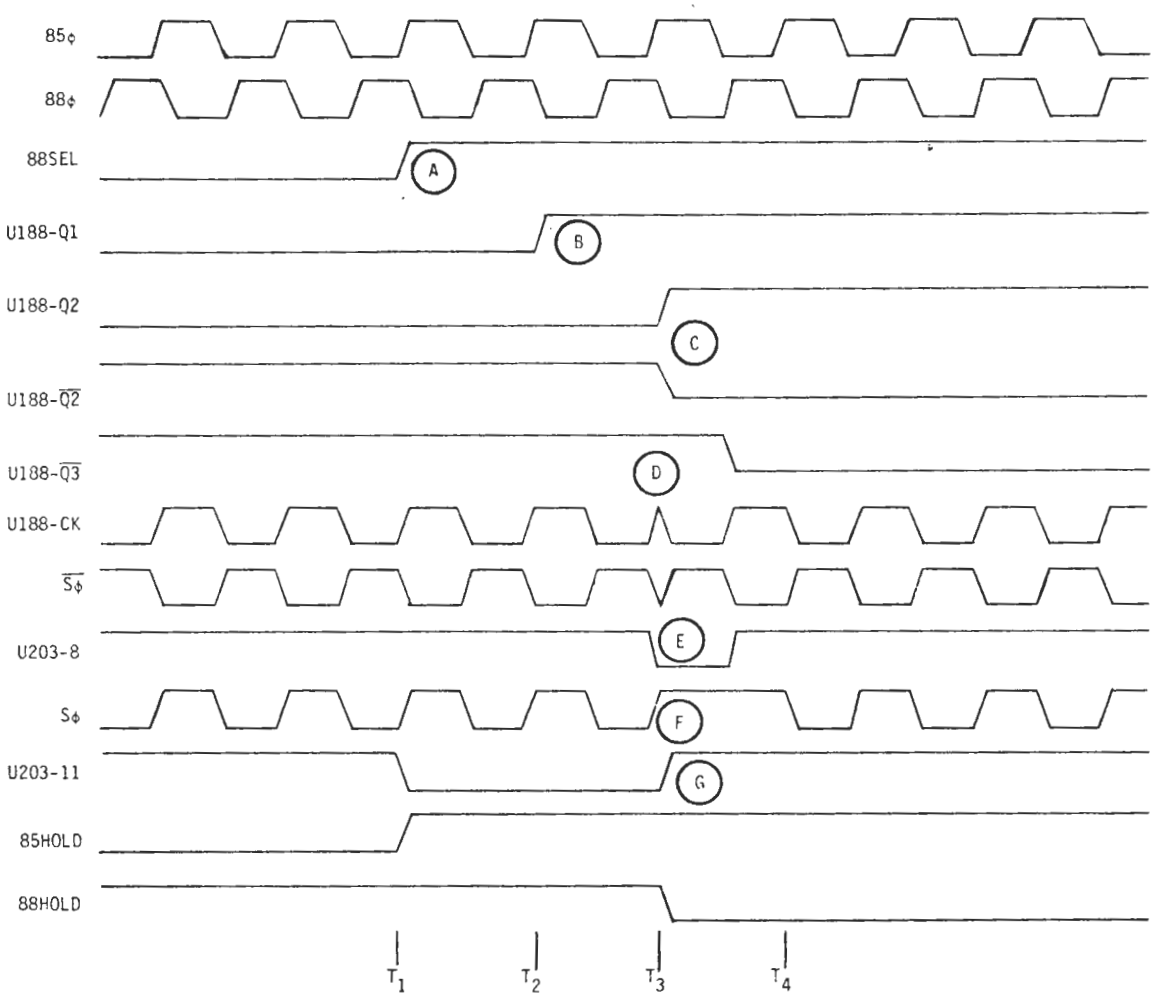
The 8SEL line, now logic one, causes U186-13 to change to logic one, U186-18 to change to logic zero, and U186-16 to change to logic one.

The HOLD* line at U185-11 asserts whenever a board on the S-100 bus takes control of the H/Z-100. This causes U186 to disable both the 8085 and the 8088 through U187. Both CPUs respond by returning their hold-acknowledge signals; the 8088 at U186-3 and the 8085 at U171-2. When this happens, U186 asserts the HAK line at pin 17. This, in turn, raises the S-100 pHLDA line to logic one at U180-9. The board that generated the HOLD* request can now take control of the H/Z-100.

SWAP TIMING

The 88SEL line also goes to U188-4, a quad D-type latch. This circuit is designed to suppress any glitches on the system clock line when the H/Z-100 switches from one CPU to the other. It also ensures that the CPU being disabled is no longer active when the other CPU is enabled.

The 8085 and the 8088 run on separate crystal-controlled clocks; the 8085 from Y101 and the 8088 from Y103. Although these clocks are stable, they aren't in phase. Switching from one clock to another can cause a glitch on the system clock line, Sϕ, which can upset the timing in other circuits.



SWITCHING FROM 8085 to 8088

To see how U188 and its associated circuits block this spike, refer to the waveforms on the previous page.

The two top waveforms are the respective clocks for the 8085 and 8088 CPUs. These are present at the inputs of inverters U200-2 and U200-14. Assuming that the 8085 is the active processor, then U200-1 is low and 85ϕ couples through the inverter to form $\overline{S\phi}$. It also couples through U225B to clock U188.

At time T1, the 8088 is selected; the 88SEL line goes to logic one as shown at A on the waveforms illustration. The next clock pulse at U188-9 latches this logic one into U188-2, the Q1 output at B.

The next clock pulse causes the Q2 output to latch high, shown at C. This tri-states U200 through the exclusive-OR gate at U203B. At the same time, $\overline{Q2}$ goes low to couple the 88ϕ clock to the $\overline{S\phi}$ line. Since, in this example, the two clocks are nearly 180-degrees out of phase, the clock immediately returns to zero, causing the spike at D in the waveforms illustration.

Up until this time, the output of U203-8, another exclusive-OR gate, has been logic one. This is because its inputs Q2 and $\overline{Q3}$ of U188 have been in opposite states. However, since Q2 went low at time T3, both inputs to U203C are the same, causing U203-8 to go to logic zero (waveform E). This forces the system clock output at U225-3 to logic one until time T4 (waveform F).

At time T4, the first positive-going edge of the 8088 clock causes the $\overline{Q3}$ output of U188 to go high. This opens the gate at U225A to pass the system clock, which is now the 8088 signal.

As mentioned earlier, the other function that 88SEL and U188 perform is to ensure that the CPU being disabled is completely disabled before the other CPU is activated. To see how this is done, again refer to the waveforms illustration.

Once again, assume that the H/Z-100 is switching from the 8085 to the 8088. At time T1, the 88SEL line goes high, which is coupled to U203-11. The other input of this exclusive-OR gate is the Q2 line from U188. Since both inputs are now the same state, U203-11 goes to logic zero to preset both HOLD latches at U187.

Both CPUs respond by going into a HOLD state and sending hold-acknowledge signals to U186; the 8088 to pin 3 and the 8085 to pin 4 through U171. This asserts HAK at pin 17 which drives the S-100 pHLDA line at U180-9.

At time T3, the $\overline{Q2}$ line goes low and U203-11 returns to logic one, thus releasing the latches at U187 from their preset states. The next $\overline{88\phi}$ clock pulse latches the logic zero at U187-2 into U187-5, removing the 8088 from the hold state.

Also at this time, U188-7 goes high to drive U215-3 high. This last IC connects to pin 21 of the S-100 bus to form the NDEF (8088) line. This line is a "not-to-be-defined" line that can be used for any function by the computer manufacturer. For the H/Z-100, this line asserts when the 8088 is active.

INTERRUPT MASK

The interrupt mask circuits ensure that interrupt requests are sent to the currently active CPU. The mask bit, MSK, is set or cleared by setting or clearing bit 0 of the processor swap port. If set, and the 8085 is active, the 8085 gets all interrupt requests. If cleared, and the 8085 is active, the interrupt request is blocked. However, the swap port will disable the 8085 and enable the 8088. If the 8088 is active, all interrupt requests are sent to the 8088 regardless of the mask bit. Here's how it's done...

Immediately after reset, the 8085 CPU is the active processor. Control lines 5SEL at U171-8 and MSK at U172-6 are logic one. These two lines connect to U225-9 and U225-10, shown near the 8085 IC on the schematic. U220-2 inverts the resulting logic zero to enable U189A and U189D. So all interrupts are sent to the 8085; maskable through U189A, non-maskable through U189D.

The 8SEL line, which is the complement of 5SEL, disables U189B and U189C, the AND gates to the 8088. Later, when the 8085 hands control to the 8088 CPU, 8SEL will go high and 5SEL will go low.

If, while the 8085 is selected, the $\overline{\text{MSK}}$ line is set to logic zero, U220-2 disables U189A and U189D. This blocks the interrupt request from both the 8085 and the 8088. However, if an interrupt request should occur, either standard or NMI, U156-6 will go high to assert the NMINT line.

The NMINT line connects to U155-9 in the processor swap port. The other input is the MSK line which is also high. As a result, U155-8 goes low to assert the 8SEL line. The H/Z-100 swaps to the 8088 processor as described previously.

When the 8088 CPU is active, 8SEL is high to enable U189B and U189C. U189A and U189D are disabled because 5SEL is logic zero at U225-9. So, no matter what the setting of the $\overline{\text{MSK}}$ bit at U225-10, all interrupt requests will be routed to the 8088 processor.

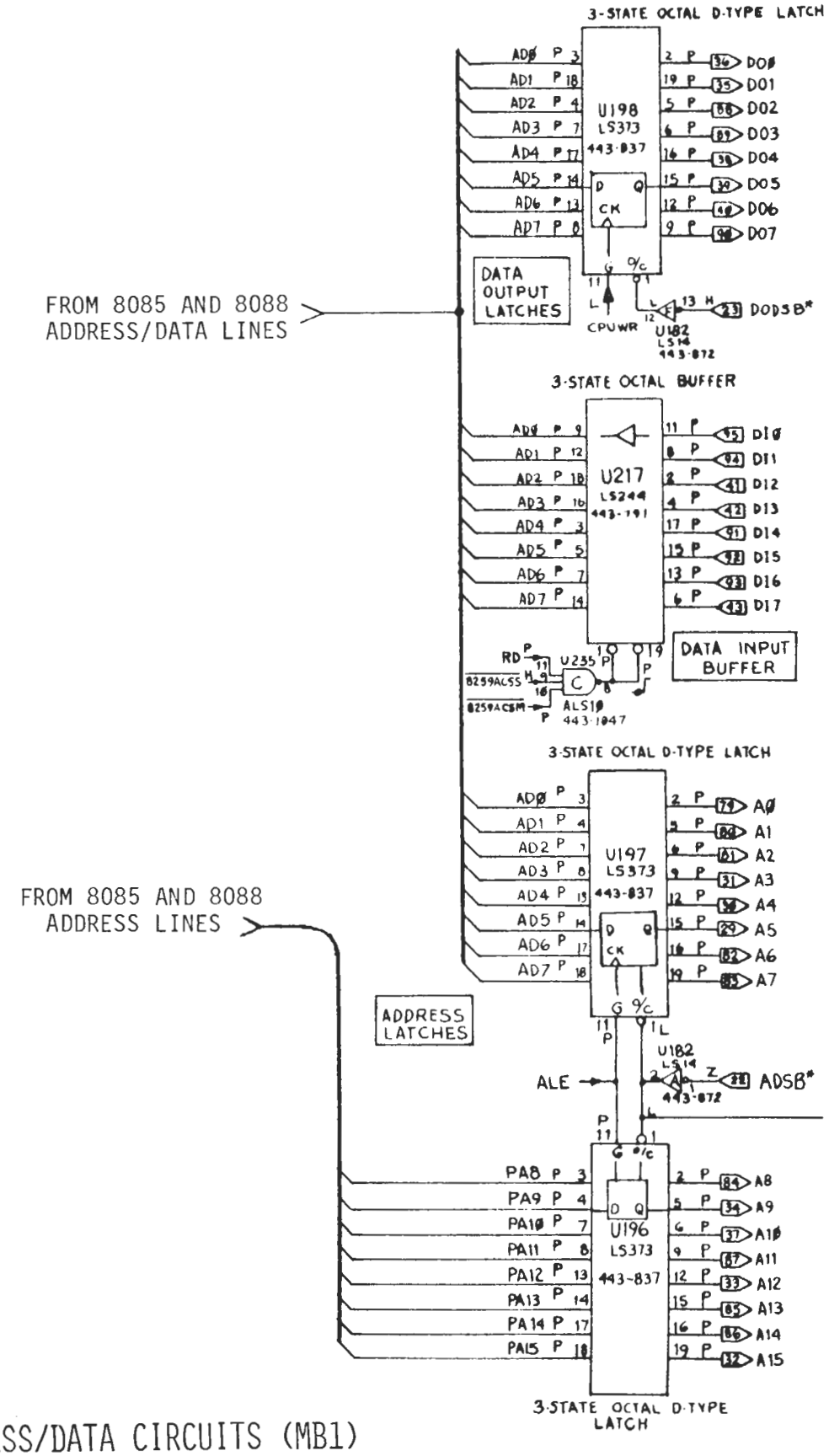
SWAP INTERRUPT

When either CPU is in the hold state, it retains the contents in its registers. So, when that CPU is again enabled, it will begin processing where it left off.

To start the disabled CPU at a different memory location than where it was when it was turned off, the active CPU can generate a swap interrupt command. The active CPU does this by selecting the proper interrupt vectors, performs an interrupt-disable upon itself (through software), and then asserts the SWAPINT line.

To generate the swap interrupt command, the computer sets bit 1 to logic one in the processor swap port. It does this by asserting $\overline{\text{SWAPCS}}$ (from the I/O decoder) at U206-5, setting AD1 to logic one at U172-12, and then asserting the $\overline{\text{WR}}$ line at U206-6. U206-4 goes high to latch U172-9 to logic one, sending the SWAPINT command to the interrupt circuits.

At the same time, the CPU also writes the correct control bits to 8SEL and MSK on the processor swap port. The H/Z-100 changes CPUs, finds that the SWAPINT line is asserted, and jumps to the correct location to process the interrupt.



ADDRESS/DATA CIRCUITS (MB1)

ADDRESS/DATA CIRCUITS

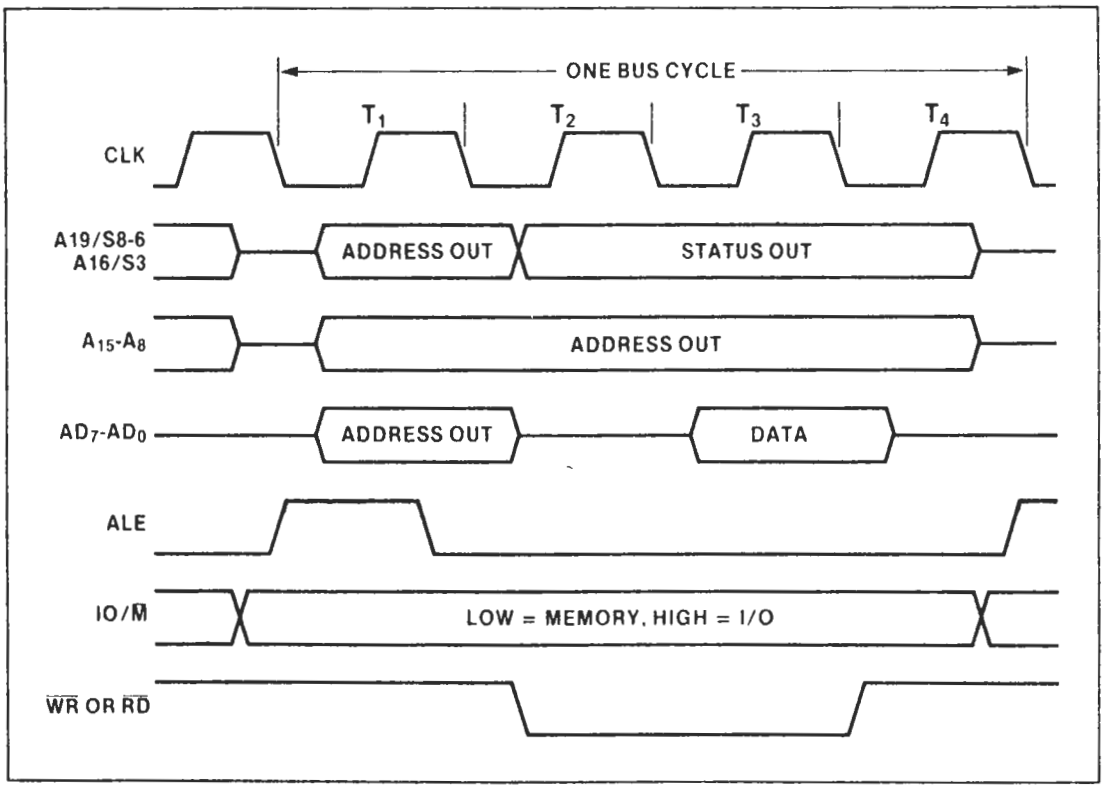
OVERVIEW

As stated in the discussions on the 8085 and the 8088, the address and data lines of these CPUs are multiplexed onto the same bus. That is, first the address is present on the bus, then the data. It's up to a control line called the address latch enable, or ALE, to separate these signals and send them to their appropriate latches.

Refer to schematic MB1 as we explain how.

Under normal operation, the CPU selection logic will enable either the 8085 CPU or the 8088 CPU. Although the address/data lines of these processors are connected in parallel, the bus of the disabled processor will be tri-stated and so will not interfere with the active CPU.

ADDRESS LATCHES



In the following description, we'll use the 8088 waveforms. Although these are slightly different than the 8085 waveforms, the description applies to both.

At the beginning of clock cycle T1, the 8088 asserts the 88ALE line at U211-25. This signal couples through the OR gate at U221-1 to pin 11 of U197 and U196, two tri-state, octal D-type latches.

A short time later, the 8088 places address data on the address lines. The lower 8 bits, AD0-AD7, go to U197 and the upper 8 bits, PA8-PA15, go to U196. These latches are transparent as long at the ALE line is high; that is, the output logic levels are the same as the input logic levels. At the end of T1, ALE goes low to latch the outputs with the address.

The line going to pin 1 of U197 and U196 provides S-100 compatibility. If an external processor or DMA device were plugged into one of the S-100 slots, and it wanted to take control of the H/Z-100, it would assert ADSB* low. This would tri-state U197 and U196, thus isolating the 8085 and 8088.

DATA LATCHES

If the CPU is writing data, either to memory or to an output port, it asserts the $\overline{WR}$ line at U211-29. This signal is inverted by U220-12 (in the center of the schematic) to form the CPUWR control signal. CPUWR connects to the data output latch at U198-11 and holds this latch transparent as long as CPUWR is high.

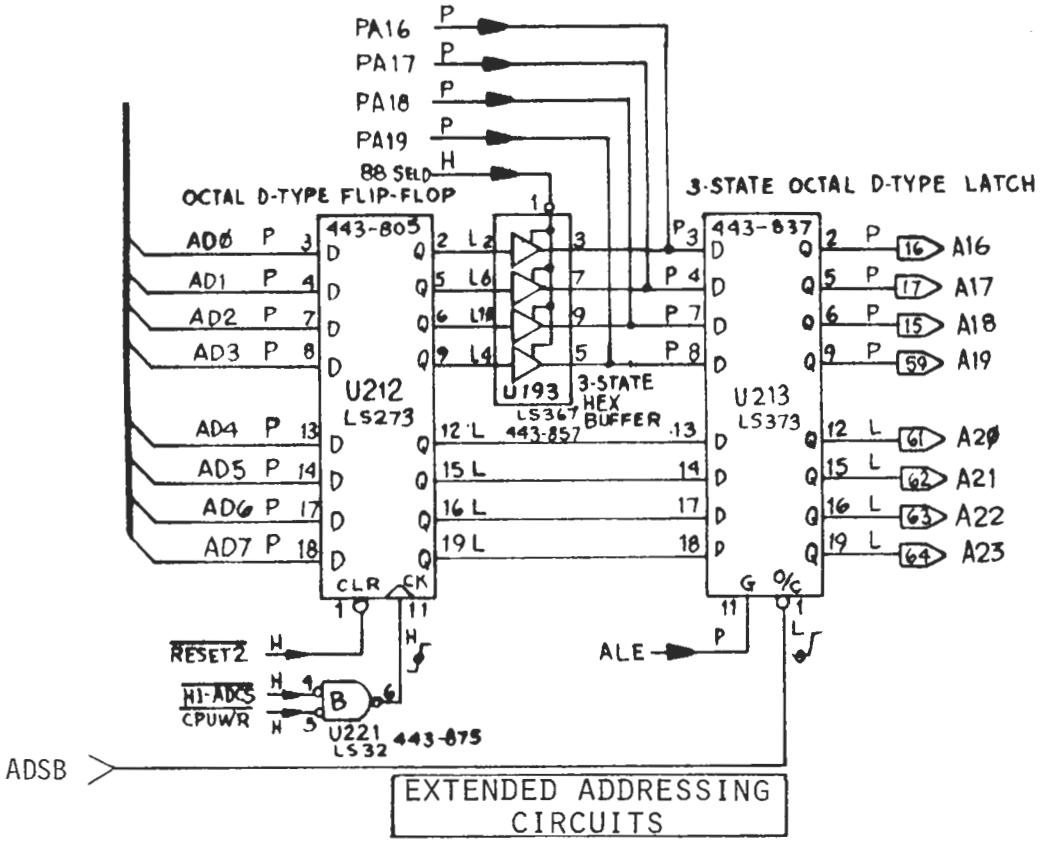
During time T3, the CPU places the data on bus lines AD0-AD7, which couple through U198 to the S-100 bus. At time T4, CPUWR goes low to latch this data onto D00-D07. From here, the data will be sent to the location pointed to by the address on the outputs of U197 and U196.

U198-1 is the inverted version of DODSB* from the S-100 bus. This signal functions in the same manner as ADSB*.

If the CPU is reading data, either from memory or an input port, its timing is the same as when it writes data. However, this time it asserts the $\overline{RD}$ line at pin 32 of the 8088. This control line is inverted by U220-4 to form RD (located near the top center of the schematic).

Control line RD connects to U235-11, a 3-input NAND gate, at the data input buffer, U217. The other two inputs to U235C, $\overline{8259ACSS}$ and $\overline{8259ACSM}$ are from the interrupt circuits and won't go low unless an interrupt occurs (see the interrupt circuit description for more details). During a data read, RD is high, so U235-8 is low, and the octal buffer, U217, passes the data on bus lines DI0-DI7 to AD0-AD7. At time T3 the CPU assumes that the data is stable and loads it into the accumulator.

EXTENDED ADDRESSING



The extended addressing circuits, U193, U212, and U213, maintain S-100 compatibility by making it possible for the CPU to address up to 16 megabytes of memory.

When the 8088 is active, 88SEL is high to tri-state U193. The 8088 extended address lines, PA16-PA19, connect to pins 3, 4, 7, and 8 of U213. When ALE asserts at U213-11, these address values are coupled to the S-100 bus. Lines A20-A23 are logic zero because the outputs of U212 have not changed from their cleared condition. In this case, the 8088 is operating normally and can directly address its natural one-megabyte range.

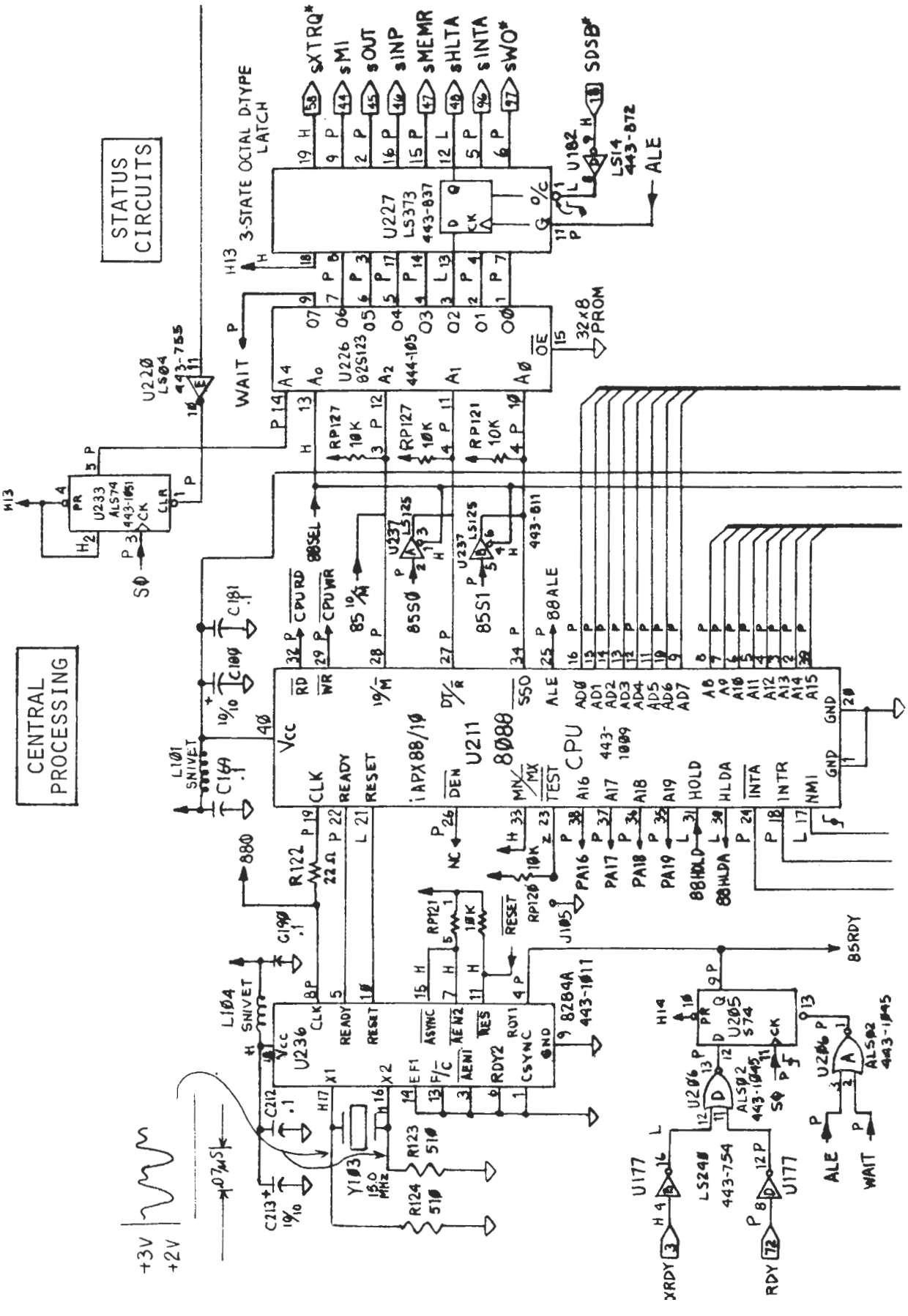
To access the address space above 1MB, the CPU asserts $\overline{\text{HI-ADCS}}$ from the I/O port decoder (U159 on MB2). Then $\overline{\text{CPUWR}}$ asserts and U221-6 goes low. Finally, the extended address is placed on lines AD4-AD7 at U212. (Lines AD0-AD5 are blocked by U193 while the 8088 is active.)

At the end of that cycle, the $\overline{\text{CPUWR}}$ line goes high and latches AD4-AD7 onto the outputs of U212.

At the beginning of the next machine cycle, when ALE again asserts, the outputs of U212 will latch into U213. For example, if U213-12 is logic one and pins 15, 16, and 19 are zero, the CPU will be in the one-megabyte to two-megabyte range.

These circuits work the same way if the 8085 is the active CPU. The only difference is that 88SEL at U193 is low so that the lower four bits of U212 couples directly to U213. This allows the 8085 to address memory between 64K and 16M. (When the 8085 is active, lines PA16-PA18 from the 8088 are tri-stated.)

Note, however, that once the CPU jumps to these higher ranges it can't return unless there is a program there to tell it to return. This is because U212 and U213 are latches and can only be changed by writing to the high-address port (or through a hard reset). One possible way around this is to preload a program in higher memory by using direct memory access.


CENTRAL PROCESSING
STATUS CIRCUITS
3-STATE OCTAL D-TYPE LATCH
U227 LS373 443-837
U233 ALS74 443-1051
U220 LS04 443-755
U226 82S123
444-105
32x8 PROM
LS14 443-872
ALE
WAIT
sXTRQ*
sM1
sOUT
sINP
sMEMR
sHLTA
sINTA
sWO*
SDSB*
CPURD
CPUWR
88SEL
8SS0
8SS1
88ALE
U211 8088 CPU
iAPX88/10
U236 8284A 443-1011
U177 LS248 443-754
U206 ALS02 443-1045
U205 S74
U182 LS14 443-872
Y1 15.0 MHz
+3V
+2V
0.7µS
BUS STATUS CIRCUITS (MB1)

S-100 BUS STATUS CIRCUITS AND WAIT TIMING

BUS STATUS

The IEEE-696 S-100 bus contains 8 status lines; these lines assert to indicate what machine cycle the computer is in. The H/Z-100 uses all but one of these lines. However, the unused line, sXTRQ*, is still available for use by plug-in boards.

Following the S-100 standard, the status lines are prefixed with a lowercase s. All but two of the lines, sWO* and sXTRQ*, assert on logic one. Briefly, here's what each status line does:

sXTRQ* Sixteen-bit request. This line allows 8-bit and 16-bit boards to share the same bus. Since the H/Z-100 is an 8-bit machine externally, and a 16-bit machine only inside the 8088, this line is disabled by connecting U227-18 to logic one.

However, if a true 16-bit CPU board is plugged into the S-100 bus, the H/Z-100 can be programmed to give control to this CPU, and this CPU can perform 16-bit transfers with other 16-bit boards on the bus.

It does this by asserting sXTRQ* and addressing the 16-bit board (U227-19 is tri-stated at this time by a high at U227-1). If the addressed device can process 16-bit words, it will assert another S-100 line called SIXTN*. Next, the data buses are ganged together; lines DO0-DO7 handle DATA0-DATA7 while lines DI0-DI7 handle DATA8-DATA15. The data transfer takes place.

If the device can't process 16-bit words, such as memory and I/O on the motherboard and video board, then SIXTN* remains high. In this case, DO and DI lines operate normally and the CPU must process the data a byte at a time.

sM1 Opcode fetch. This line asserts when the H/Z-100 fetches a new instruction from program memory. It returns to logic zero at the end of the M1 machine cycle.

sOUT Write to output port. This line asserts to indicate that the CPU is going to send data to a previously-addressed output port.

sINP Read from input port. This line asserts to indicate that the CPU is going to read data from a previously-addressed input port.

sMEMR Memory read. This line asserts to indicate that the CPU is going to read data from the addressed memory location.

sHLTA Halt acknowledge. This line asserts when the CPU processes a HALT command and has stopped executing the program.

sINTA Interrupt acknowledge. This line asserts when it is processing an interrupt.

sWO* Memory write. This line asserts when the CPU is going to write data to a previously-addressed location in memory.

These lines are derived from the status lines of whichever CPU is active. In the 8088, these lines are IO/$\overline{M}$, DT/$\overline{R}$, and $\overline{SSO}$. In the 8085, these lines are IO/$\overline{M}$, S1, and S0.

When the 8088 is active, the 88SEL line at U226-13 is logic one. This causes the 32 x 8 PROM to correctly decode the bit pattern on pins 10, 11, and 12 as an 8088 status code. As you'll see later, this code is different for the 8085.

88SEL also tri-states 85S0 and 85S1 at pins 1 and 4 of U237. The line from 85IO/$\overline{M}$ is in a high-impedance state when the 8085 is disabled, so doesn't need a buffer.

U226 decodes the machine cycle status and asserts the correct line on the output, U226-1 through U226-7. When the ALE line goes low, the outputs of U226 are latched into U227.

When the 8085 is active, the 88SEL line at U226-13 is logic zero. This causes U227 to correctly decode the bit pattern on pins 10, 11, and 12 as an 8085 status code. U226 decodes this status which is subsequently latched into U227 when ALE goes low.

The following chart shows the status codes of each CPU and what S-100 status line each code affects.

8085				8088				S-100
IO/M	S1	S0	Status	IO/M	DT/R	SSO	Status	Status
0	1	1	Opcode fetch	0	0	0	Code access	sM1
1	0	1	I/O write	1	1	0	Write I/O port	sOUT
1	1	0	I/O read	1	0	1	Read I/O port	sINP
0	1	0	Memory read	0	0	1	Memory read	sMEMR
Z	0	0	HALT	1	1	1	HALT	sHLTA
1	1	1	Interrupt Ack.	1	0	0	Interrupt Ack.	sINTA
0	0	1	Memory write	0	1	0	Write memory	sWO*

WAIT TIMING

The WAIT line at U226-9 equalizes the timing characteristics between the 8085 and 8088. It does this by adding the appropriate wait states during a memory or I/O access. The number of wait states depends on the active CPU and the type of access.

	8085 Active	8088 Active
Memory Access	1 wait state	0 wait state
I/O Access	2 wait states	1 wait state

U233-5 provides the basic wait timing. When ALE asserts, U233-5 is cleared. After ALE goes low, U233-5 will go high on the next system clock pulse. If the machine cycle is a memory or I/O access, the wait line will assert according to the above chart.

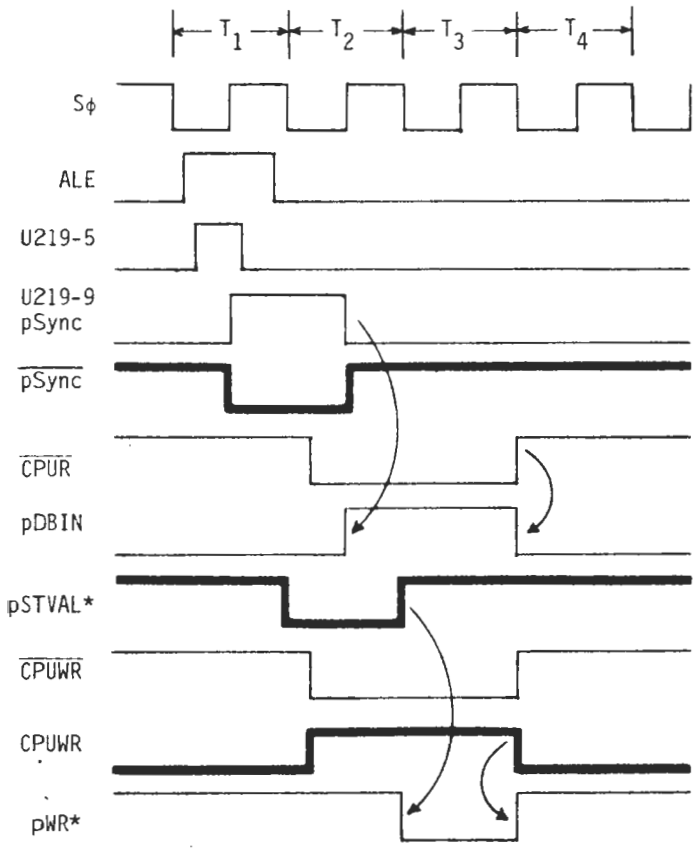
The asserted wait line is inverted by U206A to clear U205-9. This logic zero couples directly to the 8085 READY input and indirectly to the 8088 READY input through U236. The active CPU will go into a wait state until the next system clock pulse at U205-11. Operation will then proceed normally.

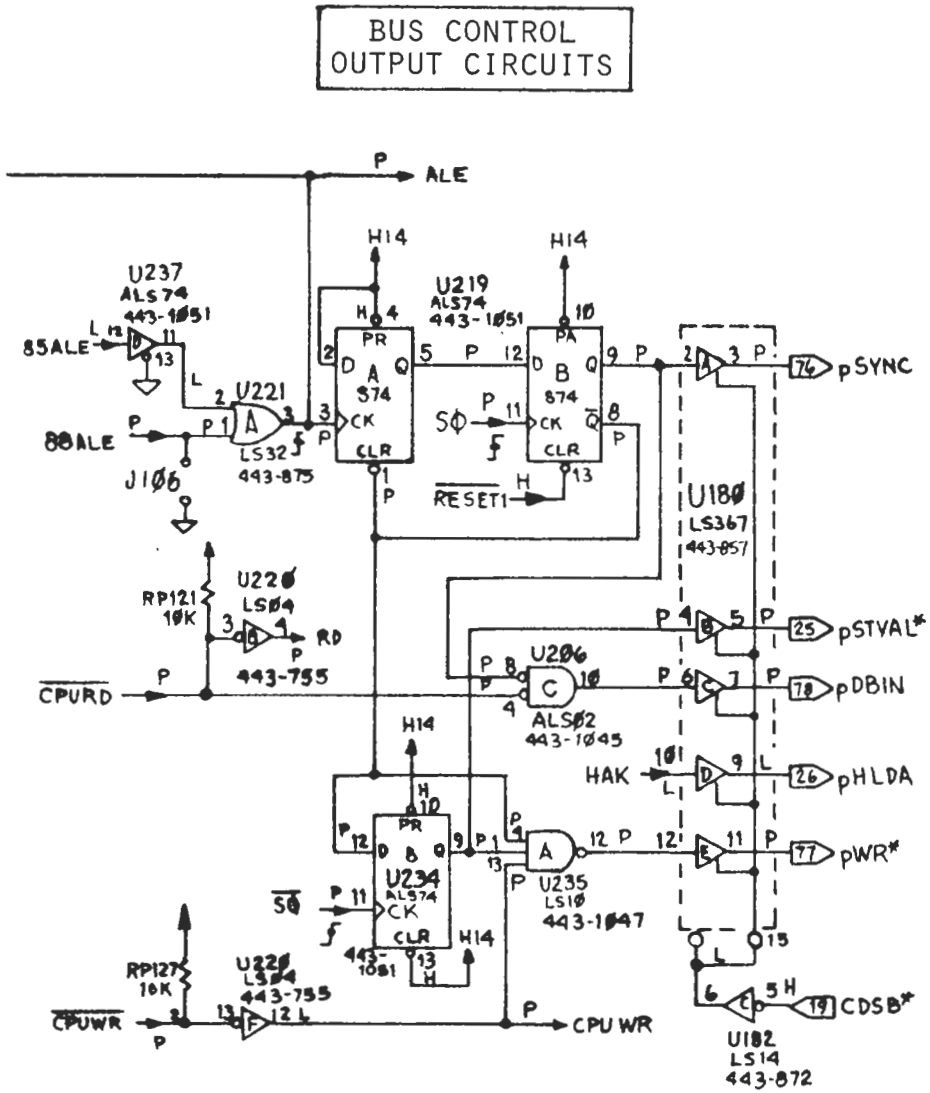
The RDY and XRDY lines are S-100 ready lines. If either line is low, the CPU will go into a wait state at the end of a machine cycle. Here's how:

The ALE line clears U205 at the beginning of each machine cycle. Both RDY and XRDY are normally logic one, which places a logic one at U205-12. Unless the wait line is asserted, the next system clock pulse will latch U205-9 to logic one; ensuring that the active CPU will not generate a wait state during that machine cycle.

If either RDY or XRDY should go low, U205-9 remains at logic zero during that bus cycle. This causes the CPU to go into a wait state at the end of the cycle. See the 8085 and 8088 specification sheets for exact timing relationships.

We'll discuss the uses of the RDY line in the H/Z-100 in the circuit descriptions on the dynamic memory, video board, and floppy disk controller board.





BUS CONTROL OUTPUT CIRCUITS (MB1)

BUS CONTROL OUTPUT CIRCUITS

The five lines of the bus control output circuits determine the timing and movement of data during any bus cycle. The mnemonics of these lines always begin with a lowercase p. Refer to the accompanying waveforms (8088 timing) and schematic MB1 as we discuss each.

pSYNC

This line goes high to indicate the start of a new bus cycle. Basically, it's the ALE signal of the currently active CPU retimed to the rising edge of the system clock.

In the 8088, the ALE line goes high at the beginning of the bus cycle. This couples through U221A to latch a logic one on U219-5. Halfway through time T1 the system clock goes high at U219-11, causing U180-3, the pSYNC output, to go high.

At the same time that pSYNC asserts, U219-8 goes low to clear U219A at pin 1.

During time T2, the next positive-going edge of the system clock latches U219-9 to logic 0; the pSYNC line is no longer asserted and U219A is no longer held cleared.

pSTVAL*

The pSTVAL* line works in conjunction with pSYNC to indicate when the S-100 address and status lines are stable.

Inverted pSYNC couples from U219-8 to U234-12 and inverted system clock connects to U234-11. Between time T1 and T2, the inverted pSYNC is logic zero. The rising edge of $\overline{S\phi}$ latches this onto U234-9, which is buffered through U180B to form the pSTVAL* signal.

On the next rising edge of $\overline{S\phi}$, between T2 and T3, the inverted pSYNC has returned to logic one; this is coupled through U234B and U180B to the pSTVAL* line.

pDBIN

This is a generalized read strobe that gates data from memory (or an input port) to the data bus.

The pDBIN signal is derived by NORing CPURD and pSYNC at U206C. This ensures that pDBIN won't assert until after the negative-going edge of pSTVAL*.

pHLDA

This is the hold acknowledge signal; it goes high when both the 8088 and the 8085 are in a hold state. Such a situation can occur if a board plugged into the S-100 bus must take control of the bus, such as when a DMA transfer is to take place.

The device requesting control of the bus asserts the S-100 HOLD* line at U185-11 (lower right on the schematic). U186-8 detects this logic zero and will write logic ones to U187-9 and U187-5. These lines send HOLD commands to the 8085 and 8088 CPUs.

In our example, the 8085 is already in a hold state, so the 85HOLD line is already high. When the 8088 CPU detects the asserted 88HOLD line, it finishes the current instruction and indicates a hold acknowledge status by asserting 88HLDA at U186-3.

Now that both 88HLDA and 85HLDA are asserted, U186-17 goes high. This line, HAK, couples through U180D to form pHLDA.

See the description on the processor swap port for more information on U186.

pWR*

This is a generalized write strobe that writes data from the data bus into memory or an output port. It's timed with pSYNC and pSTVAL* to ensure that the address lines are stable before a write takes place.

The CPU write command is inverted through U220-12 and applied to U235-13, a three-input NAND gate. The pSTVAL* line connects to pin 1 of this gate and prevents a write from taking place until the address lines are stable. The inverted pSYNC, at U235-2, ensures that a pulse doesn't occur on the pWR* line if the CPU write command should assert before pSTVAL* goes low.

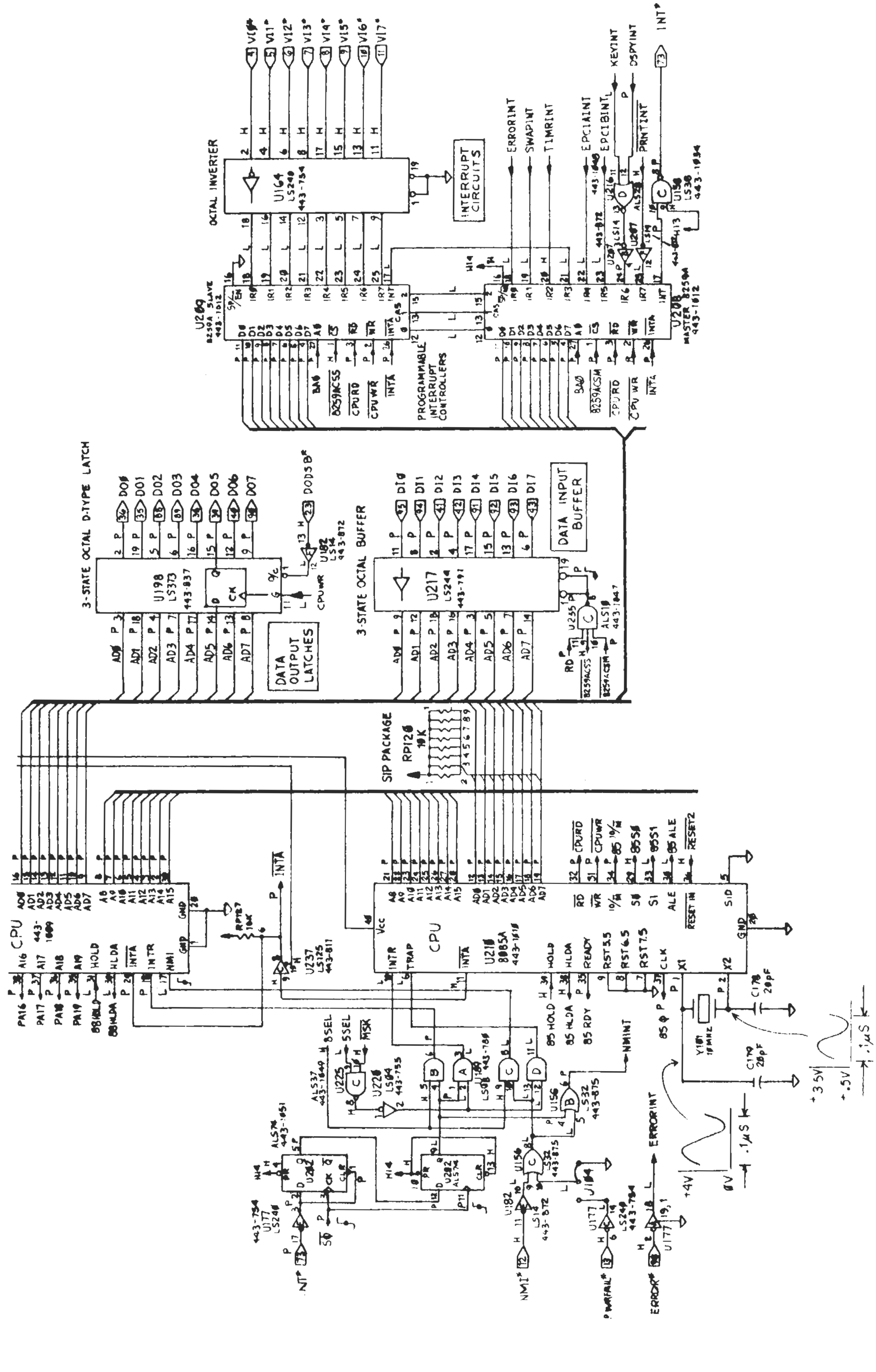
CDSB* AND MWRT

These lines are not control output lines, but are associated with them.

Asserting the CDSB* line tri-states U180 to disconnect the bus control lines. This situation can happen if another CPU board that is plugged into the S-100 bus takes control of the bus. If so, that board must supply the output control signals.

While pDBIN is a generalized write strobe for both memory and output ports, MWRT is a write strobe for memory write cycles only. In the H/Z-100, it is used in the memory refresh circuits and on the video board.

The MWRT signal is derived by NORing pWR* and sOUT (from the status circuits) at U216C. (You'll find this IC near the right side of schematic MB1.)



INTERRUPT CIRCUITS (MB1)

INTERRUPT CIRCUITS

GENERAL INFORMATION

Maskable interrupts are routed through the IC at U208, an 8259A programmable interrupt controller (PIC). This IC features an 8-level priority controller and programmable interrupt modes that, among other things, allow using this IC with either the 8085 or the 8088. Also, individual interrupt lines can be masked without affecting those above or below it. See the 8259A IC data sheets for detailed information.

Before the 8259A can be used, It must be initialized by the CPU. It does this by outputting the programming information to ports 0F2H and 0F3H for the master, and to 0F0H and 0F1H for the slave. When it accesses these ports, the I/O port decoder asserts $\overline{8259ACSM}$ for the master PIC (U208), and $\overline{8259ACSS}$ for the slave PIC (U209). In addition, it will assert BA0 to select the desired register inside the IC. Once the data to be written has settled on the data pins, D0-D7, the CPU asserts the $\overline{CPUWR}$ line at pin 2 to perform the write.

To read the status registers of the 8259A, the CPU performs the same steps as described above, except it will assert the $\overline{CPURD}$ line at pin 3.

As previously mentioned, U208 is the master PIC and handles all of the motherboard and video board interrupts. In order of priority (highest first), these interrupts are:

Level	Description
0	ERRORINT: Parity error or S-100 pin 98 (ERROR*) asserted.
1	SWAPINT: Processor swap interrupt.
2	TIMRINT: Programmable timer interrupt (Out 0 or Out 2).
3	SLAVE: S-100 vectored interrupt from the 8259A slave IC at U209.
4	EPCIAINT: Serial port A interrupt.
5	EPCIBINT: Serial port B interrupt.
6	KEYINT or DSPYINT: Interrupt from the keyboard or the slave circuits.
7	PRINTINT: Interrupt line from the printer port.

MASKABLE INTERRUPT SEQUENCE

Whenever one or more of the interrupt lines goes high, U208 evaluates its priority and sends an interrupt request to the CPU through U158-8. The 8259A will also assert the INT* line if the CPU is currently processing a lower-priority interrupt.

Assume that a master interrupt has occurred; that is, one of the interrupt lines other than U208-21 has been asserted. How the CPU responds to the interrupt depends on whether the 8085 or the 8088 is active.

If the 8085 is active, the following sequence will occur:

-- The CPU asserts the $\overline{\text{INTA}}$ line at U208-26.

-- U208 places the 8080/8085 CALL instruction (0CDH) onto the data bus at pins 4 through 11.

-- The 8085 decodes this call instruction and determines that it requires two more bytes to complete the instruction. So it sends two more $\overline{\text{INTA}}$ signals to U208.

-- When U208 receives the second $\overline{\text{INTA}}$, it sends the low byte of the vector address to the CPU. When it receives the third $\overline{\text{INTA}}$, it sends the high byte of the vector address to the CPU. (The vector addresses must be programmed into the 8259A during the initialization process.)

-- After saving the current address in stack, the CPU jumps to the address supplied by the 8259A to process the interrupt. When it finishes, the CPU returns to the location saved in stack and continues the program it was processing before interruption.

When the 8088 CPU is active, the 8259A responds somewhat differently to an interrupt acknowledge.

-- The CPU asserts the $\overline{INTA}$ line at U208-26; the 8259A will not respond at this time.

-- The CPU again asserts $\overline{INTA}$ on the next machine cycle.

-- The 8259A places a byte on D0-D7 that represents the interrupt type. The interrupt type is an 8-bit number that depends on which interrupt line is causing the interrupt.

-- The CPU multiplies the type number by four to find the correct location in the vector table. This is a reserved section in memory that stores the addresses of the interrupt service programs. See the "iAPX 88 Book" by Intel Corp. for more detail.

-- The CPU saves the current address in stack and loads the addressed vector table data into the code segment register and instruction pointer. It then processes the service routine pointed to by these registers.

-- When done, the CPU returns to the program that it was processing before the interrupt took place.

The slave PIC at U209 processes the S-100 vectored interrupt lines. If one of these lines is asserted, U209-17 goes high to cause a level-3 interrupt at U208-21. This, in turn, sends an interrupt request to the CPU through U158C. When the CPU responds, it asserts pin 26 of U208 and U209.

This time, the master does not place the vector information onto the data bus. Instead, it enables U209 through the cascade lines at pins 12, 13, and 15. U209 then places the vector information onto the bus.

If no interrupt request is present at the time the CPU sends its first $\overline{INTA}$ signal (i.e., the request duration was too short) the 8259A will issue a level-7 interrupt. Both the vectoring bytes and the cascade lines will look like a level-7 interrupt was requested.

NON-MASKABLE INTERRUPT SEQUENCE

The non-maskable interrupt is an interrupt request that can't be blocked by software. When the rising edge of the NMI pulse is present at the CPU, the processor must finish its current instruction and service the interrupt request.

The NMI circuits consist of U156C, U156B, and surrounding components. There are two signals that couple to these circuits, NMI* and PWRFAIL; both from the S-100 bus.

NMI* is a general S-100 bus non-maskable interrupt line. It can be used by S-100 boards to signal the CPU of a catastrophic event, such as imminent loss of power, memory error, or bus parity error.

PWRFAIL* is a dedicated line that asserts if system power failure is imminent. If asserted, the line must stay low until the POC* (power-on clear) line is activated. This line is tied to logic one through a 4.7-kilohm resistor on the S-100 bus. Both hardware and software must be provided to use PWRFAIL*. PWRFAIL* can be selected or disabled by the jumper at J104.

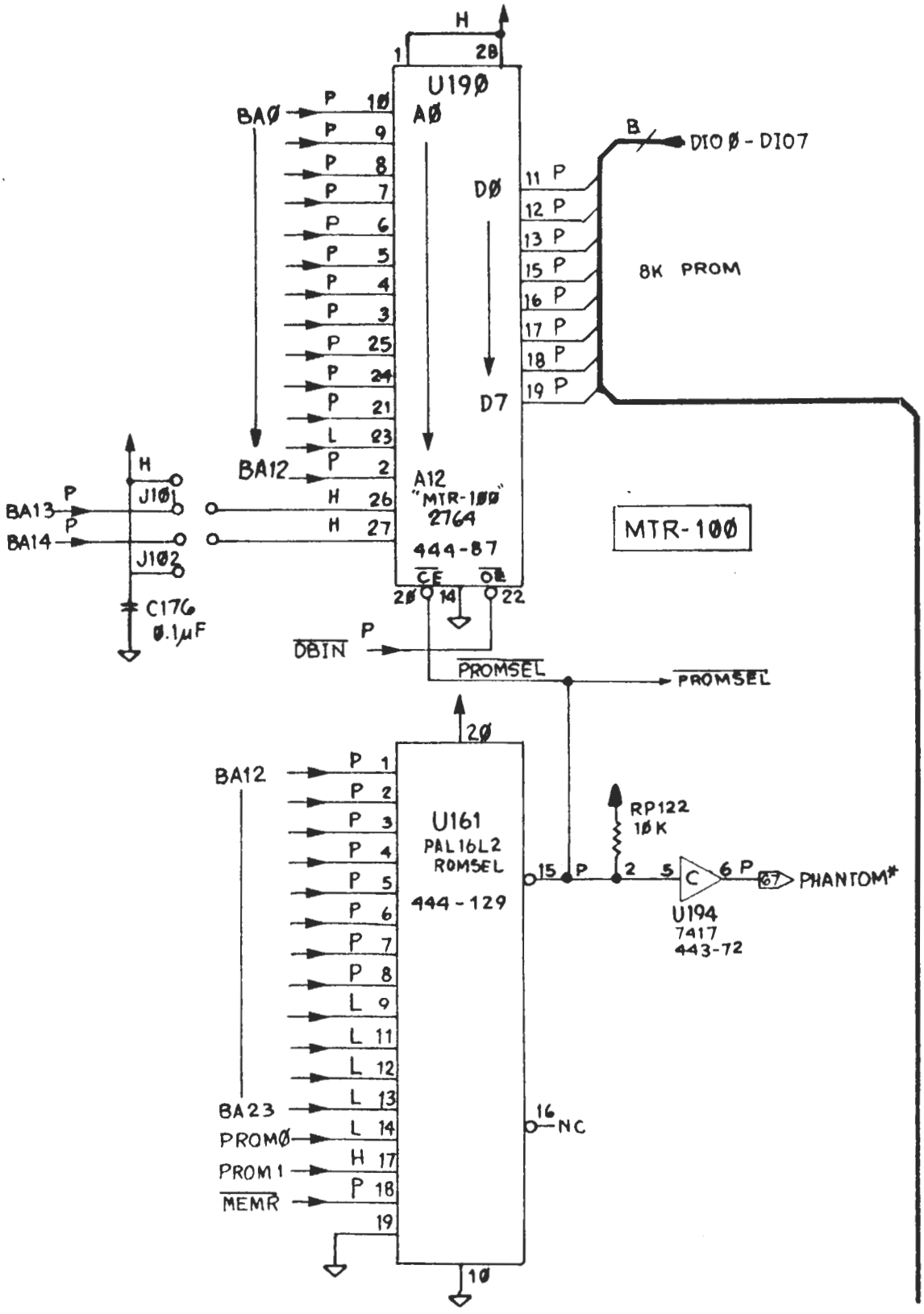
INTERRUPT ROUTING

The dual-D flip-flop at U202 retimes the maskable interrupt and applies it to U189A and U189B. If the 8085 is the active CPU, U189A couples the interrupt request to U210-10. If the 8088 is active, U189B routes the request to U211-18.

If an NMI occurs while the 8085 is active, U189D sends it to the TRAP input at U210-6; while if the 8088 is active, U189C sends the interrupt to U211-17.

If either an interrupt request or an NMI occur, U156B asserts the NMINT line. This works in conjuntion with the interrupt mask bit (MSK) in the processor swap port to force the 8088 into the active state. If MSK is low, or NMINT is low, then NMINT has no affect; if MSK is high, and NMINT is high, then NMINT disables the 8085 and enables the 8088.

See the description of the processor swap port for more details.



SYSTEM MONITOR (MB2)

SYSTEM MONITOR

ADDRESSING

The monitor ROM, U190, controls the operation of the H/Z-100 after power-up reset or hard reset. It initializes the necessary I/O ports and determines which CPU will be active in the monitor mode. Though currently 8K, jumpers J101 and J102 allow expanding this ROM to 32 kilobytes.

Whenever the CPU fetches an instruction from the ROM, it asserts $\overline{\text{DBIN}}$, pin 22, the inverted S-100 pDBIN line. This line comes from U195-16.

Accessing the monitor also asserts $\overline{\text{PROMSEL}}$ at U161-15. This IC changes the memory address that the monitor ROM responds to; effectively repositioning the ROM in memory. When $\overline{\text{PROMSEL}}$ is asserted, it enables U241 on schematic MB4. U241 couples the data from U290 to the CPU.

Here's what happens...

After power-up or a hard reset, the memory control latch at U176 is cleared by the reset line at pin 1. This places lines PROM0 and PROM1, U161-14 and U161-17, at logic zero.

when both PROM0 and PROM1 are zero, U161-15 asserts whenever the memory read line asserts at U161-18, no matter what the address. Effectively, the monitor appears to be in all of the address locations.

After a reset, the 8085 CPU is selected by the swap circuits and the 8088 is disabled. The program counter of the 8085 starts fetching op-codes starting at address zero in U190. The monitor causes the CPU to switch itself off and activate the 8088 (to see how this is done, see the "CPU Selection Logic" circuit description).

When the 8088 is in control, its program counter starts fetching monitor instructions from memory address FFFF0H, 16 bytes below the top end of the 1 megabyte address space. However, this is okay since the ROM still appears to be in all of address space.

The 8088 selects the next operating mode by latching PROM1 to logic one and leaving PROM0 at logic zero. U190 is now located in the top 8K of the 8088's natural 1 megabyte address space. This is the location that the ROM is normally in while the H/Z-100 is in the monitor mode.

Two other options are available: (1) If PROM0 = 1 and PROM1 = 0, then the ROM is effectively placed at the top 8K of every 64K page of memory. This is useful for the 8085 which has only a 64K natural address space. (2) If PROM0 = 1 and PROM1 = 1 then the ROM is disabled.

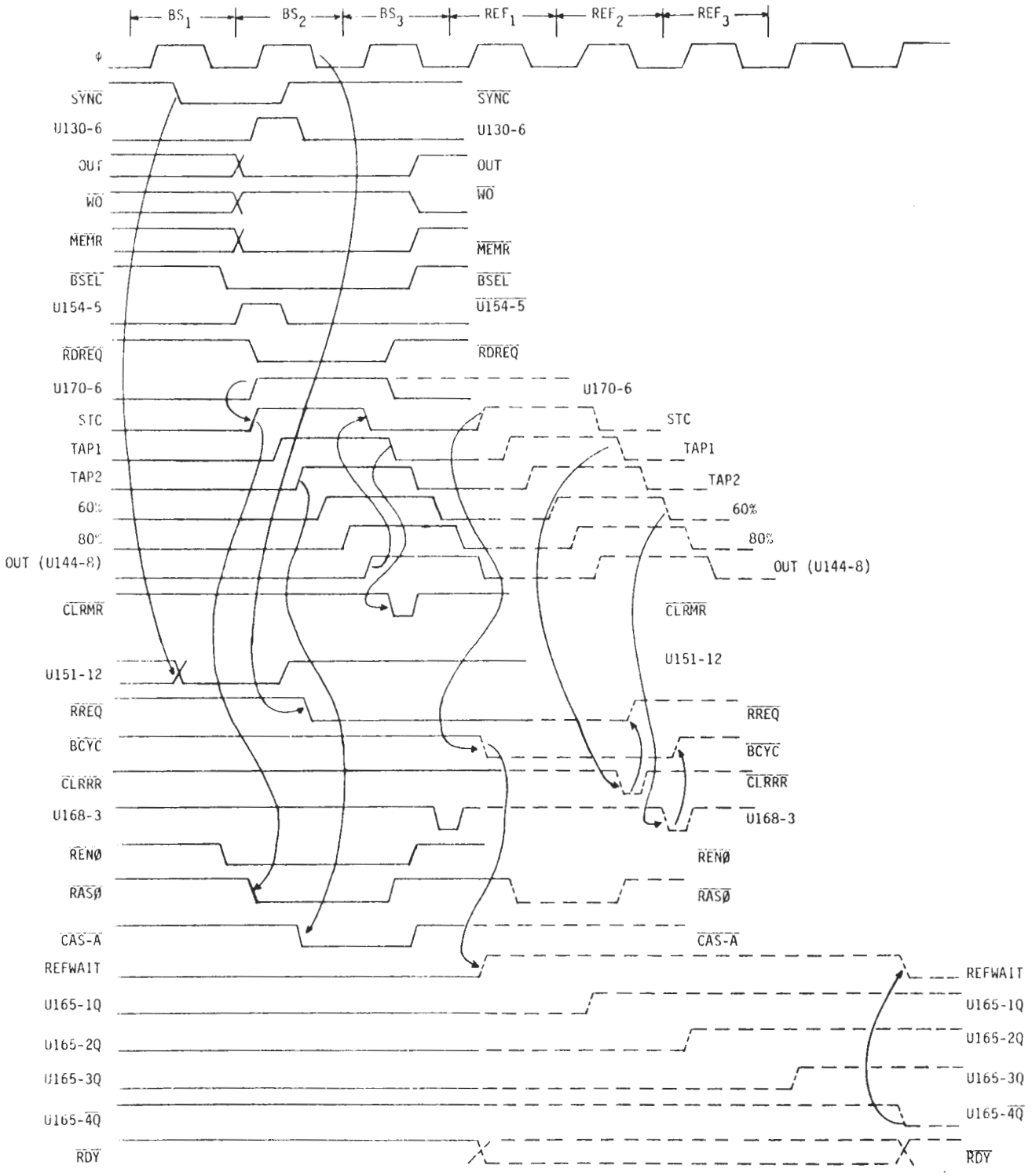
To select one of the above four options, the CPU must output a data byte to port 0FCH, the memory control latch. Data bit D2 directly affects PROM0 and D3 affects PROM1.

PHANTOM*

The $\overline{\text{PROMSEL}}$ line from U161 also connects to U194-5, an open collector buffer that connects to the PHANTOM* line on the S-100 bus. The PHANTOM* line allows overlapping blocks of memory on the S-100 bus. When properly decoded, the PHANTOM* line will disable one block of memory while enabling another.

In this case, whenever the monitor is selected by PROMSEL, the PHANTOM* line goes low and all RAM locations are disabled. Thus, when both PROM0 and PROM1 are zero at power-up, the CPU reads from ROM, but writes to RAM.

Since you can disable the monitor by raising both PROM0 and PROM1 to logic one, it's possible to have continuous read/write memory from address zero to the top end of 16 megabytes (technology permitting). However, you would have to supply your own monitor routine.



MEMORY CIRCUITS WAVEFORMS:
READ MEMORY AND REFRESH CYCLES (MB3)

DYNAMIC MEMORY

OVERVIEW

Refer to schematic MB3 as you read the following.

The dynamic memory consists of five major circuits: (1) the memory itself, which can be 64K, 128K, or 192K; (2) the address multiplexer, used to convert the 16-bit address bus to the 8-bit address bus required by the dynamic RAMs; (3) the memory map decoder, used to select the correct 64K bank of memory within 192K; (4) the refresh circuits, used to keep RAM from "forgetting" the data stored in memory; and (5) the parity circuits, which can send an error signal to the CPU if the incorrect byte is at the addressed memory location.

DYNAMIC RAM

The H/Z-100 uses 6665/TMS4164 64K x 1 bit dynamic RAMs for main memory. These ICs are upward-compatible with the 4116 16K chips and the 6633 32K memories. There is one IC per bank per bit position, so that 8 ICs make up 64 kilobytes. For the first 64K bank, U109 = MD0 and U102 = MD7.

Three sets of these RAMs make up the 192K address space:

U109-U102 = 1st 64K
U125-U118 = 2nd 64K
U145-U138 = 3rd 64K

To read or write memory, the address circuits select the correct RAM location by placing the lower 8 bits of the address onto lines MA0-MA7. One of the three RAS lines, 0-2, asserts to latch this address into RAM. The upper 8 bits of the address is placed onto MA0-MA7. After waiting a short time for the lines to settle, the CAS lines assert to latch the byte at MD0-MD7 into RAM.

If reading memory, pin 3 of all the RAM chips are logic one. This places the addressed data onto pin 14 of each RAM chip. U110-12 then enables U133 to couple this data to the S-100 bus and to the CPU.

If writing memory, the CPU enables U132 at pins 1 and 11. U132 couples the data from the S-100 bus to pin 2 of each RAM chip. U110-13 asserts WE at pin 3 of each RAM chip to latch the data into the addressed memory location.

ADDRESS MULTIPLEXER

The address multiplexers consists of U146 and U128. These ICs couple the lower 8 bits of the 16-bit address bus to MA0-MA7 during RAS time. They next pass the upper 8 bits during CAS time. Multiplexing permits keeping the pin count down on the RAM ICs.

When the CPU starts to access memory, line TAP1 is logic zero. This couples the A inputs of the multiplexer to the Y outputs at MA0-MA7. These lines now hold the lower 8 bits of the 16-bit address bus. U110, in the memory map circuits, generates a $\overline{RAS}$ signal to latch this address into RAM.

Forty nanoseconds later, TAP1 goes high. This couples the B inputs of the multiplexer to MA0-MA7; these are the upper 8 bits of the address.

Forty nanoseconds after TAP1 is asserted, TAP2 at U110-5 goes high. This clocks MA0-MA7 into the CAS latches. See the description of the refresh circuits for more detail on TAP1 and TAP2.

Another line going to the multiplexers is $\overline{BCYC}$. This line is low to indicate that a bus cycle is taking place. The memory is going through a bus cycle whenever the CPU is accessing the memory. BCYC asserts pin 15 of each multiplexer IC to activate their outputs.

If a memory refresh is taking place, $\overline{BCYC}$ is high and tri-states the multiplexers. At the same time, it activates the outputs of U126, part of the refresh address generator. U126 places a refresh address on MA0-MA7. All three RAS lines assert to refresh the same location in each 64K bank.

If the CPU attempts to read or write memory during refresh, the refresh circuits place the CPU into a wait state until refresh is complete. See the refresh circuit description.

MEMORY MAP DECODER

The memory map decoder is made up of U111, U110, and U173. It performs three major functions: (1) decodes the address bus to select the correct 64K bank. (2) provides read/write control lines for the RAM and the data bus. (3) performs correct addressing and control during refresh (this will be covered in the refresh circuit description).

Here's how it does it...

U111 selects the correct 64K bank for any memory address below 192K. The address is determined by the map select lines and BA16 and BA17. We'll cover the map select lines later. For now, assume the standard configuration (MAPSEL0 = 0, MAPSEL1 = 0; contiguous RAM from 0 to 192K).

Under normal operation, BA16 and BA17 will select the banks as follows:

BA17	BA16	Condition
0	0	0 to 64K, $\overline{\text{REN0}}$ asserted.
0	1	(64K+1) to 128K, $\overline{\text{REN1}}$ asserted.
1	0	(128K+1) to 192K, $\overline{\text{REN2}}$ asserted.
1	1	U111 disabled.

The last condition is necessary because BA17 will allow addressing up to 256K. Since there isn't any on-board RAM between 192K+1 and 256K, U111 must be disabled. However, this doesn't prevent filling this memory range with a 64K board on the S-100 bus.

Also, U111 is disabled if the CPU addresses a location above 256K. In this case, the $\overline{\text{DECODEN}}$ line at pin 14 goes high to place all of U111's outputs to logic one. $\overline{\text{DECODEN}}$ is controlled by U173 and will be discussed later.

$\overline{\text{BSEL}}$, at U111-9, asserts whenever $\overline{\text{REN0}}$, $\overline{\text{REN1}}$, or $\overline{\text{REN2}}$ asserts. This line is used in the refresh circuits and will be discussed later.

The three row-enable lines connect to pins 1, 2, and 3 of the PAL at U110. This IC decodes these, and other inputs, to assert $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and MDGATE at the appropriate times.

Basically, $\overline{RAS}$ asserts under the following Boolean conditions (* = AND, + = OR):

$$\overline{RASn} = (RENn*TAP1) + (RENn*STC*RREQ) + (BCYC*TAP1)$$

While CAS asserts when:

$$\overline{CAS\text{-}A} = \overline{CAS\text{-}B} = \overline{CAS\text{-}C} = (\overline{BCYC*TAP2*WO}) + (\overline{BCYC*TAP2*PHANTOM})$$

The PHANTOM line permits placing other memory devices into the same address space as the dynamic RAM. When PHANTOM is asserted, the CPU can access the alternate memory device without disturbing the on-board memory. For CAS, in the read mode, the addressed memory location will be placed on the memory outputs, but will not reach the S-100 bus. This is because $\overline{DIEN}$ will be logic one on U133-1, tri-stating this buffer. During memory write, PHANTOM prevents $\overline{WE}$ from asserting, causing a dummy read cycle.

Refer to the memory circuits timing diagram as we discuss the basic timing cycle.

Assume that the CPU is addressing a location in the first 64K of memory. STC goes high during bus cycle 2; TAP1 = 0 so the logic 0 on $\overline{RENO}$ couples to U110-19, $\overline{RASO}$. The lower 8 bits of the address is latched into RAM ICs U102-U109.

Forty nanoseconds later, TAP1 goes high. This line causes the address multiplexers to place the upper 8 bits of the address onto lines MA0-MA7.

In another 40 nS, TAP2 goes high, causing the CAS lines to assert. The 40-nS delay ensures that the address on MA0-MA7 has had time to settle. Since the 0-64K bank is the only one previously loaded by $\overline{RASO}$, $\overline{CAS\text{-}A}$ latches the upper 8 bits of the address into U102-U109. The other two banks aren't affected by $\overline{CAS\text{-}B}$ and $\overline{CAS\text{-}C}$.

The memory location pointed to by the address is now written to or read from by the CPU.

The two remaining outputs of U110 are the write-enable line at pin 13 and the memory data gate at pin 12. Write-enable asserts whenever there's a memory write during a bus cycle at TAP1 or TAP2 time. MDGATE asserts when TAP1 or BCYC is asserted. It blocks data from the S-100 bus during a memory write or a refresh operation.

The PAL at U173 is the final IC in the memory map decoder circuits. This IC provides an enable line to U111 (DECODEN), an enable line to U133 (DIEN), and two reset lines to the refresh circuits (CLRRR and CLRMR).

DECODEN, at U173-17, is normally low for CPU accesses to any memory locations below 256K. If above 256K, one of the extended address lines (BA18-BA23) will be low and cause DECODEN to be high. This, in turn, forces all of the outputs of U111 to go high.

DIEN, at U173-14, enables the outputs of U133 during a memory read to send the addressed data to the CPU. This line goes low when DBIN = 0, MDENB = 1, and PHANTOM = 0. MDENB asserts whenever the CPU is accessing the dynamic RAM; this will be discussed later. PHANTOM and DBIN are the inverted versions of the S-100 signals, PHANTOM* and pDBIN.

CLRRR, from pin 16, is the clear refresh request. This line resets the refresh request circuits at the end of a memory refresh cycle. This line asserts when TAP1 = 0, TAP2 = 1, and BCYC = 0. See the description of the refresh circuits for more detail.

CLRMR, from pin 15, is the clear memory request line. This signal clears the memory request circuits at the end of a CPU memory read or write cycle. It asserts when TAP1 = 0, TAP2 = 1, and BCYC = 1. See the description of the refresh circuits for more detail.

REFRESH CIRCUITS

The refresh circuits consists of a refresh clock, U147 and U148; the refresh request circuit, U152; memory request, U167; timing and control, U149 and U150; control circuits to the CPU, U168 through U158, U150, and U165; and the refresh address generator, U127 and U126.

These circuits refresh the memory when the CPU isn't accessing RAM. This is necessary because it is a characteristic of dynamic RAM to lose the contents of its memory if not accessed one every 2 mS (approximately).

The refresh circuits contain arbitration logic. If the refresh circuits generate a refresh while the CPU is accessing memory, it waits until the CPU is done before gaining control of the RAM. If the CPU attempts to access memory during a refresh operation, the refresh circuits put the CPU into a wait state until refresh is complete.

Also, the refresh circuits provide timing for RAS, CAS, BCYC, and other memory functions for both refresh and CPU operation.

Here's how it does it...

U147, a 16-uS oscillator, generates the refresh clock. The first negative-going pulse latches U148-5 to logic one; starting the refresh request. The signal at U168-11 retimes the refresh request to the system clock.

The logic one from U148-9 connects to U151-2. Two other lines to this gate must go to logic one before the refresh request can take place. The start-write ($\overline{\text{STWRT}}$) line in the memory request circuits, and the $\overline{\text{SYNC}}$ line from the S-100 bus. If either line is low, then the CPU is about to perform a memory write, or the start of a bus cycle is taking place. As a result, U151-12 stays at logic zero and a refresh request doesn't take place.

If $\overline{\text{STWRT}}$ and $\overline{\text{SYNC}}$ are high, then Sϕ latches U152-5 to logic one, causing a refresh request.

However, the memory circuits will not acknowledge this request if the CPU is executing a memory read cycle. This is because U149 and U150 time the signal so that BCYC (bus cycle active) at U150-9 can't change to its $\overline{\text{BCYC}}$ state until memory read is completed. You'll see how shortly.

If, however, no memory read or write is taking place during the refresh request, the logic zero at U150-12 will be latched into U150-9 on the next positive-going signal from U169-3. The signal from U169-3 is generated by the delay line at U149 and will be explained in more detail later.

BCYC, now logic zero, tri-states the address multiplexers, U146 and U148, and places the refresh address generator, U127 and U126, onto MA0-MA7. To allow the refresh address generator time to stabilize, U149 delays asserting TAP1 by 40 nS.

Since BCYC is low, U110 in the memory mapping circuits recognizes that this is a refresh cycle. When TAP1 goes high, all three $\overline{\text{RAS}}$ lines assert. This refreshes the entire row, pointed to by U126, in each bank.

If the CPU attempts to access memory at this time, the logic circuits at U150 through U158 will put the CPU into a wait state. When refresh occurred, $\overline{\text{BCYC}}$ went high to latch U150-5 to logic one. REFWAIT stays asserted for 4 clock cycles and is then cleared by a low at U150-1.

If the CPU attempts to write or read memory, then $\overline{\text{MEMWR}}$ or MEMR will assert at pins 10 and 9 of U170. $\overline{\text{BSEL}}$, at U130-12, is also asserted because the CPU has asserted $\overline{\text{REN0}}$, $\overline{\text{REN1}}$, or $\overline{\text{REN2}}$ at U111. Since pins 4 and 5 of U169 are both logic one, then MDENB asserts.

With both MDENB and REFWAIT high, RDY goes low and the CPU goes into a wait state until the refresh cycle is finished; i.e., when REFWAIT goes low.

Incidentally, MDENB asserts only when the CPU is attempting to access the on-board dynamic RAM. If the CPU is accessing a memory board on the S-100 bus, it won't affect the logic shown on schematic MB4, so there's no need to put the CPU in a wait state during refresh.

To get an idea of timing relationships, refer to the memory circuits waveforms and schematic MB4 as you read the following.

Assume that a memory read to an address in the 0-64K range takes place. U154-5 goes high during BS2 because $\overline{\text{MEMR}}$, $\overline{\text{BSEL}}$, and $\overline{\text{SYNC}}$ are asserted. pSTVAL* asserts shortly afterward to clock U167-6, $\overline{\text{RDREQ}}$, to logic zero. U169-2 is logic one, and because U149-8 is zero, U169-1 is 1.

This asserts STC and causes U110-19, RAS0, to assert. The lower 8 bits on MA0-MA7 are loaded into the RAM's row address latches.

STC also drives U149, a 200-nS delay line with 40-nS taps. TAP1 asserts 40 nS after STC and causes U146 and U128 to place the upper 8 bits of the 16-bit address onto MA0-MA7. Forty nanoseconds after that, TAP2 asserts and causes $\overline{\text{CAS-A}}$ to assert at U110-16. Since this is a read cycle, U110-13 is logic one, so ICs U102-U109 places the addressed data onto pin 14 of each IC--this data is sent to the CPU through U133.

After TAP2 asserts, the delay line asserts outputs 60%, 80%, and OUT at 40 nS intervals. When OUT goes high, it drives STC low through U166E and U169-1. Forty nanoseconds later, TAP1 goes low to generate a clear memory request pulse ($\overline{\text{CLRMR}}$ = $\overline{\text{TAP1}}$*TAP2*BCYC).

$\overline{\text{CLRMR}}$ clears U167 to drive U170-6 low, as shown on the solid line on the memory circuits waveforms.

The read cycle is finished; a write cycle would operate in the same manner.

Now, assume that a refresh request occurs during the read cycle previously discussed. U148-9 in the request circuits latches high. Also, U151-13 is high since this isn't a write operation. However, $\overline{\text{SYNC}}$ at U151 is low during the first part of the bus cycle, so U151-12 is low.

When $\overline{\text{SYNC}}$ goes high, U151-12 goes high and U152-5 (RREQ) goes high on the next system clock pulse (end of BS2 on the waveforms). $\overline{\text{RREQ}}$ goes low and holds U170-6 high at the end of the read cycle. This is shown as the dashed line in the memory circuits waveforms.

The low forced on STC by OUT ripples through the delay line and forces STC high during time REF1. This clocks $\overline{RREQ}$ into U150-9, driving BCYC to logic zero. In turn, $\overline{BCYC}$ tri-states the address multiplexer and places the contents of the refresh address generator onto MA0-MA7.

When TAP1 goes high, all three $\overline{RAS}$ lines assert to refresh memory as described previously.

The RAS lines return high at the end of TAP1 time and U173 asserts the clear refresh request line (CLRRR = TAP1*TAP2* BCYC). This resets U148 and U152 in the refresh request circuits.

$\overline{CLRRR}$ also increments the refresh address generator at U127-1.

Meanwhile, as the logic one ripples through the delay line (shown in dotted lines on the waveforms), the 80% tap is ORed with the inverted 60% tap to pulse U168-3 at time REF3. This places a logic one on U150-9 to restore normal bus cycle operation.

The bottom waveforms show what takes place in the ready circuits during a refresh operation.

At the start of a refresh cycle, $\overline{BCYC}$ goes high to clock REFWAIT high. The system clock at U165-9 clocks REFWAIT through U165-1Q, -2Q, -3Q, to -4Q; clearing REFWAIT at U150-1.

The four clock periods that REFWAIT is high mark the time required for the refresh circuits to activate, refresh the memory, and return to their quiescent states.

As described before, if the CPU attempts to read or write the onboard memory during this time, MDENB will go high and force RDY low--generating a wait state. After REFWAIT goes low, RDY goes high; allowing a normal bus cycle to occur.

Note that the refresh circuits don't generate a refresh request every time the CPU isn't accessing memory--only once every 16 uS. The CPU is running about 80 times faster than this and can perform many instruction cycles between refreshes. Since the RAMs can go for about 2 mS before requiring refresh, there's no danger of losing memory.

PARITY CIRCUITS

The parity circuits consist of U153, U101, U117, U137, and U152.

These circuits maintain the parity status for each byte in the 192K of RAM. If a memory location should not match its parity bit, then the parity circuits will send an error signal to the CPU.

U101, U117, and U137, are 64K by 1-bit RAMs and store one bit of parity information for each address location of RAM. These RAMs are addressed by $\overline{RAS}$ and $\overline{CAS}$ in the same way as the other RAMs. However, data transfers take place through U153 instead of the data bus. U153 is a 9-bit odd/even parity generator/checker that processes and maintains the parity status.

During a memory write, the data written into RAM is present at pins 8-13 and 1-2 of U153. Pin 14 of each parity RAM is a high-impedance state so U153-4 is logic 1 through pullup resistor R107.

The following truth table show the levels of the odd and even outputs for the number of high inputs:

Number of Input Pins That Are High. (1, 2, 4, 8-13)	Outputs	
	Even	Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

So if there is an odd number of high bits in the data byte, the logic 1 on U153-4 makes it even. U153-5 responds by going high.

If there is an even number of data bits in the data byte, U153-5 stays low, so the total bit count remains even.

U153-5 couples the one or zero through the normally-enabled gate at U151-4 to the data input pins of the parity RAMs.

The $\overline{\text{ZEROPAR}}$ line at U151-5 is normally high. This can be brought low to force all addressed parity RAM locations to zero--regardless of the byte status. It is brought low by clearing data bit D4 to zero and outputting it to port OFCH, the memory control latch. $\overline{\text{ZEROPAR}}$ is used as a quick test to see if the error-detection circuits work.

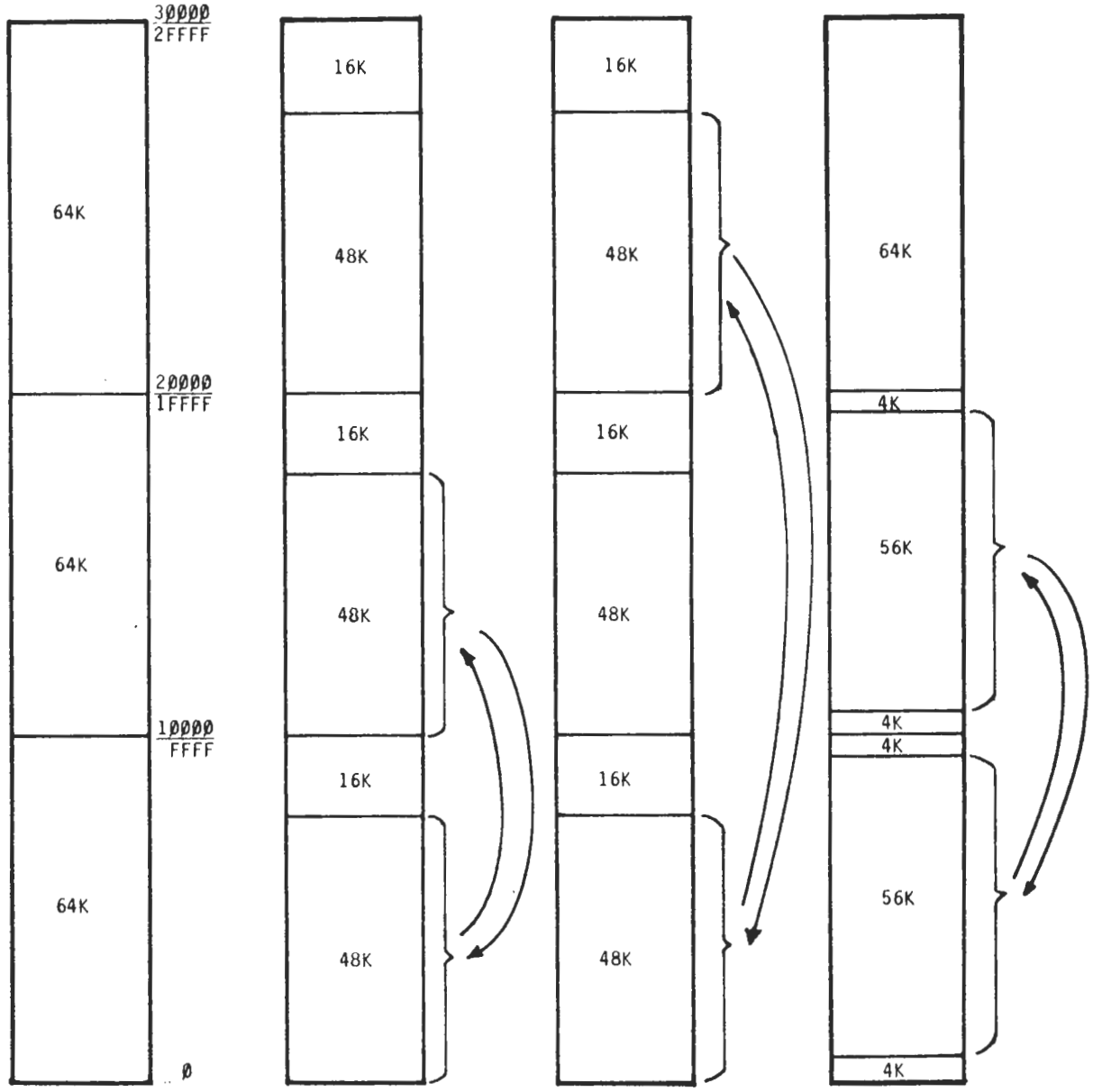
The odd-parity output goes to U152-11. During a memory write, U151-11 is low; preventing a false error signal from being generated. For the same reason, U151-9 remains low for a memory refresh.

During a memory read, data output from the addressed RAMs are present at the inputs of U153. The corresponding parity bit, from U101, U117, or U137, is placed on U153-4. If the bit pattern that was previously written into data RAM and parity RAM hasn't changed, the total number of high bits is always even.

So U153-6 remains low, the non-error condition.

If, however, the bit count totals to an odd number--due to a chip failure or soft error for example--then U153-6 goes high. When TAP2 goes low, U152-9 is latched to logic one and asserts the S-100 ERROR* line at U158-6. This will generate an error interrupt at U208-18 (schematic MB1). From here, it is up to the user's software to process the interrupt.

When $\overline{\text{KILPAR}}$ is asserted, U152 is held clear to prevent a parity error interrupt. To assert $\overline{\text{KILPAR}}$, clear data bit D5 to zero and output it to port OFCH, the memory control latch.



MOTHERBOARD MEMORY MAP OPTIONS

MAP SELECTING

Map selecting takes place at pins 1 and 15 of U111. These two lines, MAPSEL0 and MAPSEL1, also go to U173-7 and -8; but currently are not used by this IC. Depending on the logic state of U111-1 and U111-15, plus the address on lines BA12-BA15, the memory map will appear to be in one of the four configurations shown in the illustration:

Configuration #1: MAPSEL1 = 0 MAPSEL0 = 0

This is the default configuration, memory is contiguous from 0 to 192K.

Configuration #2: MAPSEL1 = 0 MAPSEL0 = 1

In this configuration, the first 48K of bank zero appears to be swapped with the first 48K of bank 1. The two 16K areas and the rest of RAM are unchanged. This configuration may be used for MP/M while running the 8085 CPU.

Configuration #3: MAPSEL1 = 1 MAPSEL0 = 0

In this configuration, the first 48K of bank zero appears to be swapped with the first 48K of bank 2. The two 16K areas and the middle 64K of RAM are unchanged. This configuration may also be used for MP/M while running the 8085 CPU.

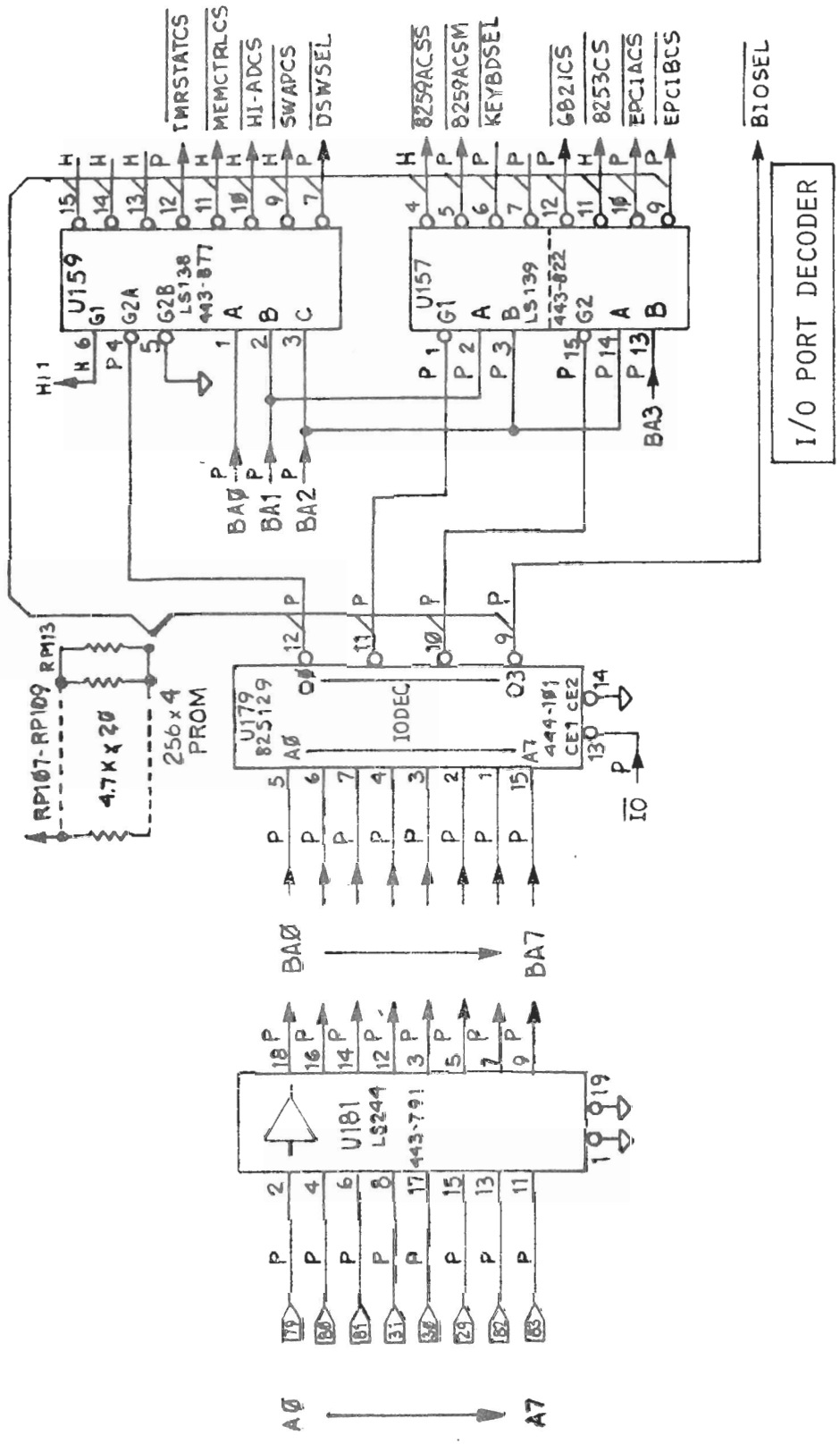
Configuration #4: MAPSEL1 = 1 MAPSEL0 = 1

In this configuration, 56K in bank 0 appears to be swapped with 56K in bank 1. Four kilobyte buffers above and below each 56K area remain unchanged, as does the top 64K bank. This configuration would permit using an extended BIOS when running CP/M-85.

Note that, in all cases, the memory only appears to be swapped from the memory's point of view. When the CPU addresses the swapped memory, the memory map decoder merely asserts a different RAS line than it normally would.

For example, assume that the H/Z-100 is operating in Configuration #4. If the CPU should write to the byte at the 6K location, U111 would assert $\overline{\text{REN1}}$ instead of $\overline{\text{REN0}}$. The memory at the 70K location will be written to. Bear in mind, however, that as far as the CPU (and the programmer) is concerned, the byte at 6K was written to.

Address lines BA12-BA15 allow the memory map decoder to keep some sections of memory in place--down to 4K increments.



I/O PORT DECODER (MB2)

I/O PORT DECODER

Refer to schematic MB2 as you read the following.

The heart of the I/O port decoder is U179, a 256 x 4 PROM. Depending on which motherboard/video port the CPU addresses, U179 will enable U159 or U157; respectively a 3-to-8 line decoder and a dual 2-to-4 line decoder.

To address one of these ports (0D8H through 0FFH), the CPU first places the appropriate port address on the inputs of U179, A0 through A7. This address comes from the S-100 address lines, A0-A7, through octal buffer U181.

When the address lines have stabilized, the CPU enables U179 by asserting pin 13, the IO line. This signal comes from U224C-10, and goes low whenever the CPU asserts the S-100 sINP or sOUT lines. Once IO is asserted, U179 decodes the address at its inputs and selects either U159 or U157. For example, it selects U159 for a memory control latch operation by bringing U179-12 to logic zero. Pins 1, 2, and 3 of U159 then decode the lower three bits of the address bus to assert pin 11, MEMCTRLCS.

U159 also selects the following ports:

$\overline{\text{TMRSTATCS}}$ This is the timer status port; U160 on schematic MB4.

$\overline{\text{HI-ADCS}}$ This line controls the extended addressing latches shown on schematic MB1.

$\overline{\text{SWAPCS}}$ This line connects to the processor swap port shown on schematic MB1.

$\overline{\text{DWSEL}}$ This line controls the power-up reset configuration port, U239 on schematic MB2.

If U179-11 is asserted, section A of decoder U157 will be selected. It will decode address lines BA1 and BA2 to enable the interrupt ports, 8259ACSS and 8259ACSM, on schematic MB1; or the keyboard port, KEYBDSEL, on schematic MB4.

If U179-10 is asserted, section B of decoder U157 is selected. It will decode address lines BA2 and BA3 to enable one of the following ports:

6821CS The parallel port, U114, on schematic MB4.

8253CS The timer port, U160, shown on schematic MB4.

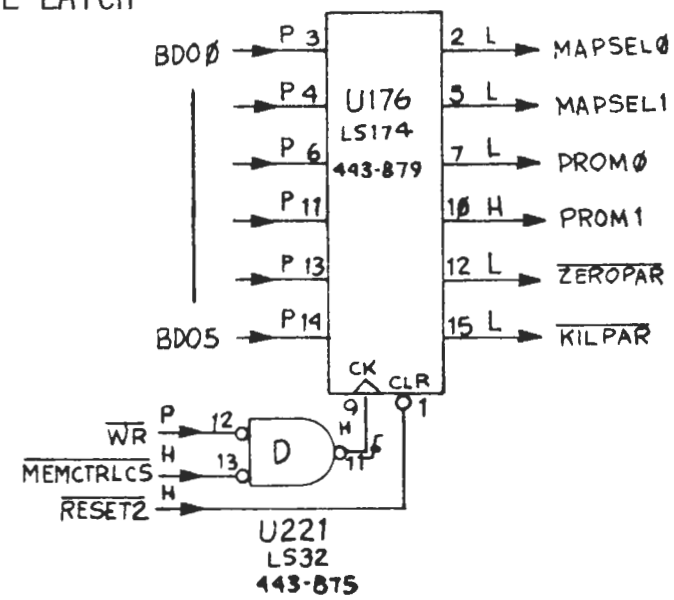
EPCIACS Serial port A on schematic MB4.

EPCIBCS Serial port B on schematic MB4.

If the keyboard, serial port A, or serial port B is selected, U179-9 will also go low. This line is further decoded by U222 (schematic MB4) to enable U241 whenever the CPU reads data from one of these ports.

See the appropriate circuit description and the block diagram description to see how each of these circuits are affected by the I/O port decoder.

MEMORY CONTROL LATCH



The memory control latch, U176, determines the addressing of RAM and ROM; it also sets the status of the parity circuits.

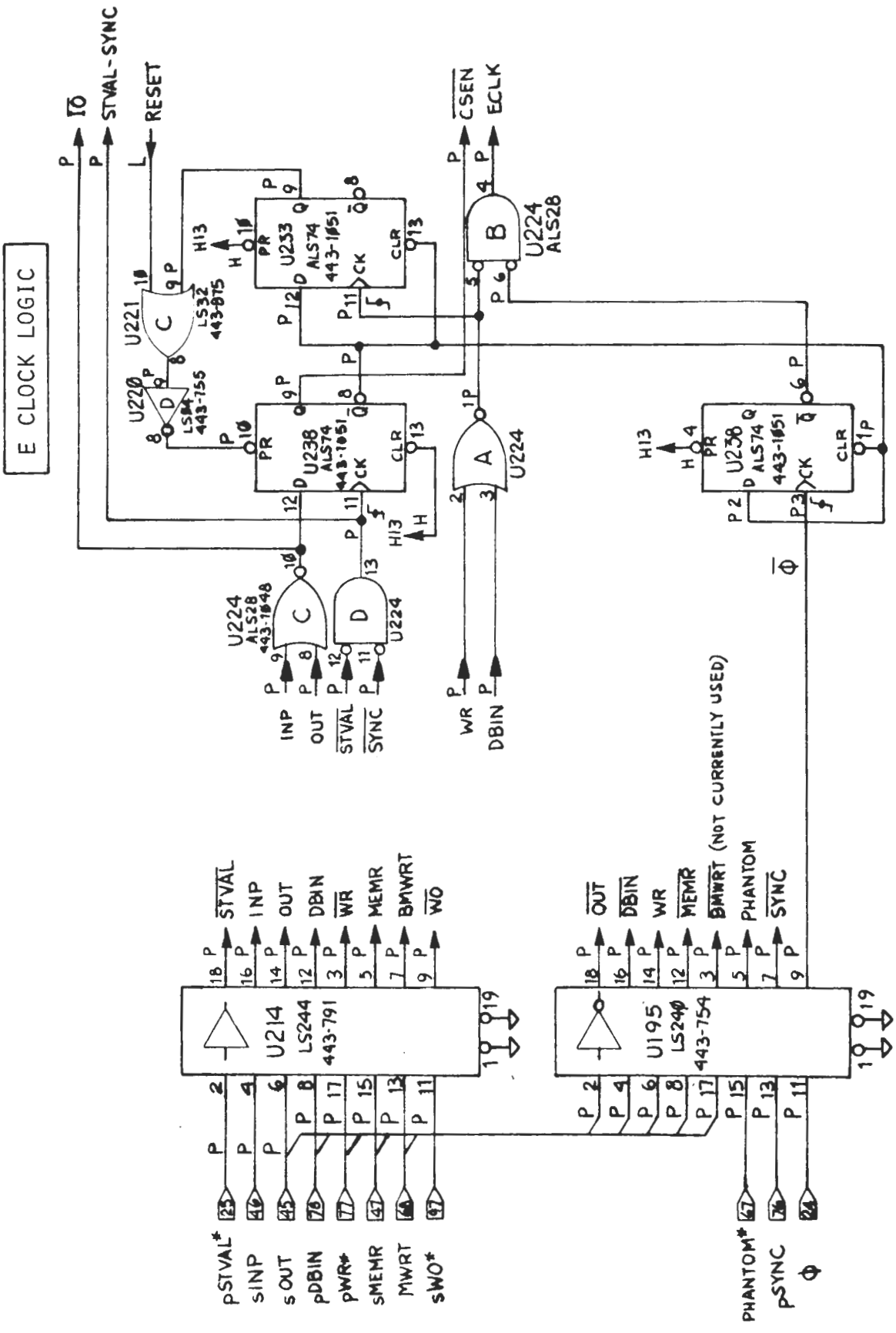
The CPU accesses this latch by writing the correct byte to port 0FCH. This is done by asserting the MEMCTRLCS line at U159-11 in the I/O port decoder. This signal is then applied to U221D-13, an OR gate.

The CPU next places the data byte to the D inputs of U176, a hex D-type flip-flop, and then asserts pWR* on the S-100 bus. U214-17 couples this control signal through U214-3 to U221-12 and drives U221-11 low.

When the data byte on the D inputs of U176 has had time to stabilize, U221-11 goes high; clocking the data bus signals into U176 on the positive-going edge.

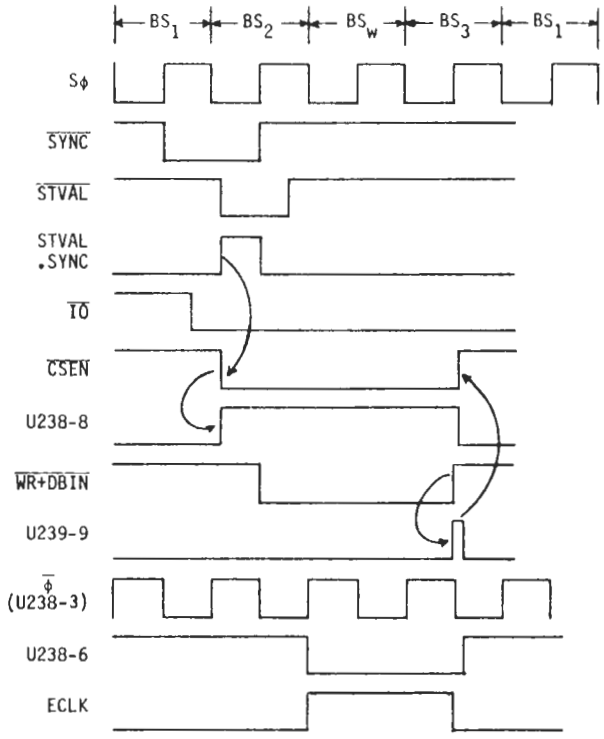
The bit pattern that was on the data bus is now latched onto the Q outputs of U176, setting the type of memory map addressing (MAPSEL0 and MAPSEL1), monitor ROM addressing (PROM0 and PROM1), and parity operation (ZEROPAR and KILPAR).

See the appropriate circuit description and the block diagram description to see how these circuits are affected.



E CLOCK LOGIC (MB2)

E CLOCK LOGIC



The E clock logic, located on schematic MB2, retimes the S-100 clock and control signals to values required by some of the ICs on the video board and I/O circuits. Refer to the accompanying timing diagram as you read the following.

U224-13 forms the STVALxSYNC signal during bus cycle 2. This provides a status valid signal to the video board.

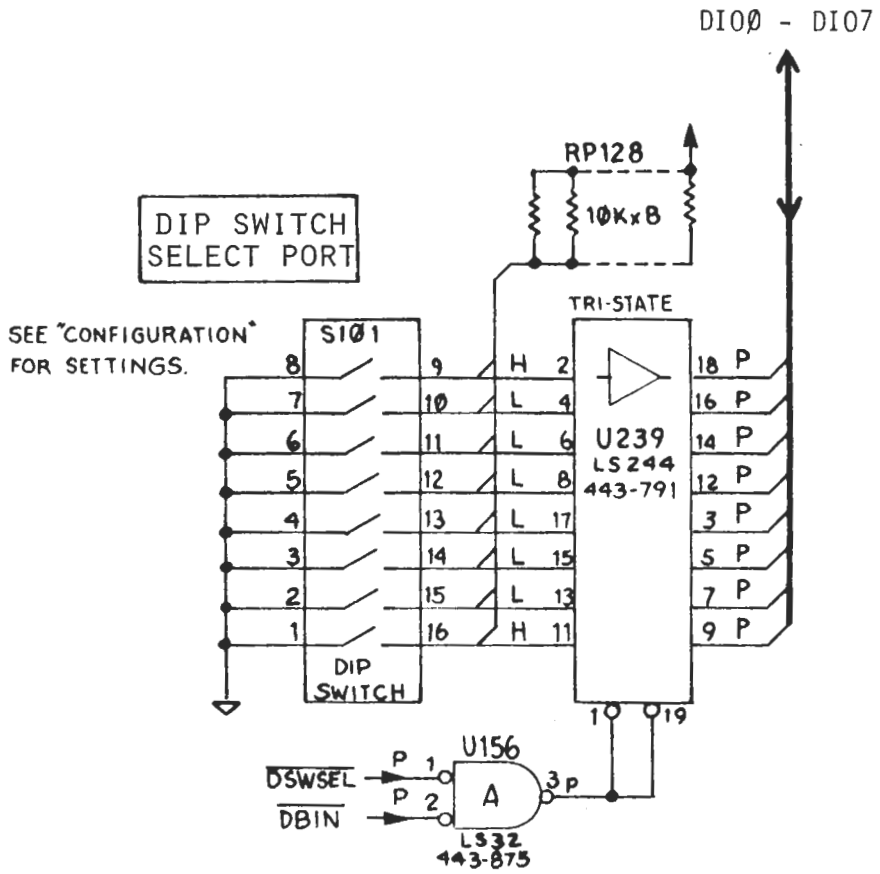
U224-10 generates $\overline{IO}$, a chip-select line to the I/O port decoder and to the video board.

The combination of $\overline{IO}$ and STVALxSYNC form $\overline{CSEN}$ at U238-9. This line provides a chip-enable signal to serial ports A and B.

At the end of the read or write pulse from U224-1, the logic one at U238-8 is latched into U233-9. This presets U238-9 and brings $\overline{CSEN}$ back to logic one during BS3. At the same time, U238-8 goes low to clear U233-9.

During this time, the inverted system clock, ϕ, works with U238-8 and $\overline{WR+DBIN}$ to form the ELCK signal. This signal provides timing to the parallel port.

See the circuit description on each of the above mentioned circuits to see how they use the E clock signals.



DIP-SWITCH SELECT (MB2) CIRCUITS

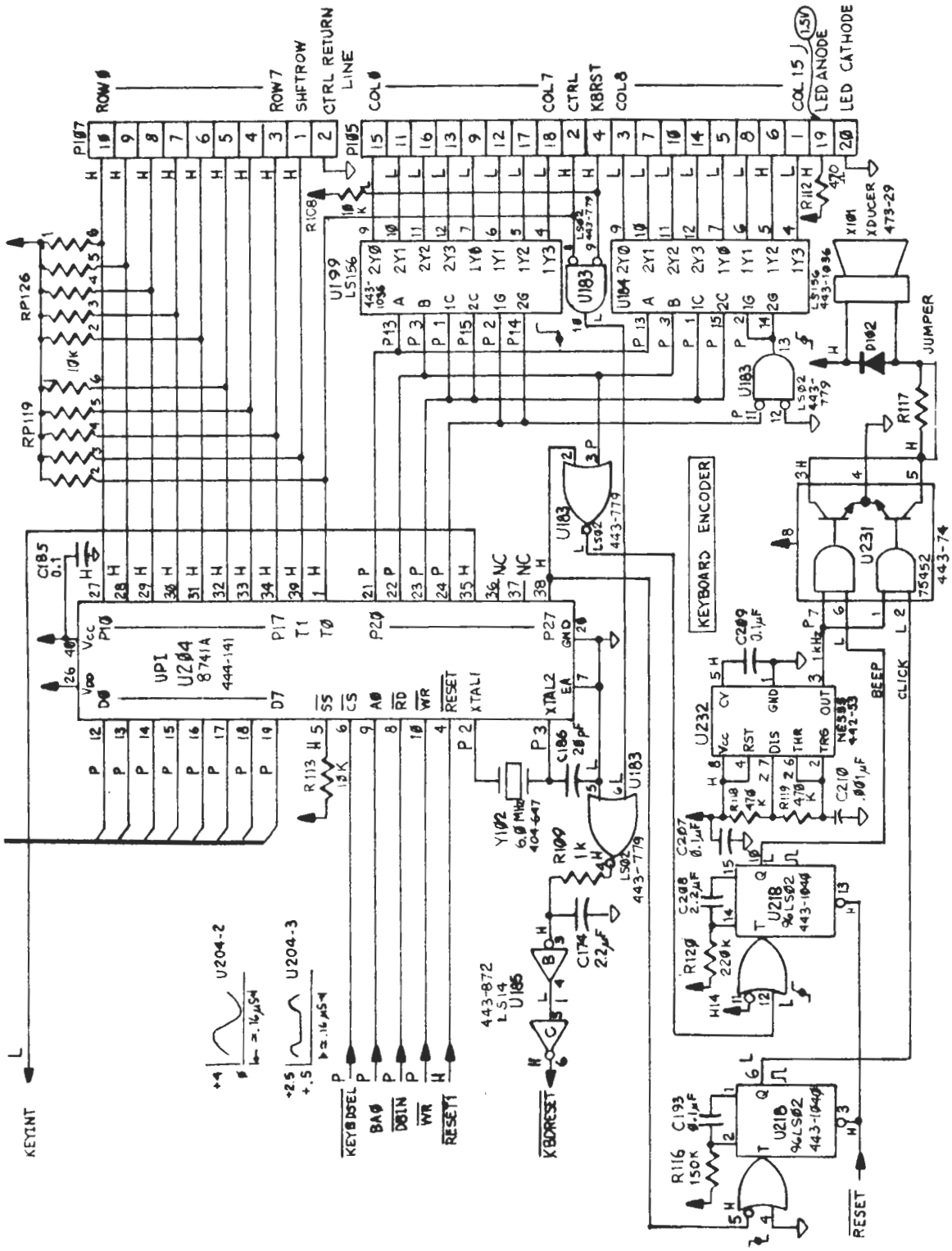
DIP-SWITCH SELECT CIRCUITS

Refer to schematic MB2.

U239, S101, and U156A make up the dip-switch select circuits. The position of these switches determine the operating mode of the H/Z-100. See the configuration section for the various options.

The H/Z-100 reads the status of S101 during power-up by addressing input port 0FFH. To read the dip-switch port, the CPU asserts the $\overline{\text{DSWSEL}}$ port select line coming from the I/O port decoder at U159-7. The CPU also asserts the S-100 pDBIN line to indicate that an I/O read operation is to take place. U195 inverts the pDBIN line to produce $\overline{\text{DBIN}}$ at U156-2.

Since U156-1 and U156-2 are both low, pin 3 of this OR gate also goes low to enable U239. The outputs of U239 go from a high-impedance state to the logic level of each switch section; this in turn is coupled through U241 (schematic MB4) to the CPU for further processing.



KEYBOARD CIRCUITS (MB4)

KEYBOARD CIRCUITS

Refer to schematic MB4 as you read the following:

The keyboard circuits are designed around the 8041A/8741A universal peripheral interface (UPI) at U204. This IC is a dedicated 8-bit microprocessor with internal RAM and ROM. The RAM is 64 by 8 bits, while the ROM is 1024 by 8 bits.

Since U204 is a dedicated processor, we will only cover the pin-outs of this IC; see the the IC Data section if you're interested in what happens inside the chip.

D0-D7 Three-state, bidirectional data bus lines used to interface the UPI to the H/Z-100 data bus. The CPU uses this bus to read the code of the pressed key, read UPI status information, and to write command words to the UPI.

$\overline{CS}$ Chip-select line. When the CPU addresses the keyboard circuits at ports 0F4H & 0F5H, the I/O port decoder asserts line KEYBDSEL. This activates U204.

A0 Address input used by the H/Z-100 to indicate whether the byte transfer to D0-D7 is data (A0 = 0) or a command (A0 = 1). This signal is derived from the buffered address line zero (BA0) from U181-18 on schematic MB2.

$\overline{RD}$ Read data line. When asserted, the UPI transfers its internal data to the D0-D7 lines. The CPU can then load this data into its accumulator.

$\overline{WR}$ Write data line. The CPU places data on pins D0-D7 of the UPI. The H/Z-100 then asserts WR to load this data into U204.

RESET Input used to clear the UPI's status flip-flops and program counter to zero.

XTAL1 & XTAL2 Provides 6-MHz crystal-controlled clock to the circuits inside the UPI.

P10-P17 Bidirectional I/O lines programmed as input lines. These lines connect to ROW0-ROW7 of the H/Z-100's matrix keyboard. When a key is pressed, a pulse from one of the column lines (P20-P23) is coupled into one of the row lines. U204 notes which row is being strobed and, by checking an internal counter, when it's being strobed.

By finding when the strobe pulse occurred, the UPI can tell which column was connected to which row when the key was pressed. From this, the UPI can look up the appropriate key code in ROM and send the code to the computer.

T1 An input pin that can be directly tested by software conditional branch instructions. When a key is pressed, the UPI checks this line to see if the SHIFT key is also pressed. If so, the UPI jumps to a routine that translates the key press at ROW0-ROW7 to its appropriate shifted code--if it has one.

T0 Input pin which can be directly tested using conditional branch instructions. When a key is pressed, the UPI checks this line to see if the CONTROL key is also pressed. If so, the UPI jumps to a routine that translates the key press at ROW0-ROW7 to its appropriate control code--if it has one.

P20-P23 Bidirectional I/O lines programmed as outputs. P20 and P21 form a 4-bit counter that connects to the A and B inputs of U199 and U184, two dual 2-line-to-4-line decoders.

P22 connects to the 1C and 2C inputs of the two decoders. When P22 is low, the data at the A and B inputs will be routed to the 2Y outputs; when P22 is high, that A and B data will be routed to the 1Y outputs.

P23 connects to the 1G and 2G inputs of U199; it's also coupled to the 1G and 2G inputs of U184 after being inverted. When P23 goes low, it selects U199 and disables U184; when high, it does the opposite.

The combination of these four lines effectively turns U199 and U184 into a 4-line-to-16-line decoder. The UPI pulses these lines in such a manner that each column will pulse low once; columns 8 through 15, then columns 0 through 7. At that point, the cycle repeats.

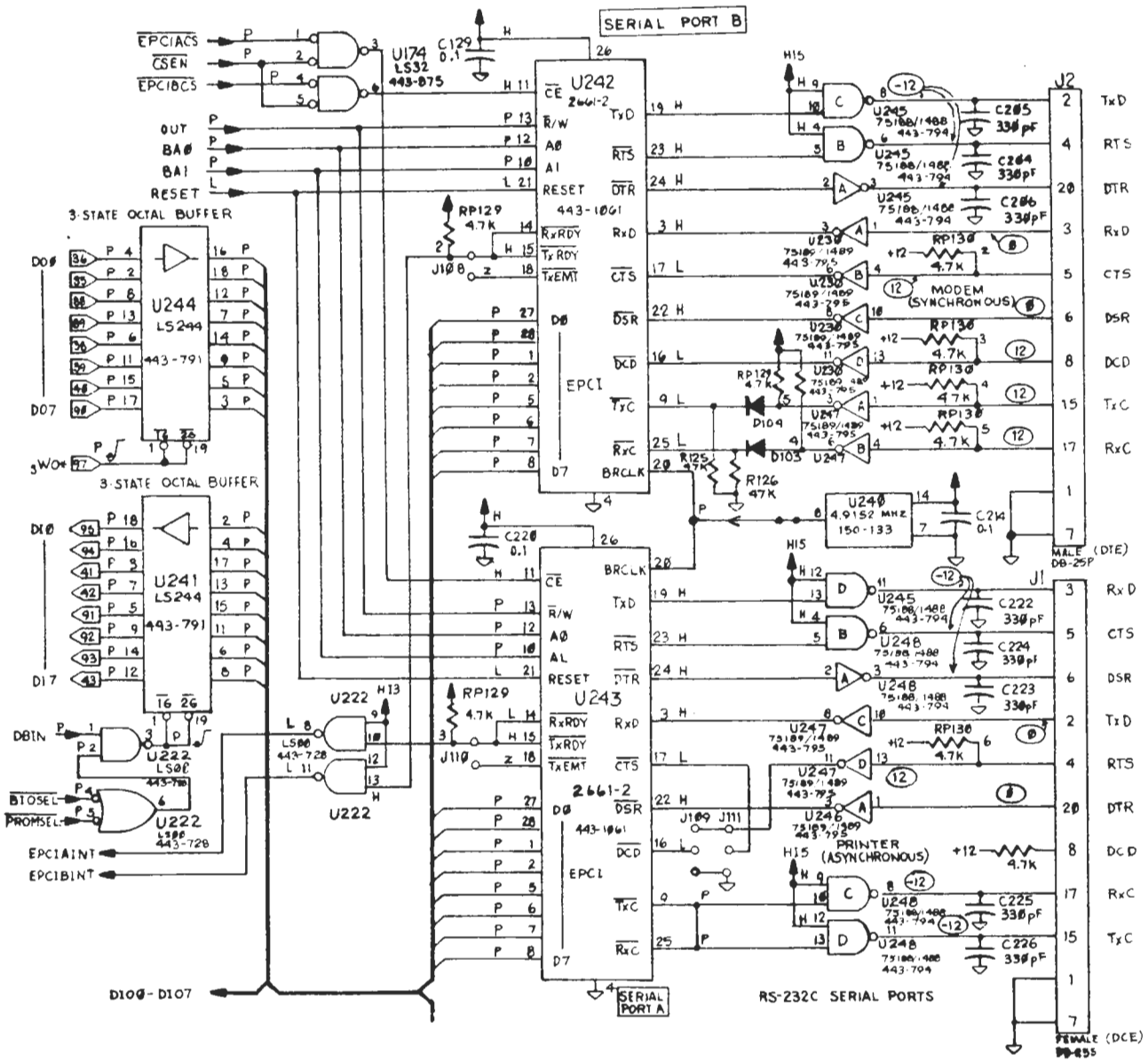
Note that U199 and U184 have open-collector outputs. When a key isn't being pressed, these lines will switch between a high-impedance state and logic zero, rather than between one and zero.

P24 Bidirectional I/O line programmed as an output. When the UPI has data to be sent to the CPU, it places the data on D0-D7 and then raises P24 to logic one. This asserts KEYINT, sending a keyboard interrupt to the CPU.

P27 Bidirectional I/O line programmed as an output. This line pulses to generate the bell and key click sounds. U183 NORs this line with P21 to generate the bell. When U183-1 goes low, it triggers the single-shot at U218. U218-10 pulses high for about 200 mS to gate U232-3, the 1-kHz oscillator, through U231 to the speaker.

To generate a key click, the negative edge of P27 directly fires the one-shot at U218-5. Pin 6 of this IC goes high for about 10 mS to gate U232 through U231 to the speaker. Note that the click line asserts whenever the bell does. However, since both circuits use the same oscillator, the click isn't heard.

See the "Keyboard" section in this manual for a complete description of the keyboard features and operating instructions.



SERIAL PORTS A AND B (MB4)

SERIAL PORTS A AND B

OVERVIEW

Refer to schematic MB4 as you read the following.

The two serial ports permit the H/Z-100 to communicate with external devices such as printers, MODEMs, plotters, and voice synthesizers. Since the serial ports are on the motherboard, the S-100 slots can be used for other purposes.

The serial ports are designed around the 2661-2 EPCI (Enhanced Programmable Communications Interface). These ICs have a large number of features, including:

Polled or interrupt mode operation.
Asynchronous or synchronous operation.
5 to 8-bit characters plus parity.
Odd, even, or no parity.
Baud rate from 45.5 baud to 38,400 baud.
Full handshaking.

See the 2661-2 IC data sheets for complete specifications.

SERIAL PORT A

Serial port A consists of U243 and its surrounding circuitry. This port is a DCE port and can be used to connect to a line printer such as the H-25.

To select this port, the CPU addresses the following ports:

0E8H	Receiver holding register (read). Transmitter holding register (write).
0E9H	Status registers (read). SYN1/SYN2/DLE registers (write).
0EAH	Mode registers (read/write).
0EBH	Command registers (read/write).

When the CPU selects one of these ports, it asserts $\overline{\text{EPCIACS}}$ from the I/O port decoder and CSEN from the E-clock logic. These lines connect to pins 1 and 2 of U174 and assert the chip-enable line (pin 11) of U243.

Also, the CPU asserts pins 12 and 10 to select the right internal register. The OUT signal at U243-13 determines whether the selected register is written to or read from. This signal is derived from the sOUT signal at U214-14 on schematic MB2.

The CPU transmits and receives data at lines D0 through D7 on U243. If the CPU is transmitting data, it chip-enables U243, selects the correct register, raises U243-13 to logic one, places the data to be transmitted on the inputs of U244, and asserts sWO* at U244-1 and U244-19.

The data is loaded into the transmit data holding register inside the EPCI. The EPCI then asserts $\overline{\text{TxRDY}}$ at pin 15 to raise the EPCIAINT line at U222-8, interrupting the CPU. The CPU responds by not sending any more data until the transmitting holding register is empty.

The EPCI serially transmits the contents of the transmit data holding register out pin 19 and through U245, which converts the TTL to RS-232 levels. In asynchronous mode, the EPCI first sends a start bit, followed by the programmed number of data bits (5 to 8--LSB first), the parity bit (if programmed), and finally the programmed number of stop bits--1, 1-1/2, or 2.

Once the transmit data holding register is empty, the $\overline{\text{TxRDY}}$ line goes low to inform the CPU that it can send another byte.

In the receive mode, serial data enters the EPCI at pin 3 through U247C, which converts the ±12-volt RS-232 levels to TTL levels. The EPCI extracts the data bits and loads it into the receive data holding register. The $\overline{\text{RxRDY}}$ line then goes low to interrupt the CPU through U222-10. When the CPU processes the interrupt, it addresses U243, places a logic zero on pin 13, and reads the data at D0-D7 through U241. U241 is selected by asserting the $\overline{\text{BIOSEL}}$ line (from the I/O port decoder) and DBIN at U222-1.

The handshake lines are standard EIA RS-232 control lines. These are clear to send (CTS), data set ready (DSR), request to send (RTS), and data terminal ready (DTR). To maintain RS-232 standards, they are swapped with their complementary lines at the DCE connector.

Jumpers J109 and J111 allow connecting the DCE RTS line to either CTS or to DCD on the EPCI. If connected to the clear-to-send line, pin 17, the RTS line controls the transmitter. If connected to the data carrier detect line at pin 16, then RTS controls the receiver.

Depending upon the peripheral, these lines may or may not be used; see the peripheral's technical manual for this information.

The crystal-controlled oscillator, U240, provides a 4.9152-MHz clock to U243-20. The EPCI uses this clock to generate the baud rate frequencies.

Pins 9 and 25 of U243 provide clock to the peripheral device, if it requires it. This timing can be either 1X or 16X the baud rate. Pins 9 and 25 are connected together since TxC is tri-stated during receive and RxC is tri-stated during transmit.

SERIAL PORT B

Serial port B consists of U242 and its surrounding circuitry. This port is a DTE port and can be used to connect to devices such as a MODEM or to another computer.

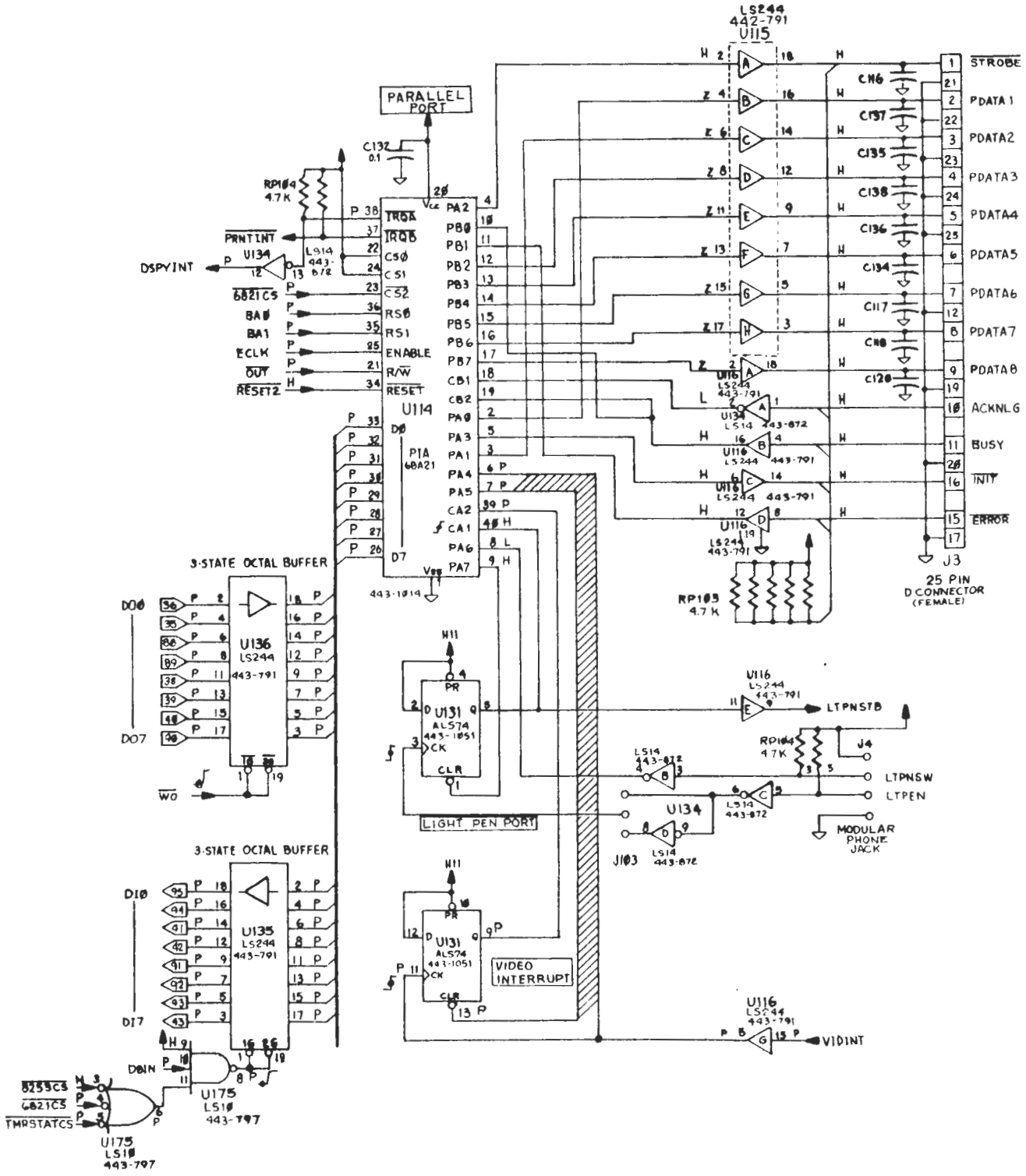
To select this IC, the CPU addresses the following ports:

0ECH	Receiver holding register (read). Transmitter holding register (write).
0EDH	Status registers (read). SYN1/SYN2/DLE registers (write).
0EEH	Mode registers (read/write).
0EFH	Command registers (read/write).

The differences between this port and serial port A are minor. To chip-select this IC, the CPU asserts $\overline{\text{EPCIBCS}}$ instead of $\overline{\text{EPCIACS}}$; the EPCI interrupts the computer through EPCIBINT instead of EPCIAINT; and pins 9 and 25 are clock inputs instead of outputs. This last feature is taken care of when the CPU initially programs the EPCI. The frequency can be 1X, 16X, or 64X the serial baud rate.

In the asynchronous mode, pins 9 and 25 act as outputs. Under these conditions, D103 and D104 isolate these pins from U247A and U247B.

Regulators U228 and U229 convert the ±16-volt power supplies to the ±12 volts required for RS-232 operation.



PARALLEL PORT (MB4)

PARALLEL PORT

OVERVIEW

Refer to schematic MB4 as you read the following circuit description.

The parallel port is designed around a 68A21 peripheral interface adapter (PIA) at U114. This IC performs three functions: (1) it operates as a printer port, (2) it serves as a port for a light pen, and (3) it couples the video board vertical retrace signal to the CPU.

The CPU accesses U114 for programming or data transfer through U135 and U136. At the same time it will chip-select U114 by asserting the $\overline{6821CS}$ control line from the I/O port decoder. The CPU also asserts address lines BA0 and BA1 (pins 36 and 35) to select the correct internal register.

The enable line, ECLK, comes from the E-clock logic circuits on schematic MB2 and provides timing to U114. All other signals to the PIA are referenced to either the rising or falling edges of this line.

The CPU asserts the $\overline{OUT}$ line, U114-21, when the computer needs to write to the PIA. In all other cases, the PIA is in the read mode. Actual data transfer between the CPU and PIA takes place when the CPU asserts $\overline{WO}$ at U136-1 for a write, or DBIN at U175-10 for a read.

The other connections to U114 will be covered in the following sections. For a complete description of the internal operation of the PIA, see the IC data sheets.

PRINTER PORT

The printer port is a parallel output port with handshaking capabilities. It allows connecting the H/Z-100 to some of the more popular printers without having to add a serial interface to the printer.

The parallel data leaves U114 at PB0 through PB7, couples through U115 to J3 where it becomes PDATA1 through PDATA8. J3 couples this data to the printer. When this data is sent, the $\overline{\text{STROBE}}$ line goes low to inform the printer that a new byte is present at its input.

The ACKNLG line asserts when the printer has processed the received byte and is ready to receive another character. This signal is inverted by U134A and sent to U114-18, CB1. This input can be programmed to detect either a negative-going or positive-going signal; allowing ACKNLG to assert on logic one or a logic zero.

CB1 detects the voltage transition and asserts the printer interrupt line at U114-37. When the H/Z-100 processes the interrupt, it will address U114's control register to determine which circuit caused the interrupt. When the CPU detects that the ACKNLG caused it, it will transmit the next byte to the printer.

The BUSY line asserts if the printer cannot accept a data byte at the time $\overline{\text{STROBE}}$ occurs. This can happen if the print head is moving (such as during a carriage return), or if the printer is in the off-line mode.

The BUSY signal is buffered by U116B and couples to CB2 and PA0 on U114. Input CB2 generates an interrupt in the same manner as CB1 in the ACKNLG circuits. The CPU responds to the interrupt, finds that a printer BUSY signal has occurred, and stops printing until the BUSY line goes to its inactive state.

To see when the BUSY line goes to the inactive state, the CPU monitors the logic level of PB0. This simplifies programming since, otherwise, CB2 must be reprogrammed to respond to the opposite-polarity signal transition.

The CPU uses the $\overline{\text{INIT}}$ line to initialize some printers. It does this by sending a short pulse (typically 50 nS) to the printer.

The $\overline{\text{ERROR}}$ line asserts if a printer failure occurs, such as when the ribbon needs changing, or when the printer runs out of paper. The CPU stops sending characters until the error is fixed.

LIGHT PEN PORT

The light pen circuits consist of U134B, C, and D, U116E, U131, and part of the PIA at U114.

By itself, the CPU will not respond to a signal from the light pen circuits. It must have a user-supplied program to set up interrupts, handle timing, and take care of bit locations pointed to by the light pen. As a result, this discussion will only be general.

When the CPU lights a dot on the CRT within the range of the light pen, the light pen sends a pulse to U134-5. Jumper J103 allows triggering from either the leading or trailing edge of this pulse.

This pulse will latch a logic one into U131-5 which couples through U116E to the light pen strobe input in the CRTC, U330, on the video board. The CRTC saves the address of the byte being accessed. See the video board circuit description for more details.

The output of U131 also couples to U114-40, the PIA. The rising edge of the signal at pin 40 causes IRQA at U114-38 to go low, which is inverted by U134-12 to cause a display interrupt at the CPU.

When the CPU acknowledges the interrupt, it must assert the $\overline{6821CS}$ line (from the I/O decoder port) at U175-4. Line $\overline{6821CS}$ also chip-selects U114 at pin 23 while BA0/BA1 addresses the PIA control register to see if the light pen circuits generated the interrupt. The OUT line at pin 21 and the DBIN line at U175-10 go to logic one to transfer the PIA data to the CPU.

If the interrupt was caused by light pen activity, the CPU processes it according to its program. Before finishing, the CPU clears U131-5 by pulsing a logic zero to U131-1.

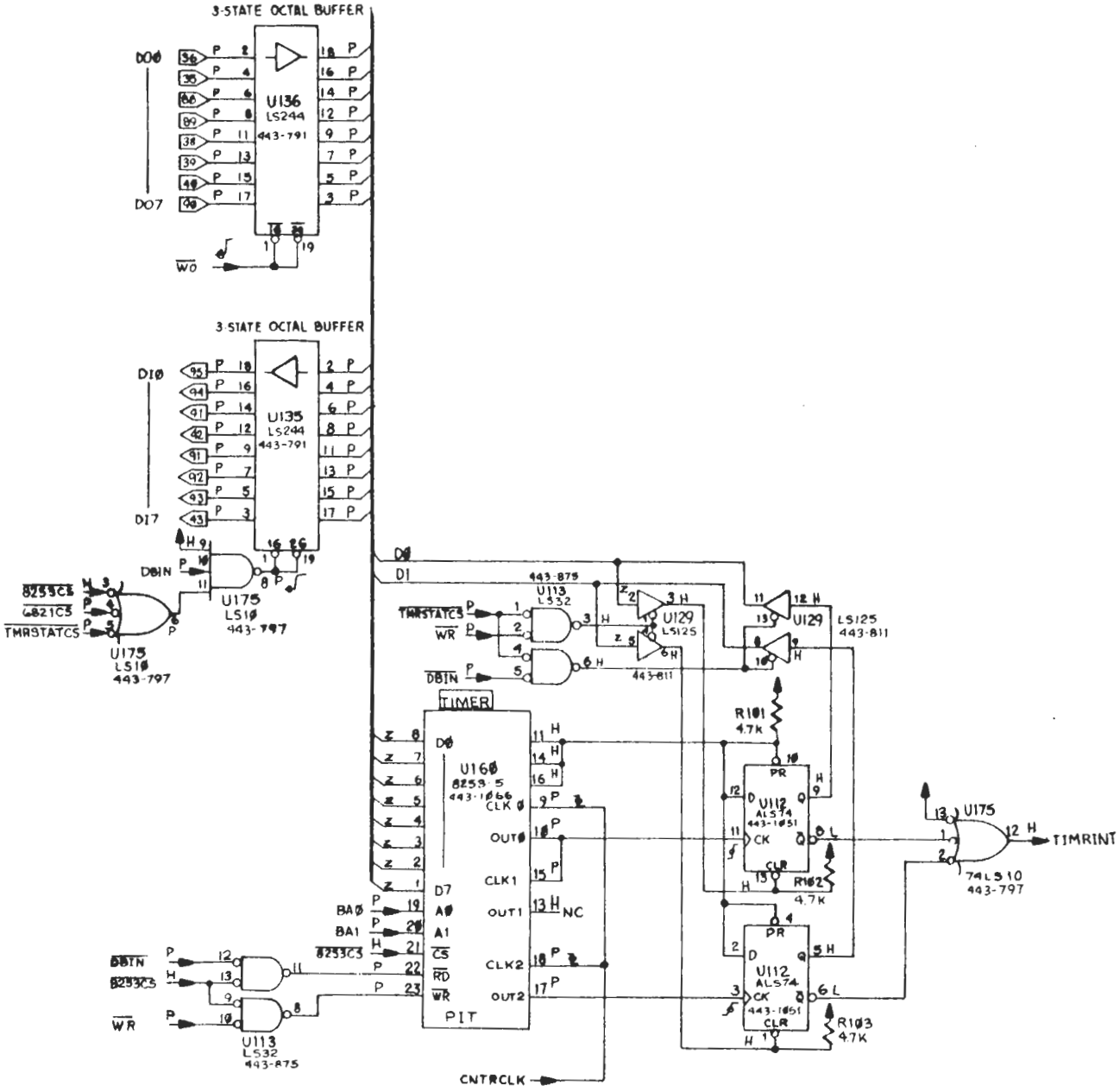
U134B, the light pen switch inverter, allows the CPU to monitor the status of a SPST switch connected to LTPNSW at J4. It does this by continually polling PA6 at U114-8. This allows you, for example, to move a dot around the CRT face with the light pen. As before, the H/Z-100 must be programmed to use this feature.

VIDEO INTERRUPT PORT

The video interrupt port consists of U116G, U131, and U114. The signal at U116-15, VIDINT, is the vertical sync pulse, VSYNC1D, buffered through U366-9 on the video board. The CPU times itself from this pulse so that it can update the display during vertical retrace; thus preventing interference on the display. See the video board circuit description for more details.

When a vertical sync pulse occurs, the positive-going edge from U116-5 latches a logic one into U131-9. This couples to U114-39 and causes the PIA to generate a display interrupt at U114-38.

When the CPU responds, it checks the PIA control register to determine which line caused the interrupt. Once it finds that VIDINT caused it, the CPU clears U131 by pulsing U114-7 low and then updates the display circuits as necessary.



TIMER CIRCUITS (MB4)

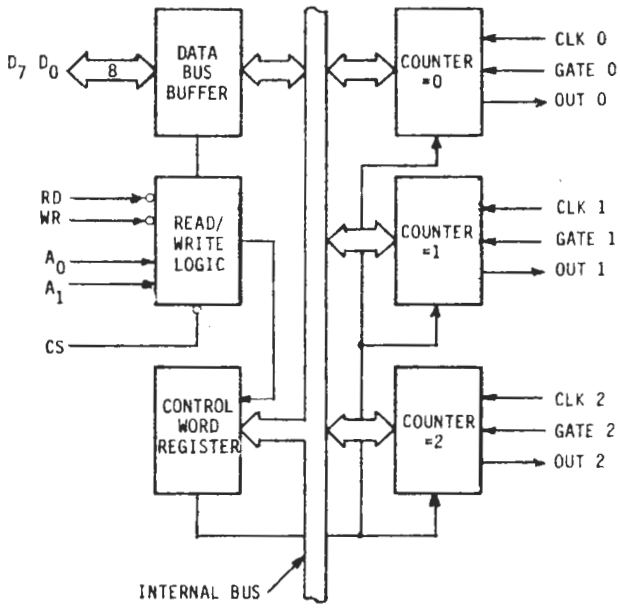
TIMER

8253-5 BASICS

PIN NAMES

D_7 D_0	DATA BUS (8 BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
RD	READ COUNTER
WR	WRITE COMMAND OR DATA
CS	CHIP SELECT
A_0 A_1	COUNTER SELECT
V_{cc}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM



The H/Z-100 timer circuit is designed around the 8253-5 programmable interval timer IC at U160.

Referring to the above block diagram, you'll see that the 8253-5 consists of three counters, a data buffer bus, read/write logic, and a control word register.

The counters are sixteen-bit down-counters with separate clock inputs, gate inputs, and outputs. The clock input causes its associated counter to decrement on the negative-going edge of the clock pulse. The gate input disables its associated counter when brought to logic zero. The output line will assert when the counter reaches zero; whether it asserts high or low depends on how its associated counter is programmed.

The read/write logic allows the CPU to communicate with the 8253-5. It communicates through the data bus buffer when $\overline{CS}$ and either $\overline{RD}$ or $\overline{WR}$ are asserted. Address lines A0 and A1 connect the data bus buffer to one of the counters or to the control word register.

If connected to one of the three counters, the CPU can load a starting count into the counter, or read the current count as the counter is down-counting. This data can be either 8 bits or 16 bits.

The CPU writes to the control word register to load it with an 8-bit programming byte. This byte selects the counter to be programmed, determines whether the counter is going to count an 8-bit or 16-bit word, and if it's going to count in binary or BCD. In addition, the control byte sets the operating mode of the counter.

The 8253-5 timer has 6 programmable operating modes. Briefly, these are:

Interrupt on Terminal Count – The output goes to logic one when the counter reaches zero (terminal count).

Programmable One-Shot – Not used in the H/Z-100 since the gate lines are tied to logic one.

Rate Generator – Divide-by-N counter. The output goes low for one clock period, returns high and counts down the number stored in the counter. When the counter reaches zero, the output pulses low again and the count starts over.

Square Wave Generator – The output remains high for one-half the count in the down-counter, then goes low for the remaining count.

Software Triggered Strobe – After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one clock period.

Hardware Triggered Strobe – Not used in the H/Z-100 because the gate lines are tied to logic one.

See the IC data sheet on the 8235-5 for detailed programming information.

TIMER OPERATION IN THE H/Z-100

Refer to schematic MB4 to see how the 8235-5 timer functions at U160.

The CPU selects the timer whenever it reads or writes port 0E4 through 0E7. These ports select counters 0 through 2 and the control word register, respectively. Line $\overline{8253CS}$, from the I/O port decoder, chip-selects U160-21 while BA0 and BA1 select the internal counter or register.

The $\overline{8253CS}$ line also enables the two OR gates connected to pins 22 and 23 of U160. If the CPU is reading the data in U160, it asserts the DBIN line at U113-12; if it is writing to U160, it asserts WR at U113-10.

The output of counter #0, U160-10, couples to the input of counter #1 at U160-15. The counter #1 output isn't connected, but the CPU can still use this counter. When the output of counter #0 goes low, U160-10 decrements the count in counter #1 and also clocks the interrupt status latch (U112-11) to cause an interrupt. The CPU, if programmed to respond to this interrupt, will address U160 at pins 19 through 21, send a read command to pin 22, and then read the counter #1 data at pins 1 through 8.

The output of counter #2, U160-17, only connects to U112-3, the other interrupt status latch. Since both latches operate the same way, we will only discuss the operation of the latch for counter #2.

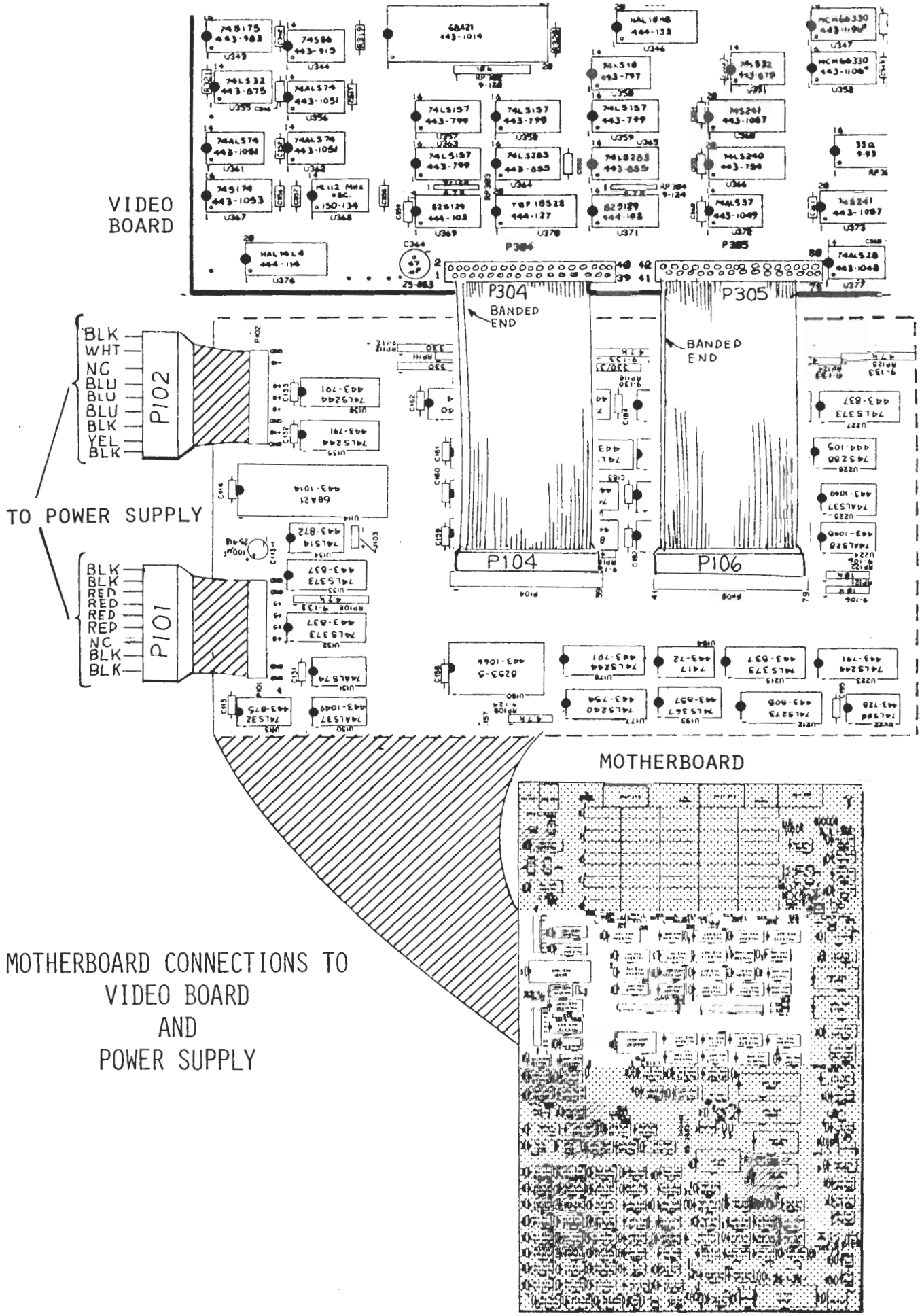
Assume that counter #2 of U160 is programmed to operate as a software-triggered strobe and that both status latches have previously been cleared. When counter #2 counts down to zero, U160-17 goes low for one clock period, then high again. This positive-going transition latches a logic one into U112-5. At the same time, U112-6 goes low to generate a timer interrupt at U175-12.

The CPU responds by asserting the $\overline{TMRSTATCS}$ line from the I/O port decoder and the data bus input line, $\overline{DBIN}$. U113-6 goes low to enable U129 at pins 13 and 10. In turn, these two inverters couple the status of pins 9 and 5 of U112 to D0 and D1 of the data bus. The CPU notes that U112-5 has toggled so it processes the interrupt caused by U160-17.

To clear the latch, the CPU again asserts $\overline{TMRSTATCS}$, places a logic zero on data line D1, and asserts the write control line, $\overline{WR}$. U129 couples D1 to U112-1 which forces pin 6 to one and pin 5 to zero.

The counter #0 circuits operate in the same manner.

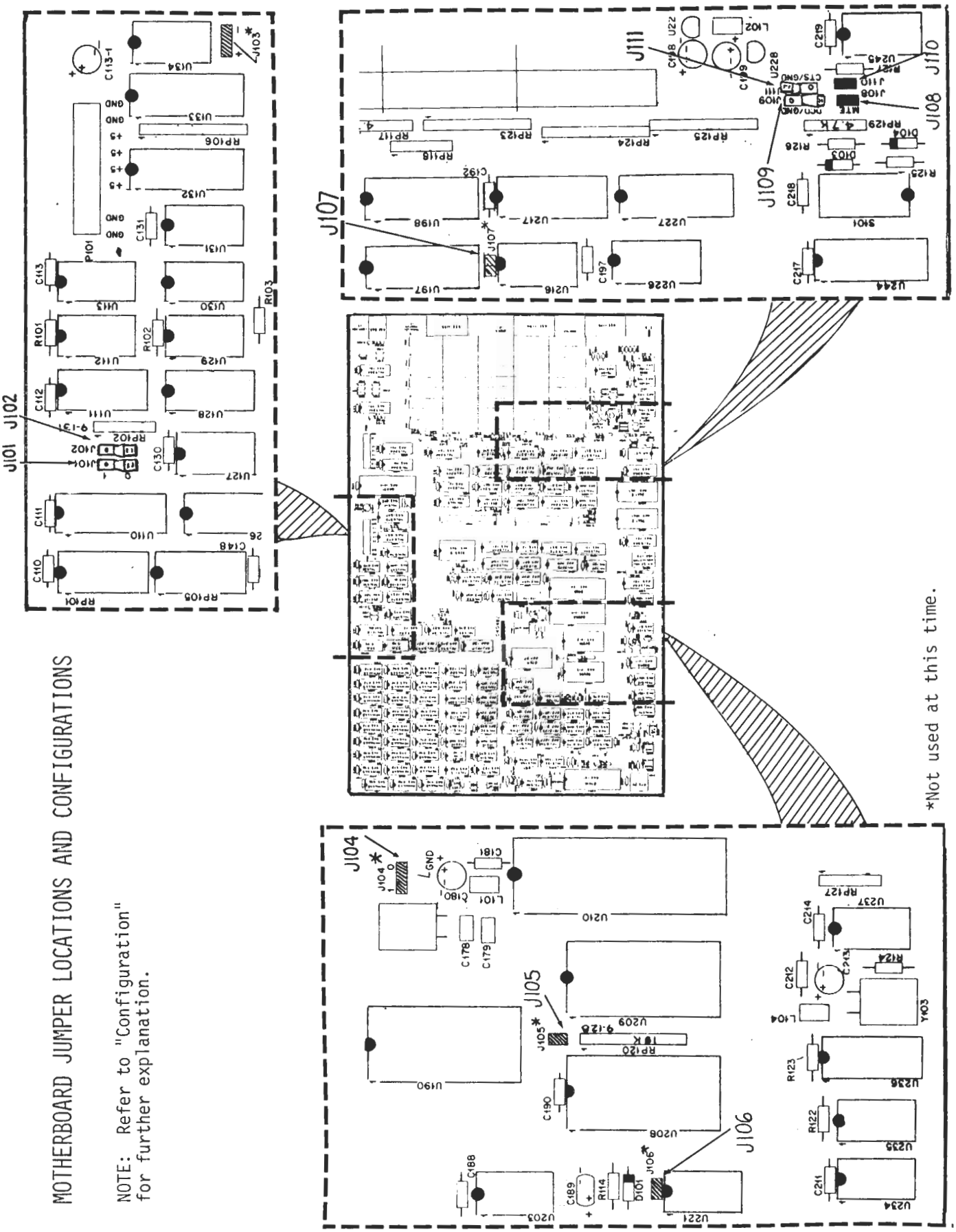
VISUAL CHECKS

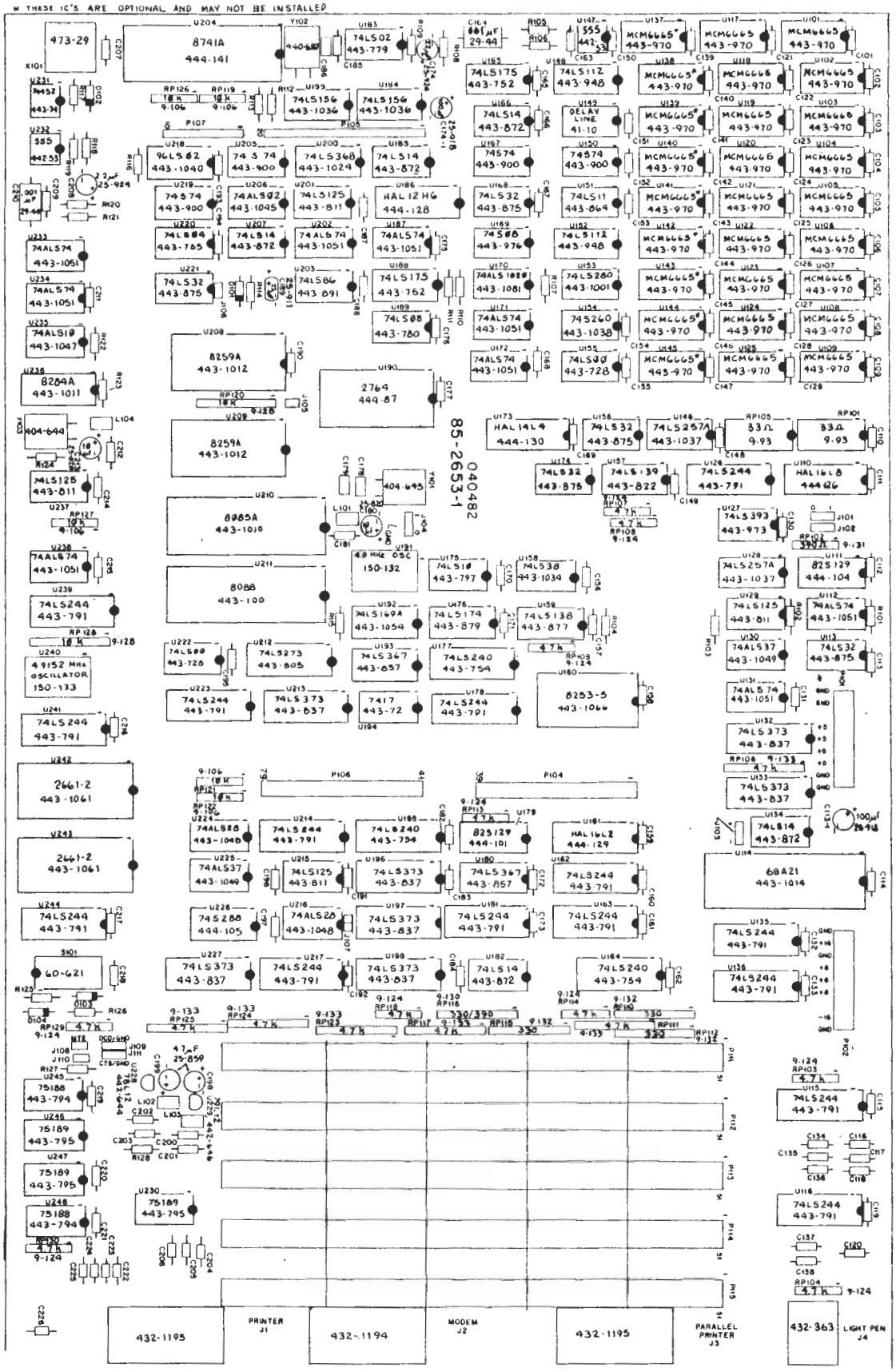


MOTHERBOARD CONNECTIONS TO
VIDEO BOARD
AND
POWER SUPPLY

MOTHERBOARD JUMPER LOCATIONS AND CONFIGURATIONS

NOTE: Refer to "Configuration" for further explanation.





7-82

MOTHERBOARD (HE-181-3630-1)
COMPONENT LOCATIONS AND VALUES

TROUBLESHOOTING

INTRODUCTION

The following procedure will help you repair the motherboard to the point where you can boot a diagnostic disk. Diagnostic programs will allow more thorough and faster testing of the H/Z-100.

Currently, there aren't many diagnostic programs available. For this reason, we've included some checkout procedures that will help you test circuits that aren't critical to the boot-up operation. Though these tests aren't comprehensive, they'll help you narrow the problem down to two or three components.

As diagnostic programs become available, we will publish them for inclusion in the Diagnostics section of this manual. Also, if you develop any troubleshooting techniques or diagnostic programs that you'd like to share, send it to:

Heath Company
Service Publications and Training
Dept. 741
Benton Harbor, Mi. 49022

We will evaluate your submission, and when approved, publish it for inclusion in the Service Bulletins or Diagnostics sections of this manual. Be sure to include a complete description of the troubleshooting technique, symptoms caused by the failed component, and any special equipment needed to repair the problem. If submitting a diagnostic program, we will need a copy of the source listing; preferably on disk.

SERVICE GUIDE

As you become more experienced troubleshooting the H/Z-100, you'll be able to skip this section and go directly to the group of circuits causing the problem. Until then, use the following guide to locate the most likely circuits to test for a particular symptom.

Detailed checkout procedures for the major circuits on the video board follow the service guide. If this is your first time troubleshooting the H/Z-100, read the introduction to the checkout procedure before proceeding with those tests.

Finally, bear in mind that these test procedures are for isolating problems on the video board. All the other modules in the H/Z-100 must be known to be operating properly. Otherwise, you won't get the correct results.

1. Video circuits won't initialize. No power-up/reset beep heard.

   Perform the following tests in the order listed:

   Reset Circuits Tests
   Processor Swap Tests
   General CPU Tests
   Interrupt Circuits Tests

2. Video circuits won't initialize. Power-up/reset beep heard.

   Check U178 and U223 (schematic MB2).

   Perform the following tests in the order listed:

   E-Clock Logic Tests
   Interrupt Circuits Tests
   I/O Port Decoder Tests

3. System powers up properly, but characters on CRT are missing or distorted.

   Check the system monitor, U190 (schematic MB2).

   Perform the following tests:

   Interrupt Circuits Tests
   I/O Port Decoder Tests

4. Keyboard doesn't operate properly.

   Perform the following tests:

   Keyboard Circuit Tests
   I/O Port Decoder Tests

5. Z-DOS will not complete the boot-up procedure; display locks up.

   Perform the following test:

   Timer Circuits Test

6. When booting Z-DOS, the CRT displays a parity error message.

   Check parity circuits: U158, U152, U153, U151, U101, U117, and U137 (schematic MB3).

   Perform the following tests:

   Memory Circuits Tests #1
   Memory Circuits Tests #2
   I/O Port Decoder Tests

7. Intermittent problem when running a Z-DOS program.

   Perform the system memory test described in the Diagnostics section (MEMTEST, option S).

8. Parallel printer port doesn't work.

   Check Diagnostics section for in-depth testing.

   Perform the following test:

   Parallel Port Tests

9. Serial printer port doesn't work.

   Check Diagnostics section for in-depth testing.

   Perform the following test:

   Serial Port A Tests

10. MODEM port doesn't work.

    Check Diagnostics section for in-depth testing.

    Perform the following test:

    Serial Port B Tests

INTRODUCTION TO CHECKOUT PROCEDURES

In the following tests, you need only test the ICs in the left column indicated by an asterisk (*). If you don't get the suggested logic state, then check each IC listed immediately to the right. The logic states for these ICs are listed in the left column below the ICs with the asterisks.

Continue tracing backwards using this procedure until you test an IC that matches the suggested logic state. The previous IC that you tested is likely the bad IC.

Before you replace the suspected IC, check the other lines leading up to it. You must do this because this checkout procedure gives only the most likely causes to the problem. It doesn't cover such things as open ground foils, foil runs shorted together, open resistors, or missing power supplies.

To help you locate the IC on a schematic, the schematic number is shown in parenthesis to the right of the IC under test.

Unless instructed otherwise, perform these tests with the H/Z-100 configured for 5-1/4" drives (primary) and with auto-boot defeated. See the Configuration section. Also, unless noted otherwise, all logic states are those present after a power-up reset or CTRL/RESET.

BUS CONTROL OUTPUT TESTS

CHECK			IF NOT OKAY, CHECK
*U180-3	= P	(MB1)	U180-2, U180-1, U180-15
*U180-5	= P	(MB1)	U180-4, U180-1, U180-15
*U180-7	= P	(MB1)	U180-6, U180-1, U180-15
*U180-9	= L	(MB1)	U180-10, U180-1, U180-15
*U180-11	= P	(MB1)	U180-12, U180-1, U180-15

Go to BUS CONTROL OUTPUT RESET TESTS.

U180-1	= L	(MB1)	U182-6
U180-2	= P	(MB1)	U219-9
U180-4	= P	(MB1)	U234-9
U180-6	= P	(MB1)	U206-10
U180-10	= L	(MB1)	See PROCESSOR SWAP TESTS.
U180-12	= P	(MB1)	U235-12
U180-15	= L	(MB1)	U182-6
U182-5	= H	(MB1)	Check S-100 bus, pin 19.
U182-6	= L	(MB1)	U182-5
U206-8	= P	(MB1)	U219-9
U206-9	= P	(MB1)	See GENERAL CPU TESTS.
U206-10	= P	(MB1)	U206-8, U206-9
U219-1	= P	(MB1)	U219-3, U219-8
U219-3	= P	(MB1)	U221-3
U219-5	= P	(MB1)	U219-3, U219-1
U219-8	= P	(MB1)	U219-11, U219-12, U219-13. NOTE: If you're "stuck in a loop" on this test, see the BUS CONTROL OUTPUT RESET TESTS.
U219-9	= P	(MB1)	U219-11, U219-12, U219-13
U219-11	= P	(MB1)	See CLOCK CIRCUITS TESTS.
U219-12	= P	(MB1)	U219-5
U219-13	= H	(MB1)	See RESET CIRCUITS TESTS.
U220-12	= P	(MB1)	See GENERAL CPU TESTS.

U221-1	= P	(MB1)	See GENERAL CPU TESTS.
U221-2	= L	(MB1)	U237-11
U221-3	= P	(MB1)	U221-1, U221-2
U234-9	= P	(MB1)	U234-11, U234-12
U234-11	= P	(MB1)	See CLOCK CIRCUITS TESTS.
U234-12	= P	(MB1)	U219-8
U235-1	= P	(MB1)	U234-9
U235-2	= P	(MB1)	U219-8
U235-12	= P	(MB1)	U235-1, U235-2, U235-13
U235-13	= P	(MB1)	U220-12
U237-11	= L	(MB1)	U237-12
U237-12	= L	(MB1)	See GENERAL CPU TESTS.

==========

BUS CONTROL OUTPUT RESET TESTS

Press and release the CTRL/RESET keys as you make the following measurements.

CHECK			IF NOT OKAY, CHECK
*U180-3	= L	(MB1)	U180-2
*U180-5	= H	(MB1)	U180-4
*U180-7	= L	(MB1)	U180-6
*U180-9	= L	(MB1)	U180-10
*U180-11	= H	(MB1)	U180-12

End of tests.

U180-2	= L	(MB1)	U219-9
U180-4	= H	(MB1)	U234-9
U180-6	= L	(MB1)	U206-10
U180-10	= L	(MB1)	See PROCESSOR SWAP TESTS.
U180-12	= H	(MB1)	U235-12
U206-9	= H	(MB1)	See GENERAL CPU TESTS.
U206-10	= L	(MB1)	U206-9
U219-8	= H	(MB1)	U219-13
U219-9	= L	(MB1)	U219-13
U219-13	= L	(MB1)	See RESET CIRCUITS TESTS.
U220-12	= L	(MB1)	See GENERAL CPU TESTS.
U234-9	= H	(MB1)	U234-11, U234-12
U234-11	= P	(MB1)	See CLOCK CIRCUITS TESTS.
U234-12	= P	(MB1)	U219-8
U235-12	= H	(MB1)	U235-13
U235-13	= L	(MB1)	U220-12

CLOCK CIRCUITS TESTS

CHECK			IF NOT OKAY, CHECK
*U192-11	= P	(MB1)	U192-2
*U216-4	= P	(MB1)	U216-5
*U225-3	= P	(MB1)	U225-1, U225-2
*U225-11	= P	(MB1)	U225-12, U225-13

End of tests.

U188-2	= H	(MB1)	U188-4
U188-4	= H	(MB1)	See PROCESSOR SWAP TESTS
U188-5	= H	(MB1)	U188-2
U188-6	= L	(MB1)	U188-7
U188-7	= H	(MB1)	U188-9, U188-5
U188-9	= P	(MB1)	U225-6
U188-11	= L	(MB1)	U188-9, U188-12
U188-12	= H	(MB1)	U188-7
U191-8	= P	(MB1)	U191 or C115 is defective.
U192-2	= P	(MB1)	U191-8
U192-14	= P	(MB1)	U192-2
U200-1	= H	(MB1)	U203-6
U200-2	= P	(MB1)	U210 (8085 CPU) is defective.
U200-13	= Pulse 180 degrees out of phase with U200-14 (use dual-trace oscilloscope).		If not 180 degrees out of phase, check U200-15 and U200-1. If missing, then U236 is defective.
U200-15	= L	(MB1)	U203-3
U203-2	= L	(MB1)	U188-6
U203-3	= L	(MB1)	U203-2
U203-4	= H	(MB1)	U188-7
U203-6	= H	(MB1)	U203-4
U203-8	= H	(MB1)	U203-9, U203-10
U203-9	= H	(MB1)	U188-7
U203-10	= L	(MB1)	U188-11

U216-5	= P	(MB1)	U192-14
U225-1	= P	(MB1)	U200-13
U225-2	= H	(MB1)	U203-8
U225-5	= P	(MB1)	U200-13
U225-6	= P	(MB1)	U225-5
U225-12	= H	(MB1)	U203-8
U225-13	= P	(MB1)	U200-13, U200-2

E-CLOCK LOGIC TESTS

CHECK			IF NOT OKAY, CHECK
*U224-4	= P	(MB2)	U224-5, U224-6
*U224-10	= P	(MB2)	U224-8, U224-9
*U224-13	= P	(MB2)	U224-11, U224-12
*U238-9	= P	(MB2)	U238-10, U238-11, U238-12

Go to E CLOCK LOGIC RESET TESTS

U195-6	= P	(MB2)	See BUS CONTROL OUTPUT CIRCUIT TESTS.
U195-7	= P	(MB2)	U195-13
U195-9	= P	(MB2)	U195-11
U195-11	= P	(MB2)	See CLOCK CIRCUITS TESTS.
U195-13	= P	(MB2)	See BUS CONTROL OUTPUT CIRCUITS TESTS.
U195-14	= P	(MB2)	U195-6
U214-4	= P	(MB2)	See STATUS CIRCUITS TESTS.
U214-6	= P	(MB2)	See STATUS CIRCUITS TESTS.
U214-8	= P	(MB2)	See BUS CONTROL OUTPUT CIRCUITS TESTS.
U214-12	= P	(MB2)	U214-8
U214-14	= P	(MB2)	U214-6 See BUS CONTROL OUTPUT CIRCUITS TESTS.
U214-16	= P	(MB2)	U214-4
U214-18	= P	(MB2)	U214-2
U220-8	= P	(MB2)	U220-9
U220-9	= P	(MB2)	U221-8
U221-8	= P	(MB2)	U221-10, U221-9
U221-9	= P	(MB2)	U233-9
U221-10	= L	(MB2)	See RESET CIRCUITS TESTS.

U224-1	= P	(MB2)	U224-2, U224-3
U224-2	= P	(MB2)	U195-14
U224-3	= P	(MB2)	U214-12
U224-5	= P	(MB2)	U224-1
U224-6	= P	(MB2)	U238-6
U224-8	= P	(MB2)	U214-14
U224-9	= P	(MB2)	U214-16
U224-10	= P	(MB2)	U224-8, U224-9
U224-11	= P	(MB2)	U195-7
U224-12	= P	(MB2)	U214-18
U224-13	= P	(MB2)	U224-11, U224-12
U233-9	= P	(MB2)	Check the foil runs to U233, pins 11, 12, and 13 against the schematic. If these are okay, then replace U233.
U238-1	= P	(MB2)	U238-8
U238-2	= P	(MB2)	U238-8
U238-3	= P	(MB2)	U195-9
U238-6	= P	(MB2)	U238-1, U238-2, U238-3
U238-8	= P	(MB2)	U238-10, U238-11, U238-12
U238-10	= P	(MB2)	U220-8
U238-11	= P	(MB2)	U224-13
U238-12	= P	(MB2)	U224-10

E-CLOCK LOGIC RESET TESTS

Press and release the CTRL/RESET keys as you make the following measurements.

CHECK			IF NOT OKAY, CHECK
*U224-4	= L	(MB2)	U224-6
*U233-9	= L	(MB2)	U233-13
*U238-9	= H	(MB2)	U238-10

End of tests.

U220-8	= L	(MB2)	U220-9
U220-9	= H	(MB2)	U221-8
U221-8	= H	(MB2)	U221-10
U221-10	= H	(MB2)	See RESET CIRCUITS TESTS.
U224-6	= H	(MB2)	U238-6
U233-13	= L	(MB2)	U238-8
U238-1	= L	(MB2)	U238-8
U238-6	= H	(MB2)	U238-1
U238-8	= L	(MB2)	U238-10
U238-10	= L	(MB2)	U220-8

GENERAL CPU TESTS

In the following tests, the CPU will not be able to initialize the video board. This results in a high-pitched whine from the monitor fly-back transformer and an incorrect raster on the CRT. To avoid this distraction, disconnect the video cable (and power cable for the all-in-one model) between the video board and monitor (or video sweep board for the all-in-one).

Now perform the following steps.

-- Unplug U187 (schematic MB1).

   This puts both processors into a hold state.

-- Unplug U217 (schematic MB1).

   This isolates the CPUs from the monitor ROM.

-- Plug the programming plug described under Systems Troubleshooting into the socket at U187.

-- Turn on the H/Z-100 and press and release the CTRL/RESET keys once.

-- Refer to schematic MB1 and check for a logic one on each line of the address/data bus, AD0-AD7.

   If any line is low, check for a short circuit on the bus. This includes internal shorts on U211, U210, U198, U197, U209, U208 and U212.

   If the lines are pulsing, then one of the CPUs isn't in a hold state. Check U211-30 and U210-38. If either pin is logic zero, replace the appropriate IC. Also check for leakage to ground on U211-31 and U210-39.

-- Check the logic states of the ICs in the following chart. If any are incorrect, check the suggested ICs in the right column. Otherwise go on to the next test.

CHECK		IF NOT OKAY, CHECK
*U211-19 = P	(MB1)	U236 or Y103 defective.
*U211-22 = P	(MB1)	U336-5
*U211-29 = P	(MB1)	U211 defective.
*U211-32 = P	(MB1)	U211 defective.

Go on to the next test.

U177-4 = H	(MB1)	Short on pin 3 of S-100 bus.
U177-12 = P	(MB1)	U177-13
U177-13 = P	(MB1)	Short on pin 72 of S-100 bus, or U194-12 defective (MB2).
U177-16 = L	(MB1)	U177-4
U205-9 = P	(MB1)	U205-11, U205-12, U205-13
U205-11 = P	(MB1)	Restore U187 and U217 and perform the CLOCK CIRCUITS TEST.
U205-12 = P	(MB1)	U206-13
U205-13 = H	(MB1)	U206-1
U206-1 = H	(MB1)	U206-2, U206-3
U206-2 = L	(MB1)	U226-9
U206-3 = L	(MB1)	U221, U237, U210, or U211 defective.
U206-11 = P	(MB1)	U177-12
U206-12 = L	(MB1)	U177-16
U220-10 = H	(MB1)	U220-11
U220-11 = L	(MB1)	U221, U237, U210, or U211 defective.
U226-9 = L	(MB1)	U226-10, U226-11, U226-12, U226-13, U226-14
U226-10 = H	(MB1)	U210, U211, or U237 defective.
U226-11 = H	(MB1)	U210, U211, or U237 defective.
U226-12 = H	(MB1)	U210 or U211 defective.
U226-13 = H	(MB1)	Restore U187 and U217 and perform the PROCESSOR SWAP TESTS.
U226-14 = H	(MB1)	U233-5
U233-1 = H	(MB1)	U220-10
U233-3 = P	(MB1)	Restore U187 and U217 and perform the CLOCK CIRCUITS TESTS.
U233-5 = H	(MB1)	U233-1, U233-3
U236-4 = P	(MB1)	U205-9
U236-5 = P	(MB1)	U236-4

-- Check for the following logic states on the 8085 CPU, U210. If any are incorrect, replace U210.

Pin 29 = H
Pin 30 = L
Pins 31-34 = H
Pin 39 = P

-- Connect a jumper wire from U187-9 to ground.

This will activate the 8085 CPU.

-- Reset the computer once to ensure that the circuits are in a known state.

-- Check for pulses on pins 12-19 and pins 21-28 of U210.

If incorrect, replace U210. Also check for shorted or open circuits on the address/data bus.

-- Check for the following logic states on U210. If any are incorrect, replace U210.

Pin 29 = H
Pins 30-33 = P
Pin 34 = L
Pin 38 = L
Pin 39 = L

-- Remove the jumper wire from U187-9.

-- Connect the jumper wire from ground to U187-5.

This will activate the 8088 CPU.

-- Reset the computer once to ensure that the circuits are in a known state.

-- Check for pulses on pins 2-16 and 36-39 on U211.

If any are incorrect, replace U211. Also check the appropriate bus line for short circuits.

-- Check for the following logic states on U211. If any are incorrect, replace U211.

Pin 25 = P
Pin 27 = P
Pin 28 = L
Pin 29 = P
Pins 30-31 = L
Pin 32 = P
Pin 34 = P

-- Check for the following logic states. If incorrect, check U213, U193, and U212 (MB1).

U213-2 = P
U213-5 = P
U213-6 = P
U213-9 = P
U213-12 = L
U213-15 = L
U213-16 = L
U213-19 = L

-- Check the output pins (2, 5, 6, 9, 12, 15, 16, and 19) of U197 and U196 for pulses (MB1).

If any of these lines aren't pulsing, replace the appropriate IC.

-- Check for pulses on the following pins of the socket of U217 (MB1): 2, 4, 6, 8, 11, 13, 15, 17.

If any pulses are missing, check U244 and U241 on schematic MB4. Also check the following components on schematic MB2.

U239
U161 (ROMSEL)
U190 (MTR-100)

Pins 11-19, 20, and 22 of U190 should pulse. If not, then check the above three ICs and U195-16 (MB2).

-- Restore U187 and U217 to their sockets.

Tests complete.

INTERRUPT TESTS

CHECK		IF NOT OKAY, CHECK
*U208-18 = L	(MB1)	U177-18
*U208-19 = L	(MB1)	U172-9
*U208-20 = H	(MB1)	See TIMER CIRCUITS TEST.
*U208-21 = L	(MB1)	U209-17
*U208-22 = L	(MB1)	U222-8
*U208-23 = L	(MB1)	U222-11
*U208-24 = P	(MB1)	U207-4
*U208-25 = L	(MB1)	U207-12
*U210-6 = L	(MB1)	U189-11
*U210-10 = L	(MB1)	U189-3
*U211-17 = L	(MB1)	U189-8
*U211-18 = P	(MB1)	U189-6

End of tests.

J104 = Ground	(MB1)	J104 is a foil run to ground; no connector pins are installed here. If U156-5 = H, then J104 is open or connected to U177-14.
U114-38 = P	(MB4)	See PARALLEL PORT TESTS.
U134-12 = P	(MB4)	U134-13
U134-13 = P	(MB4)	U114-38
U151-8 = P	(MB3)	See MEMORY CIRCUITS TEST.
U152-9 = L	(MB3)	U152-11, U152-13, U152-14
U152-11 = P	(MB3)	U153 or U151 is defective. Also check parity RAM.
U152-13 = L	(MB3)	U151-8
U152-14 = L	(MB3)	See MEMORY CONTROL LATCH TEST.
U155-8 = H	(MB1)	U155-9, U155-10
U155-9 = P	(MB1)	U156-6
U155-10 = L	(MB1)	U172-5

U156-4 = P	(MB1)	U202-9
U156-5 = L	(MB1)	U156-8
U156-6 = P	(MB1)	U156-4, U156-5
U156-8 = L	(MB1)	U156-9, U156-10
U156-9 = L	(MB1)	U182-10
U156-10 = L	(MB1)	J104, U177-14
U158-4 = L	(MB3)	U152-9
U158-5 = L	(MB3)	U152-9
U158-6 = H	(MB3)	U158-4, U158-5
U158-8 = P	(MB1)	U158-10
U158-10 = P	(MB1)	U208-17
U164-2 = H	(MB1)	Pin 4 of S-100 bus shorted to ground.
U164-3 = L	(MB1)	U164-17
U164-4 = H	(MB1)	Pin 5 of S-100 bus shorted to ground.
U164-5 = L	(MB1)	U164-15
U164-6 = H	(MB1)	Pin 6 of S-100 bus shorted to ground.
U164-7 = L	(MB1)	U164-13
U164-8 = H	(MB1)	Pin 7 of S-100 bus shorted to ground.
U164-9 = L	(MB1)	U164-11
U164-11 = H	(MB1)	Pin 11 of S-100 bus shorted to ground.
U164-12 = L	(MB1)	U164-8
U164-13 = H	(MB1)	Pin 10 of S-100 bus shorted to ground.
U164-14 = L	(MB1)	U164-6
U164-15 = H	(MB1)	Pin 9 of S-100 bus shorted to ground.
U164-16 = L	(MB1)	U164-4
U164-17 = H	(MB1)	Pin 8 of S-100 bus shorted to ground.
U164-18 = L	(MB1)	U164-2
U171-8 = L	(MB1)	U171-10, U171-11, U171-12, U171-13
U171-9 = H	(MB1)	U171-8
U171-10 = H	(MB1)	U155-8
U171-11 = L	(MB1)	U206-4
U171-12 = P	(MB1)	See GENERAL CPU TESTS.
U171-13 = H	(MB1)	See the RESET CIRCUITS TESTS.

U172-1 = H	(MB1)	See the RESET CIRCUITS TESTS.
U172-2 = P	(MB1)	See GENERAL CPU TESTS.
U172-3 = L	(MB1)	U206-4
U172-5 = L	(MB1)	U172-1, U172-2, U172-3
U172-6 = H	(MB1)	U172-5
U172-9 = L	(MB1)	U172-11, U172-12, U172-13
U172-11 = L	(MB1)	U206-4
U172-12 = P	(MB1)	See GENERAL CPU TESTS.
U172-13 = H	(MB1)	See RESET CIRCUITS TESTS.
U177-2 = H	(MB1)	U158-6 or short circuit on pin 98 of S-100 bus.
U177-3 = P	(MB1)	U177-17
U177-6 = H	(MB1)	Short circuit on pin 13 of S-100 bus.
U177-14 = L	(MB1)	U177-6
U177-17 = P	(MB1)	U158-8 or short circuit on S-100 bus, pin 73.
U177-18 = L	(MB1)	U177-2
U182-10 = L	(MB1)	U182-11
U182-11 = H	(MB1)	Pin 12 of S-100 bus shorted to ground.
U189-1 = P	(MB1)	U202-9
U189-2 = L	(MB1)	U220-2
U189-3 = L	(MB1)	U189-1, U189-2
U189-4 = P	(MB1)	U202-9
U189-5 = H	(MB1)	U171-9
U189-6 = P	(MB1)	U189-4, U189-5
U189-8 = L	(MB1)	U189-9, U189-10
U189-9 = H	(MB1)	U171-9
U189-10 = L	(MB1)	U156-8
U189-11 = L	(MB1)	U189-12, U189-13
U189-12 = L	(MB1)	U220-2
U189-13 = L	(MB1)	U156-8
U202-1 = P	(MB1)	U177-3
U202-2 = P	(MB1)	U177-3
U202-3 = P	(MB1)	See CLOCK CIRCUITS TEST.
U202-5 = P	(MB1)	U202-1, U202-2, U202-3
U202-9 = P	(MB1)	U202-12, U202-11
U202-11 = P	(MB1)	See CLOCK CIRCUITS TESTS.
U202-12 = P	(MB1)	U202-5

U206-4 = L	(MB1)	U206-5, U206-6
U206-5 = H	(MB1)	See I/O PORT DECODER TESTS.
U206-6 = P	(MB1)	See the BUS CONTROL OUTPUT TESTS.
U207-3 = P	(MB1)	U216-13
U207-4 = P	(MB1)	U207-3
U207-12 = L	(MB1)	U207-13
U207-13 = H	(MB1)	See PARALLEL PORT TESTS.
U208-17 = P	(MB1)	U208-18, U208-19, U208-20, U208-21, U208-22, U208-23, U208-24, U208-25
U208-18 = L	(MB1)	U177-18
U208-19 = L	(MB1)	U172-9
U208-20 = H	(MB1)	See TIMER CIRCUITS TEST.
U208-21 = L	(MB1)	U209-17
U208-22 = L	(MB1)	U222-8
U208-23 = L	(MB1)	U222-11
U208-24 = P	(MB1)	U207-4
U208-25 = L	(MB1)	U207-12
U209-17 = L	(MB1)	U209-18, U209-19, U209-20, U209-21, U209-22, U209-23, U209-24, U209-25
U209-18 = L	(MB1)	U164-18
U209-19 = L	(MB1)	U164-16
U209-20 = L	(MB1)	U164-14
U209-21 = L	(MB1)	U164-12
U209-22 = L	(MB1)	U164-3
U209-23 = L	(MB1)	U164-5
U209-24 = L	(MB1)	U164-7
U209-25 = L	(MB1)	U164-9
U216-11 = L	(MB1)	See KEYBOARD TESTS.
U216-12 = P	(MB1)	U134-12
U216-13 = P	(MB1)	U216-11, U216-12
U220-1 = H	(MB1)	U225-9, U225-10
U220-2 = L	(MB1)	U220-1
U222-8 = L	(MB4)	U222-10
U222-10 = H	(MB4)	See SERIAL PORT A TESTS.
U222-11 = L	(MB4)	U222-13
U222-13 = H	(MB4)	See SERIAL PORT B TESTS.
U225-9 = L	(MB1)	U171-8
U225-10 = H	(MB1)	U172-6

KEYBOARD CIRCUIT TESTS

The 2-line-to-4-line decoders, U199 and U184, have open-collector outputs. These outputs are left floating; that is, they're not tied to logic one through pull-up resistors. So, although the outputs are continually switching on and off, you won't see a pulse unless a key is pressed.

Note, however, that some logic probes will show pulses on the decoder outputs when no key is pressed. This is due to the probe sensitivity and system noise. If your logic probe shows pulses where there should be none, check with an oscilloscope.

-- Turn on the H/Z-100.

-- Check for pulses at pins 21 through 24 of U204.

   If these pulses aren't present, then check the logic levels of pins 2 through 10 against the schematic. If these are incorrect, then check the I/O port decoder, the status circuits, the bus control output circuits, and the reset circuits.

   Also check the crystal at Y102.

-- Turn off the H/Z-100.

-- Locate U185 (near P105 on the right-front side of the motherboard) and lift pin 11.

-- Turn on the H/Z-100.

-- Connect a jumper wire between U185-11 and ground.

   This places both CPUs into the HOLD state to prevent the monitor from sounding the bell when you perform the following tests.

-- Press the SPACE BAR once.

You should hear a key click from the audio transducer, X101. If not, then check U231, U232, U218, and U204. If U204-38 pulses when you press the SPACE BAR, then skip the following steps and perform the tests under "Keyboard Test Chart."

-- Simultaneously press the left SHIFT and RESET keys.

The display, if connected, will go blank. This is normal.

-- Press the SPACE BAR 18 times.

You should hear a key click for the first 17 presses; the 18th should be silent. This indicates the internal type-ahead buffer of U204 is working properly.

-- Reset the computer.

-- Press and hold the SPACE BAR down.

The keyclick should occur 17 times and then go silent. This verifies U204's auto-repeat function.

-- Reset the computer.

KEYBOARD TEST CHART

Measure the following pins on P105 as you press the indicated key. Unless noted otherwise, the pin should pulse as you hold the key down. Note that the line under test will latch to a logic one after 17 key clicks, so you must periodically reset the computer.

Refer to the keyboard schematic in the Keyboard section of this manual to check the keys not listed in the following chart.

P105 No.	Key	Possible Cause
1	FAST REPEAT	U204-39, U183, U184, RP119
2	CTRL (UP = H)	RP119, U204-1
	CTRL (DOWN = L)	Ground return (P107-2)
3	BREAK	U204-34, U183, U184, RP119
4	RESET (UP = H)	R108
	RESET (DOWN = L)	Ground return (P107-2)
5	L. SHIFT (UP = L)	U204-39, U183, U184, RP119
	L. SHIFT (DOWN = H)	
6	CAPS LOCK (UP = L)	U204-39, U183, U184, RP119
	CAPS LOCK (DOWN = H)	
7	TAB	U204-33, U183, U184, RP119
8	R. SHIFT (UP = L)	U204-39, U183, U184, RP119
	R. SHIFT (DOWN = H)	
9	F2	U204-32, U199, RP119
10	4/$	U204-31, U183, U184, RP126
11	T	U204-30, U199, RP126
12	F9	U204-29, U199, RP126
13	P	U204-29, U199, RP126
14	[	U204-28, U183, U184, RP126
15	K	U204-27, U199, RP126
16	M	U204-28, U199, RP126
17	HOME	U204-34, U199, RP119
18	ENTER	U204-27, U199, RP126
19	+1.5 volts	R112, LED in RESET key
20	GROUND	R112, LED in RESET key

-- Turn off the computer.

-- Restore U185-11 to its original condition.

If you're still having keyboard problems, then check the monitor ROM, I/O port decoder, and bus lines between the CPU and U204.

I/O PORT DECODER TESTS

CHECK			IF NOT OKAY, CHECK
*U157-4	= H	(MB2)	U157-1, U157-2, U157-3
*U157-5	= P	(MB2)	U157-1, U157-2, U157-3
*U157-6	= P	(MB2)	U157-1, U157-2, U157-3
*U157-9	= P	(MB2)	U157-15, U157-4, U157-13
*U157-10	= P	(MB2)	U157-15, U157-4, U157-13
*U157-11	= H	(MB2)	U157-15, U157-4, U157-13
*U157-12	= P	(MB2)	U157-15, U157-14, U157-13
*U159-7	= P	(MB2)	U159-4, U159-1, U159-2, U159-3
*U159-9	= H	(MB2)	U159-4, U159-1, U159-2, U159-3
*U159-10	= H	(MB2)	U159-4, U159-1, U159-2, U159-3
*U159-11	= H	(MB2)	U159-4, U159-1, U159-2, U159-3
*U159-12	= P	(MB2)	U159-3
*U159-12	= P	(MB2)	U159-4, U159-1, U159-2,
*U179-4	= P	(MB2)	U179-13 and INPUT CHECKS

End of test.

INPUT CHECKS		(MB2)	U179-1, U179-2, U179-2,
INPUT CHECKS		(MB2)	U179-3, U179-4, U179-5,
INPUT CHECKS		(MB2)	U179-6, U179-7, U179-15
U157-1	= P	(MB2)	U179-11
U157-2	= P	(MB2)	U181-16
U157-3	= P	(MB2)	U181-14
U157-13	= P	(MB2)	U181-12
U157-14	= P	(MB2)	U181-14
U157-15	= P	(MB2)	U179-10
U159-1	= P	(MB2)	U181-18
U159-2	= P	(MB2)	U181-16
U159-3	= P	(MB2)	U181-14
U159-4	= P	(MB2)	U179-12

U179-1	= P	(MB2)	U181-7
U179-2	= P	(MB2)	U181-5
U179-3	= P	(MB2)	U181-3
U179-4	= P	(MB2)	U181-12
U179-5	= P	(MB2)	U181-18
U179-6	= P	(MB2)	U181-16
U179-7	= P	(MB2)	U181-14
U179-10	= P	(MB2)	U179-13 and INPUT CHECKS
U179-11	= P	(MB2)	U179-13 and INPUT CHECKS
U179-12	= P	(MB2)	U179-13 and INPUT CHECKS
U179-13	= P	(MB2)	See E-CLOCK LOGIC TESTS.
U179-15	= P	(MB2)	U181-9
U181-2	= P	(MB2)	See GENERAL CPU TESTS.
U181-3	= P	(MB2)	U181-17
U181-4	= P	(MB2)	See GENERAL CPU TESTS.
U181-5	= P	(MB2)	U181-15
U181-6	= P	(MB2)	See GENERAL CPU TESTS.
U181-7	= P	(MB2)	U181-13
U181-8	= P	(MB2)	See GENERAL CPU TESTS.
U181-9	= P	(MB2)	U181-11
U181-11	= P	(MB2)	See GENERAL CPU TESTS.
U181-12	= P	(MB2)	U181-8
U181-13	= P	(MB2)	See GENERAL CPU TESTS.
U181-14	= P	(MB2)	U181-6
U181-15	= P	(MB2)	See GENERAL CPU TESTS.
U181-16	= P	(MB2)	U181-4
U181-17	= P	(MB2)	See GENERAL CPU TESTS.
U181-18	= P	(MB2)	U181-2

I/O PORT DECODER RESET TESTS

Press and release the CTRL/RESET keys as you make the following measurements. A logic state in parenthesis indicates that the line under test pulses one or more times when you release the CTRL/RESET keys.

CHECK	IF NOT OKAY, CHECK
*U157-4 = (H) (MB2)	See GENERAL CPU TESTS.
*U157-11 = (H) (MB2)	See GENERAL CPU TESTS.
*U159-9 = (H) (MB2)	See GENERAL CPU TESTS.
*U159-11 = (H) (MB2)	See GENERAL CPU TESTS.

MEMORY CONTROL LATCH TESTS

CHECK			IF NOT OKAY, CHECK
*U176-1	= H	(MB2)	See RESET CIRCUITS TESTS.
*U176-9	= H	(MB2)	U221-11

Perform the suggestions under "MEMCTL NOTES."

U214-3	= H	(MB2)	U214-17
U214-17	= H	(MB2)	See the BUS CONTROL OUTPUT CIRCUIT TESTS.
U221-11	= H	(MB2)	U221-12, U221-13
U221-12	= H	(MB2)	U214-3
U221-13	= H	(MB2)	See the I/O PORT DECODER TESTS.

MEMCTL NOTES:

1. Check the data outputs and inputs of the memory control latch (U176 on MB2). Trace these back to U178 outputs and inputs. If U178's inputs are bad, check the S-100 bus and see GENERAL CPU TESTS.

2. Hold the CTRL/RESET keys down and take the following measurements. Pulses enclosed in parenthesis indicate that the line under test pulses at least once when you release the reset keys.

CHECK			IF NOT OKAY, CHECK
*U176-1	= L	(MB2)	See RESET CIRCUITS TESTS.
*U176-9	= (H)	(MB2)	U221-11

End of test.

U214-3	= (H)	(MB2)	U214-17
U214-17	= (H)	(MB2)	See the BUS CONTROL OUTPUT CIRCUITS TESTS.
U221-11	= (L)	(MB2)	U221-12, U221-13
U221-12	= (H)	(MB2)	U214-3
U221-13	= (H)	(MB2)	See the I/O PORT DECODER TESTS.

MEMORY CIRCUIT TESTS

TEST #1

1. Lift pin 2 of U169.
2. Temporarily jumper U169-2 to U170-6 as you apply power to the H/Z-100. This ensures that the display is properly initialized.
3. Connect U169-2 to ground.
4. Perform the following checks. If you are instructed to go to another test (other than MEMORY CIRCUITS TEST #2), restore U169 to its normal condition.

CHECK			IF NOT OKAY, CHECK
*U110-14	= H	(MB3)	U110-5
*U110-15	= H	(MB3)	U110-5
*U110-16	= H	(MB3)	U110-5
*U110-18	= H	(MB3)	U110-4, U110-6
*U110-19	= H	(MB3)	U110-4, U110-6
*U169-1	= H	(MB3)	U166-10
*U170-4	= P	(MB3)	U167-6
*U170-5	= P	(MB3)	U130-3
*U170-6	= H	(MB3)	U170-1

Go to MEMORY CIRCUITS TEST #2.

U110-4	= L	(MB3)	U149 Defective
U110-5	= L	(MB3)	U149 Defective
U110-6	= L	(MB3)	U149 Defective
U111-1	= L	(MB3)	See MEMORY CONTROL LATCH TESTS.
U111-2	= P	(MB3)	U163-16
U111-3	= P	(MB3)	U163-18
U111-4	= P	(MB3)	U162-9
U111-5	= P	(MB3)	U162-3
U111-6	= P	(MB3)	U162-5
U111-7	= P	(MB3)	U162-7
U111-9	= P	(MB3)	U111-1, U111-2, U111-3, U111-4, U111-5, U111-6, U111-7, U111-14, U111-15
U111-14	= P	(MB3)	U173-14
U111-15	= L	(MB3)	See MEMORY CONTROL LATCH TESTS.

U130-1	= P	(MB3)	U167-9
U130-2	= P	(MB3)	U214-7
U130-3	= P	(MB3)	U130-1, U130-2
U130-4	= P	(MB3)	See BUS CONTROL OUTPUT TESTS.
U130-6	= P	(MB3)	U130-4
U147-3	= P	(MB3)	U147 defective.
U148-1	= P	(MB3)	U147-3
U148-5	= H	(MB3)	U148-1, U148-15
U148-9	= H	(MB3)	U148-11, U148-13, U148-14
U148-11	= H	(MB3)	U148-5
U148-13	= P	(MB3)	U168-11
U148-14	= H	(MB3)	U173-16
U148-15	= H	(MB3)	U173-16
U151-1	= P	(MB3)	U195-7
U151-2	= H	(MB3)	U148-9
U151-12	= P	(MB3)	U151-1, U151-2, U151-13
U151-13	= P	(MB3)	U167-8
U152-1	= P	(MB3)	U168-11
U152-3	= P	(MB3)	U151-12
U152-6	= L	(MB3)	U152-1, U152-3, U152-15
U152-15	= H	(MB3)	U173-16
U154-3	= P	(MB3)	U195-12
U154-4	= P	(MB3)	U214-14
U154-6	= P	(MB3)	U154-4, U154-8, U154-10, U154-11
U154-8	= P	(MB3)	U214-9
U154-10	= P	(MB3)	U154-3, U154-12, U154-13, U111-9
U154-11	= P	(MB3)	U195-7
U154-12	= P	(MB3)	U195-7
U154-13	= P	(MB3)	U111-9
U162-3	= P	(MB2)	U162-17
U162-5	= P	(MB2)	U162-15
U162-7	= P	(MB2)	U162-13
U162-9	= P	(MB2)	U162-11
U162-11	= P	(MB2)	See GENERAL CPU TESTS.
U162-13	= P	(MB2)	See GENERAL CPU TESTS.
U162-15	= P	(MB2)	See GENERAL CPU TESTS.
U162-17	= P	(MB2)	See GENERAL CPU TESTS.

U163-2 = P	(MB2)	See GENERAL CPU TESTS.
U163-3 = L	(MB2)	U163-17
U163-4 = P	(MB2)	See GENERAL CPU TESTS.
U163-5 = L	(MB2)	U163-15
U163-6 = P	(MB2)	See GENERAL CPU TESTS.
U163-7 = L	(MB2)	U163-13
U163-8 = P	(MB2)	See GENERAL CPU TESTS.
U163-9 = L	(MB2)	U163-11
U163-11 = L	(MB2)	See GENERAL CPU TESTS.
U163-12 = P	(MB2)	U163-8
U163-13 = L	(MB2)	See GENERAL CPU TESTS.
U163-14 = P	(MB2)	U163-6
U163-15 = L	(MB2)	See GENERAL CPU TESTS.
U163-16 = P	(MB2)	U163-4
U163-17 = L	(MB2)	See GENERAL CPU TESTS.
U163-18 = P	(MB2)	U163-2
U166-10 = H	(MB3)	U166-11
U166-11 = L	(MB3)	U169-3
U167-1 = H	(MB3)	U173-15
U167-2 = P	(MB3)	U154-10
U167-3 = P	(MB3)	U130-6
U167-6 = P	(MB3)	U167-1, U167-2, U167-3
U167-8 = P	(MB3)	U167-11, U167-12, U167-13
U167-9 = P	(MB3)	U167-11, U167-12, U167-13
U167-11 = P	(MB3)	U130-6
U167-12 = P	(MB3)	U154-6
U167-13 = H	(MB3)	U173-15
U168-11 = P	(MB3)	U168-12
U168-12 = P	(MB3)	See CLOCK CIRCUITS TESTS.
U169-3 = L	(MB3)	If U169-3 = H, then replace U169. Otherwise, replace U149. Also check for open or shorted solder runs to U149.

U170-1	= L	(MB3)	U152-6
U173-1	= P	(MB3)	U163-14
U173-2	= P	(MB3)	U163-12
U173-3	= L	(MB3)	U163-3
U173-4	= L	(MB3)	U163-5
U173-5	= L	(MB3)	U163-7
U173-6	= L	(MB3)	U163-9
U173-14	= P	(MB3)	U173-1, U173-2, U173-3, U173-4, U173-5, U173-6
U173-15	= H	(MB3)	U173-18
U173-16	= H	(MB3)	U173-18
U173-18	= L	(MB3)	U149 defective or open foil run.
U195-7	= P	(MB2)	U195-13
U195-8	= P	(MB2)	See STATUS CIRCUITS TESTS.
U195-12	= P	(MB2)	U195-8
U195-13	= P	(MB2)	See BUS CONTROL OUTPUT TESTS.
U214-6	= P	(MB2)	See STATUS CIRCUITS TESTS.
U214-7	= P	(MB2)	U214-13
U214-9	= P	(MB2)	U214-11
U214-11	= P	(MB2)	See STATUS CIRCUITS TESTS.
U214-13	= P	(MB2)	See BUS CONTROL OUTPUT TESTS.
U214-14	= P	(MB2)	U214-6

TEST #2

Remove the jumper wire between U169-2 and ground so that U169-2 is floating.

CHECK		IF NOT OKAY, CHECK
*U110-13 = P	(MB3)	U110-4, U110-5, U110-7, U110-9
*U110-14 = P	(MB3)	U110-5, U110-7, U110-9, U110-11
*U110-15 = P	(MB3)	U110-5, U110-7, U110-9, U110-11
*U110-16 = P	(MB3)	U110-5, U110-7, U110-9, U110-11
*U110-17 = P	(MB3)	U110-1, U110-4, U110-6, U110-8
*U110-18 = P	(MB3)	U110-2, U110-4, U110-6, U110-8
*U110-19 = P	(MB3)	U110-3, U110-4, U110-6, U110-8
*U127-8 = P	(MB3)	U127-1
*U133-1 = P	(MB3)	U173-14
*U133-11 = P	(MB3)	U110-12
*U150-1 = P	(MB3)	U165-14
*U158-3 = P	(MB3)	U158-1, U158-2
*U169-1 = P	(MB3)	U169-1 & -3 should be the same logic states. If not, then replace U169. U166-10 & -11 should be opposite logic states. If not, then replace U166. U169-3 and U166-11 should be the same logic states. If not, then replace U149.

Restore U169 to its original condition. End of test.

U110-1 = P	(MB3)	U111-10
U110-2 = P	(MB3)	U111-11
U110-3 = P	(MB3)	U111-12
U110-4 = P	(MB3)	U149-12 defective.
U110-5 = P	(MB3)	U149-4 defective.

U110-6 = P	(MB3)	U169-3 defective.
U110-7 = P	(MB3)	U150-9
U110-8 = P	(MB3)	U152-5
U110-9 = P	(MB3)	U214-9
U110-11 = P	(MB3)	U194-6
U110-12 = P	(MB3)	U110-4, U110-7
U111-10 = P	(MB3)	U111 defective.
U111-11 = P	(MB3)	U111 defective.
U111-12 = P	(MB3)	U111 defective.
U127-1 = P	(MB3)	U173-16
U148-5 = P	(MB3)	U148-15
U148-9 = P	(MB3)	U148-11, U148-13, U148-14
U148-11 = P	(MB3)	U148-5
U148-13 = P	(MB3)	U168-11
U148-14 = P	(MB3)	U173-16
U148-15 = P	(MB3)	U173-16
U150-3 = P	(MB3)	U150-8
U150-5 = P	(MB3)	U150-3
U150-8 = P	(MB3)	U150-10, U150-11, U150-12
U150-9 = P	(MB3)	U150-10, U150-11, U150-12
U150-10 = P	(MB3)	U168-3
U150-11 = P	(MB3)	Open foil run between U169-3 and U150-11.
U150-12 = P	(MB3)	U152-6
U151-1 = P	(MB3)	U195-7
U151-2 = P	(MB3)	U148-9
U151-12 = P	(MB3)	U151-1, U151-2, U151-13
U151-13 = P	(MB3)	U167-8
U152-1 = P	(MB3)	U168-11
U152-3 = P	(MB3)	U151-12
U152-5 = P	(MB3)	U152-1, U152-3, U152-15
U152-6 = P	(MB3)	U152-1, U152-3, U152-15
U152-15 = P	(MB3)	U173-16
U158-1 = P	(MB3)	U150-5
U158-2 = P	(MB3)	U169-6
U165-9 = P	(MB3)	U168-11
U165-12 = P	(MB3)	U150-5
U165-14 = P	(MB3)	U165-9, U165-12
U166-12 = P	(MB3)	U166-13
U166-13 = P	(MB3)	U149 defective.

U167-8	= P	(MB3)	U167-13
U167-13	= P	(MB3)	U173-15
U168-1	= P	(MB3)	U149 defective.
U168-2	= P	(MB3)	U166-12
U168-3	= P	(MB3)	U168-1, U168-2
U168-8	= P	(MB3)	U168-9, U168-10
U168-9	= P	(MB3)	U214-9
U168-10	= P	(MB3)	U214-14
U168-11	= P	(MB3)	U168-12
U168-12	= P	(MB3)	See CLOCK CIRCUITS TESTS.
U169-4	= P	(MB3)	U169-11
U169-5	= P	(MB3)	U170-8
U169-6	= P	(MB3)	U169-4, U169-5
U169-11	= P	(MB3)	U169-12, U169-13
U169-12	= P	(MB3)	U111-9 defective.
U169-13	= P	(MB3)	U111-9 defective.
U170-8	= P	(MB3)	U170-9, U170-10
U170-9	= P	(MB3)	U214-5
U170-10	= P	(MB3)	U168-8
U173-9	= P	(MB3)	U149-12 defective.
U173-11	= P	(MB3)	U195-16
U173-12	= P	(MB3)	U169-6
U173-13	= P	(MB3)	U194-6
U173-14	= P	(MB3)	U173-11, U173-12, U173-13
U173-15	= P	(MB3)	U173-9, U173-18, U173-19
U173-16	= P	(MB3)	U173-9, U173-18, U173-19
U173-18	= P	(MB3)	U149-4 defective.
U173-19	= P	(MB3)	U150-9 defective.
U194-6	= P	(MB2)	See GENERAL CPU TESTS.
U195-4	= P	(MB2)	See BUS CONTROL OUTPUT TESTS.
U195-7	= P	(MB2)	U195-13
U195-13	= P	(MB2)	See BUS CONTROL OUTPUT TESTS.
U195-16	= P	(MB2)	U195-4
U214-5	= P	(MB2)	U214-15
U214-6	= P	(MB2)	See STATUS CIRCUITS TESTS.
U214-9	= P	(MB2)	U214-11
U214-11	= P	(MB2)	See STATUS CIRCUITS TESTS.
U214-14	= P	(MB2)	U214-6
U214-15	= P	(MB2)	See STATUS CIRCUITS TESTS.

PARALLEL PORT TESTS

CHECK		IF NOT OKAY, CHECK
*U114-10 = H	(MB4)	U116-16
*U114-11 = H	(MB4)	U116-12
*U114-18 = L	(MB4)	U134-2
*U114-19 = H	(MB4)	U116-16
*U115-3 = H	(MB4)	U115-17
*U115-5 = H	(MB4)	U115-15
*U115-6 = H	(MB4)	U115-4
*U115-7 = H	(MB4)	U115-13
*U115-9 = H	(MB4)	U115-11
*U115-12 = H	(MB4)	U115-8
*U115-14 = H	(MB4)	U115-6
*U115-18 = H	(MB4)	U115-2
*U116-14 = H	(MB4)	U116-6
*U116-18 = H	(MB4)	U116-2
*U134-12 = P	(MB4)	U134-13

End of test.

INPUT CHECKS	(MB4)	U114-23, U114-36, U114-35,
INPUT CHECKS	(MB4)	U114-25, U114-21, U114-34,
INPUT CHECKS	(MB4)	U114-26 through U114-33.
U114-2 = Z	(MB4)	See INPUT CHECKS.
U114-3 = Z	(MB4)	See INPUT CHECKS.
U114-4 = H	(MB4)	See INPUT CHECKS.
U114-5 = H	(MB4)	See INPUT CHECKS.
U114-6 = P	(MB4)	U116-5
U114-7 = P	(MB4)	See INPUT CHECKS.
U114-12 = Z	(MB4)	See INPUT CHECKS.
U114-13 = Z	(MB4)	See INPUT CHECKS.
U114-14 = Z	(MB4)	See INPUT CHECKS.
U114-15 = Z	(MB4)	See INPUT CHECKS.
U114-16 = Z	(MB4)	See INPUT CHECKS.
U114-17 = Z	(MB4)	See INPUT CHECKS.
U114-21 = P	(MB4)	U195-18
U114-23 = P	(MB4)	See I/O PORT DECODER TESTS.
U114-25 = P	(MB4)	See E-CLOCK LOGIC TESTS.

U114-26 through U114-33 = P	(MB4)	U136-1, U136-19, U135-1, U135-19 (NOTE: If these lines are okay, then check for shorts or opens on the bus; try replacing U136 and U135.)
U114-34 = H	(MB4)	See RESET CIRCUITS TESTS.
U114-35 = P	(MB4)	U181-16
U114-36 = P	(MB4)	U181-18
U114-38 = P	(MB4)	U114-6, U114-39, INPUT CHECKS.
U114-39 = P	(MB4)	U131-9
U115-2 = H	(MB4)	U114-4
U115-4 = Z	(MB4)	U114-2
U115-6 = Z	(MB4)	U114-3
U115-8 = Z	(MB4)	U114-12
U115-11 = Z	(MB4)	U114-13
U115-13 = Z	(MB4)	U114-14
U115-15 = Z	(MB4)	U114-15
U115-17 = Z	(MB4)	U114-16
U116-2 = Z	(MB4)	U114-17
U116-4 = H	(MB4)	RP103 or shorted foil run.
U116-5 = P	(MB4)	U116-15
U116-6 = H	(MB4)	U114-5
U116-8 = H	(MB4)	RP103 or shorted foil run.
U116-12 = H	(MB4)	U116-8
U116-15 = P	(MB4)	See GENERAL CPU TESTS and VIDEO BOARD TROUBLESHOOTING.
U116-16 = H	(MB4)	U116-4
U131-9 = P	(MB4)	U131-11, U131-13
U131-11 = P	(MB4)	U116-5
U131-13 = P	(MB4)	U114-7
U134-1 = H	(MB4)	RP103 or shorted foil run.
U134-2 = L	(MB4)	U134-1
U134-13 = P	(MB4)	U114-38
U135-1 = P	(MB4)	U175-8
U135-19 = P	(MB4)	U175-8
U136-1 = P	(MB4)	U214-9
U136-19 = P	(MB4)	U214-9

U175-3	= H	(MB4)	See I/O PORT DECODER TESTS.
U175-4	= P	(MB4)	See I/O PORT DECODER TESTS.
U175-5	= P	(MB4)	See I/O PORT DECODER TESTS.
U175-6	= P	(MB4)	U175-3, U175-4, U175-5
U175-8	= P	(MB4)	U175-10, U175-11
U175-10	= P	(MB4)	U214-12
U175-11	= P	(MB4)	U175-6
U181-2	= P	(MB2)	See GENERAL CPU TESTS.
U181-4	= P	(MB2)	See GENERAL CPU TESTS.
U181-16	= P	(MB2)	U181-4
U181-18	= P	(MB2)	U181-2
U195-2	= P	(MB2)	See STATUS CIRCUITS TESTS.
U195-18	= P	(MB2)	U195-2
U214-8	= P	(MB2)	See BUS CONTROL OUTPUT CIRCUITS TESTS.
U214-9	= P	(MB2)	U214-11
U214-11	= P	(MB2)	See STATUS CIRCUITS TESTS.
U214-12	= P	(MB2)	U214-8

PROCESSOR SWAP TESTS

SWAP TEST #1

1. Lift pin 5 of U186 (MB1).
2. Jumper U186-5 to ground.
3. Apply power and perform the following steps:

CHECK			IF NOT OKAY, CHECK
*S100-21	= L	(MB1)	U215-3
*U180-9	= L	(MB1)	U180-10
*U186-3	= H	(MB1)	U211-30
*U186-4	= L	(MB1)	U171-5

Go to Swap Test #2

U171-1	= L	(MB1)	U210-38
U171-5	= L	(MB1)	U171-1
U180-10	= L	(MB1)	U186-17
U186-3	= H	(MB1)	U211-30
U186-4	= L	(MB1)	U171-5
U186-16	= L	(MB1)	U186-3
U186-17	= L	(MB1)	U186-4
U186-18	= H	(MB1)	U186 is defective.
U187-2	= H	(MB1)	U186-18
U187-3	= P	(MB1)	Restore U186-5 and go to CLOCK CIRCUITS TESTS.
U187-5	= H	(MB1)	U187-2, U187-3
U187-9	= L	(MB1)	U187-10, U187-11, U187-12
U187-10	= H	(MB1)	U203-11
U187-11	= P	(MB1)	Restore U186-5 and go to CLOCK CIRCUITS TESTS.
U187-12	= L	(MB1)	U186-3
U203-11	= H	(MB1)	U203-12, U203-13
U203-12	= L	(MB1)	U186-16
U203-13	= H	(MB1)	Restore U186-5 and go to CLOCK CIRCUITS TESTS.

U210-38 = L (MB1)		U210-39
U210-39 = L (MB1)		U187-9
U211-30 = H (MB1)		U211-31
U211-31 = H (MB1)		U187-5
U215-2 = L (MB1)		Restore U186-5 and go to CLOCK CIRCUITS TESTS.
U215-3 = L (MB1)		U215-2

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SWAP TEST #2

1. Lift pins 4 and 5 of U186.
2. Jumper U186-4 and U186-5 to 5 volts.
3. Apply power and perform the following tests:

CHECK		IF NOT OKAY, CHECK
*S100-21 = H (MB1)		U215-3
*U171-5 = H (MB1)		U171-3, U171-2, U171-1
*U180-9 = L (MB1)		U180-10

Go to Swap Test #3.

U171-1 = H (MB1)		U210-38
U171-2 = H (MB1)		U210-38
U171-3 = P (MB1)		Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U180-10 = L (MB1)		U186-17
U186-3 = L (MB1)		U211-30
U186-13 = H (MB1)		U186-3
U186-16 = H (MB1)		U186-3
U186-17 = L (MB1)		U186-3
U186-18 = L (MB1)		U186 is defective.

U187-2	= L	(MB1)	U186-18
U187-3	= P	(MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U187-4	= H	(MB1)	U203-11
U187-5	= L	(MB1)	U187-2, U187-3, U187-4
U187-9	= H	(MB1)	U187-11, U187-12
U187-11	= P	(MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U187-12	= H	(MB1)	U186-13
U203-11	= H	(MB1)	U203-13, U203-12
U203-12	= H	(MB1)	U186-16
U203-13	= L	(MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U210-38	= H	(MB1)	U210-39
U210-39	= H	(MB1)	U187-9
U211-30	= L	(MB1)	U211-31
U211-31	= L	(MB1)	U187-5
U215-2	= H	(MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U215-3	= L	(MB1)	U215-2

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SWAP TEST #3

1. Restore pin 4 of U186; leave pin 5 lifted.
2. Jumper U186-5 to ground.
3. Turn on the H/Z-100.
4. Connect a jumper wire from ground to pin 74 of the S-100 bus (HOLD*).
5. Perform the following tests:

CHECK			IF NOT OKAY, CHECK
*U180-9	= H	(MB1)	U180-10

Go to Swap Test #4.

U180-10 = H	(MB1)	U186-17
U186-13 = H	(MB1)	U186 is defective.†
U186-16 = H	(MB1)	U186 is defective.†
U186-17 = H	(MB1)	U186-13, U186-18

†NOTE: Before replacing U186, check the continuity between pins 6 and 15, and between pins 7 and 14. Also check for ground at pins 2, 8, 9, 10, 11, 12, and 19.

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SWAP TEST #4

1. Remove the jumper between ground and pin 5.
2. Connect the jumper from pin 5 to +5 volts.

CHECK		IF NOT OKAY, CHECK
*U180-9 = H	(MB1)	U180-10

End of tests.

U180-10 = H	(MB1)	U180-17
U186-13 = H	(MB1)	U186 is defective.†
U186-17 = H	(MB1)	U186-13, U186-18
U186-18 = H	(MB1)	U186 is defective.†

†NOTE: Before replacing U186, check the continuity between pins 6 and 15, and between pins 7 and 14. Also check for ground at pins 2, 8, 9, 10, 11, 12, and 19.

RESET CIRCUITS TESTS

CHECK			IF NOT OKAY, CHECK
*U177-5	= H	(MB1)	U177-15
*U177-7	= H	(MB1)	U177-13
*U177-11	= L	(MB1)	U201-8, U201-13
*U201-3	= H	(MB1)	U201-1, U201-2
*U201-6	= H	(MB1)	U201-4, U201-5

Perform the RESET ACTIVE TESTS.

U177-9	= L	(MB1)	U177-11
U177-11	= H	(MB1)	U201-8, U201-13
U177-13	= L	(MB1)	U177-9
U177-15	= L	(MB1)	U177-9
U183-4	= H	(MB4)	U183-6
U183-6	= L	(MB4)	U183-10
U183-8	= H	(MB4)	See KEYBOARD TESTS.
U183-9	= H	(MB4)	See KEYBOARD TESTS.
U183-10	= L	(MB4)	U183-8, U183-9
U185-3	= H	(MB1)	U183-4
U185-4	= L	(MB4)	U185-3
U185-5	= L	(MB4)	U185-4
U185-6	= H	(MB4)	U185-5
U201-1	= H	(MB1)	U207-8
U201-2	= L	(MB1)	Open circuit between U201-2 and ground.
U201-4	= L	(MB1)	Open circuit between U201-4 and ground.
U201-5	= H	(MB1)	U207-8
U201-8	= H	(MB1)	U201-9, U201-10
U201-9	= L	(MB1)	Open circuit between U201-9 and ground.
U201-10	= H	(MB1)	U207-8
U201-13	= H	(MB1)	U185-6
U207-8	= H	(MB1)	U207-9
U207-9	= L	(MB1)	U207-10
U207-10	= L	(MB1)	U207-11
U207-11	= H	(MB1)	R114, D101, or C189 defective.

RESET ACTIVE TESTS

Press and hold the CTRL/RESET keys as you make the following tests:

CHECK			IF NOT OKAY, CHECK
*U177-5	= L	(MB1)	U177-15
*U177-7	= L	(MB1)	U177-13

End of tests.

U177-9	= H	(MB1)	U177-11
U177-11	= L	(MB1)	U201-11
U177-13	= H	(MB1)	U177-9
U177-15	= H	(MB1)	U177-9
U183-4	= L	(MB4)	U183-6
U183-6	= H	(MB4)	U183-10
U183-8	= L	(MB4)	See KEYBOARD TESTS.
U183-9	= L	(MB4)	See KEYBOARD TESTS.
U183-10	= H	(MB4)	U183-8, U183-9
U185-3	= L	(MB4)	U183-4
U185-4	= H	(MB4)	U185-3
U185-5	= H	(MB4)	U185-4
U185-6	= L	(MB4)	U185-5
U201-11	= L	(MB1)	U201-12, U201-13
U201-12	= L	(MB1)	Open circuit between U201-12 and ground.
U201-13	= L	(MB1)	U185-6

SERIAL PORT A TESTS

CHECK		IF NOT OKAY, CHECK
*U243-3 = H	(MB4)	U243 or U247 is defective.
*U243-14 = H	(MB4)	Perform INPUT CHECKS.
*U243-15 = H	(MB4)	Perform INPUT CHECKS.
*U243-16 = L	(MB4)	Shorting plugs at J109 and J111 incorrectly positioned or U247 defective.
*U243-17 = L	(MB4)	Shorting plugs at J109 and J111 incorrectly positioned or U247 defective.
*U243-18 = Z	(MB4)	Perform INPUT CHECKS.
*U243-20 = P	(MB4)	U240-8
*U243-22 = H	(MB4)	U243 or U246 is defective.
*U245-11 = -12V	(MB4)	U245-13, U228-3, U229-1
*U248-3 = -12V	(MB4)	U248-2
*U248-6 = -12V	(MB4)	U248-5, U228-3, U229-1
*U248-8 = P	(MB4)	U248-10
*U248-11 = P	(MB4)	U248-13

Perform SERIAL PORT A RESET CHECK.

INPUT CHECKS	(MB4)	U243-10, U243-21, U243-27,
INPUT CHECKS	(MB4)	U243-11, U243-13, U243-12,
INPUT CHECKS	(MB4)	U243-28, U243-1, U243-2,
INPUT CHECKS	(MB4)	U243-5, U243-6, U243-7, U243-8
U174-1 = P	(MB4)	See I/O PORT DECODER TESTS.
U174-2 = P	(MB4)	See E-CLOCK LOGIC TESTS.
U174-3 = H	(MB4)	U174-1, U174-2
U181-2 = P	(MB2)	See GENERAL CPU TESTS.
U181-4 = P	(MB2)	See GENERAL CPU TESTS.
U181-16 = P	(MB2)	U181-4
U181-18 = P	(MB2)	U181-2
U214-6 = P	(MB2)	See STATUS CIRCUITS TESTS.
U214-14 = P	(MB2)	U214-6
U228-1 = +16V	(MB4)	Check POWER SUPPLY MODULE.
U228-3 = +12V	(MB4)	U228-1
U229-1 = -12V	(MB4)	U229-2
U229-2 = -16V	(MB4)	Check POWER SUPPLY MODULE.

U240-8 = P	(MB4)	U240 OR C214 is bad.
U243-1 = P	(MB4)	See GENERAL CPU TESTS.
U243-2 = P	(MB4)	See GENERAL CPU TESTS.
U243-5 = P	(MB4)	See GENERAL CPU TESTS.
U243-6 = P	(MB4)	See GENERAL CPU TESTS.
U243-7 = P	(MB4)	See GENERAL CPU TESTS.
U243-8 = P	(MB4)	See GENERAL CPU TESTS.
U243-9 = P	(MB4)	Perform INPUT CHECKS.
U243-10 = P	(MB4)	U181-16
U243-11 = H	(MB4)	U174-3
U243-12 = P	(MB4)	U181-18
U243-13 = P	(MB4)	U214-14
U243-19 = H	(MB4)	Perform INPUT CHECKS.
U243-21 = L	(MB4)	See RESET CIRCUITS TESTS.
U243-23 = H	(MB4)	Perform INPUT CHECKS.
U243-24 = H	(MB4)	Perform INPUT CHECKS.
U243-25 = P	(MB4)	Perform INPUT CHECKS.
U243-27 = P	(MB4)	See GENERAL CPU TESTS.
U243-28 = P	(MB4)	See GENERAL CPU TESTS.
U245-13 = H	(MB4)	U243-19
U248-2 = H	(MB4)	U243-24
U248-5 = H	(MB4)	U243-23
U248-10 = P	(MB4)	U243-9, U243-25
U248-13 = P	(MB4)	U243-9, U243-25

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SERIAL PORT A RESET TEST

Press and release the CTRL/RESET keys as you make the following measurements. A logic state in parenthesis indicates that the line under test pulses one or more times when you release the CTRL/reset keys.

CHECK		IF NOT OKAY, CHECK
*U243-9 = Z	(MB4)	U243-21
*U243-13 = (L)	(MB4)	U214-14

End of test.

U214-6 = (L)	(MB2)	See STATUS CIRCUITS TESTS.
U214-14 = (L)	(MB2)	U214-6
U243-21 = H	(MB4)	See RESET CIRCUITS TESTS.

SERIAL PORT B TESTS

CHECKS		IF NOT OKAY, CHECK
*U242-3 = H	(MB4)	U242 or U230 is defective.
*U242-9 = L	(MB4)	U242, D104, or U247 is defective.
*U242-14 = H	(MB4)	Perform INPUT CHECKS.
*U242-15 = H	(MB4)	Perform INPUT CHECKS.
*U242-16 = L	(MB4)	U242 or U230 is defective.
*U242-17 = L	(MB4)	U242 or U230 is defective.
*U242-18 = Z	(MB4)	Perform INPUT CHECKS.
*U242-20 = P	(MB4)	U240-8
*U242-22 = H	(MB4)	U242 or U230 is defective.
*U242-25 = L	(MB4)	U242, D103, or U247 is defective.
*U245-3 = -12V	(MB4)	U245-2, U228-3, U229-1
*U245-6 = -12V	(MB4)	U245-5, U228-3, U229-1
*U245-8 = -12V	(MB4)	U245-10, U228-3, U229-1

Go to SERIAL PORT B RESET CHECK.

INPUT CHECKS	(MB4)	U242-11, U242-13, U242-12,
INPUT CHECKS	(MB4)	U242-10, U242-21, U242-27,
INPUT CHECKS	(MB4)	U242-28, U242-1, U242-2,
INPUT CHECKS	(MB4)	U242-5, U242-6, U242-7,
INPUT CHECKS	(MB4)	U242-8
INPUT CHECKS	(MB4)	(If these are okay, then
INPUT CHECKS	(MB4)	replace U242.)
U174-4 = P	(MB4)	See I/O PORT DECODER TESTS.
U174-5 = P	(MB4)	See E-CLOCK LOGIC TESTS.
U174-6 = H	(MB4)	U174-4, U174-5
U181-2 = P	(MB2)	See GENERAL CPU TESTS.
U181-4 = P	(MB2)	See GENERAL CPU TESTS.
U181-16 = P	(MB2)	U181-4
U181-18 = P	(MB2)	U181-2
U214-6 = P	(MB2)	See STATUS CIRCUITS TESTS.
U214-14 = P	(MB2)	U214-6
U228-1 = +16V	(MB4)	Check Power Supply Module.
U228-3 = +12V	(MB4)	U228-1

U229-1 = -12V (MB4)		U229-2
U229-2 = -16V (MB4)		Check Power Supply Module.
U240-8 = P (MB4)		U240 or C214 is defective.
U242-1 = P (MB4)		See GENERAL CPU TESTS.
U242-2 = P (MB4)		See GENERAL CPU TESTS.
U242-5 = P (MB4)		See GENERAL CPU TESTS.
U242-6 = P (MB4)		See GENERAL CPU TESTS.
U242-7 = P (MB4)		See GENERAL CPU TESTS.
U242-8 = P (MB4)		See GENERAL CPU TESTS.
U242-10 = P (MB4)		U181-16
U242-11 = H (MB4)		U174-6
U242-12 = P (MB4)		U181-18
U242-13 = P (MB4)		U214-14
U242-19 = H (MB4)		Perform INPUT CHECKS.
U242-21 = L (MB4)		See RESET CIRCUITS TESTS.
U242-23 = H (MB4)		Perform INPUT CHECKS.
U242-24 = H (MB4)		Perform INPUT CHECKS.
U242-27 = P (MB4)		See GENERAL CPU TESTS.
U242-28 = P (MB4)		See GENERAL CPU TESTS.
U245-2 = H (MB4)		U242-24
U245-5 = H (MB4)		U242-23
U245-10 = H (MB4)		U242-19

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SERIAL PORT B RESET TEST

Press and release the CTRL/RESET keys as you make the following measurements. A logic state in parenthesis indicates that the line under test pulses one or more times when you release the CTRL/RESET keys.

CHECK	IF NOT OKAY, CHECK
*U242-13 = (L) (MB4)	U214-14
*U242-21 = H (MB4)	See RESET CIRCUITS TESTS.

End of test.

U214-6 = (L) (MB2)	See STATUS CIRCUITS TESTS.
U214-14 = (L) (MB2)	U214-6

STATUS CIRCUITS TESTS

CHECK			IF NOT OKAY, CHECK
*U226-9	= P	(MB1)	See INPUT CHECKS
*U227-2	= P	(MB1)	U227-1, U227-3, U227-11
*U227-5	= P	(MB1)	U227-1, U227-4, U227-11
*U227-6	= P	(MB1)	U227-1, U227-7, U227-11
*U227-9	= P	(MB1)	U227-1, U227-8, U227-11
*U227-12	= L	(MB1)	U227-1, U227-11, U227-13
*U227-15	= P	(MB1)	U227-1, U227-11, U227-14
*U227-16	= P	(MB1)	U227-1, U227-11, U227-17
*U227-19	= H	(MB1)	U227-18

Tests complete.

INPUT CHECKS			U226-14, U226-13, U226-12,
INPUT CHECKS			U226-11, U226-10
U182-8	= L	(MB1)	U182-9
U182-9	= H	(MB1)	Problem on Pin 18 of S-100 BUS.
U220-10	= P	(MB1)	U220-11
U220-11	= P	(MB1)	U221-3
U221-1	= P	(MB1)	See GENERAL CPU TESTS.
U221-2	= L	(MB1)	U237-11
U221-3	= P	(MB1)	U221-1, U221-2
U226-1	= P	(MB1)	See INPUT CHECKS.
U226-2	= P	(MB1)	See INPUT CHECKS.
U226-3	= L	(MB1)	See INPUT CHECKS.
U226-4	= P	(MB1)	See INPUT CHECKS.
U226-5	= P	(MB1)	See INPUT CHECKS.
U226-6	= P	(MB1)	See INPUT CHECKS.
U226-7	= P	(MB1)	See INPUT CHECKS.
U226-10	= P	(MB1)	See GENERAL CPU TESTS.
U226-11	= P	(MB1)	See GENERAL CPU TESTS.
U226-12	= P	(MB1)	See GENERAL CPU TESTS.
U226-13	= H	(MB1)	See PROCESSOR SWAP TESTS.
U226-14	= P	(MB1)	U233-5

U227-1	= L	(MB1)	U182-8
U227-3	= P	(MB1)	U226-6
U227-4	= P	(MB1)	U226-1
U227-8	= P	(MB1)	U226-7
U227-11	= P	(MB1)	U221-3
U227-13	= L	(MB1)	U226-3
U227-14	= P	(MB1)	U226-4
U227-17	= P	(MBA)	U226-5
U227-18	= H	(MB1)	R121 open or shorted foil to U227-18.
U233-1	= P	(MB1)	U220-10
U233-3	= P	(MB1)	See CLOCK CIRCUITS TESTS.
U233-5	= P	(MB1)	U233-1, U233-3
U237-11	= L	(MB1)	U237-12
U233-12	= L	(MB1)	See GENERAL CPU TESTS.

TIMER CIRCUITS TESTS

CHECK			IF NOT OKAY, CHECK
*U160-10	= P	(MB4)	U160-9
*U160-17	= P	(MB4)	U160-18
*U175-12	= H	(MB4)	U175-1, U175-2

End of test.

U112-1	= H	(MB4)	U129-6
U112-8	= L	(MB4)	U112-13
U112-13	= H	(MB4)	U129-3
U113-1	= P	(MB4)	See I/O PORT DECODER TESTS.
U113-2	= P	(MB4)	U214-3
U113-3	= H	(MB4)	U113-1, U113-2
U113-4	= P	(MB4)	See I/O PORT DECODER TESTS.
U113-5	= P	(MB4)	U195-16
U113-6	= H	(MB4)	U113-4, U113-5

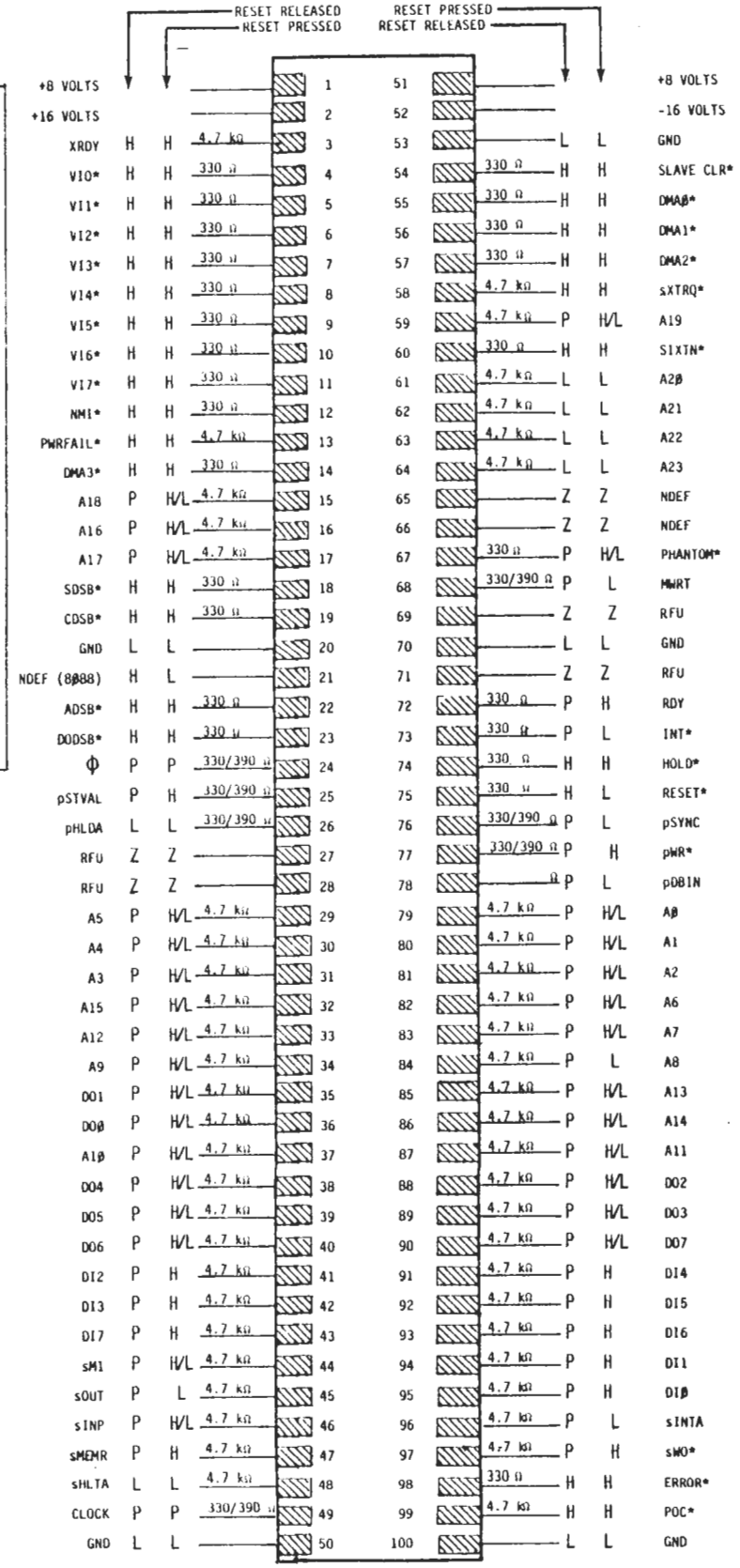
U129-1	= H	(MB4)	U113-3
U129-2	= P	(MB4)	U129-3. Also check U135, U136, and perform GENERAL CPU TESTS.
U129-3	= H	(MB4)	U129-1, U129-2
U129-4	= H	(MB4)	U113-3
U129-5	= P	(MB4)	U129-10. Also check U135, U136, and perform GENERAL CPU TESTS.
U129-6	= H	(MB4)	U129-4, U129-5
U129-10	= P	(MB4)	U113-6
U129-13	= H	(MB4)	U113-6
U160-9	= P	(MB4)	U192-11
U160-18	= P	(MB4)	U192-11
U175-1	= L	(MB4)	U112-8
U175-2	= L	(MB4)	U112-1
U192-2	= P	(MB1)	U191 or C115 is defective.
U192-11	= P	(MB1)	U192-2
U195-4	= P	(MB2)	See BUS CONTROL OUTPUT TESTS.
U195-16	= P	(MB2)	U195-4
U214-3	= P	(MB2)	U214-17
U214-17	= P	(MB2)	See BUS CONTROL OUTPUT TESTS.

H/Z-1ØØ S-1ØØ CONNECTOR PIN LOCATIONS

NOTES:

1. PULSES TAKEN WITH LOGIC PROBE HP545A OR IT-7410.
2. LOGIC STATES IN "RESET RELEASED" COLUMNS SHOULD BE PRESENT AFTER YOU PRESS AND RELEASE THE CTRL/RESET KEYS.
3. LOGIC STATES IN "RESET PRESSED" COLUMNS SHOULD BE PRESENT WHEN YOU PRESS AND HOLD THE CTRL/RESET KEYS.
4. LOGIC DEFINITIONS:
   - H = LOGIC ONE
   - L = LOGIC ZERO
   - P = PULSE
   - Z = HIGH IMPEDANCE STATE
   - H/L = MAY BE EITHER HIGH OR LOW--DEPENDS ON STATUS OF LATCH WHEN RESET IS PRESSED.
5. LINES MARKED "330 Ω" and "4.7 kΩ" CONNECT TO PULL-UP RESISTOR PACKS.
6. LINES MARKED "330/390 Ω" CONNECT TO TERMINATING RESISTOR PACKS.

FRONT OF H/Z-1ØØ COMPUTER



PARTS LIST

MOTHER BOARD PART LIST
(Assembled HE 181-3630-1)

CAPACITORS

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
C101	.1 uF ceramic	HE 21-762
C102	.1 uF ceramic	HE 21-762
C103	.1 uF ceramic	HE 21-762
C104	.1 uF ceramic	HE 21-762
C105	.1 uF ceramic	HE 21-762
C106	.1 uF ceramic	HE 21-762
C107	.1 uF ceramic	HE 21-762
C108	.1 uF ceramic	HE 21-762
C109	.1 uF ceramic	HE 21-762
C110	.1 uF ceramic	HE 21-762
C111	.1 uF ceramic	HE 21-762
C112	.1 uF ceramic	HE 21-762
C113	.1 uF ceramic	HE 21-762
C113-1	100 uF electrolytic	HE 25-918
C114	.1 uF ceramic	HE 21-762
C115	.1 uF ceramic	HE 21-762
C116	470 pF ceramic	HE 21-773
C117	470 pF ceramic	HE 21-773
C118	470 pF ceramic	HE 21-773
C119	.1 uF ceramic	HE 21-762
C120	470 pF ceramic	HE 21-773
C121	.1 uF ceramic	HE 21-762
C122	.1 uF ceramic	HE 21-762
C123	.1 uF ceramic	HE 21-762
C124	.1 uF ceramic	HE 21-762
C125	.1 uF ceramic	HE 21-762
C126	.1 uF ceramic	HE 21-762
C127	.1 uF ceramic	HE 21-762
C128	.1 uF ceramic	HE 21-762
C129	.1 uF ceramic	HE 21-762
C130	.1 uF ceramic	HE 21-762
C131	.1 uF ceramic	HE 21-762
C132	.1 uF ceramic	HE 21-762
C133	.1 uF ceramic	HE 21-762
C134	470 pF ceramic	HE 21-773
C135	470 pF ceramic	HE 21-773
C136	470 pF ceramic	HE 21-773
C137	470 pF ceramic	HE 21-773
C138	470 pF ceramic	HE 21-773
C139	.1 uF ceramic	HE 21-762

CAPACITORS (CONTINUED)

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
C140	.1 uF ceramic	HE 21-762
C141	.1 uF ceramic	HE 21-762
C142	.1 uF ceramic	HE 21-762
C143	.1 uF ceramic	HE 21-762
C144	.1 uF ceramic	HE 21-762
C145	.1 uF ceramic	HE 21-762
C146	.1 uF ceramic	HE 21-762
C147	.1 uF ceramic	HE 21-762
C148	.1 uF ceramic	HE 21-762
C149	.1 uF ceramic	HE 21-762
C150	.1 uF ceramic	HE 21-762
C151	.1 uF ceramic	HE 21-762
C152	.1 uF ceramic	HE 21-762
C153	.1 uF ceramic	HE 21-762
C154	.1 uF ceramic	HE 21-762
C155	.1 uF ceramic	HE 21-762
C156	.1 uF ceramic	HE 21-762
C157	.1 uF ceramic	HE 21-762
C158	.1 uF ceramic	HE 21-762
C159	.1 uF ceramic	HE 21-762
C160	.1 uF ceramic	HE 21-762
C161	.1 uF ceramic	HE 21-762
C162	.1 uF ceramic	HE 21-762
C163	.1 uF ceramic	HE 21-762
C164	.001 uF polystyrene	HE 29-44
C165	.1 uF ceramic	HE 21-762
C166	.1 uF ceramic	HE 21-762
C167	.1 uF ceramic	HE 21-762
C168	.1 uF ceramic	HE 21-762
C169	.1 uF ceramic	HE 21-762
C170	.1 uF ceramic	HE 21-762
C171	.1 uF ceramic	HE 21-762
C172	.1 uF ceramic	HE 21-762
C173	.1 uF ceramic	HE 21-762
C174	2.2 uF electrolytic	HE 25-924
C174-1	100 uF electrolytic	HE 25-918
C175	.1 uF ceramic	HE 21-762
C176	.1 uF ceramic	HE 21-762
C177	.1 uF ceramic	HE 21-762
C178	none	
C179	none	

CAPACITORS (CONTINUED)

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
C180	10 uF electrolytic	HE 25-820
C181	.1 uF ceramic	HE 21-762
C182	.1 uF ceramic	HE 21-762
C183	.1 uF ceramic	HE 21-762
C184	.1 uF ceramic	HE 21-762
C185	.1 uF ceramic	HE 21-762
C186	20 pF ceramic	HE 21-718
C187	.1 uF ceramic	HE 21-762
C188	.1 uF ceramic	HE 21-762
C189	100 uF electrolytic	HE 25-918
C190	.1 uF ceramic	HE 21-762
C191	.1 uF ceramic	HE 21-762
C192	.1 uF ceramic	HE 21-762
C193	.1 uF ceramic	HE 21-762
C194	.1 uF ceramic	HE 21-762
C195	.1 uF ceramic	HE 21-762
C196	.1 uF ceramic	HE 21-762
C197	.1 uF ceramic	HE 21-762
C198	.47 uF electrolytic	HE 25-859
C199	.47 uF electrolytic	HE 25-859
C200	.01 uF ceramic	HE 21-769
C201	.1 uF ceramic	HE 21-762
C202	.01 uF ceramic	HE 21-769
C203	.1 uF ceramic	HE 21-762
C204	330 pF ceramic	HE 21-763
C205	330 pF ceramic	HE 21-763
C206	330 pF ceramic	HE 21-763
C207	.1 uF ceramic	HE 21-762
C208	2.2 uF electrolytic	HE 25-924
C209	.1 uF ceramic	HE 21-762
C210	.001 uF polystyrene	HE 29-44
C211	.1 uF ceramic	HE 21-762
C212	.1 uF ceramic	HE 21-762
C213	10 uF electrolytic	HE 25-820
C214	.1 uF ceramic	HE 21-762
C215	.1 uF ceramic	HE 21-762
C216	.1 uF ceramic	HE 21-762
C217	.1 uF ceramic	HE 21-762
C218	.1 uF ceramic	HE 21-762
C219	.1 uF ceramic	HE 21-762
C220	.1 uF ceramic	HE 21-762
C221	.1 uF ceramic	HE 21-762
C222	330 pF ceramic	HE 21-763
C223	330 pF ceramic	HE 21-763
C224	330 pF ceramic	HE 21-763
C225	330 pF ceramic	HE 21-763
C226	330 pF ceramic	HE 21-763

PARTS LIST

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INDUCTORS		
L101	35 uH	HE 235-229
L102	35 uH	HE 235-229
L103	35 uH	HE 235-229
L104	35 uH	HE 235-229
RESISTORS		
R101	4700 ohm 1/4 watt, 5%	HE 6-472-12
R102	4700 ohm 1/4 watt, 5%	HE 6-472-12
R103	4700 ohm 1/4 watt, 5%	HE 6-472-12
R104	1000 ohm 1/4 watt, 5%	HE 6-102-12
R105	6650 ohm 1/4 watt, 1%	HE 6-6651-12
R106	6810 ohm 1/4 watt, 1%	HE 6-6611-12
R107	10 kilohm 1/4 watt, 5%	HE 6-103-12
R108	10 kilohm 1/4 watt, 5%	HE 6-103-12
R109	1000 ohm 1/4 watt, 5%	HE 6-102-12
R110	1000 ohm 1/4 watt, 5%	HE 6-102-12
R111	1000 ohm 1/4 watt, 5%	HE 6-102-12
R112	470 ohm 1/4 watt, 5%	HE 6-471-12
R113	10 kilohm 1/4 watt, 5%	HE 6-103-12
R114	10 kilohm 1/4 watt, 5%	HE 6-103-12
R115	4700 ohm 1/4 watt, 5%	HE 6-472-12
R116	150 kilohm 1/4 watt, 5%	HE 6-154-12
R117	jumper	
R118	470 kilohm 1/4 watt, 5%	HE 6-474-12
R119	470 kilohm 1/4 watt, 5%	HE 6-474-12
R120	220 kilohm 1/4 watt, 5%	HE 6-224-12
R121	1000 ohm 1/4 watt, 5%	HE 6-102-12
R122	22 ohm 1/4 watt, 5%	HE 6-220-12
R123	510 ohm 1/4 watt, 5%	HE 6-511-12
R124	510 ohm 1/4 watt, 5%	HE 6-511-12
R125	10 kilohm 1/4 watt, 5%	HE 6-103-12
R126	10 kilohm 1/4 watt, 5%	HE 6-103-12
R127	1000 ohm 1/4 watt, 5%	HE 6-102-12
R128	4700 ohm 1/4 watt, 5%	HE 6-472-12
RESISTOR PACKS		
RP101	33 ohm	HE 9-93
RP102	390 ohm	HE 9-131
RP103	4.7 kilohm	HE 9-124
RP104	4.7 kilohm	HE 9-124
RP105	33 ohm	HE 9-93
RP106	4.7 kilohm	HE 9-133
RP107	4.7 kilohm	HE 9-124
RP108	4.7 kilohm	HE 9-124
RP109	4.7 kilohm	HE 9-124

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
RESISTORS (CONTINUED)		
RP110	330 ohm	HE 9-132
RP111	4.7 kilohm	HE 9-133
RP112	330 ohm	HE 9-132
RP113	4.7 kilohm	HE 9-124
RP114	4.7 kilohm	HE 9-124
RP115	330 ohm	HE 9-132
RP116	330/390 ohm	HE 9-130
RP117	4.7 kilohm	HE 9-133
RP118	4.7 kilohm	HE 9-124
RP119	10 kilohm	HE 9-106
RP120	10 kilohm	HE 9-128
RP121	10 kilohm	HE 9-106
RP122	10 kilohm	HE 9-106
RP123	4.7 kilohm	HE 9-133
RP124	4.7 kilohm	HE 9-133
RP125	4.7 kilohm	HE 9-133
RP126	10 kilohm	HE 9-106
RP127	10 kilohm	HE 9-106
RP128	10 kilohm	HE 9-128
RP129	4.7 kilohm	HE 9-124
RP130	4.7 kilohm	HE 9-124
INTEGRATED CIRCUITS		
U101	MCM6665	HE 443-970
U102	MCM6665	HE 443-970
U103	MCM6665	HE 443-970
U104	MCM6665	HE 443-970
U105	MCM6665	HE 443-970
U106	MCM6665	HE 443-970
U107	MCM6665	HE 443-970
U108	MCM6665	HE 443-970
U109	MCM6665	HE 443-970
U110	HAL16L8	HE 444-126
U111	82S129 PROM	HE 444-104
U112	74ALS74	HE 443-1051
U113	74LS32	HE 443-875
U114	68A21	HE 443-1014
U115	74LS244	HE 443-791
U116	74LS244	HE 443-791
U117	MCM6665	HE 443-970
U118	MCM6665	HE 443-970
U119	MCM6665	HE 443-970
U120	MCM6665	HE 443-970
U121	MCM6665	HE 443-970
U122	MCM6665	HE 443-970

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS (CONTINUED)		
U123	MCM6665	HE 443-970
U124	MCM6665	HE 443-970
U125	MCM6665	HE 443-970
U126	74LS244	HE 443-791
U127	74LS393	HE 443-973
U128	74LS257A	HE 443-1037
U129	74LS125	HE 443-811
U130	74ALS37	HE 443-1049
U131	74ALS74	HE 443-1051
U132	74LS373	HE 443-837
U133	74LS373	HE 443-837
U134	74LS14	HE 443-872
U135	74LS244	HE 443-791
U136	74LS244	HE 443-791
U137	MCM6665 (optional)	HE 443-970
U138	MCM6665 (optional)	HE 443-970
U139	MCM6665 (optional)	HE 443-970
U140	MCM6665 (optional)	HE 443-970
U141	MCM6665 (optional)	HE 443-970
U142	MCM6665 (optional)	HE 443-970
U143	MCM6665 (optional)	HE 443-970
U144	MCM6665 (optional)	HE 443-970
U145	MCM6665 (optional)	HE 443-970
U146	74LS257A	HE 443-1037
U147	555 timer	HE 442-53
U148	74LS112	HE 443-948
U149	200 ns Delay Line	HE 41-10
U150	74S74	HE 443-900
U151	74LS11	HE 443-864
U152	74LS112	HE 443-948
U153	74LS280	HE 443-1001
U154	74S260	HE 443-1038
U155	74LS00	HE 443-728
U156	74LS32	HE 443-875
U157	74LS139	HE 443-822
U158	74LS38	HE 443-1034
U159	74LS138	HE 443-877
U160	8253-5	HE 443-1066
U161	HAL16L2	HE 444-129
U162	74LS244	HE 443-791
U163	74LS244	HE 443-791
U164	74LS240	HE 443-754
U165	74LS175	HE 443-752
U166	74LS14	HE 443-872
U167	74S74	HE 443-900
U168	74LS32	HE 443-875
U169	74S08	HE 443-976

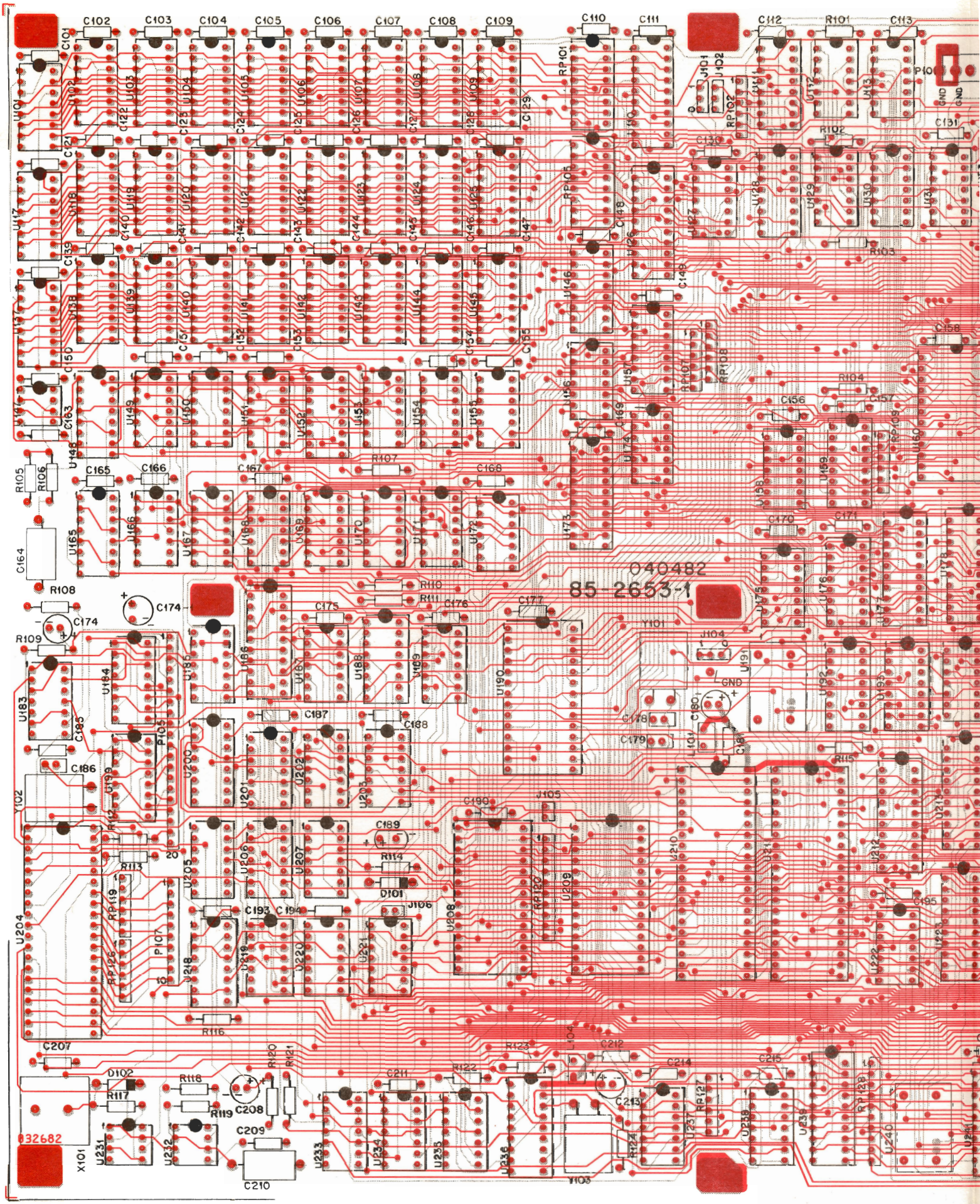
PARTS LIST

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS (CONTINUED)		
U170	74ALS1020	HE 443-1081
U171	74ALS74	HE 443-1051
U172	74ALS74	HE 443-1051
U173	HAL14L4	HE 444-130
U174	74LS32	HE 443-875
U175	74LS10	HE 443-797
U176	74LS174	HE 443-879
U177	74LS240	HE 443-754
U178	74LS244	HE 443-791
U179	82S129 PROM	HE 444-101
U180	74LS367	HE 443-857
U181	74LS244	HE 443-791
U182	74LS14	HE 443-872
U183	74LS02	HE 443-779
U184	74LS156	HE 443-1036
U185	74LS14	HE 443-872
U186	HAL12H6	HE 444-128
U187	74ALS74	HE 443-1051
U188	74LS175	HE 443-752
U189	74LS08	HE 443-780
U190	2764 ROM	HE 444-87
U191	4.000 MHz oscillator	HE 150-132
U192	74LS169	HE 443-1054
U193	74LS367	HE 443-857
U194	7417	HE 443-72
U195	74LS240	HE 443-754
U196	74LS373	HE 443-837
U197	74LS373	HE 443-837
U198	74LS373	HE 443-837
U199	74LS156	HE 443-1036
U200	74LS368	HE 443-1024
U201	74LS125	HE 443-811
U202	74ALS74	HE 443-1051
U203	74LS86	HE 443-891
U204	8741A	HE 444-141
U205	74S74	HE 443-900
U206	74ALS02	HE 443-1045
U207	74LS14	HE 443-872
U208	8259A	HE 443-1012
U209	8259A	HE 443-1012

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS (CONTINUED)		
U210	8085A	HE 443-1010
U211	8088	HE 443-1009
U212	74LS273	HE 443-805
U213	74LS373	HE 443-837
U214	74LS244	HE 443-791
U215	74LS125	HE 443-811
U216	74ALS28	HE 443-1048
U217	74LS244	HE 443-791
U218	96LS02	HE 443-1040
U219	74ALS74	HE 443-1051
U220	74LS04	HE 443-755
U221	74LS32	HE 443-875
U222	74LS00	HE 443-728
U223	74LS244	HE 443-791
U224	74ALS28	HE 443-1048
U225	74ALS37	HE 443-1049
U226	74S288 PROM	HE 444-105
U227	74LS373	HE 443-837
U228	78L12 +12V regulator	HE 442-644
U229	79L12 -12V regulator	HE 442-646
U230	75189	HE 443-795
U231	75452	HE 443-74
U232	555 timer	HE 442-53
U233	74ALS74	HE 443-1051
U234	74ALS74	HE 443-1051
U235	74ALS10	HE 443-1047
U236	8284A	HE 443-1011
U237	74LS125	HE 443-811
U238	74ALS74	HE 443-1051
U239	74LS244	HE 443-791
U240	4.9152 MHz oscillator	HE 150-133
U241	74LS244	HE 443-791
U242	2661-2	HE 443-1061
U243	2661-2	HE 443-1061
U244	74LS244	HE 443-791
U245	75188	HE 443-794
U246	75189	HE 443-795
U247	75189	HE 443-795
U248	75188	HE 443-794

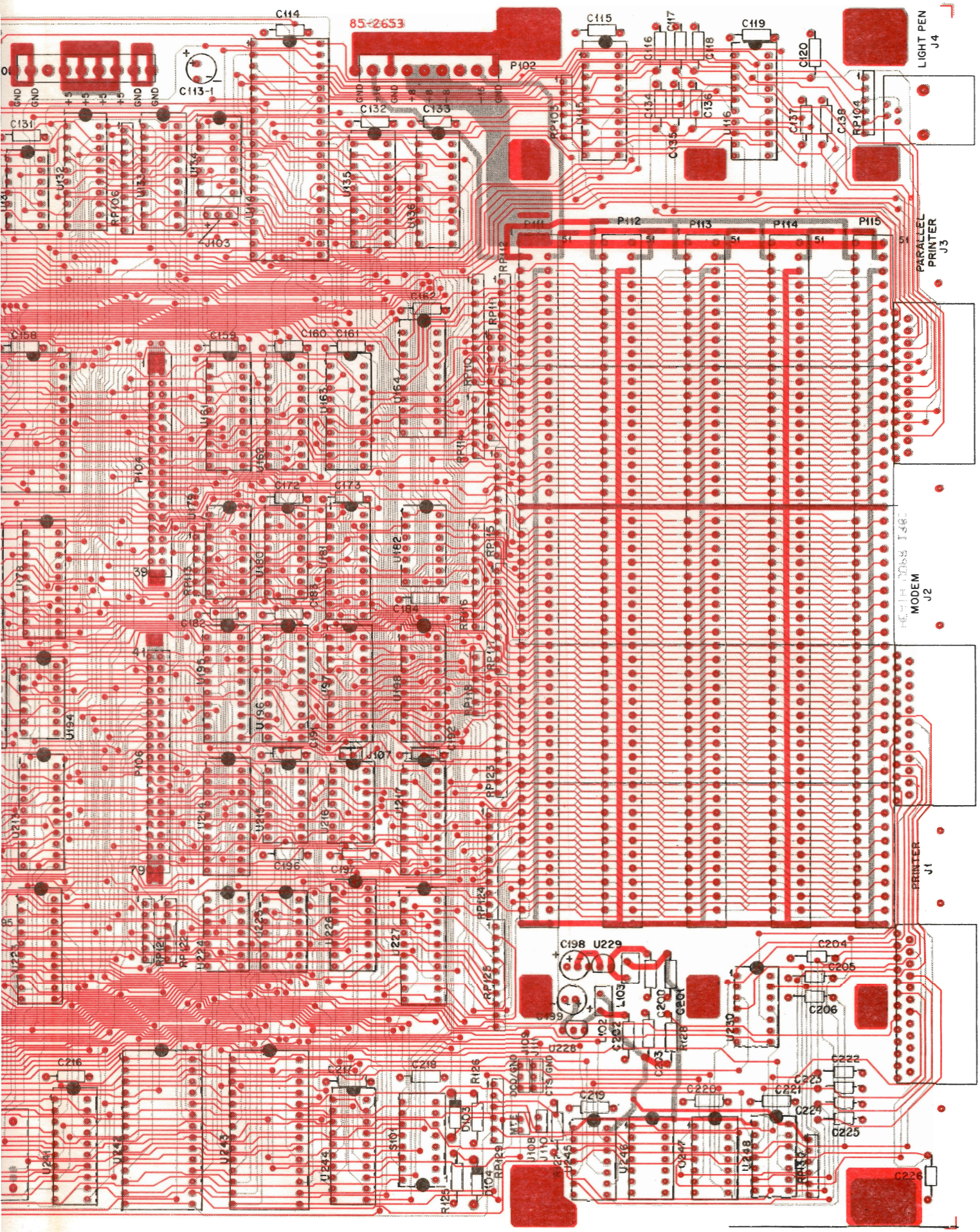
CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CRYSTALS		
Y101	10.000 MHz crystal	HE 404-645
Y102	6.000 MHz crystal	HE 404-647
Y103	15.000 MHz crystal	HE 404-644
CONNECTORS - SOCKETS		
	8-pin IC socket	HE 434-230
	14-pin IC socket	HE 434-298
	16-pin IC socket	HE 434-299
	18-pin IC socket	HE 434-310
	20-pin IC socket	HE 434-311
	24-pin IC socket	HE 434-307
	28-pin IC socket	HE 434-310
	40-pin IC socket	HE 434-253
	2-pin connector	HE 432-1171
	3-pin connector	HE 432-1102
	4-pin right-angle connector	HE 432-363
	9-pin right-angle molex connector	HE 432-1202
	10-pin connector	HE 432-903
	20-pin connector	HE 432-1227
	25-pin F right-angle "D" connector	HE 432-1195
	25-pin M right-angle "D" connector	HE 432-1194
	40-pin connector	HE 432-1062
	Jumper	HE 432-1041
	S-100 board edge connector	HE 432-1193
HARDWARE		
	#4 lockwasher	HE 254-9
	#4 nut	HE 252-15
	4-40 x 5/16" hex "D" spacer	HE 255-757
	4-40 x 5/16" black phillips-head screw	HE 250-1469
MISCELLANEOUS		
	PC board	HE 85-2653-1
	Wire, bare	HE 340-8
	Wire, blue wirewrap	HE 344-189
D101	1N5817 diode	HE 57-507
D102	1N4149 diode	HE 56-56
D103	1N4149 diode	HE 56-56
D104	1N4149 diode	HE 56-56
SW101	8-section slide switch	HE 60-621
X101	Audio transducer	HE 473-29

CIRCUIT BOARD X-RAY VIEWS



Early Motherboard (2653)
Later MB was "2801"

MOTHER CIRCUIT BOARD (###
OUTER FOILS OF FOUR-LAYER
(COMPONENT SIDE SHOWN IN RED)



ARD (#HE-181-3630-1)
R-LAYER CIRCUIT BOARD
IN RED; FOIL SIDE IN GRAY)

MOTHERBOARD CUTS AND JUMPERS

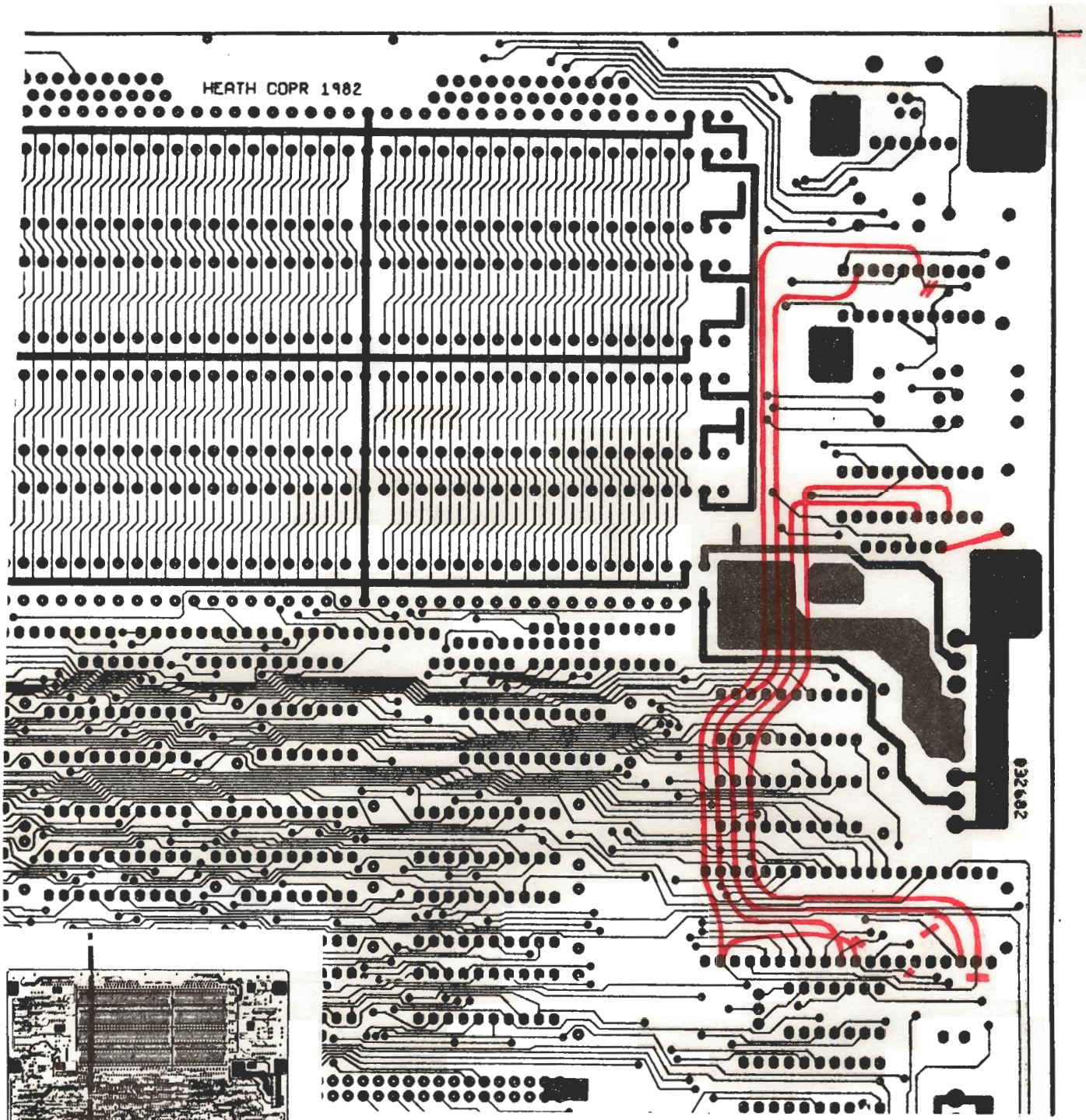
The pictorial on the facing page shows a section of the foil side of the motherboard. The red slashes (//) are cuts in existing foil runs. The lines in red are jumper wires. The schematics in this manual reflect these changes. Use this pictorial in conjunction with the other X-Ray Views. A summary of the cuts and jumpers follows:

Cuts: (all cuts on foil side of PCB)

1. Trace from U114 pin 2.
2. Trace from U114 pin 3.
3. Trace from U114 pin 10.
4. Trace from U114 pin 11.
5. Trace from U116 pin 16.

Jumpers:

1. Jumper from U116 pin 16 to U114 pin 19.
2. Jumper from U114 pin 19 to U114 pin 10.
3. Jumper from U114 pin 11 to U116 pin 12.
4. Jumper from U114 pin 2 to U115 pin 4.
5. Jumper from U114 pin 3 to U115 pin 6.
6. Jumper from RP103 pin 1 to +5V end of C115.

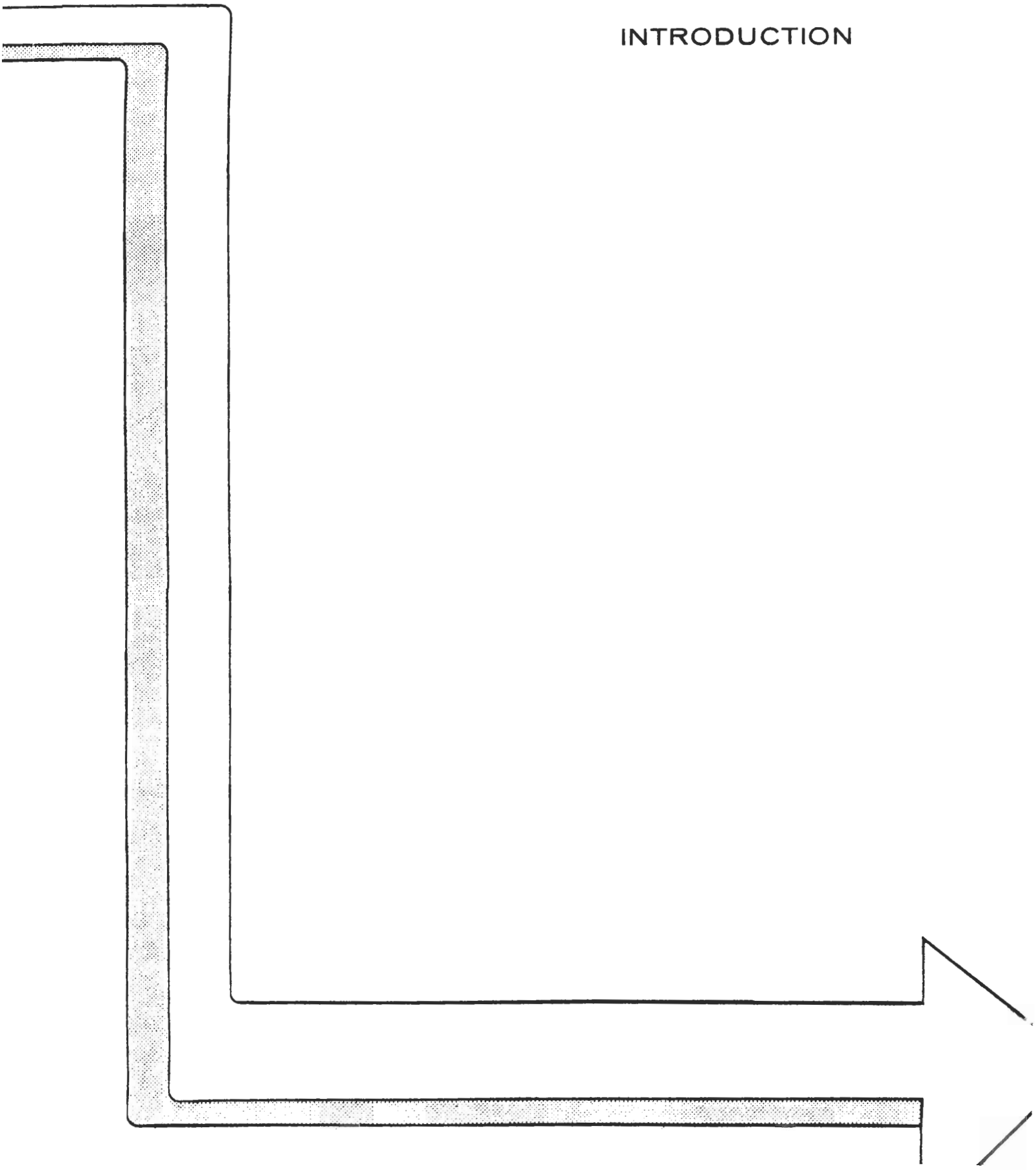


CUT FOIL AT FIVE POINTS MARKED

MOTHERBOARD
(Outer Bottom Foil)

VIDEO BOARD

INTRODUCTION



The color video board functions as a interface between the CPU and the video monitor. The video board receives data from the CPU and translates it into a meaningful display on a video monitor. The H/Z-100 video board features eight color capability, high-resolution graphics and S-100 bus signal compatibility.

The video board uses three banks of memory called memory planes. Each plane may contain up to 64K of RAM. A minimally configured video board will have one plane of memory and support a monochrome display. When the color option is installed, the video board contains three planes of memory. This enables the video board to produce an 8-color or an 8-level gray scale display. The type of display produced depends on the type of monitor used. When a color monitor is used, the 8 pixel colors may be mixed to produce more colors. When a monochrome display is used, pixel mixing produces more shades of gray.

To produce high-resolution graphics, the video board supports a resolution of 640 x 225 pixels. This can be visualized as 25 lines of 80 characters. A character is defined within an 8 x 9 pixel matrix. This matrix enables the H/Z-100 to display, in addition to high-resolution graphics, full width/height alphanumeric characters as currently defined by the H-19. By using this definition of character width and height, the H/Z-100 can use existing software that requires full width/height characters.

Although it is not an S-100 card, the video board is signal compatible with the S-100 bus. This allows the user to access the video board through slave processors located in the S-100 card cage. This compatibility gives the video board an added amount of flexibility.

In this section of the H/Z-100 Service Data Manual, the information supplied will familiarize you with the video board and will help you to efficiently troubleshoot it.

CIRCUIT DESCRIPTION

OVERVIEW

The video board uses a bit-mapped technique to generate a 640 x 250 pixel display. A pixel equals one bit in each character location. A character is 8 pixels wide and 10 pixels high. In normal operation, there are 80 characters across the screen and 25 rows of characters.

There are three colors available to the H/Z-100. Each color -- red, green, and blue -- requires a 32K x 8 bank of memory. These memory banks are located 64K apart near the top end of the 1 megabyte address space: Blue starts at C0000H, red starts at D0000H, and green starts at E0000H. Sixty-four kilobyte RAM can be used at these locations; however, the system software only supports 32K. A minimum system, for monochrome, uses the green memory bank.

Unless programmed otherwise, the H/Z-100 emulates the H-19 Video Terminal. This includes most escape sequences. In addition, if you want to write high-density graphics routines, you can by directly addressing the above memory location.

The video board uses many of the S-100 lines; however, it also uses some special control lines to provide more efficient operation. For this reason, it uses non-S-100 connectors at P304 and P305.

VIDEO PROCESSING CIRCUITS

CATHODE-RAY TUBE CONTROLLER

The CRTC, U330 on schematic VB1, fetches the characters to be displayed and provides horizontal and vertical timing. It also keeps track of the affected character if the light-pen circuits are used.

Briefly, here's what each line does. See the 6845 IC data sheet for more information.

$\overline{\text{POC}}$ Power-on clear, from the S-100 bus, sets all registers to their initial conditions on power-up or reset.

$\overline{\text{6845CS}}$ Chip-selects the CRTC for accessing the internal registers.

ECLK Latches the data into or out from the registers on its trailing edge.

BA0 Helps select a specific register inside the $\overline{\text{CRTC}}$.

$\overline{\text{OUT}}$ When low, writes data into the selected register. Otherwise, reads data from it.

DI00-DI07 Data bus used by the CPU to access the CRTC registers.

CLK Provides character-clock timing to the CRTC.

HSYNC Horizontal sync pulse.

VSYNC Vertical sync pulse.

CURSOR Provides an indication where the next character will be printed.

DISEN Disables the display during horizontal and vertical retrace.

MA0-MA11 Memory address lines. Point to the current character line, and the character in that line.

RA0-RA3 Row address lines. Points to the current scan line in the current character line.

WRITING TO A CRTC REGISTER

To select a specific CRTC register (R0-R17), the CPU must first program the address register (AR). For example, to write to R12, the CPU outputs 0CH to port 0DCH. This places the number 12 into AR. The CPU then outputs the data it wants to write to port 0DDH, which is loaded into register 12. Here's how it happens.

The CPU outputs the number 12 (0CH) to port 0DCH. This is coupled through U338 to the data lines of the CRTC. At this time, 6845CS at VIOSEL (U369) asserts the chip-select line at pin 25 of the CRTC. Since the port address is 0DCH, line BA0 = 0; thus accessing the AR.

When ECLK goes low, the data (0CH) on the bus lines is loaded into the address register. AR now points to register 12.

The CPU now outputs the byte it wants to write into port 0DDH; line 6845CS is again asserted. Since the port address is 0DDH, line BA0 = 1, telling the CRTC to route the data to the register pointed to by AR. When ECLK goes low, this data is loaded into register 12.

READING DATA FROM THE CRTC

The procedure is the same as writing data, except that U331 is selected instead of U338. This is done by $\overline{\text{DBIN}}$ from the S-100 bus and by $\overline{\text{4521CS}}$ from U366-14.

HOW THE CRTC ADDRESSES RAM

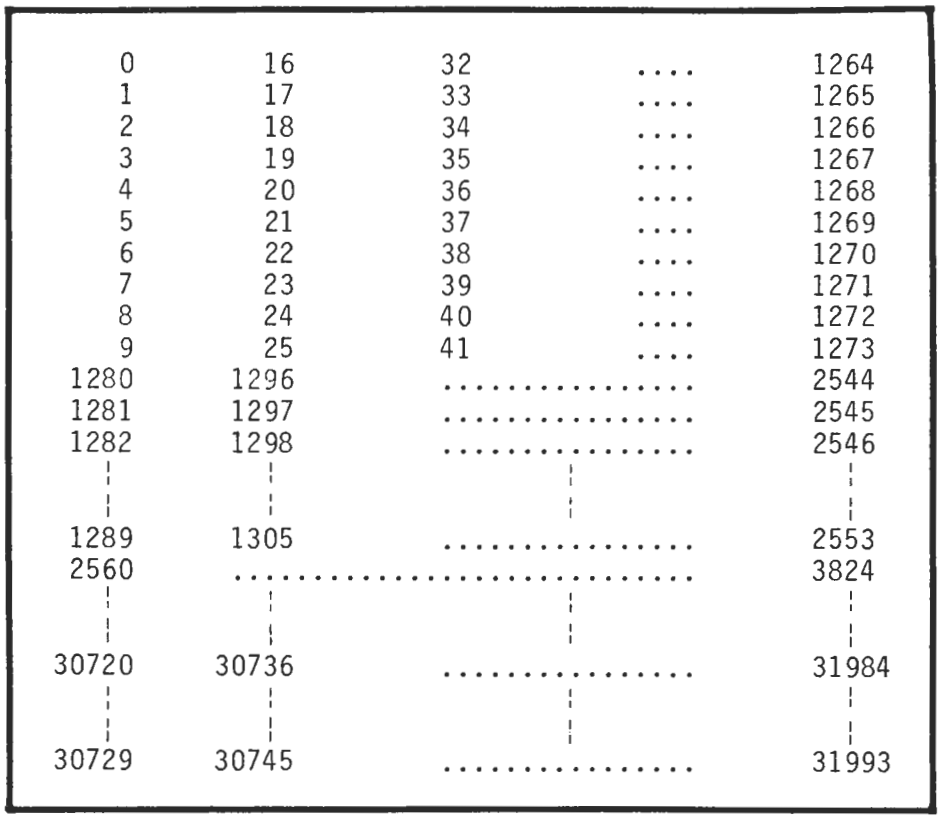
As mentioned before, the CRTC is normally programmed to emulate the H19 video terminal. That is, the display will contain 25 lines, 80 characters per line, and 10 scan lines (rows) per character line.

MA0-MA11 points to the character location within a character line and also points to the current character line. It does this by incrementing its base address by ten after every ten scan lines. RA0-RA3 counts the number of scan lines. After one scan line is complete (MA0-MA11 counts to 79), RA0-RA3 resets to 0 and MA0-MA11 resets to its base address. The count begins again. This procedure continues until 10 scan lines are processed. RA0-RA3 again returns to zero, but MA0-MA11 increments its base address by ten to point to the next character line.

For each address, a byte is read from video RAM (VRAM) and shifted serially out to the video amplifier with the horizontal and vertical sync pulses. The scan rate is such that each address row appears beneath the previous one so that the serial dots form characters on the screen. Once the last character row is processed, both RA0-RA3 and MA0-MA11 reset to zero, vertical retrace takes place, and the process repeats.

Incidentally, at vertical retrace a sync pulse is sent through U366 (lower left on the schematic) to interrupt the CPU. This permits the CPU to access the CRTC registers (for example, to scroll the display) without interfering with the display.

The address lines reach memory by passing through a set of multiplexers. RA0-RA3 connects to multiplexer U357 while MA0-MA11 connects to U363, U358, and U359. These ICs allow coupling the CRTC address lines to VRAM, or the CPU address lines to VRAM.



Relative Memory Location for Each Scanned Character (80 characters per line; 10 scan lines per character line, 25 character lines)

When line VIDRAMSEL is low, the multiplexers pass the CRTC address bus to the VRAM address bus. RA0-RA11 is the lower 4 bits, DA0-DA3; and MA0-MA11 are bits DA4-DA15. This causes the address line to increment by 16 for every scanned character. See the table on the previous page. This shows the on-screen character location and its relative address (decimal).

Lines DA0-DA15 connect to address multiplexer U360 and U373. This circuit splits the address for RAS and CAS timing. RAS timing occurs when ADMUX is high, coupling the following lines to the outputs:

VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0
DA9	DA8	DA7	DA6	DA5	DA4	DA1	DA2

CAS timing occurs when ADMUX goes low, causing:

VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0
DA15	DA14	DA13	DA12	DA11	DA10	DA0	DA3

The address lines at VA0 and VA1 are arranged so they can get refreshed during a normal CRTC scan. This results in a reduction of components in the video circuits.

Jumper J307 permits using 64K RAMs or 32K RAMs. To use 64K RAMs, connect the jumper from DA15 to U373-11. To use 32K RAMs located in the upper half of the 64K address space, remove the jumper. To use 32K RAMs in the lower half of the 64K address space, connect the jumper from U373-11 to ground. Note that if the computer uses 32K RAMs, they all must be located in either the upper 32K of each 64K bank or all in the lower 32K--they can't be mixed. See the H/Z-100 Memory Map located further on in this description.

CONVERTING THE RAM DATA TO VIDEO

There are two sets of data lines at the video memory. One is an 8-bit bus, BD0-BD7, used by the CPU to write to RAM (from U178 on schematic MB2); and three 8-bit output buses, one for each color.

The output buses go to the CPU through U339, U310, and U316. Only one of these ICs will be selected to place the data on BDI0-BDI7. This, in turn couples through U323 on MB2 to the CPU. This will be covered in more detail later.

The three output buses also couple to the video processing circuits through U332, U302, and U311. Here's how the data is processed.

When the CRTC has control of RAM (which is most of the time, since it has priority), the VRAM is in the read mode. This is due to a logic zero on VDRAMSEL (U337-4) and CLRSCRN (U366-3). When the addressed data settles, VIDSTRB from U376-17 asserts to latch the RGB data into U332, U302, and U311. (Note: If this is a minimum system--green only--U332 and U311 outputs will remain a steady state.)

Next, the load shift register line from U320-6 goes low to latch the RGB data into the parallel-to-serial converters, U325, U301, and U303. This line pulses at the character clock rate.

The dot clock, at pin 6 of these ICs, then shifts the data out through pin 13. This takes place at 8 times the character clock rate, or 14.112 MHz. While the video information is being shifted out, VIDSTRB is loading the next byte into the D latches. When the last dot is shifted out of the parallel-in/serial-out converter, the bytes in the D latches are loaded in and the cycle repeats.

The three serial dot lines connect to RIN, GIN, and BIN of U337, the VIDATTR PAL. Other inputs to U337 include the $\overline{\text{FLASH}}$ line and three enable lines at pins 1, 2, and 3.

When asserted, the enable lines from the PIA (U345) gate their respective dot video color to the outputs at pins 14, 15, and 16.

When the $\overline{\text{FLASH}}$ line--also from the PIA--is asserted, the output lines selected by the enable lines will go high, saturating that color onto the screen and masking any video data on that line.

For example, if $\overline{\text{ENBL-G}}$ were the only asserted enable line, then dot video would only be present on GOUT. Asserting the $\overline{\text{FLASH}}$ line would cause GOUT to go to logic one, causing the screen to appear solid green.

Two other lines enter U337; the display enable and the cursor signal. The display enable (DISEN) goes low to blank the video data during horizontal and vertical retrace. It comes from pin 18 of the CRTC and is delayed by two character clocks through the hex D flip-flop. This delay is used to match the timing of DISEN to the video signal delayed by the parallel-in/serial-out converters. If DISEN wasn't delayed, retrace blanking will occur 2 clock cycles early, blanking the last 2 character positions.

The cursor signal enters pin 6 to generate a cursor at ROUT, GOUT, and BOUT. It comes from pin 19 of the CRTC and goes through the hex D flip-flop to be delayed by two character clocks. This two-character delay places the cursor to the right of the last displayed character.

The horizontal and vertical sync pulses also come from the CRTC and are clocked through the D flip-flop. These signals, however, bypass U337 and connect to U329, another hex D flip-flop. The RGB lines enter this flip-flop at pins 11, 13, and 14. All five signals are clocked out by the dot clock entering at pin 9. The purpose of this flip-flop is to correct for any propagation delays in the various signal paths.

VIDEO OUTPUT

COLOR OUTPUT

The 3 RGB lines from U329 connect to U307 on schematic VB3. This buffer provides red, green, and blue video pulses to P303. Logic 1 equals color on; 0 is black level.

The horizontal and vertical sync pulses connect to U320, pins 12 and 9. These signals then pass through the drivers at U322 to P303. P303 connects through a mating cable to an RGB color monitor. Jumpers J302 and J304 allow selecting the polarity of the sync signals, while J303 allows sending composite sync to U320-9 by connecting it to U355-11.

MONOCHROME OUTPUT

RDOTA, GDOTA, and BDOTA also connect to U323, a 3-to-8-line demultiplexer. J306 and J305 connect one color to each input at pins 1, 2, and 3. If this is a minimum system (green only), then pins 1 and 2 are jumpered to pin 3.

U323 decodes the three inputs to assert only one output at Q0-Q7. This signal connects to U309, which is clocked through by the dot clock. The mnemonics on the output lines indicate the color represented by the combination of the three inputs. These outputs couple through the inverters to the resistive weighting network.

This network converts the associated line to a specific voltage level before applying it to the emitter followers at Q302 and Q301. This network forms a monochrome gray scale by controlling the current through the emitter followers.

For example, if RDOTA, GDOTA, and BDOTA were all asserted, U309-19 would go high, driving U308-8 low. This gives the highest emitter resistance, causing the most positive voltage at the output and giving maximum brightness.

If none of the RGB lines were asserted, then U309-2 would go high to place U322-6 at logic zero. This lowers Q301's emitter voltage to the black level.

Composite sync from U355-11 provides horizontal and vertical sync pulses at the blacker-than-black level.

The composite video output of P301 connects to the video input of the internal or external monochrome monitor.

CPU-VIDEO COMMUNICATIONS

OVERVIEW

The CPU can communicate with the video board through several I/O ports, or by read/writing the video RAM. It uses the I/O ports to access the CRTC, the PIA, and the light pen circuits. It can read/write the video RAM to set up the character font or draw high-density graphics.

VIDEO I/O CIRCUITS

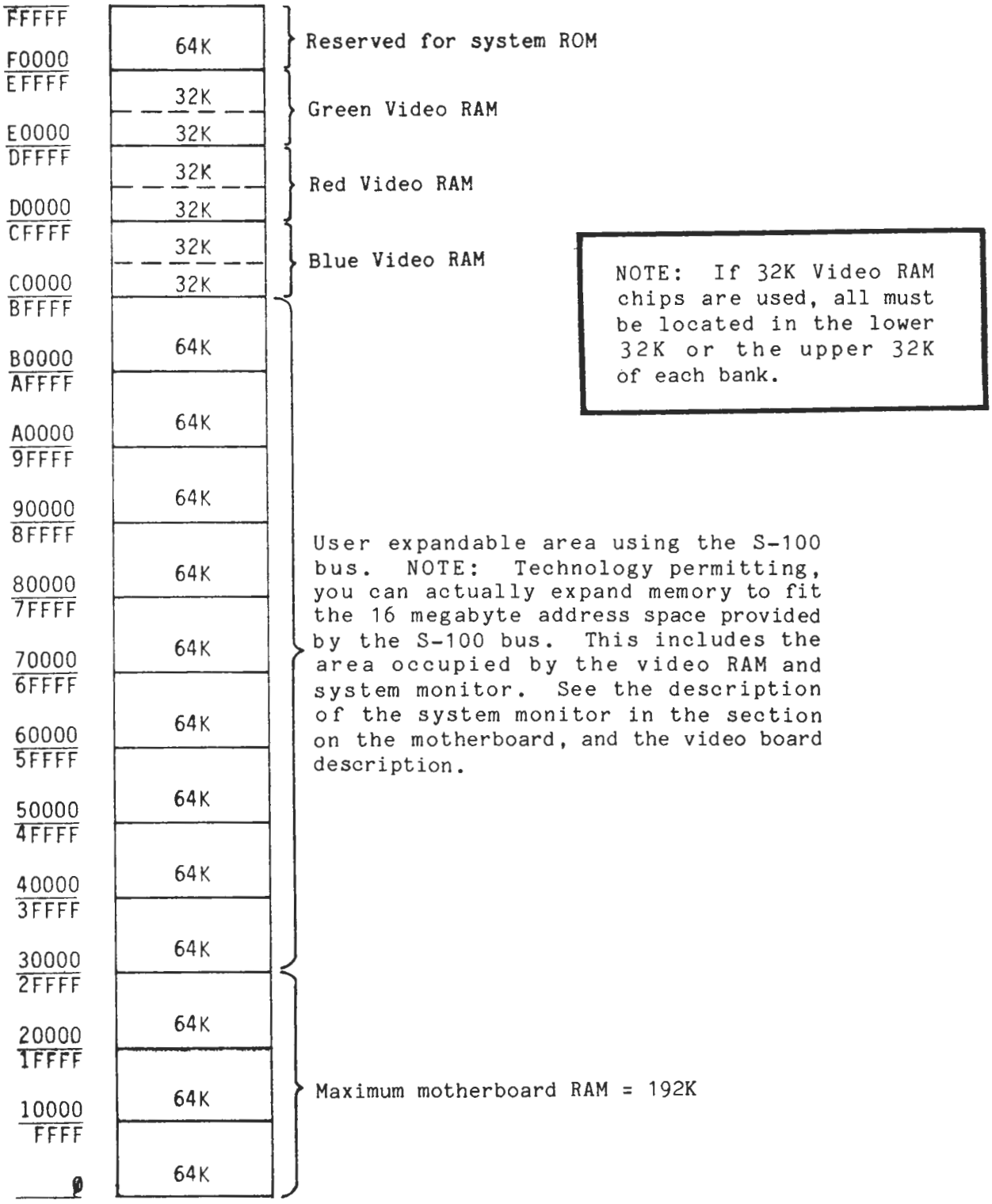
Video I/O addresses are decoded by VIOSEL, U369, a 256 x 4 PROM. This IC (on schematic VB1) is selected by the appropriate address on BA0-BA7 and the $\overline{IO}$ line from the E-clock logic on schematic MB2. The outputs are:

$\overline{6845CS}$ Selects the CRTC programming as described earlier.

$\overline{CRTIOCS}$ (A) Chip-selects the PIA at U345, and (B) provides one input to the OR gate, U372/U366. The other input to this OR gate is $\overline{6845CS}$; the output is $\overline{4521CS}$. This line chip-selects U331 when the CPU is reading data from the CRTC or from the PIA.

$\overline{LPNCS}$ Chip-selects the light-pen counter circuits at U315 if the CPU is processing a light-pen interrupt request. See the discussion on the light-pen circuits.

$\overline{VIDBSEL}$ Asserts when pins 12, 13, or 10 asserts. This line goes to U372-13 and is NANDed with $\overline{DBIN}$ at U366-13. The result is $\overline{RDBFRENBL}$ at P304-57; this enables the read buffer, U223 on schematic MB2, when one of the VIOSEL lines is asserted.



H/Z-100 MEMORY MAP

Another video I/O circuit is the PIA at U345 (near the center of schematic VB1). This is used for address decoding, controlling the display, and performing some VRAM operations.

The CPU selects the PIA at ECLK time (pin 25) by asserting CRTIOCS at pin 23. BA0 and BA1 select the register to be accessed while OUT determines if data is to be read from or written to that register. For this PIA, all I/O lines are programmed to be outputs. Here's what they do:

ENBL-R, -G, -B, & FLASH Enables the selected video line without affecting RAM. FLASH causes the selected line to appear as a solid color. See "Converting the RAM Data to Video" for more information.

WRT-R, WRT-G, WRT-G Selects the red, green, or blue banks when the CPU writes to VRAM. These lines are necessary because there's only one 8-bit data bus from the CPU; so red, green, and blue data must be written at separate times.

CRTRAM ENBL Chip-selects VRAMSEL, U371-4, which selects the red, green, or blue banks when the CRT reads the VRAM.

LA8-LA15 Goes to the memory mapping module to decode the selected video memory location.

CLRSCRN Goes to the video memory circuits to provide a quick means to clear the screen.

MEMORY SELECT CIRCUITS

The memory select circuits are centered around U371, VRAMSEL, a 256 x 4 PROM. This IC is used when the CPU wants to access the red, green, or blue memory banks. VRAMSEL is selected by asserting CRTRAM ENABLE at the PIA. Also, MEMR or WO is gated through U377 (near VRAMSEL) for further chip-selecting. The OUT line at U377-2 ensures that U371 won't activate on an OUT port operation.

The outputs assert depending on what location in the video memory map is selected:

RSEL = 0D0000H-0DFFFFH
GSEL = 0E0000H-0EFFFFH
BSEL = 0C0000H-0CFFFFH

Each line has a 64-kilobyte range; currently, Heath Company supports only 32K.

$\overline{\text{CRTRAMSEL}}$ asserts whenever pin 11, 10, or 9 asserts. This connects to U372-12 in the lower left corner of the schematic. It is combined with $\overline{\text{VIDBDSEL}}$ and $\overline{\text{DBIN}}$ to assert $\overline{\text{RDBFR ENBL}}$. This line enables U223 (on schematic MB2) during a memory read operation.

$\overline{\text{CRTRAMSEL}}$ is double-inverted at U366-5 to form $\overline{\text{CRTRAMSEL1}}$ at P305-61. This line asserts PHANTOM* at U194-4 on MB2. If an S-100 memory card is occupying the same memory space as VRAM, PHANTOM* prevents the CPU from writing to the S-100 memory when it's accessing video RAM. This permits installing read/write memory in the same address space as VRAM without them interfering with each other.

$\overline{\text{CRTRAMSEL}}$ also goes to U372-3, $\overline{\text{VIDRAMRDY}}$, through an inverter. If the CRTC is busy processing a video signal, it won't let the CPU access the RAM circuits. U372-2 is also high, causing $\overline{\text{VIDRAMRDY}}$ to go low. This drives RDY low at U194-12 on schematic MB2, putting the CPU into a wait state. The CPU will hold $\overline{\text{CRTRAMSEL}}$ asserted until the CRTC gives the CPU control of the video circuits.

Finally, $\overline{\text{CRTRAMSEL}}$ goes to U379-11, part of the CPU/video arbitration circuits. These circuits synchronize the video circuits to the CPU circuits and determine when the CPU can access the video RAM. See the previous paragraph and the description of the control and timing circuits.

READ DATA BUFFERS

The CPU reads the addressed data through either U339, U310, or U316. When the CPU reads VRAM, the memory places data on the inputs of these latches. To read a particular bank, the CPU asserts $\overline{\text{RSEL}}$, $\overline{\text{GSEL}}$, or $\overline{\text{BSEL}}$. For example, to read the data in the green video memory bank, the CPU addresses the desired video memory section (to be explained shortly) and asserts $\overline{\text{GSEL}}$ at U371-10 (upper left on schematic VB1). This signal connects to U351-9 (right center on schematic VB1). When $\overline{\text{DBIN}}$ from the S-100 bus asserts, U351-8 goes low to couple the data in U310's latches to the BDI bus. In turn, this data couples through U223 (on schematic MB2) to S-100 lines DI0-DI7 before coupling to the CPU.

MEMORY MAPPING MODULE

The memory mapping module consists of U370, U364, and U365. It translates the CPU address range into the address range used by the CRTC. The CRTC sees the VRAM in the range of 0-64K, while the CPU sees the memory in the range of 768K to 960K.

To convert the CRT address range to 0-64K, the CPU latches a bit pattern into LA8-LA15. The CPU then requests access of the video RAM by asserting VIDRAMSEL, the desired color bank (RSEL, BSEL, GSEL), and the appropriate address lines on the inputs of U370.

U370 decodes the address and feeds it to the adders at U364 and U365. These ICs add the decoded address to LA8-LA15 and places the result onto the B inputs of U358 and U359. The rest of the CPU address is present on the B inputs of U357 and U363.

When the CRTC is finished accessing the display, it brings VIDRAMSEL low at U377-4 (lower left corner of schematic). This couples the B inputs of the multiplexer ICs onto address lines DA0-DA15. The correct VRAM location can now be read or written.

VIDEO RAM

OVERVIEW

Schematic VB2 shows a close-up of the video RAM.

The video RAMs are 32K x 1-bit dynamic RAMs; 64K RAMs can also be used, but aren't currently supported. The RAMs are arranged into three banks, 64K apart; one bank for each of the primary colors. In a minimum system, only the green bank will contain memory. The CPU can read/write RAM, while the CRTC can only read.

CPU WRITE

The CPU writes to RAM through U346; it places data onto the bus and asserts WE of each chip through U374-11. This comes from BMWRT and VIDRAMSEL at U355-5 and U351-4.

The RAS portion of the address is present on VA0-VA7.

The correct color bank(s) is selected by asserting $\overline{\text{WRT-R}}$, $\overline{\text{WRT-G}}$, and $\overline{\text{WRT-B}}$ at pins 2, 4, and 10 of U350. This gates the RAS line through U375-11, U375-8, and U374-8 for the selected bank.

Next, the CAS address is placed on VA0-VA7 and the CAS line asserts U375-3, U375-6, and U374-6. Only the bank(s) previously selected by RAS will be affected.

Data present at the inputs of U346 are coupled into the appropriate memory location(s) in the video RAM.

CPU READ

When the CPU reads from RAM, it asserts $\overline{\text{R-SEL}}$, $\overline{\text{G-SEL}}$, or $\overline{\text{B-SEL}}$ to select the appropriate color bank. The RAS and CAS lines operate as before. The addressed data is placed on the DOUT lines of the selected banks and read by the CPU as explained previously.

CRTC READ

The CRTC reads all three banks at the same time; the enable lines at U337 (schematic VB1) select which banks are to be displayed as explained previously. When the CRTC has control, VIDRAMSEL is low and couples to pins 13, 5, and 11 of U350. This forces pins 12, 6, and 8 of U350 to logic 1.

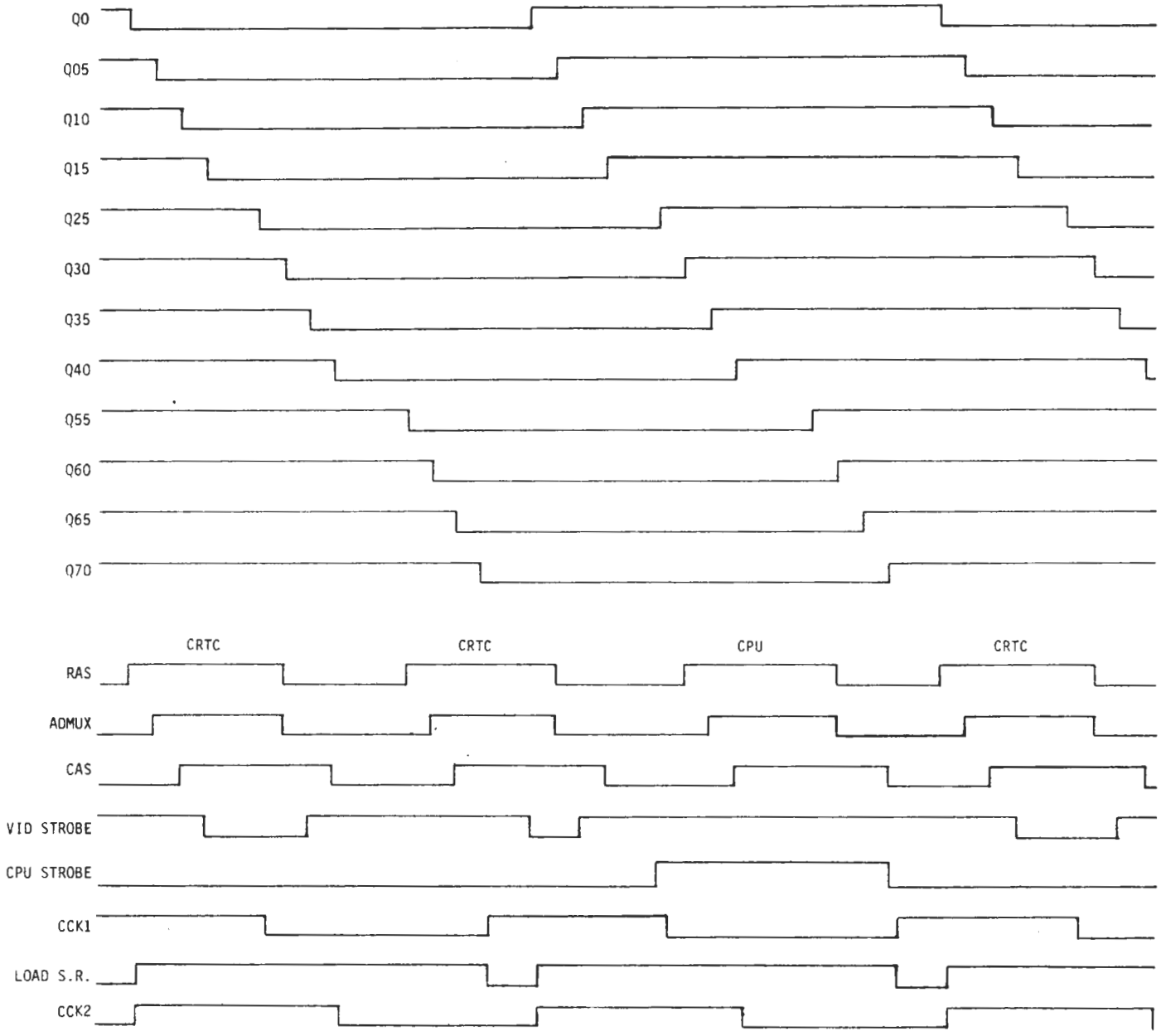
When RAS occurs, the address on VA0-VA7 is latched into all three banks. Next, CAS asserts and also addresses all three banks. The data from each bank is placed onto the appropriate bus and sent to the parallel/serial conversion circuits.

CLEAR SCREEN FUNCTION

The clear screen function allows the CPU to quickly clear the screen. Instead of directly writing to memory, which is time-consuming, the CPU uses the fast scanning feature of the CRTC. Here's how.

The CPU asserts the CLRSCRN line at the PIA; it also clears or sets the SET line. These lines connect to the PAL at U346; CLRSCRN disconnects the PAL from the data on its input, while SET places all ones or zeros on the output lines, depending on the logic level at pin 11. (If logic one, the screen will be painted white instead of blanked.)

CLRSCRN also connects to U355-4 and U351-5 to force the $\overline{WE}$ line low on all RAMs. During this time, the CRTC has control of the bus. Since the CRTC scans all memory locations, each bank will be filled with ones or zeros, depending on the level on SET. The CRT is quickly blanked or flashes white.



VIDEO BOARD TIMING

TIMING AND VIDEO ARBITRATION

TIMING

Refer to schematic VB1 and the accompanying waveforms as you read the following.

The 14.112 MHz crystal-controlled oscillator at U368 provides the basic timing for the video circuits. This signal couples through U344-11 to provide dot clock and couples through U344-6 for inverted dot clock. This method was used instead of series-connected inverters to ensure that the two clock signals are exactly 180-degrees out of phase.

DOTCLK drives U336 and U343; these ICs are wired as a ring counter to derive Q0-Q70 shown in the adjacent waveforms. U367, driven by $\overline{\text{DOTCLK}}$, uses some of these outputs to generate the odd-numbered waveforms from Q05 to Q65. These signals connect to the VIDRAM PAL at U376.

U376 uses the Q signals to generate VIDSTRB, ADMUX, RAS, and CAS. VIDSTRB clocks addressed data into the latches prior to parallel-to-serial conversion as described previously. ADMUX multiplexes the 16-bit address bus onto an 8-bit address bus in time with RAS and CAS. ADMUX is low during RAS and high during CAS.

The CRTC has control of the video circuits for 2/3 of any timing cycle. This ensures fast display refresh while the remaining 1/3 allows the CPU to rapidly update the display memory.

The CRTC's portion of the cycle begins on the negative transition of Q0. This is indicated by the two RAS waveforms marked "CRTC" on the Video Board Timing waveforms. Video arbitration circuits (to be explained presently) ensure that the CRTC always has control during these two RAS cycles.

The third RAS cycle of the video timing cycle is reserved for the CPU. If the CPU doesn't attempt to read or write memory, RAS will not assert during the time marked "CPU." If the CPU does attempt to read or write memory, RAS will assert and the memory access can take place. Note that during CPU RAS time, VIDSTRB (U376-17) doesn't pulse. This prevents the addressed memory location from being latched into U322, U302, and U311; keeping unwanted noise off the display.

If the CPU attempts to access video memory during the CRTC portion of the cycle, the arbitration circuits places a logic zero on P305-62. This logic zero couples to the CPUs READY line which puts the CPU into a wait state. The CPU ceases activity until the "CPU" RAS cycle begins. At this time, P305-62 goes high to activate the CPU.

Obviously, the CPU processing time will slow down if it performs a lot of reading and writing to video RAM. However, the video arbitration circuits do not slow down the CPU for non-video operations (such as I/O and system memory accesses). As long as the CPU isn't accessing the video circuits, P305-62 remains high and the CPU operates at full speed.

Now for a closer look at the video arbitration circuits.

VIDEO ARBITRATION

The video arbitration circuits determine if the CPU is requesting access to the video RAM. If the CRTC is not using the RAM, it gives control to the CPU. However, the CRTC always has priority.

As mentioned previously, the CPU requests control of the VRAM by asserting $\overline{\text{RSEL}}$, $\overline{\text{GSEL}}$, or $\overline{\text{BSEL}}$ at U371. This asserts $\overline{\text{CRTRAMSEL}}$ which couples through U372-3 to put the CPU into a wait state after the CPU finishes the 2nd processor cycle.

$\overline{\text{CRTRAMSEL}}$ also goes to U379-11 to set up the bus arbitration circuits for a read/write request from the CPU. If the operation is a CPU write, then U379-3 goes high. If the operation is a CPU read, then MEMR is clocked into U378-5 when STVAL*SYNC asserts. In turn, U378-5 couples the logic one to U379-2.

At this time, U361-8 is latched to logic one which is coupled to U372-2. U372-1 is also logic one due to the asserted CRTRAMSEL line at U366-4. U372-3 holds the CPU in a wait state as described previously. Because of this, pins 11 and 12 of U379 remain at logic zero. The resulting logic 1 at U379-13 is the CPU request signal which couples to pin 2 of U361.

When the CRTC has completed processing the video circuits, Q15 at U361-3 goes high. This latches U361-6 to logic zero and, because U361-9 is also zero, drives the VIDRAMSEL line at U377-4 to logic one. VIDRAMSEL connects to the control inputs of the CPU/CRTC address multiplexers to couple the CPU address lines to the video memory circuits.

If the CPU is writing memory, data from the S-100 bus is present on lines BD00-BD07. BMWRT writes this data into memory. If the CPU is reading memory, the addressed memory location places the data onto U339, U310, or U316; depending on the RGB select lines going into memory.

When line Q65 goes high, the logic one at U361-5 is latched into U361-9. This latches the data on the inputs of U339, U310, and U316 onto their outputs; if memory read. The status of the gate at the input of each octal latch will determine which latch will be coupled to the bus.

At the same time, U361-8 goes low to bring $\overline{\text{VIDRAMRDY}}$ high. The CPU leaves the wait state and finishes processing the instruction. $\overline{\text{CRTRAMSEL}}$ goes high to drive U379-13 low. Since VIDRAMSEL is also low, U355-3 goes to logic zero to clear U361.

The CRTC again has control of the video board.

LIGHT PEN CIRCUITS

The light pen strobe enters U362-12 (at top center of schematic VB1) from U116-9 on schematic MB4 (see the parallel port description for more detail). The $\overline{\text{DOTCLK}}$ signal toggles LTPNSTB through U362-9 to U356-5. Next, the clock signal at U356-11 latches the LTPNSTB signal onto U356-9. This positive-going signal latches the refresh address into the CRTCs light pen register. The refresh address points to the first line of characters to be displayed after vertical retrace. See the CRTC IC data sheets.

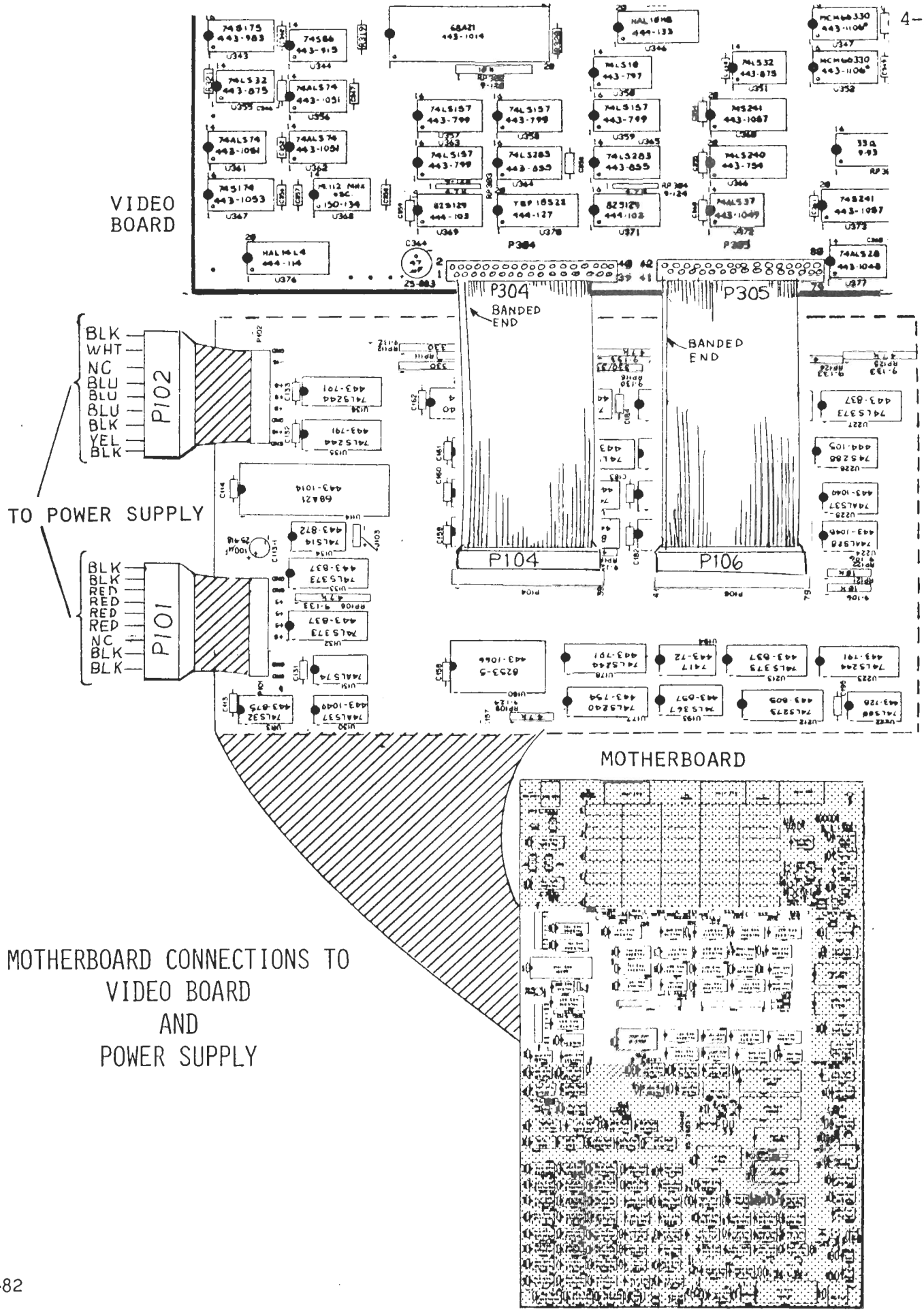
Also, the output of U356-5, PENSTBD, goes to U315-11 (lower right corner of the schematic). U315 is an octal latch that is loaded by the CRTC row address lines, RA0-RA3, and the 4-bit down-counter, U324.

At the time of PENSTBD, RA0-RA3 point to the row that was active when the light pen strobe occurred; U324 points to the dot position.

As explained in the parallel port description, when LTPNSTB asserts, the parallel port (on schematic MB2) sends an interrupt to the CPU. From here, it's up to the user's program to process the interrupt.

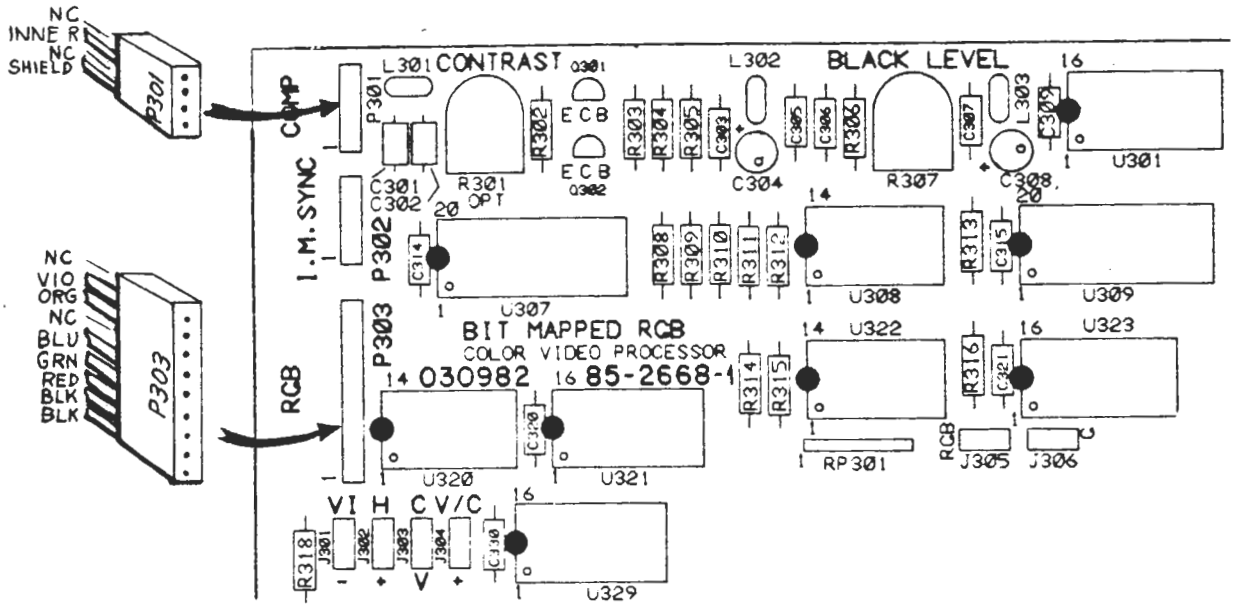
If the CPU is programmed to respond to a light-pen interrupt, it will read the data stored in the CRTC light-pen register and the data stored U315 to find the exact pixel location. The CPU reads the CRTC as described earlier; it reads U315 by asserting $\overline{\text{LTPNCS}}$ from the VIOSEL PROM and $\overline{\text{DBIN}}$ from the S-100 bus. From here, the CPU can compute the video memory location and access the bit in that memory location to be processed.

VISUAL CHECKS

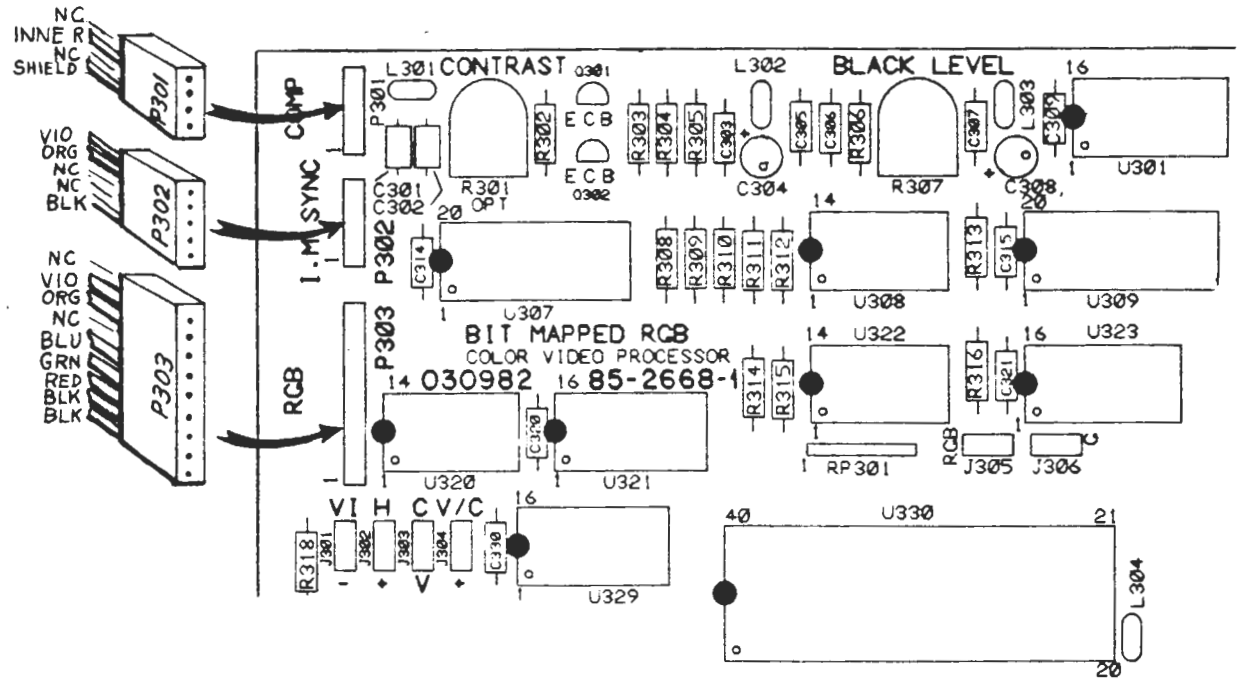


MOTHERBOARD CONNECTIONS TO
VIDEO BOARD
AND
POWER SUPPLY

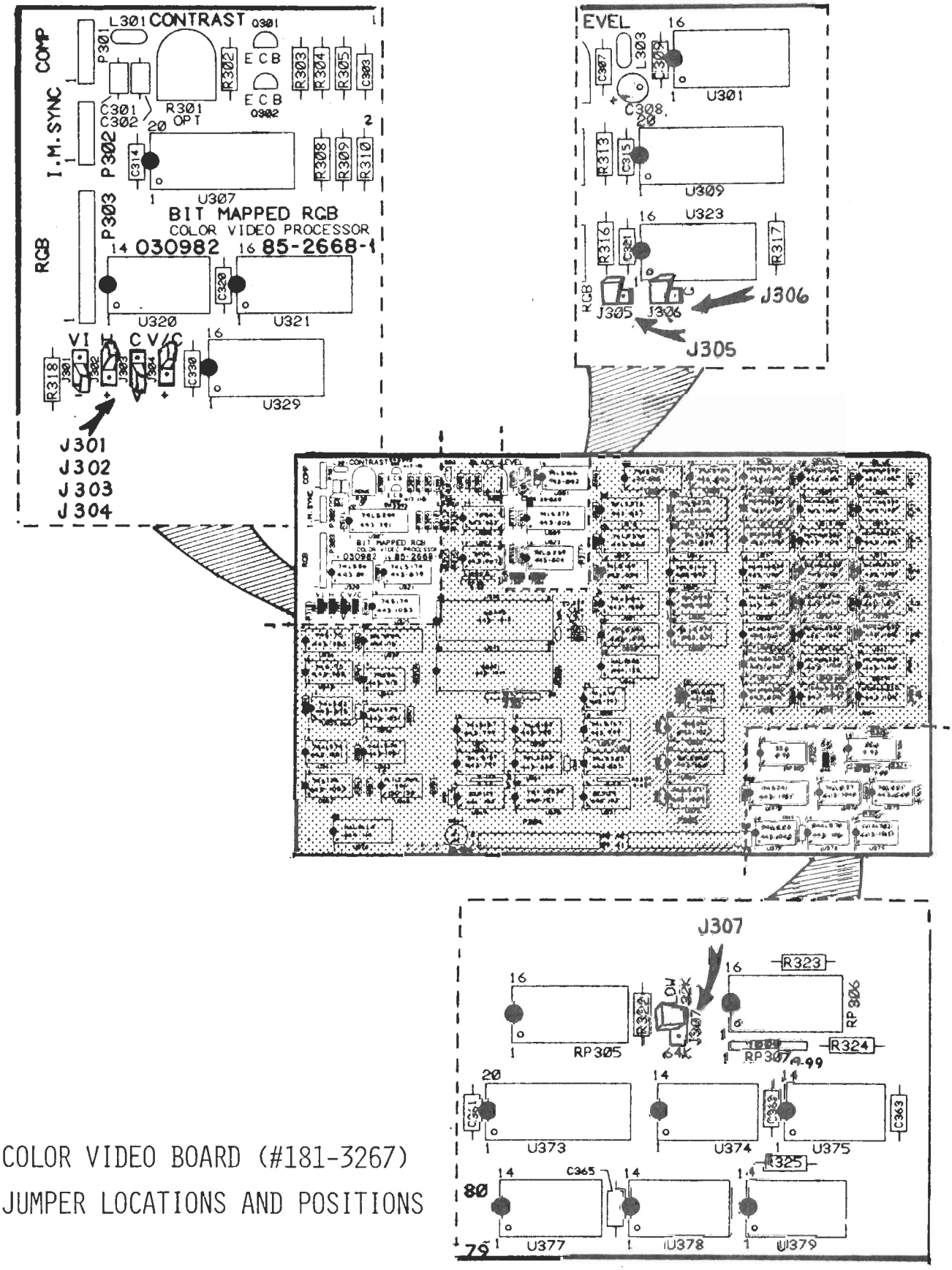
VIDEO BOARD CONNECTIONS



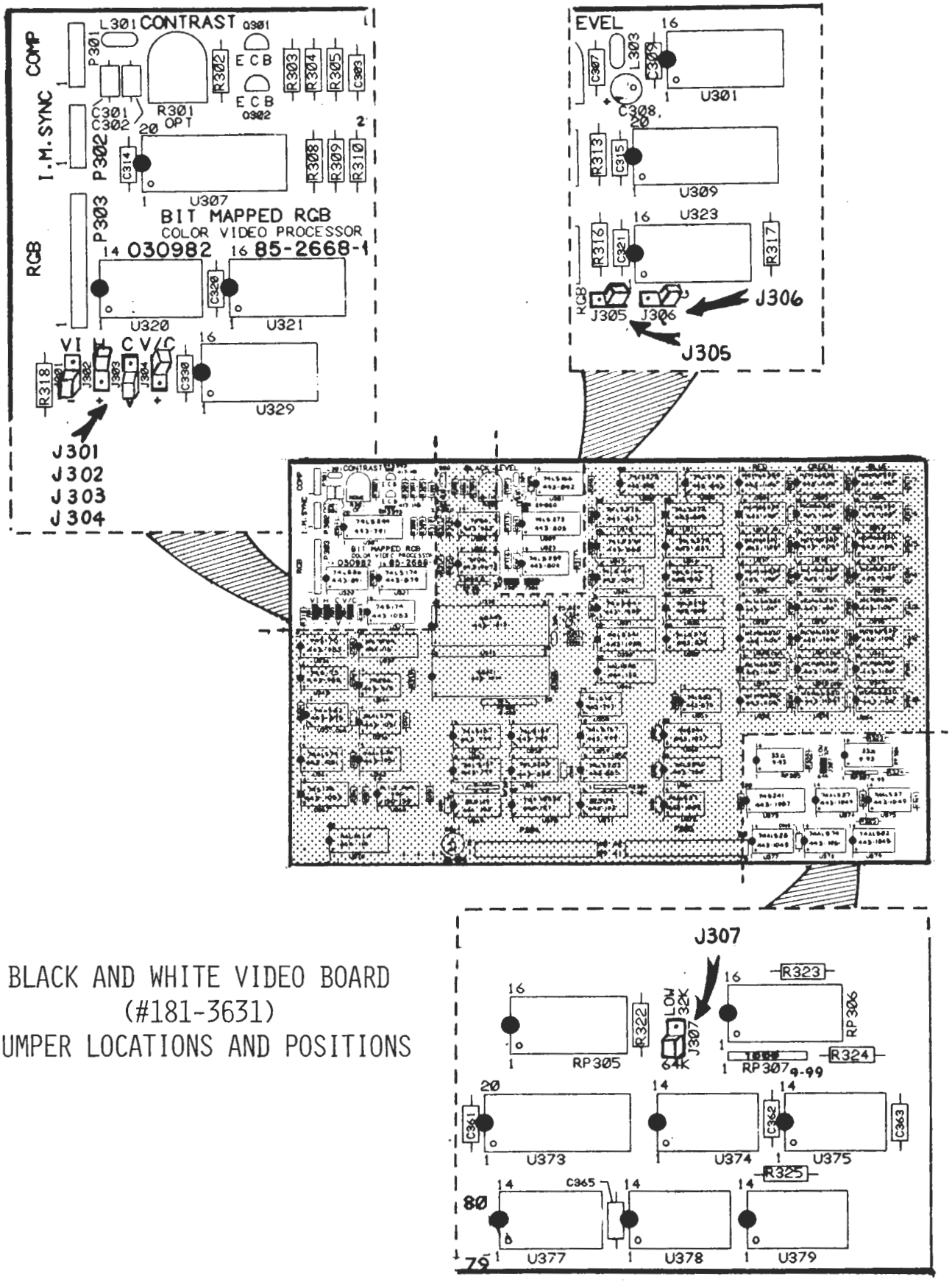
LOW-PROFILE VIDEO BOARD CONNECTIONS



ALL-IN-ONE VIDEO BOARD CONNECTIONS

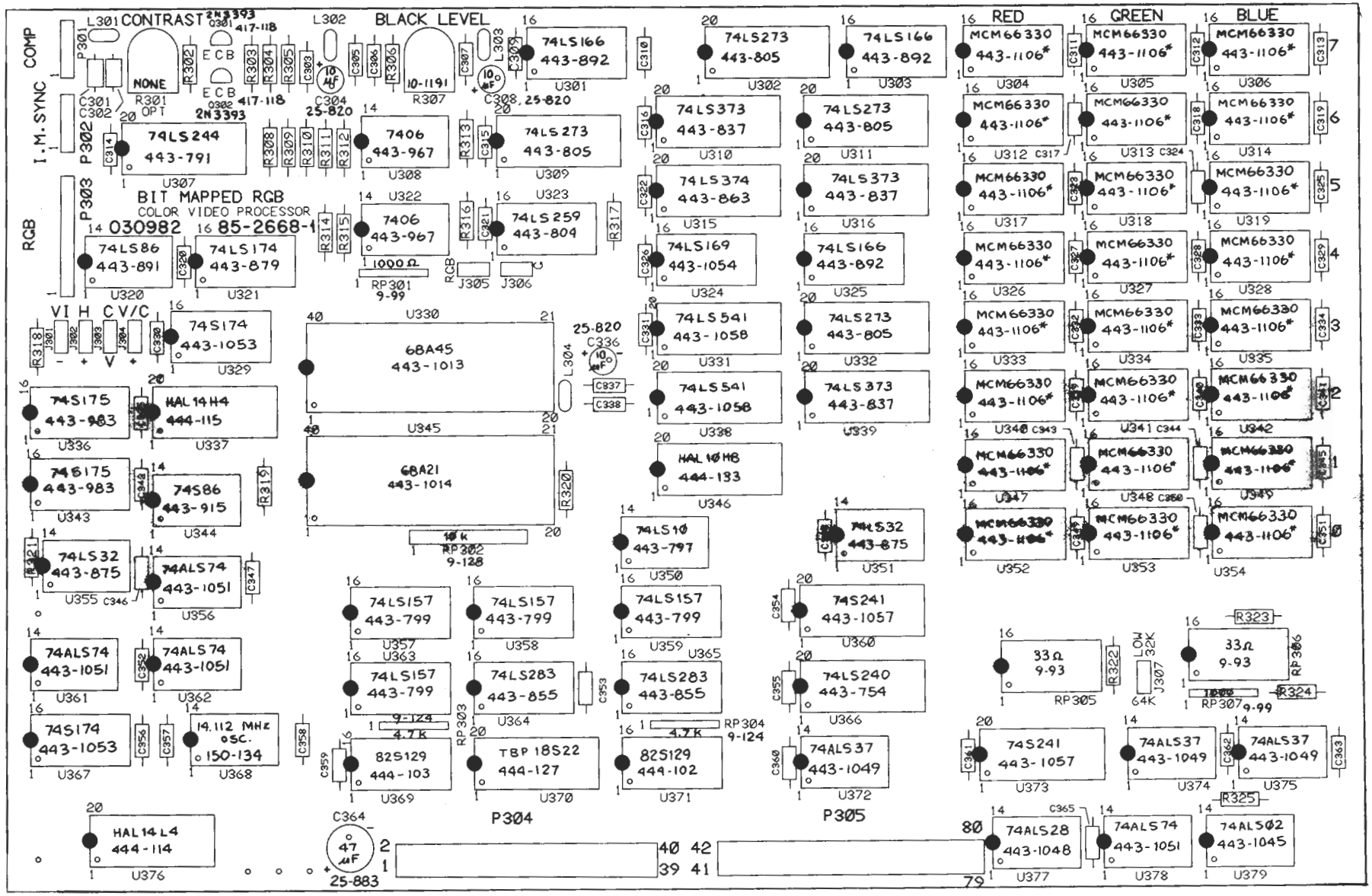


COLOR VIDEO BOARD (#181-3267)
JUMPER LOCATIONS AND POSITIONS



BLACK AND WHITE VIDEO BOARD
(#181-3631)
JUMPER LOCATIONS AND POSITIONS

CIRCUIT COMPONENT LOCATIONS AND VALUES



**NOTE: The ICs in these locations may be MCM6665 (HE 443-970). Refer to "Configuration" for further information.*

COLOR VIDEO BOARD

BLACK AND WHITE: HE 181-3631
COLOR: HE 181-3267

VIDEO BOARD
COMPONENT LOCATION AND VALUES, FOIL SIDE OF BOARD

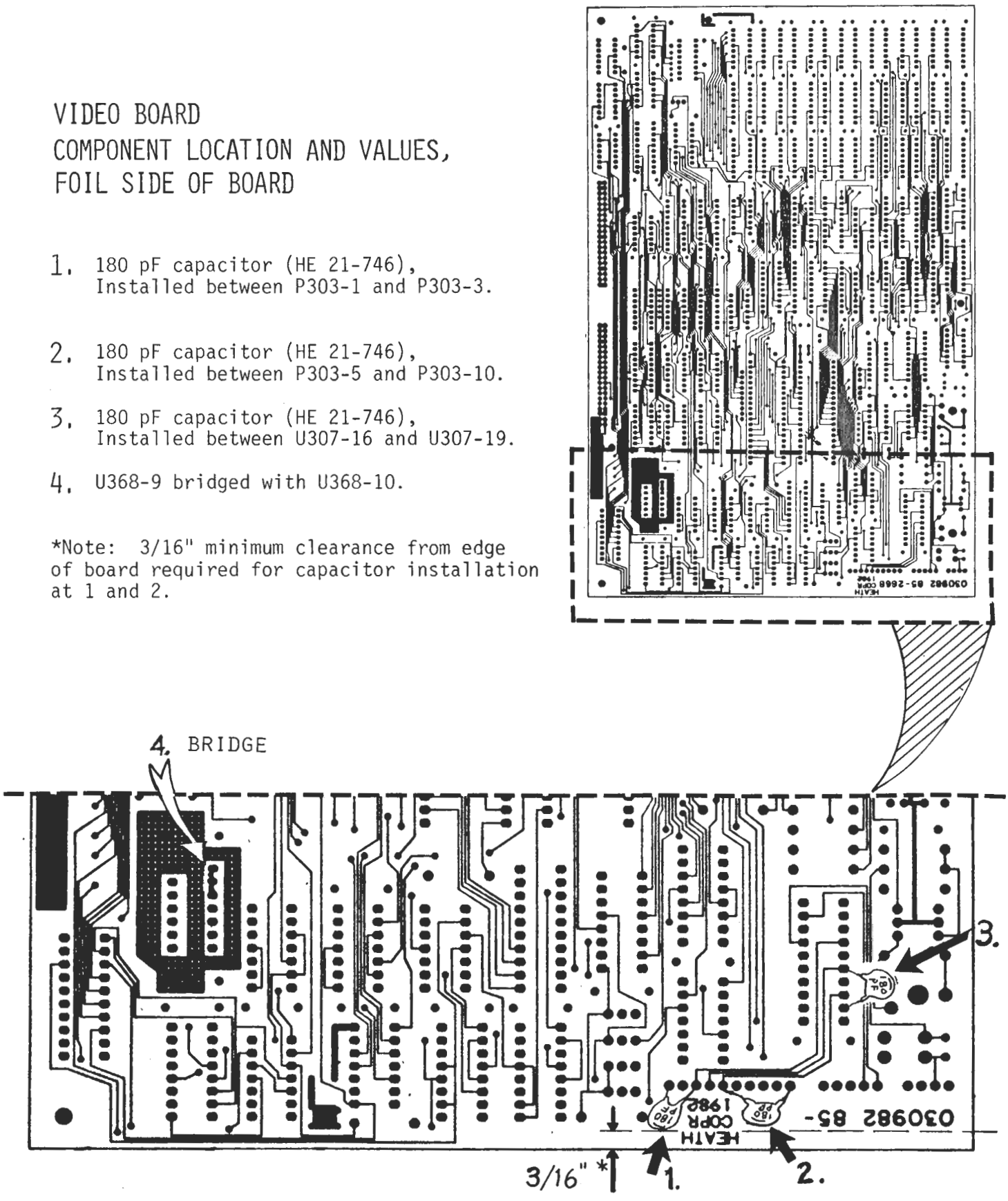
1. 180 pF capacitor (HE 21-746), Installed between P303-1 and P303-3.

2. 180 pF capacitor (HE 21-746), Installed between P303-5 and P303-10.

3. 180 pF capacitor (HE 21-746), Installed between U307-16 and U307-19.

4. U368-9 bridged with U368-10.

*Note: 3/16" minimum clearance from edge of board required for capacitor installation at 1 and 2.



TROUBLESHOOTING

INTRODUCTION

The following procedure will help you repair the video board to the point where you can get a display on the screen. Though these tests aren't as fast or thorough as a diagnostics program, they'll help you narrow the problem down to two or three components. Once you get the display working, run the video memory test described in the Diagnostics section of this manual.

As diagnostic programs become available, we will publish them for inclusion in the Diagnostics section of this manual. Also, if you develop any troubleshooting techniques or diagnostic programs that you'd like to share, send it to:

Heath Company
Service Publications and Training
Dept. 741
Benton Harbor, Mi. 49022

We will evaluate your submission and, when approved, publish it for inclusion in the Service Bulletins or Diagnostics sections of this manual. Be sure to include a complete description of the troubleshooting technique, symptoms caused by the failed component, and any special equipment needed to repair the problem. If submitting a diagnostic program, we will need a copy of the source listing; preferably on disk.

SERVICE GUIDE

As you become more experienced troubleshooting the H/Z-100, you'll be able to skip this section and go directly to the group of circuits causing the problem. Until then, use the following guide to locate the most likely circuits to test for a particular symptom.

Detailed checkout procedures for the major circuits on the video board follow the service guide. If this is your first time troubleshooting the H/Z-100, read the introduction to the checkout procedure before proceeding with those tests.

Finally, bear in mind that these test procedures are for isolating problems on the video board. All the other modules in the H/Z-100 must be known to be operating properly. Otherwise, you won't get the correct results.

1. No display, or no horizontal or vertical sync.

   Perform the Video Signal and Sync Tests.

   Check the video monitor or video sweep board for proper operation.

2. Video circuits won't initialize. High-pitched squeal heard from monitor and torn raster seen on the CRT.

   The CRTC isn't being programmed properly by the CPU on the motherboard. Check for secure connections on P304 and P305.

   Perform the checks under Video I/O Tests.

3. Characters on the CRT are distorted.

   Nonlinear sweep in the video monitor.

   Perform the video memory tests in the Diagnostics section of this manual.

TECHNICIAN NOTES:

CHECKOUT PROCEDURES

In the following tests, you need only test the ICs in the left column indicated by an asterisk (*). If you don't get the suggested logic state, then check each IC listed immediately to the right. The logic states for these ICs are listed in the left column below the ICs with the asterisks.

Continue tracing backwards using this procedure until you test an IC that matches the suggested logic state. The previous IC that you tested is likely the bad IC.

Before you replace the suspected IC, check the other lines leading up to it. You must do this because this checkout procedure gives only the most likely causes of the problem. It doesn't cover such things as open ground foils, foil runs shorted together, open resistors, or missing power supplies.

To help you locate the IC on a schematic, the schematic number is shown in parenthesis to the right of the IC under test.

Unless instructed otherwise, perform these tests with the H/Z-100 configured for 5-1/4" drives (primary) and with auto-boot defeated. See the Configuration section. Also, unless noted otherwise, all logic states are those present after a hard reset.

VIDEO SIGNAL AND SYNC TESTS

CHECK		IF NOT OKAY, CHECK
*U307-7 = P	(VB3)	U307-13
*U307-9 = P	(VB3)	U307-11
*U307-14 = P	(VB3)	U307-6
*U307-16 = P	(VB3)	U307-4
*U307-18 = P	(VB3)	U307-2
*U322-2 = P	(VB3)	U322-1
*U322-12 = P	(VB3)	U322-13
*U355-11 = P	(VB3)	U355-12, U355-13

End of test.

J301	(VB3)	See Configuration Section.
J302	(VB3)	See Configuration Section.
J303	(VB3)	See Configuration Section.
J304	(VB3)	See Configuration Section.
U301-6 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U301-13 = P	(VB1)	U301-6, U301-15, U302-11
U301-15 = P	(VB1)	U320-6
U302-11 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U303-6 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U303-13 = P	(VB1)	U303-6, U303-15, U311-11
U303-15 = P	(VB1)	U320-6
U307-2 = P	(VB3)	U329-15
U307-4 = P	(VB3)	U329-12
U307-6 = P	(VB3)	U329-10
U307-11 = P	(VB3)	U329-2
U307-13 = P	(VB3)	U320-3
U311-11 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U320-1 = P	(VB3)	U329-5
U320-3 = P	(VB3)	U320-1, J301
U320-4 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U320-5 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U320-6 = P	(VB1)	U320-5, U320-4
U320-8 = P	(VB3)	U320-9, J304
U320-9 = P	(VB3)	J303, U329-5
U320-11 = P	(VB3)	U320-12, J302
U320-12 = P	(VB3)	U329-2

U321-2	= P	(VB1)	U321-3, U321-9
U321-3	= P	(VB1)	U330-39
U321-4	= P	(VB1)	U330-40
U321-5	= P	(VB1)	U321-4, U321-9
U321-6	= P	(VB1)	U330-19
U321-7	= P	(VB1)	U321-6
U321-9	= P	(VB1)	U344-8
U321-10	= P	(VB1)	U321-11, U321-9
U321-11	= P	(VB1)	U321-7
U321-12	= P	(VB1)	U321-13
U321-13	= P	(VB1)	U330-13
U321-14	= P	(VB1)	U321-12
U321-15	= P	(VB1)	U321-14, U321-9
U322-1	= P	(VB3)	U320-8
U322-13	= P	(VB3)	U320-11
U325-6	= P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U325-13	= P	(VB1)	U325-6, U325-15, U332-11
U325-15	= P	(VB1)	U320-6
U329-2	= P	(VB1)	U329-3, U329-9
U329-3	= P	(VB1)	U321-2
U329-4	= P	(VB1)	U321-5
U329-5	= P	(VB1)	U392-4, U329-9
U329-9	= P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U329-10	= P	(VB1)	U329-11, U329-9
U329-11	= P	(VB1)	U337-14
U329-12	= P	(VB1)	U329-13, U329-9
U329-13	= P	(VB1)	U337-15
U329-14	= P	(VB1)	U337-16
U329-15	= P	(VB1)	U329-14, U329-9
U330-13	= P	(VB1)	U330-21, VIDEO I/O TESTS. If the unit passes these tests, then replace U330, U338, and U331.
U330-19	= P	(VB1)	U330-21, VIDEO I/O TESTS.
U330-21	= P	(VB1)	U344-3
U330-39	= P	(VB1)	U331-21, VIDEO I/O TESTS. If the unit passes these tests, then replace U330, U338, and U331.
U330-40	= P	(VB1)	U330-21, VIDEO I/O TESTS. If the unit passes these tests, then replace U330, U338, and U331.

U332-11 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U337-1 = L	(VB1)	U345-2
U337-2 = L	(VB1)	U345-3
U337-3 = L	(VB1)	U345-4
U337-4 = H	(VB1)	U345-5
U337-5 = P	(VB1)	U321-15
U337-6 = P	(VB1)	U321-10
U337-7 = H/P	(VB1)	If the unit is a monochrome H/Z-100, then U337-7=H; replace U337. Otherwise, if the unit is color, U337-7=P. If not, check U325-13.
U337-8 = P	(VB1)	U301-13
U337-9 = H/P	(VB1)	If the unit is a monochrome H/Z-100, then U337-9=H; replace U337. Otherwise, if the unit is color, then U337-9=P. If not, check U303-13.
U337-14 = P	(VB1)	U337-1, U337-5, U337-6, U337-7, U337-4
U337-15 = P	(VB1)	U337-2, U337-5, U337-6, U337-8, U337-4
U337-16 = P	(VB1)	U337-3, U337-5, U337-6, U337-9, U337-4
U344-1 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U344-2 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U344-3 = P	(VB1)	U344-1, U344-2
U344-8 = P	(VB1)	U344-9, U344-10
U344-9 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U344-10 = P	(VB1)	See VIDEO TIMING and CONTROL TESTS.
U345-2 = L	(VB1)	Perform the VIDEO I/O TESTS. If the unit passes these tests, then replace U345, U338, and U331.
U345-3 = L	(VB1)	Perform the VIDEO I/O TESTS. If the unit passes these tests, then replace U345, U338, and U331.
U345-4 = L	(VB1)	Perform the VIDEO I/O TESTS. If the unit passes these tests, then replace U345, U338, and U331.
U345-5 = H	(VB1)	Perform the VIDEO I/O TESTS. If the unit passes these tests, then replace U345, U338, and U331.
U355-12 = P	(VB3)	U329-2
U355-13 = P	(VB3)	U329-5

VIDEO TIMING AND CONTROL TESTS

TEST #1

-- Check for dot clock pulses at U344-11, U344-6, and U368-11. If missing, replace U344 or U368 (VB1).

-- Check for pulses at pins 1 through 9 and 11 through 13 of U376. If any of these are missing, check U336, U343, and U367. Check the reset and dot clock lines to these ICs (VB1).

-- Perform the following test.

CHECK			IF NOT OKAY, CHECK
*U377-4	= L	(VB1)	U377-6

Go to Test #2.

U355-2	= L	(VB1)	U355-13
U355-3	= L	(VB1)	U355-2, or open on U355-1
U355-11	= H	(VB1)	U371 or U377 defective.
U355-13	= L	(VB1)	U355-11
U361-1	= L	(VB1)	U355-3
U361-6	= H	(VB1)	U361-1
U377-6	= H	(VB1)	U361-6

==========

TEST #2

-- Press the CTRL/RESET keys. You should get the following logic states. Those shown in parenthesis will pulse one or more times when you release reset.

CHECK	IF NOT OKAY, CHECK
*U377-4 = (L) (VB1)	U377-5, U377-6

Go to Test #3.

U355-2 = (L) (VB1)	U379-13
U355-3 = (L) (VB1)	U355-2
U361-1 = (L) (VB1)	U355-3
U361-2 = (L) (VB1)	U379-13
U361-3 = P (VB1)	Open foil run to U367-5.
U361-5 = (L) (VB1)	U361-2, U361-3, U361-1
U361-6 = (H) (VB1)	U361-2, U361-3, U361-1
U361-9 = (L) (VB1)	U361-12, U361-11, U361-13
U361-11 = P (VB1)	Open foil run to U367-15.
U361-13 = (L) (VB1)	U355-3
U361-12 = (L) (VB1)	U361-5
U377-5 = (L) (VB1)	U361-9
U377-6 = (H) (VB1)	U361-6
U378-1 = H (VB1)	U378 defective.
U378-2 = H (VB1)	Open foil run to P305-69.
U378-3 = L (VB1)	Open foil run to P305-70.
U378-5 = L (VB1)	U378-2, U378-3, U378-1
U379-1 = H (VB1)	U379-2, U379-3
U379-2 = L (VB1)	U378-5
U379-3 = (L) (VB1)	Open foil run to P305-71.
U379-13 = (L) (VB1)	U379-12, U379-11
U379-11 = (H) (VB1)	U371 or U377 defective.
U379-12 = H (VB1)	U379-1

==========

TEST #3

-- Check for logic zero at U346-1 (VB2). If missing, check U366-3 and U345-39 on VB1. If U345 appears defective, perform the VIDEO I/O TESTS before replacing the IC.

-- Check for logic one at U346-11 (VB2). If missing, trace it back to U345-19 (VB1). If U345 appears defective, perform the VIDEO I/O TESTS before replacing the IC.

-- Check for pulses on pins 12 through 19 on U346 (VB2). If any are missing, check the appropriate input pin (2 through 9) and trace back to P304 and P305. Otherwise replace U346.

--Perform the following tests.

CHECK			IF NOT OKAY, CHECK
*U353-3	= H	(VB2)	U374-11
*U353-4	= P	(VB2)	U375-8
*U353-15	= P	(VB2)	U375-6

End of test. If testing a color unit, go to Test #4.

U345-7	= L	(VB1)	See VIDEO I/O TESTS.
U345-39	= H	(VB1)	See VIDEO I/O TESTS.
U350-3	= H	(VB2)	U371 or U377 defective.
U350-4	= L	(VB2)	U345-7
U350-5	= L	(VB2)	Open foil run to U377-4.
U350-6	= H	(VB2)	U350-3, U350-4, U350-5
U351-4	= L	(VB2)	Open foil run to U377-4.
U351-5	= L	(VB2)	U366-3
U351-6	= L	(VB2)	U351-4, U351-5
U366-3	= L	(VB1)	U366-17
U366-17	= H	(VB1)	U345-39
U374-11	= H	(VB2)	U374-13
U374-13	= L	(VB2)	U351-6

U375-5	= P	(VB2)	U376-15
U375-6	= P	(VB2)	U375-5
U375-8	= P	(VB2)	U375-9, U375-10
U375-9	= H	(VB2)	U350-6
U375-10	= P	(VB2)	U376-14
U376-14	= P	(VB1)	U376 defective.
U376-15	= P	(VB1)	U376 is defective.

==========

TEST #4

-- For color units, perform the following.

CHECK			IF NOT OKAY, CHECK
*U352-4	= P	(VB2)	U375-11
*U352-15	= P	(VB2)	U375-3
*U354-4	= P	(VB2)	U374-8
*U354-10	= P	(VB2)	U374-6

End of test.

U345-6	= L	(VB1)	See VIDEO I/O TESTS.
U345-8	= L	(VB1)	See VIDEO I/O TESTS.
U350-1	= H	(VB2)	U371 or U377 is defective.
U350-2	= L	(VB2)	U345-6
U350-8	= H	(VB2)	U350-9, U350-10, U350-11
U350-9	= H	(VB2)	U371 or U377 is defective.
U350-10	= L	(VB2)	U345-8
U350-11	= L	(VB2)	Open foil run to U377-4.
U350-12	= H	(VB2)	U350-1, U350-2, U350-13
U350-13	= L	(VB2)	Open foil run to U377-4.
U374-5	= P	(VB2)	U376-15
U374-6	= P	(VB2)	U374-5
U374-8	= P	(VB2)	U374-9, U374-10
U374-9	= H	(VB2)	U350-8
U374-10	= P	(VB2)	U376-14
U375-2	= P	(VB1)	U376-15
U375-3	= P	(VB2)	U375-2
U375-11	= P	(VB2)	U375-12, U375-13
U375-12	= H	(VB2)	U350-12
U375-13	= P	(VB2)	U376-14
U376-14	= P	(VB1)	U376 is defective.
U376-15	= P	(VB1)	U376 is defective.

VIDEO I/O TESTS

Press and release the CTRL/RESET keys as you make the following tests. A logic state in parenthesis indicates the line under test will pulse one or more times upon release of RESET.

CHECK	IF NOT OKAY, CHECK
*U330-25 = (H) (VB1)	U369-12
*U331-13 = (H) (VB1)	U366-14
*U345-23 = (H) (VB1)	U369-11
*U372-13 = (H) (VB1)	U369-9

End of test.

U336-6 = (L) (VB1)	U372-6
U336-14 = (H) (VB1)	U366-6
U369-9 = (H) (VB1)	Check continuity on pins 1-7, 14, and 15 of U369.
U369-11 = (H) (VB1)	Check continuity on pins 1-7, 14, and 15 of U369
U369-12 = (H) (VB1)	Check continuity on pins 1-7, 14, and 15 of U369.
U372-6 = (L) (VB1)	U372-9, U372-10
U372-9 = (H) (VB1)	U369-12
U372-10 = (H) (VB1)	U369-11

TROUBLESHOOTING NOTES:

PARTS LIST

PARTS LIST

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.

VIDEO BOARD PART LIST
(Assembled HE 181-3631 B&W)
(HE 181-3267 Color)

CAPACITORS

C301	180 pF ceramic	HE 21-746
C302	180 pF ceramic	HE 21-746
C303	.1 uF ceramic	HE 21-762
C304	10 uF electrolytic	HE 25-820
C305	.1 uF ceramic	HE 21-762
C306	.1 uF ceramic	HE 21-762
C307	.1 uF ceramic	HE 21-762
C308	10 uF electrolytic	HE 25-820
C309	.1 uF ceramic	HE 21-762
C310	.1 uF ceramic	HE 21-762
C311	.1 uF ceramic	HE 21-762
C312	.1 uF ceramic	HE 21-762
C313	.1 uF ceramic	HE 21-762
C314	.1 uF ceramic	HE 21-762
C315	.1 uF ceramic	HE 21-762
C316	.1 uF ceramic	HE 21-762
C317	.1 uF ceramic	HE 21-762
C318	.1 uF ceramic	HE 21-762
C319	.1 uF ceramic	HE 21-762
C320	.1 uF ceramic	HE 21-762
C321	.1 uF ceramic	HE 21-762
C322	.1 uF ceramic	HE 21-762
C323	.1 uF ceramic	HE 21-762
C324	.1 uF ceramic	HE 21-762
C325	.1 uF ceramic	HE 21-762
C326	.1 uF ceramic	HE 21-762
C327	.1 uF ceramic	HE 21-762
C328	.1 uF ceramic	HE 21-762
C329	.1 uF ceramic	HE 21-762
C330	.1 uF ceramic	HE 21-762
C331	.1 uF ceramic	HE 21-762
C332	.1 uF ceramic	HE 21-762
C333	.1 uF ceramic	HE 21-762
C334	.1 uF ceramic	HE 21-762
C335	.1 uF ceramic	HE 21-762
C336	10 uF electrolytic	HE 25-820
C337	.1 uF ceramic	HE 21-762
C338	.1 uF ceramic	HE 21-762
C339	.1 uF ceramic	HE 21-762

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.

CAPACITORS (CONTINUED)

C340	.1 uF ceramic	HE 21-762
C341	.1 uF ceramic	HE 21-762
C342	.1 uF ceramic	HE 21-762
C343	.1 uF ceramic	HE 21-762
C344	.1 uF ceramic	HE 21-762
C345	.1 uF ceramic	HE 21-762
C346	.1 uF ceramic	HE 21-762
C347	.1 uF ceramic	HE 21-762
C348	.1 uF ceramic	HE 21-762
C349	.1 uF ceramic	HE 21-762
C350	.1 uF ceramic	HE 21-762
C351	.1 uF ceramic	HE 21-762
C352	.1 uF ceramic	HE 21-762
C353	.1 uF ceramic	HE 21-762
C354	.1 uF ceramic	HE 21-762
C355	.1 uF ceramic	HE 21-762
C356	.1 uF ceramic	HE 21-762
C357	.1 uF ceramic	HE 21-762
C358	.1 uF ceramic	HE 21-762
C359	.1 uF ceramic	HE 21-762
C360	.1 uF ceramic	HE 21-762
C361	.1 uF ceramic	HE 21-762
C362	.1 uF ceramic	HE 21-762
C363	.1 uF ceramic	HE 21-762
C364	47 uF electrolytic	HE 25-883
C365	.1 uF ceramic	HE 21-762

The following capacitors have no component numbers and are located on the bottom of the board (for location see Visual Checks).

	180 pF ceramic	HE 21-746
	180 pF ceramic	HE 21-746
	180 pF ceramic	HE 21-746

INDUCTORS

L301	1.22 uH	HE 475-15
L302	35 uH	HE 235-229
L303	35 uH	HE 235-229
L304	35 uH	HE 253-229

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.

RESISTORS

R301	none		
R302	jumper		
R303	1000 ohm	1/4 watt, 5%	HE 6-102-12
R304	47 ohm	1/4 watt, 5%	HE 6-470-12
R305	1000 ohm	1/4 watt, 5%	HE 6-102-12
R306	27 ohm	1/4 watt, 5%	HE 6-270-12
R307	100 ohm control		HE 10-1191
R308	620 ohm	1/4 watt, 5%	HE 6-621-12
R309	220 ohm	1/4 watt, 5%	HE 6-221-12
R310	110 ohm	1/4 watt, 5%	HE 6-111-12
R311	33 ohm	1/4 watt, 5%	HE 6-330-12
R312	47 ohm	1/4 watt, 5%	HE 6-470-12
R313	27 ohm	1/4 watt, 5%	HE 6-270-12
R314	39 ohm	1/4 watt, 5%	HE 6-390-12
R315	62 ohm	1/4 watt, 5%	HE 6-620-12
R316	27 ohm	1/4 watt, 5%	HE 6-270-12
R317	1000 ohm	1/4 watt, 5%	HE 6-102-12
R318	1000 ohm	1/4 watt, 5%	HE 6-102-12
R319	10 kilohm	1/4 watt, 5%	HE 6-103-12
R320	10 kilohm	1/4 watt, 5%	HE 6-103-12
R321	1000 ohm	1/4 watt, 5%	HE 6-102-12
R322	4700 ohm	1/4 watt, 5%	HE 6-472-12
R323	1000 ohm	1/4 watt, 5%	HE 6-102-12
R324	1000 ohm	1/4 watt, 5%	HE 6-102-12
R325	1000 ohm	1/4 watt, 5%	HE 6-102-12

RESISTOR PACKS

RP301	1000 ohm	HE 9-99
RP302	10 kilohm	HE 9-128
RP303	4.7 kilohm	HE 9-124
RP304	4.7 kilohm	HE 9-124
RP305	33 ohm	HE 9-93
RP306	33 ohm	HE 9-93
RP307	1000 ohm	HE 9-99

PARTS LIST

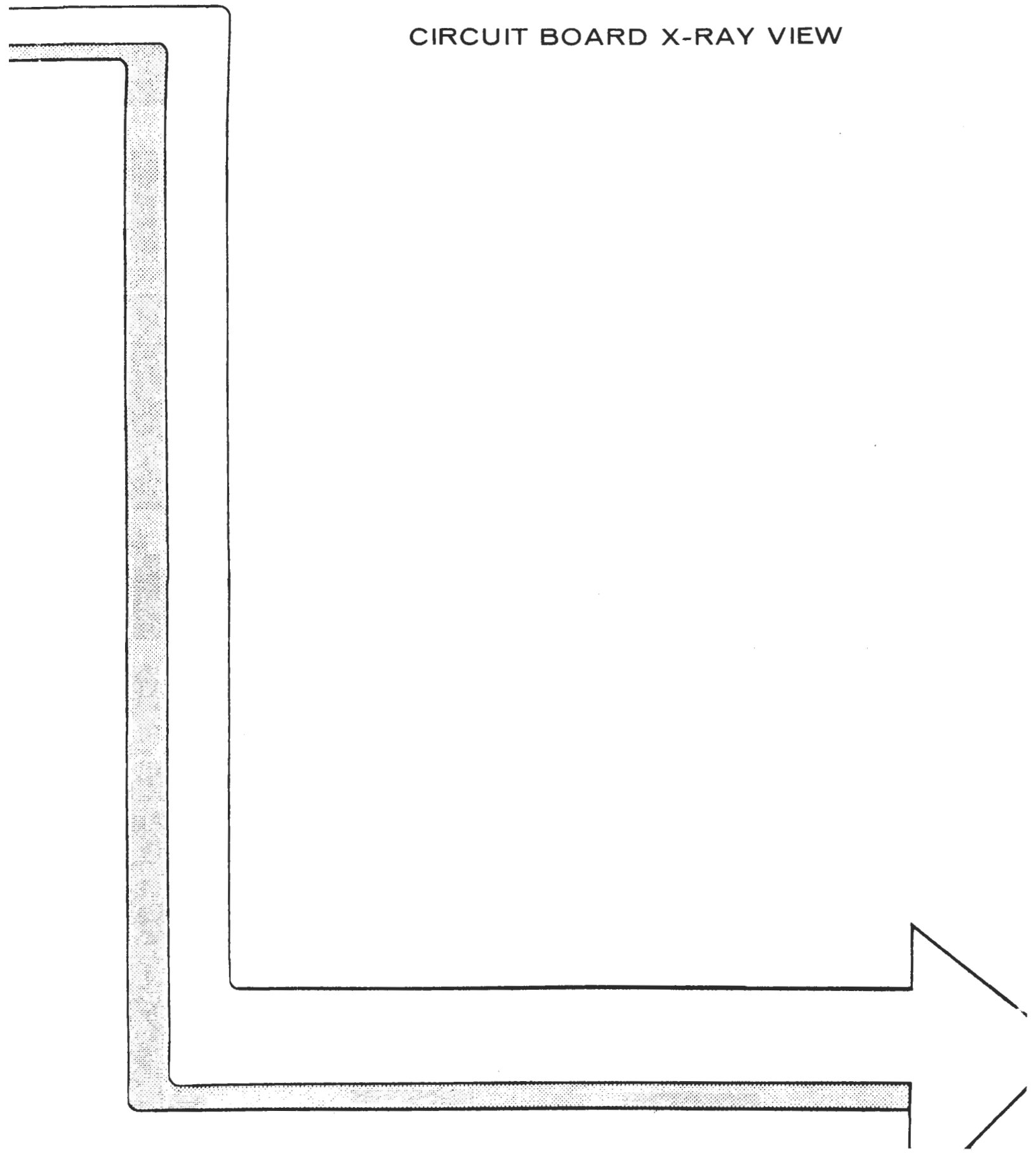
CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS		
U301	74LS166	HE 443-892
U302	74LS273	HE 443-805
U303	74LS166	HE 443-892
U304	MCM66330 (optional)	HE 443-1106*
U305	MCM66330	HE 443-1106*
U306	MCM66330 (optional)	HE 443-1106*
U307	74LS244	HE 443-791
U308	7406	HE 443-967
U309	74LS273	HE 443-805
U310	74LS373	HE 443-837
U311	74LS273	HE 443-805
U312	MCM66330 (optional)	HE 443-1106*
U313	MCM66330	HE 443-1106*
U314	MCM66330 (optional)	HE 443-1106*
U315	74LS374	HE 443-863
U316	74LS373	HE 443-837
U317	MCM66330 (optional)	HE 443-1106*
U318	MCM66330	HE 443-1106*
U319	MCM66330 (optional)	HE 443-1106*
U320	74LS86	HE 443-891
U321	74LS174	HE 443-879
U322	7406	HE 443-967
U323	74LS259	HE 443-804
U324	74LS169	HE 443-1054
U325	74LS166	HE 443-892
U326	MCM66330 (optional)	HE 443-1106*
U327	MCM66330	HE 443-1106*
U328	MCM66330 (optional)	HE 443-1106*
U329	74S174	HE 443-1053
U330	68A45	HE 443-1013
U331	74LS541	HE 443-1058
U332	74LS273	HE 443-805
U333	MCM66330 (optional)	HE 443-1106*
U334	MCM66330	HE 443-1106*
U335	MCM66330 (optional)	HE 443-1106*
U336	74S175	HE 443-983
U337	HAL14H4	HE 444-115
U338	74LS541	HE 443-1058
U339	74LS373	HE 443-837
U340	MCM66330 (optional)	HE 443-1106*
U341	MCM66330	HE 443-1106*

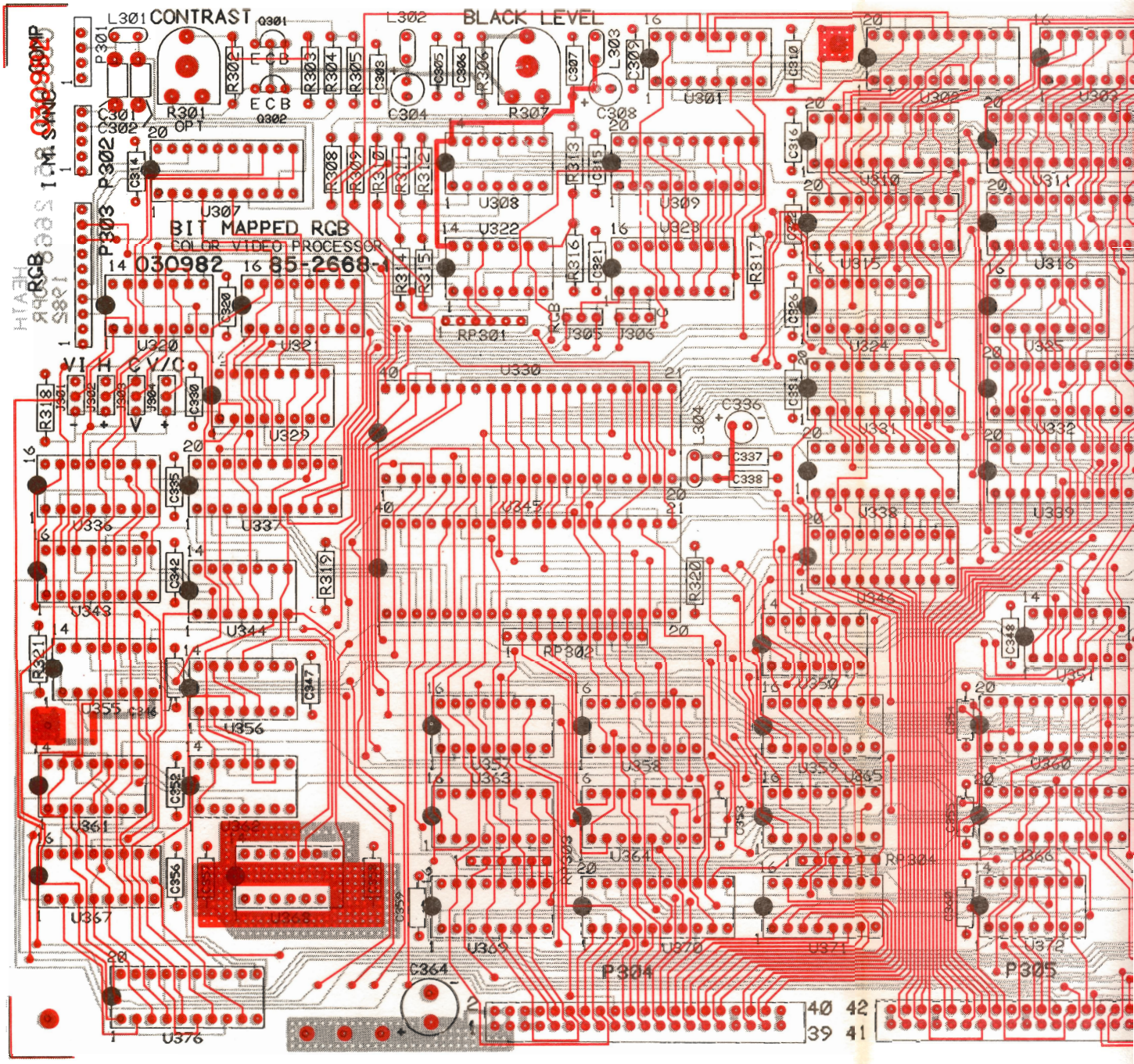
CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS (CONTINUED)		
U342	MCM66330 (optional)	HE 443-1106*
U343	74S175	HE 443-983
U344	74S86	HE 443-915
U345	68A21	HE 443-1014
U346	HAL10H8	HE 444-133
U347	MCM66330 (optional)	HE 443-1106*
U348	MCM66330	HE 443-1106*
U349	MCM66330 (optional)	HE 443-1106*
U350	74LS10	HE 443-797
U351	74LS32	HE 443-875
U352	MCM66330 (optional)	HE 443-1106*
U353	MCM66330	HE 443-1106*
U354	MCM66330 (optional)	HE 443-1106*
U355	74LS32	HE 443-875
U356	74ALS74	HE 443-1051
U357	74LS157	HE 443-799
U358	74LS157	HE 443-799
U359	74LS157	HE 443-799
U360	74S241	HE 443-1057
U361	74ALS74	HE 443-1051
U362	74ALS74	HE 443-1051
U363	74LS157	HE 443-799
U364	74LS283	HE 443-855
U365	74LS283	HE 443-855
U366	74LS240	HE 443-754
U367	74S174	HE 443-1053
U368	14.112 MHz oscillator	HE 150-134
U369	82S129 PROM	HE 444-103
U370	TBP18S22 PROM	HE 444-127
U371	82S129 PROM	HE 444-102
U372	74ALS37	HE 443-1049
U373	74S241	HE 443-1057
U374	74ALS37	HE 443-1049
U375	74ALS37	HE 443-1049
U376	HAL14L4	HE 444-114
U377	74ALS28	HE 443-1048
U378	74ALS74	HE 443-1051
U379	74ALS02	HE 443-1045

* MCM66330 ICs will be installed on the color versions of the video board while MCM6665 (443-970) ICs will be installed on the B/W versions. A further explaination of this is given in Configuration.

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CONNECTORS - SOCKETS		
	14-pin IC socket	HE 434-298
	16-pin IC socket	HE 434-299
	20-pin IC socket	HE 434-311
	40-pin IC socket	HE 434-253
	3-pin connector	HE 432-1102
	4-pin right-angle connector	HE 432-1231
	5-pin right-angle connector	HE 432-1232
	10-pin right-angle connector	HE 432-1233
	20-pin connector	HE 432-1062
	Jumper	HE 432-1041
MISCELLANEOUS		
	PC board	HE 85-2668-1
	Wire, solid	HE 340-8
Q301	2N3393 transistor	HE 417-118
Q302	2N3393 transistor	HE 417-118

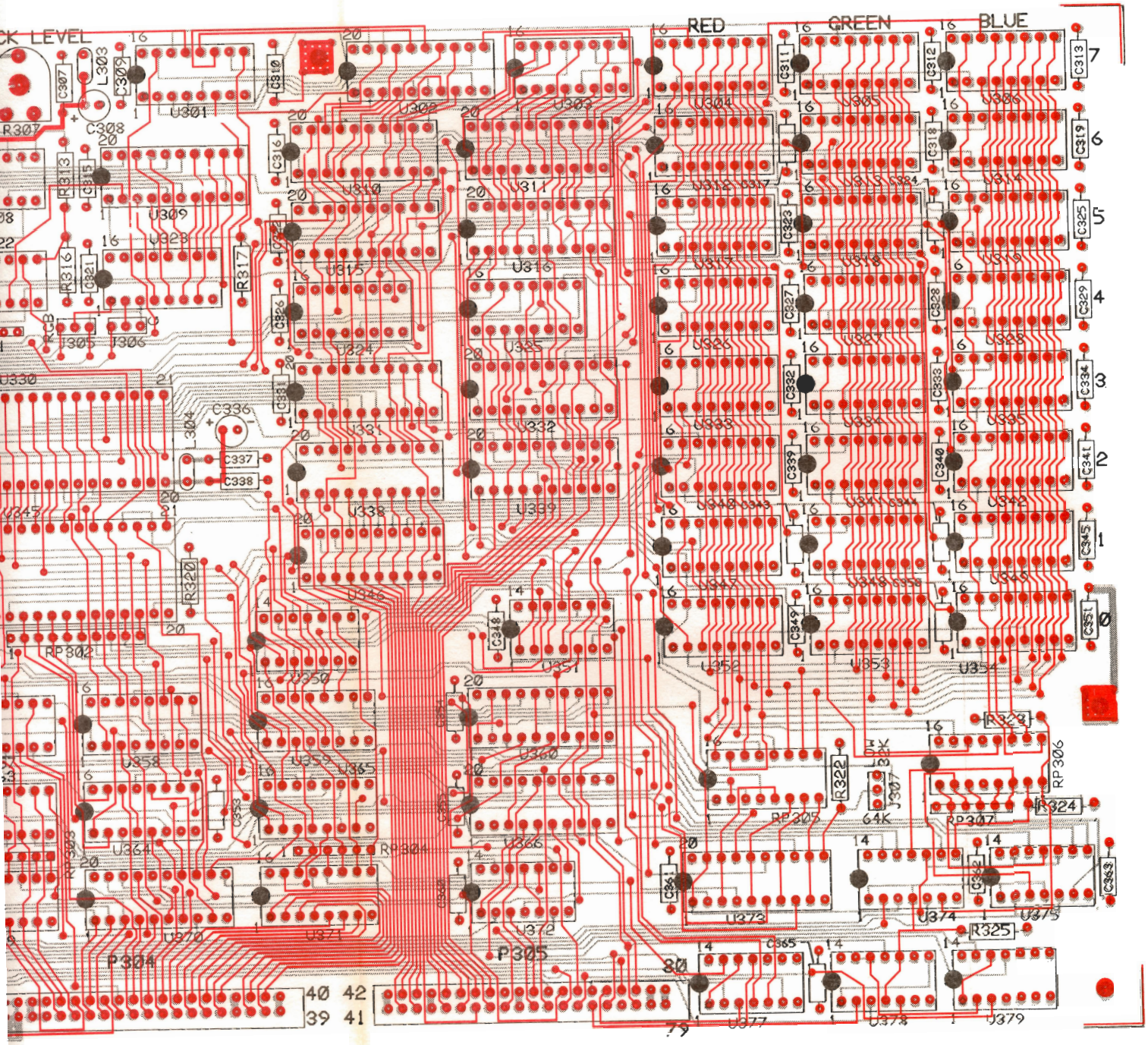
CIRCUIT BOARD X-RAY VIEW





COLOR VIDEO BOARD (#HE-181-3631-1/HE-181-

(SHOWN FROM COMPONENT SIDE)



COLOR VIDEO BOARD (#HE-181-3631-1/HE-181-3267-1)

(SHOWN FROM COMPONENT SIDE)

DISK CONTROLLER AND DRIVES

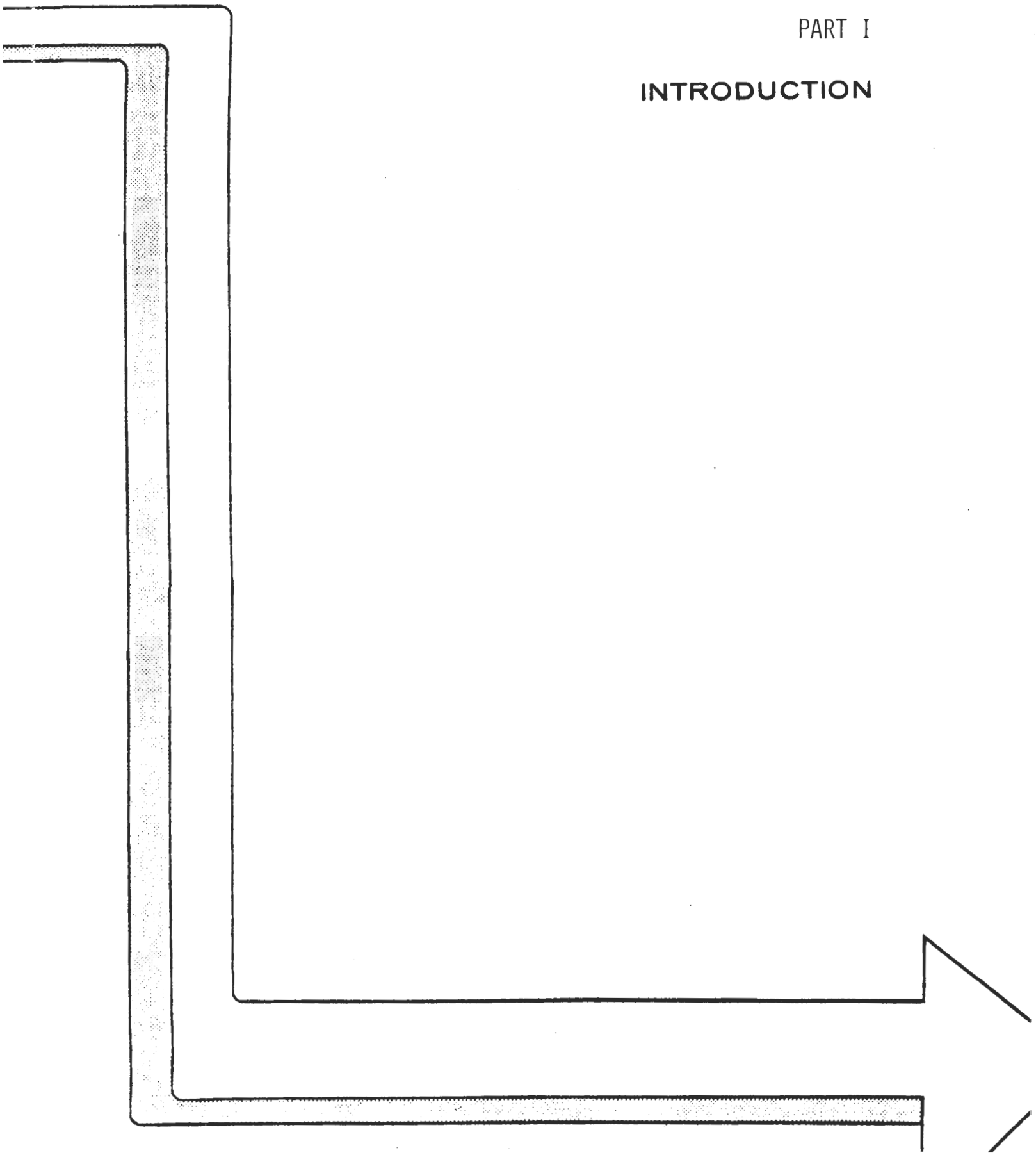
PART I - H/Z-207

PART II - H-207

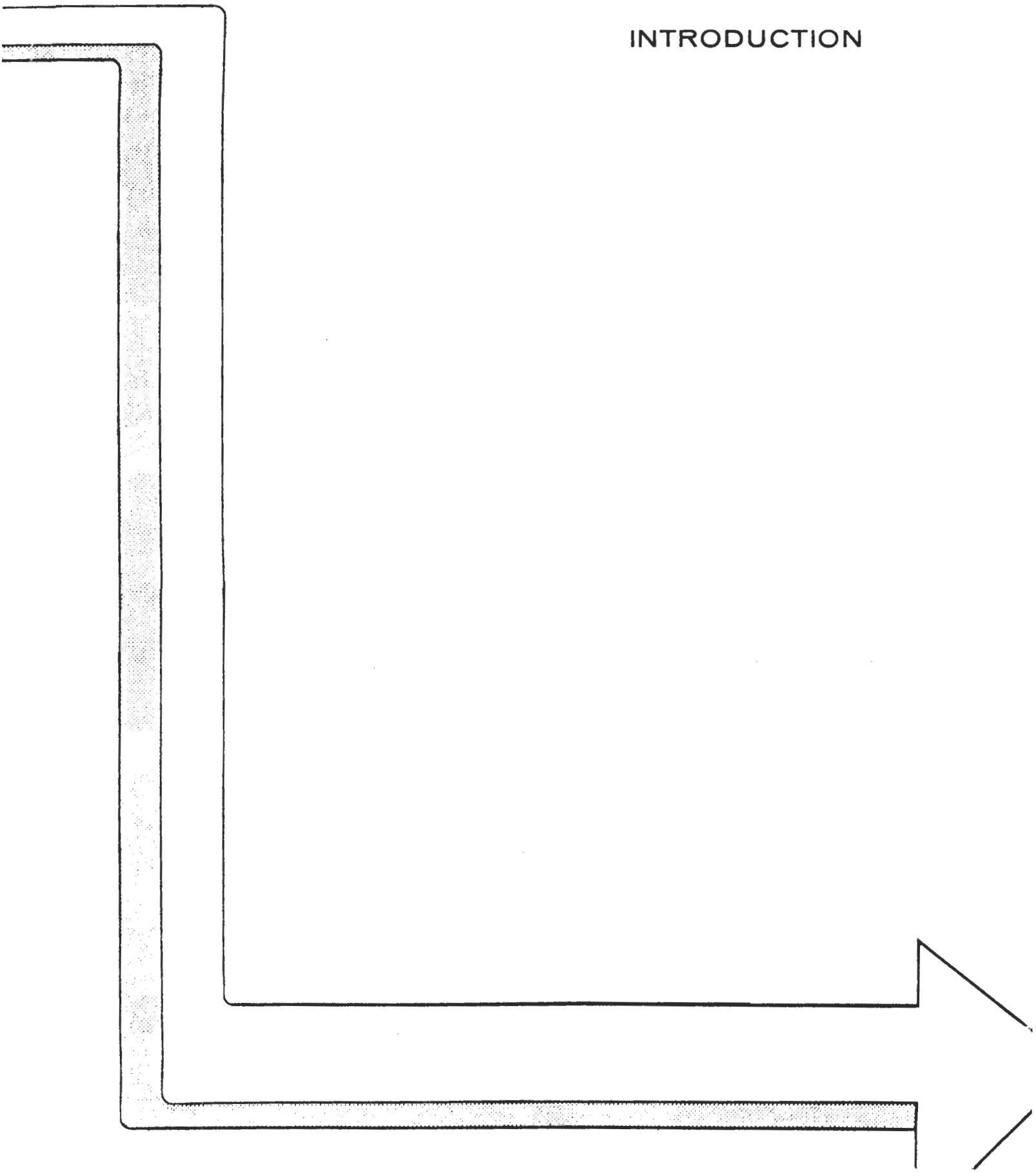
(CONTINUED)

PART I

INTRODUCTION



INTRODUCTION



The Z-207 is a floppy disk controller board. It functions as an intelligent interface between the CPU and the disk drives. The Z-207 selects the correct drive in a multi-drive system and properly handles the data flow to and from the drives. This allows the H/Z-100 to store and retrieve large quantities of data.

The Z-207 operates as a slave processor. This means the disk controller board contains its own processor which is controlled by the master CPU. Thus, the disk controller board takes commands from the master CPU and converts them into the necessary signals required to control the drives. This type of system allows the master CPU to do other tasks while the disk controller board processor actually does the work of controlling the disk drives.

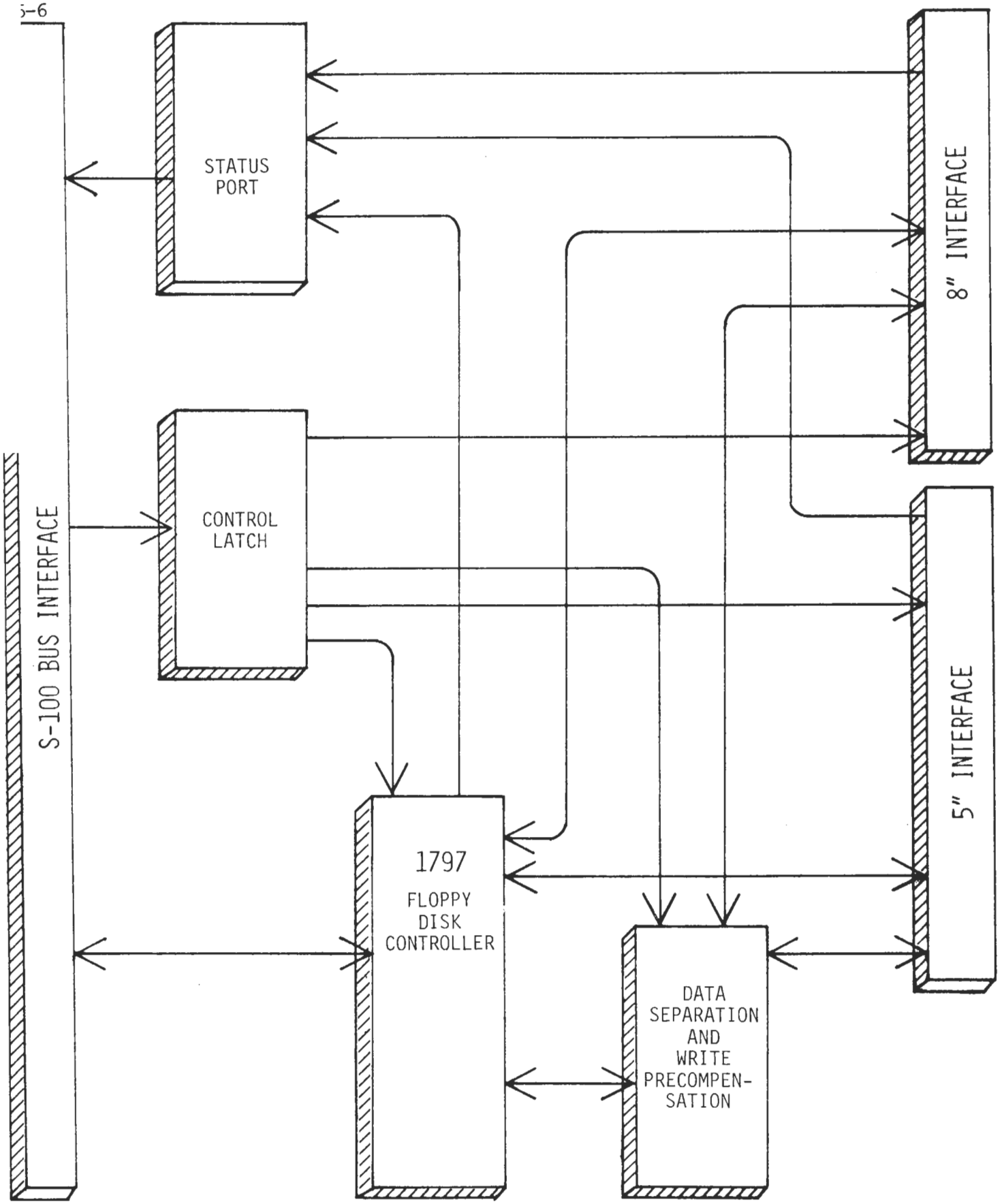
The Z-207 is versatile. It can support up to four 5-1/4" and four 8" disk drives. User software will select the type of drive used and the density of the media. However, present Heath Company software limits the number of drives to three.

The Z-207 can be operated in three different modes; Wait State, Polled I/O, or Interrupt. This allows the disk controller board to support almost all available soft-sectored disk formats. When placed in the H/Z-100, the disk controller board uses the Wait State mode of operation. By using the Wait State mode, the board can be jumpered to operate at speeds up to 6 MHz.

Because the Z-207 is a S-100 compatible card, it can be installed in other makes of computers using the S-100 bus. Additional features that make the controller board acceptable to other computers are: user selectable addressing, software controllable formatting, Shugart compatible 8" interface, and adjustable precompensation.

The information provided in this section of the manual will familiarize you with the operation and troubleshooting of the drive system. Using this information, you will be able to troubleshoot the disk controller board to the component level and determine the condition of the disk drives.

CIRCUIT DESCRIPTION



Z-207 BLOCK DIAGRAM

BLOCK DIAGRAM DESCRIPTION

Refer to the H/Z-207 block diagram as you read the following.

The H/Z-207 Floppy Disk controller board consists of seven major sections: the bus interface, the status port, the control latch, the 1797 floppy disk controller, the data separation & write precompensation circuits, and the two drive interfaces.

The bus interface is made up of two octal bus buffers, an octal tri-state latch, an address comparator, and some miscellaneous enabling circuitry. These components interface the H/Z-207 to the S-100 bus in the H/Z-100.

The status port is a read-only device that tells the CPU the status of the disk drives and the controller. This includes track density, number of recording sides to the disk, and if precompensation is being used.

The control latch accepts commands to the disk drives such as DRIVE SELECT, 5" FASTEP, and others that have to do with the selection and mode of the drives.

The 1797 controller controls the placement of information on the diskette. That is, the movement of the drive head, the formation of written data, and the separation of the read data is controlled by the 1797.

The data separation and write precompensation circuitry control how the data is read to or written from the diskette. It does this by separating the data from the clock signal during read operations and precompensating data during the double-density write operations.

The 8" and 5.25" drive interfaces include buffers and filter circuitry. Up to four drives can be connected to each interface.

DETAILED CIRCUIT DESCRIPTION

S-100 BUS INTERFACE

The S-100 Bus Interface is compatible with any IEEE 696-standard S-100 Bus. See the S-100 specification sheets in the appendices of this manual for definitions of the lines.

DATA IN

Data in to the bus (out from the controller board) travels through signal lines 91-95 and signal lines 41-43 on the bus interface. These pins are used in read operations from the status latch or from the 1797 controller. The data is buffered from the board's internal data bus to the S-100 bus by means of U36, a 74LS244 buffer.

DATA OUT

Data out from the bus (into the controller board) travels through pins 35, 36, 38, 39, 40, 88, 89, and 90 on the bus interface plug. This data is latched by tri-state latch U35. The latch is used because data on the S-100 bus is not present long enough for the 1797 to receive properly. The tri-state latch holds the data on the board's internal data bus so that the 1797 can read it. Valid data is latched in U35 on every write cycle. The latch is enabled through pin 1 when the ALE (Address Latch Enable) signal latches an asserted sOUT (Status Out) signal via U20.

ADDRESS LINES

The address lines from the bus enter the board through pins 29, 30, 31, 79, and 80 through 83 of the bus interface. They are buffered by the 74LS244 chip, U34.

CONTROL LINES

The control lines from the S-100 bus enter the board through pins 24, 25, 45, 46, and 75 through 78 of the bus interface. These lines are buffered by U33.

VECTOR INTERRUPT LINES

The vector interrupt lines from the bus enter the board at pins 4 through 11 of the bus interface. They may be driven by U32.

READY LINE

The ready line, RDY, enters through pin 72 of the bus interface. It is driven by U32. The controller board uses this line to put the CPU in a wait state during some operations to give the controller time to finish the operation.

RESET CIRCUITS

POWER UP/RESET

On power up, the CPU sends RESET* through the S-100 bus to the H/Z-207 board. This places the 1797 controller, the control latch, the write precompensation control, and the U26 flip-flops in a known state before the CPU accesses the board.

In the 1797, the reset line sets the command register of 03H, the sector register to 01H, and bit 7 of the status register (Not Ready bit) to logic zero.

After the reset line goes high, the 1797 executes the restore command. The drive read/write head seeks track 0 and sends an interrupt to the computer once the track is found. See the 1797 IC data sheets for more details.

The reset line connects to pin 1 of the control latch, U30, to clear all of the outputs.

The reset state of the phase lock loop control, U1, makes the phase four (phi 4) input equal to 0 (see the 1691 IC data sheets).

Finally, the U26 Q-outputs are made equal to 1; pin 9 sends an RDY (ready) signal to the CPU and pin 5 provides part of the qualification needed for read/write enabling through U27-11.

POWER-UP WRITE PROTECTION

On power up, the TTL circuits will be at an undefined state until the power supply voltage rises above 4 volts. This could generate a write command in the drives and damage any disks that may be installed.

To protect the disk, the WG (write gate) output from the 1797 is coupled to the 5" and 8" drives through Q3 and Q2. These transistors are biased by R25, D3-D1, and R24 to remain cut off until the power supply voltage is at or above 4 volts. When the supply reaches this value, Q2 and Q3 are biased near their operating region and will conduct whenever WG is asserted.

CPU/CONTROLLER LOGIC

Reading and writing in the H/Z-207 board involves three types of information: data which can be read or written, status signals, and control signals. Status signals can only be read and control signals can only be written.

READ STATUS LATCH (U31)

Assume a status signal needs to be read. There are two sources of status information for the S-100 bus, the status port at U31 and the 1797 status register in U22.

To read from the status port, the CPU selects the H/Z-207 by placing the address of the board on the address lines, A0-A7. Lines A3-A7 are checked by the address comparator, U29, for the proper address. The proper address is defined by the user by setting DIP switch DS1. If the address is correct, the EOUT signal pin 19 asserts.

The EOUT signal is gated through U28-13 by I/O at pin 12. I/O asserts on a data transfer between the CPU and an I/O port. If I/O is low, indicating that the sINP signal or sOUT signal is asserted, then the simultaneous assertion of EOUT and I/O signals sends a logic one to U20-2. This logic one is latched onto pin 5 when ALE (address latch enable) asserts. ALE, derived from pSTVAL* and pSYNC, goes high when the H/Z-207 port address is stable.

The Q output of U20 is NANDed with pDBIN from the S-100 bus to form $\overline{\text{RDME}}$ at U27-8. This line goes low to indicate that the H/Z-207 board is being read by the CPU, and activates the status latch, U31-1.

The status latch still can not be read until the status port select line (STPS) is asserted at pin 15 of U31. This line comes from U17-14, the I/O address decoder.

The I/O address decoder activates STPS by decoding the address lines A0, A1, and A2. If A0 and A1 are low and A2 is high, and if BDSEL or board select is active, then U17's Y1 line goes low. This causes U31 to place the status word onto the board's internal data bus, where it is buffered by U36 to the S-100 bus.

The organization of the status latch is as follows:

BIT	SIGNAL NAME	FUNCTION
0	INTRQ	0 = no interrupt request; 1 = interrupt request from 1797
1	MOTORON (5")	0 = spindle motor not running; 1 = spindle motor running
3	96TP1	0 = 5.25" drives are 48 TPI; 1 = 5.25" drives are 96 TP1
4	PRECOMP	0 = 5.25" drives do not need precomp; 1 = 5.25" drives need precomp
6	TWOSIDED	0 = 8" diskette not two sided; 1 = 8" diskette two sided
7	DRQ	0 = not ready for data transfer; 1 = ready for data transfer

READ STATUS REGISTER OF 1797 (U22)

Assume now that the 1797's status register is to be read. The procedure is the same as described previously, except that address lines A0, A1, and A2 are low. Because the address bits A0-A2 are different, the I/O address decoder (U17) does not enable the status latch (U31). Instead the status register of the 1797 is selected and read onto the data bus.

WRITE CONTROL LATCH (U30)

The control latch, U30, is written at the falling edge of CLEN, which is the simultaneous assertion of pWR and the Y0 output of the I/O address decoder. The pWR signal comes directly from the CPU, and the Y0 signal occurs when A0, A1, and A2 are high, low, and high, respectively. The Y0 and pWR signals are ORed at U21-6 to form CLEN.

The organization of each bit in the control latch is as follows:

BIT	SIGNAL NAME	FUNCTION	
0,1	DSA, DSB	00 = select drive 1 01 = select drive 2	10 = select drive 3 11 = select drive 4
2	8"/5"	0 = select 5.25"	1 = select 8"
3	DSEN	0 = deselect all drives	1 = select drive specified by bits 0, 1, and 2
4	PRECOMP*		
	5.25" DDEN	0 = precomp all tracks	1 = disable precomp
	8" DDEN	0 = precomp all tracks	1 = precomp tracks 44-76
5	5" FASTEP	0 = 1797 operates as specified by bit 2	1 = 1797 operates in 8" mode
6	WAITEN	0 = wait state enable	1 = wait state enable
7	SDEN	0 = double density	1 = single density

*(Note: Precomp is disabled in single density.)

When the WAITEN bit in the control latch is asserted, a wait state is initiated on the next read or write of the data register. WAITEN couples through U23, U26, and U32 to the S-100 RDY line. RDY goes low to put the CPU in a wait state until the disk controller asserts DRQ at U22-38.

Upon DRQ becoming active, an additional delay is needed to fulfill the access time requirements of the 1797 Controller. The access delay and synchronization to the S-100 Bus are both accomplished by counting system clocks. An on-board jumper selects whether one system clock is counted (for systems with clocks up to 3 MHz) or two system clocks are counted (for systems with clocks up to 6 MHz). For operation at less than 3 MHz, jumper J1 (near U19) should be jumpered between F and G. For operation between 3 and 6 MHz, this jumper should be between F and E (normal position for the H/Z-100).

At the completion of the access delay, the wait state is cleared. RDY is asserted, and the CPU completes the read or write of the data register in the 1797. A RESET or an INTRQ signal also clears the wait state, so that the CPU does not hang up after an error during a disk access.

WRITE COMMAND REGISTER IN THE 1797 (U22)

The command register in the 1797 can be written when A0, A1, and A2 are all low. The FDWR signal at U22-2 is asserted when both FDEN and pWR* are logic zero. The signal pWR comes directly from the CPU, while FDEN is a composite signal made up of FDSEL and U26-5. The output of U26-5 is the signal that starts the access of the 1797 controller at the end of the wait state.

DATA READ/WRITE OPERATIONS

During a data write operation, the controller board is enabled by the proper address and by pWR*. After the proper control words are sent to select the proper drive, address lines A0 and A1 are made high and A2 is made low. This connects the data register of the 1797 to the internal data bus. As long as A0 and A1 are high and A2 and FDWR are low, the data from the S-100 bus will go to the 1797 data register and be shifted out serially on pin 31, the write output line. Also, on pin 31, clock pulses are inserted between each bit.

The track and sector registers in the 1797 determine where the data is to be written to on the disk. Whenever a sector is filled with data, software determines the next sector to be written to by making the A0 and A1 signals equal to 0 and 1, A2 equal to 0. Software then writes the sector number to the sector register and the track number to the track register.

The 1797 translates the track numbers into the proper step and direction commands to the drive.

A read operation requires the board to be enabled as described earlier. However, the I/O address decoder does not enable the status latch because the address provided by the CPU is not correct for a status read from the latch. Instead, the address lines causes the 1797 to dump the bits in its data register onto the internal data bus of the H/Z-207, which connects to the U36 buffer and the S-100 bus.

The 1797 fills its data register from the data shift register, which fills serially from the RAWREAD data stream at U22-27. See "Data Separation and Precompensation" for a discussion on RAWREAD data processing.

RDY DELAY

U19 is a quad flip-flop that acts as a delay line for the DRQ signal from the 1797 to the S-100 RDY line. The input at U19-4, D1, is output at Q1 after one clock cycle. Q1 is tied to D2 and is output to Q2 after another clock cycle. Q2 is also tied to U25-1 and D3.

From U25-12, the D2 signal presets flip-flop U26. Flip-flop U26 qualifies the FDSEL signal to enable read/write operations in anticipation of the RDY line being made active.

From D3 of U19, the delayed DRQ signal is output to Q3, which is connected to D4 and to jumper J1, post G. Post G is connected to Post F in 3 MHz operations, which do not need additional delay of the DRQ signal. Instead, the output of Q4, which contains the DRQ signal delayed by three to four clock cycles, is connected to jumper J1, post E. For 6 MHz operation, J1 is connected between post E and post F.

INTERRUPTS

There are two interrupts that the H/Z-207 board can make. They are the interrupt request (INTRQ) and the data request (DRQ). Both of these interrupts originate from the 1797. The INTRQ signal is sent to indicate a command completion or an error. The DRQ signal is sent to indicate data will be accepted in response to a disk read or write command.

The interrupts can be detected two ways, as either a vectored interrupt on any of the bus interface pins from 4 to 11, or as a bit set in the status port, U31, which can then be polled by the CPU.

The INTRQ signal pulls the bus out of a wait state caused by a logic zero at U26-9. When pin 39 of the 1797 asserts, it is inverted at U25-6 to set pin 9 of U26.

CONTROLLER/DISK-DRIVE LOGIC

DATA SHAPING

Data pulses to the drive are reshaped by U16, a one-shot multivibrator, to 400 ns. Raw data from the drive are reshaped to 250 ns.

DATA SEPARATION AND PRECOMPENSATION

Data separation and precompensation are performed primarily by U1, U3, U4, U5, and U22. The data separation circuits are used when the controller is receiving data from the disk drive, while the precompensation circuits are used when the controller is writing data to the disk.

Data Separation

$\overline{\text{READDATA}}$ ($\overline{\text{RDD}}$) from the drive couples through U9 and U16 to U1-11 and U22-27 ($\overline{\text{RAWREAD}}$). $\overline{\text{RDD}}$ contains both data bits and clock bits. U1 extracts the clock bits and sends them to U22-26 as RCLK. These pulses are synchronized with RDD. The 1797 uses the RCLK signal to extract the data bits from the $\overline{\text{RAWREAD}}$ stream. U22 then formats the data and sends it to the CPU.

U1 uses a phase-locked loop to keep RCLK in phase with the incoming data stream. The phase-locked loop consists of U5, U4, U13, and U1. U5 is a 4-MHz voltage-controlled oscillator that drives U4 and U13. U4 and U13 select either 4 MHz or 2 MHz, depending on the disk size. If a 5-1/4" disk is being read, U4-9 is low. This couples the 2-MHz signal to U1-16. Four megahertz is coupled to U1 for 8" drives.

If the phase of RCLK should drift with respect to the incoming $\overline{\text{RDD}}$ signal, U1 will send feedback pulses from U1-13 or U1-14 to the VCO at U5. These pulses will increase or lower the VCO frequency. In turn, the VCO frequency will increase or decrease the RCLK frequency until it again in phase with $\overline{\text{RRD}}$. Here's how...

> If the frequency of $\overline{\text{RDD}}$ is higher than RCLK, then $\overline{\text{RDD}}$ will go low at the beginning of RCLK. The pump-up output (PU) at U1-13 will go from a high-impedance state to a logic one. This increases the VCO frequency which increases frequency of RCLK.

If the frequency of $\overline{RDD}$ is lower than RCLK, then $\overline{RDD}$ will go low at the end of RCLK. The pump-down output ($\overline{PD}$) responds by going from a high-impedance state to logic zero. This decreases the VCO frequency and thus decreases the frequency of RCLK.

If RCLK and $\overline{RDD}$ are in phase, then PU and $\overline{PD}$ are in a high-impedance state and the VCO frequency remains constant.

Pins 5, 7, and 8 of U1 allow the 1797 to control clock separation and data recovery. When pins 7 and 8 are low, the data recovery circuits are enabled. If pin 7 is high, which happens during a write operation, then the data recovery circuits are disabled.

Pin 8, DDEN, controls the frequency of RCLK. When pin 8 is logic one, the frequency of RCLK is equal to the VCO frequency divided by 16. When pin 8 is logic zero, RCLK is equal to the VCO frequency divided by 8.

Data Precompensation

Precompensation, used for 80-track double-density disk write operations, places data properly on the disk so that it can be read back with minimum error. Error is introduced by the shifting of old data that is adjacent to new data being written. This shifting is due to the nature of the magnetic fields on the disk (like fields repel).

The precompensation circuits consist of U22, U1, and U3. U22 sends the write data from pin 31 to U1-1. U3 provides delay timing for the write data in U1. U22 selects the amount of precompensation by setting the logic levels on pin 18 (LATE) and pin 17 (EARLY).

Here's what happens...

When the 1797 sends a data bit to U1-1, the strobe line at U1-5 latches high. This triggers U3-11 and causes a negative-going pulse to ripple through $\overline{\phi 1}$, $\overline{\phi 2}$, $\overline{\phi 3}$, and $\overline{\phi 4}$. R3 sets the pulse width of these signals and, therefore, the amount of precompensation.

With no precompensation (EARLY = LATE = 0), the data pulse is coupled to U1-6 at $\overline{\phi 2}$ time. If LATE precompensation is selected, the data bit leaves U1-6 at $\overline{\phi 3}$ time. EARLY precompensation synchronizes the data bit to $\overline{\phi 1}$.

When $\overline{\phi 4}$ pulses low, it couples through U7 to U1-19 to clear the strobe at U1-5 in anticipation of the next write data pulse.

Precompensation must be enabled for double-density operation. The CPU does this by setting U30-19 to logic one and sending it to the DDEN input at U1-15. The CPU also asserts the $\overline{\text{PRECOMP}}$ line at U30-12. This couples through U6-8 to TG43 at U1-9. TG43 must be high before precompensation can take place.

Even if $\overline{\text{PRECOMP}}$ isn't asserted, the write data should be precompensated on the inner tracks, where the data is packed closer together. This condition is taken care of by U22-29, which asserts on tracks greater than 43. The TG43 signal couples through U6-8 to the TG43 input of U1.

HEAD LOAD TIMING

The single-shot at U15 provides read/write head-load timing. When the 1797 sends a head-load command, pin 28 goes high to load the drive head and to trigger U15.

U15-7 goes low for about 50 mS. This signal couples to U22-23 to prevent a data read or write until U15 times out. This delay compensates for bounce when the read/write head contacts the disk surface.

1797 TIMING

U18, U12, U14, and U30 provide timing and control of timing to the 1797. Depending on the state of U14, the clock frequency to U22-24 will be either 1 MHz or 2 MHz.

The operating frequency of the 1797 is automatically switched from 1 MHz to 2 MHz when changing from 5-1/4" drives to 8" drives. This is done by U30-6 and is coupled through U7-11 to the latch at U14.

One drawback of the 1797 is that it won't allow 5-1/4" drives to step at a 3-mS rate during track seek. To circumvent this problem, U30-15 sets the 5" FASTSTEP signal. This signal couples through U7-12 to U14. U14 increases the operating frequency to 2 MHz to speed up the step rate. At the end of the track-seek function, the clock frequency is reduced to 1 MHz again for normal 5-1/4" operation.

8" DRIVE INTERFACE

The 8" drive interface is through P1. All output signals to the drives are buffered through U8 and U10 except WG and HLD. The WG signal is sent through transistor Q2, as described previously. The HLD signal is inverted by U7-10 before being transmitted to the drives.

All input signals except READY and TWOSIDED are buffered through the upper section of U9 when enabled by a high on the 8"/$\overline{5}$" line. The READY signal is inverted at U6-6, while the TWOSIDED signal is inverted at U6-11.

5" DRIVE INTERFACE

The 5" drive interface is through P2. All output signals to the drives are buffered through U10 and U11 except WG and MOTOR. The WG signal is sent through transistor Q3, as described previously. The MOTOR signal turns on the disk drive motor whenever a logic zero is present at pins 9, 10, 12, and 13 of U23. The single-shot at U15 keeps the drive motor on for about 20 seconds after the disk access is complete. This provides a proper turn-off delay.

All input signals are buffered through the lower section of U9, which is enabled by a low on the 8"/$\overline{5}$" line.

Z-207 FLOPPY DISK CONTROLLER BOARD DEFINITIONS

AØ-A7	Address bits.
ALE	Address latch enable. Data and address lines from the CPU have valid information.
BDSEL	Board Select. The Z-207 board is selected (enabled).
CLK	Clock signal.
CS	Chip select. When asserted, the 1797 chip is enabled.
DØ-D7	Data bits on the Z-207 board's internal data bus.
DDEN	Double density enable.
D1Ø-D17	Data-in bits on the S-100 bus ("in" with respect to the CPU, not the Controller).
DIR	Direction of drive head. When high, the drive head is stepping in. When low, the drive head is stepping out.
DOØ-DO7	Data-out bits on the S-100 bus ("out" with respect to the CPU, not the Controller).
DRQ	Data request. The 1797 data register needs data for write operations or the register has data for read operations.
DSA	Drive select A. Used with DSB to address the drives.
DSB	Drive select B. Used with DSA to address the drives.
EARLY	Write data bit early to disk drive (used for precompensation).
HLD	Head load.

HLT	Head load timing. The drive head is engaged when this signal is high.
INDEX	The index hole on the diskette has been detected.
INTRQ	Interrupt request. Z-207 board has input for the CPU.
LATE	Write data bit late for drive precompensation.
MR	Master reset pin on the 1797 Controller chip that sets all registers in the chip to a known state.
pSTAVAL*	Status valid.
pSYNC	New bus cycle may begin.
PD	Pump down. Decreases the frequency of the raw read data tracking clock.
PRECOMP	Enables precompensation when low.
PU	Pump up. Increases frequency of the raw read data tracking clock.
pWR	Valid data is on data-out bus (write bus).
RAW READ	Unprocessed data from the drive.
RCLK	Clock that separates data from drive data and clock stream.
RDD	Data and clock stream from the drive.
RDME	Data or status signals input for the bus are enabled.
RDY	Slave board is ready. (Z-207 board is a slave board.)
RE	Read enable. Enables the 1797 chip for read operations when low.
READY	The 8" disk drive is ready.

RESET	Reset signal.
SIDE1	Otherwise known as side select output. When high, side 1 is selected in the drive. When low, side 0 is selected.
sINP	Status signal signifying data input to the bus (read cycle) may occur.
sOUT	Status signal signifying data output from the bus (write cycle) may occur.
STEP	Steps the drive head one step per pulse.
STB	Strobe output from the 1691 (U1) phase lock loop control.
TG43	Track greater than 43. The drive read/write head is over or past track 43 (track of mandatory precompensation in double density 8" drive).
TKØ	Track 0. The drive read/write head is over track 0 on the diskette.
TWOSIDED	The 8" drive is set for two-sided operation with a two-sided diskette.
VFOE/WF	VFO enable/write fault. This input is used in conjunction with the WG signal to enable the data recovery circuit. When WG is high, a write operation is taking place and the data recovery circuits are disabled.
VIØ*-VI7*	Vector interrupts.
WAIT	RDY line is low (not ready).
WAITEN	Wait enable. Set RDY line low on all accesses of the 1797 data register.
WD	Write data. Contains the data to be written onto the diskettes as well as the clock signals.
WDIN	Write data into the 1691 phase lock loop control.

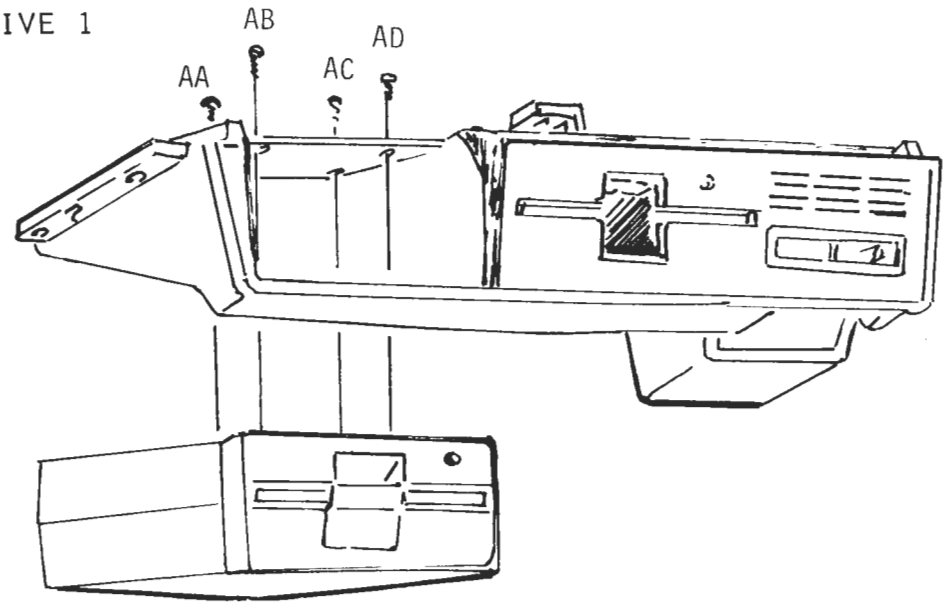
WDOUT	Write data out of the 1691 phase lock loop and precompensation controller.
WG	Write gate. Output to the disk drive is valid.
WE	Write enable. Enables the 1797 floppy disk controller chip for write operations.
WPRT	Write protect. When this signal is received, no write command can take place and write protect bit in the status register is set.
WRDATA	Precompensated write data pulses that have been reshaped by U16.
5DSØ-5DS3	Five inch drive select signals.
5"FASTEP	Enables fast stepping in the 5.25" drives.
8"/$\overline{5}$"	Selects between the 8" and the 5.25" drives.
8DSØ-8DS3	Eight-inch drive select signals.
CLOCK	Master clock signal.
ϕ1-ϕ4	Precompensation phase signals.

DISASSEMBLY

DRIVE REMOVAL

Follow the appropriate procedure to remove either drive 1, drive 2, or both drives from the H/Z-100 Low-Profile computer.

DRIVE 1

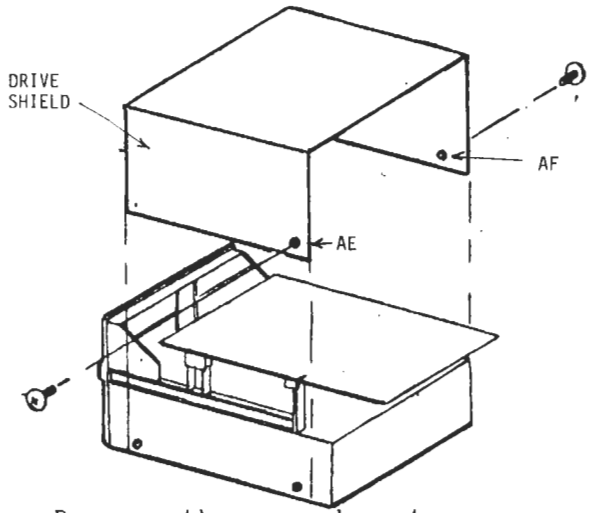


-- Place the disk drive assembly upside down and remove the four 6-32 x 5/8" hex-head screws from AA, AB, AC, and AD.

-- Carefully lift the drive shelf off the drive and set it aside.

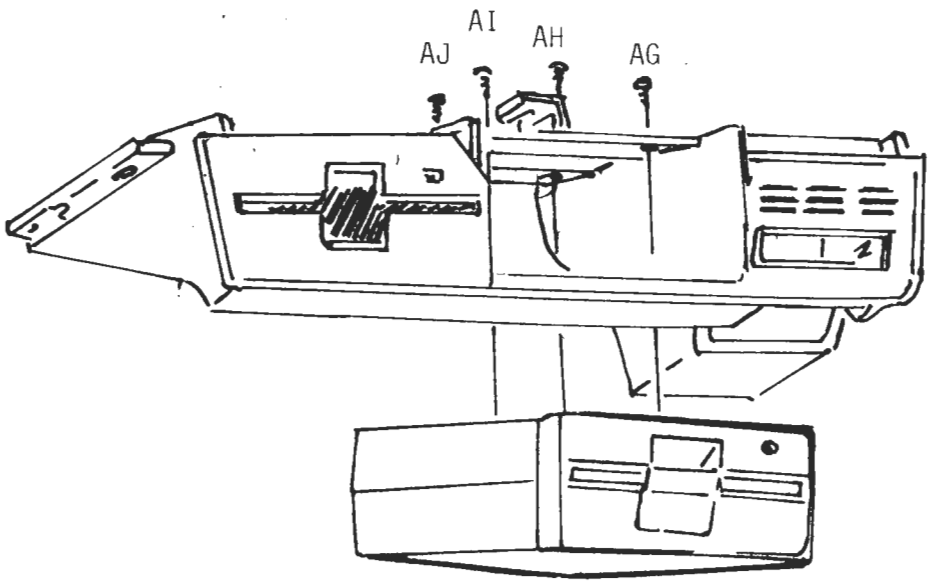
-- Turn the drive right-side-up and remove the two 6-32 x 1/4" flat-head screws from AE and AF.

-- Lift the drive shield from the drive.



This completes Drive 1 Removal. Reverse the procedure to reinstall the drive in the drive shelf.

DRIVE 2

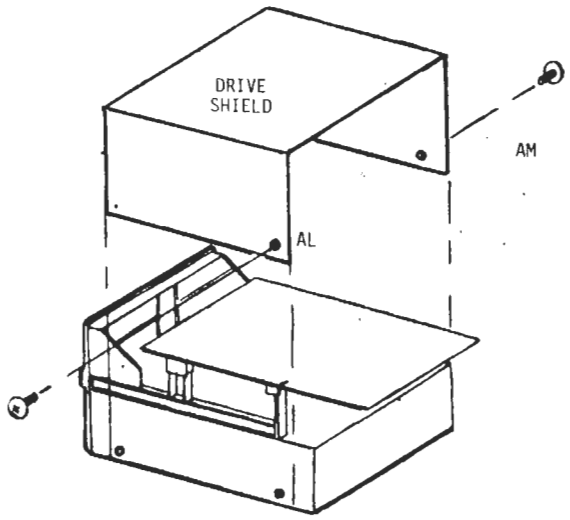


-- Place the disk drive assembly upside down and remove the four 6-32 x 5/8" hex-head screws from AG, AH, AI, and AJ.

-- Carefully lift the drive shelf off the drive and set it aside.

-- Turn the drive right-side-up and remove the two 6-32 x 1/4" flat-head screws from AK and AL.

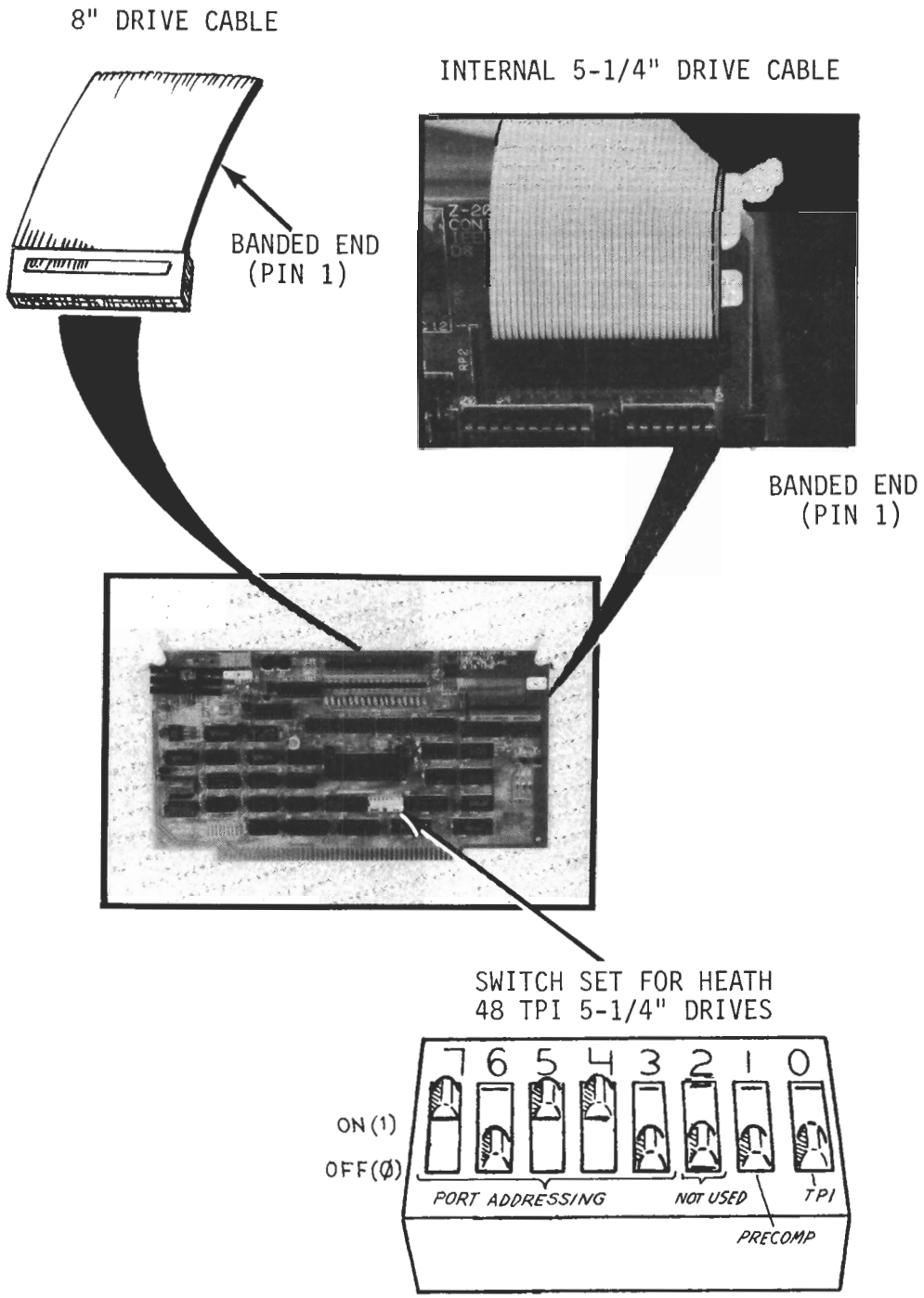
-- Lift the drive shield from the drive.



This completes Drive 2 Removal. Reverse the procedure to reinstall the drive in the drive shelf.

VISUAL CHECKS

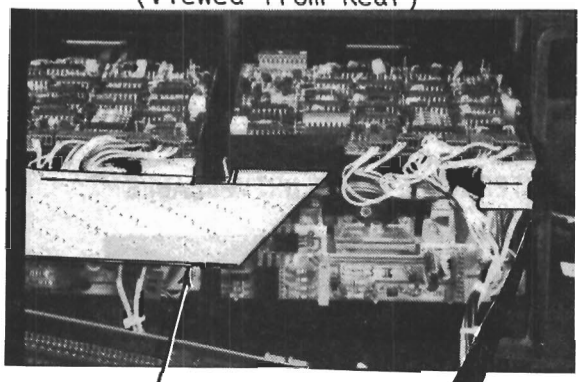
DISK CONTROLLER BOARD CABLE CONNECTIONS AND SWITCH POSITIONS



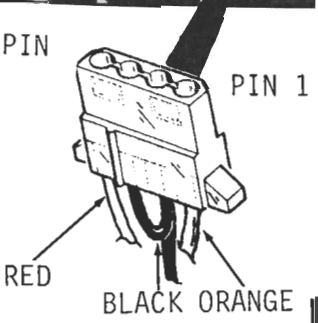
DISK CONTROLLER BOARD
5-1/4" DISK DRIVE CONNECTIONS

LOW PROFILE COMPUTER (SHOWN WITH DRIVE SHIELDS REMOVED)

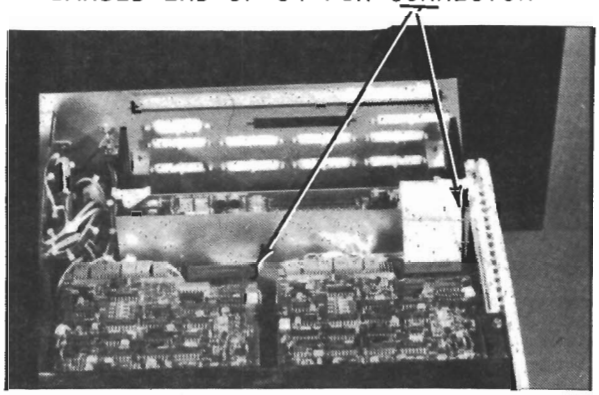
(Viewed from Rear)



BANDED END OF 34-PIN CONNECTOR



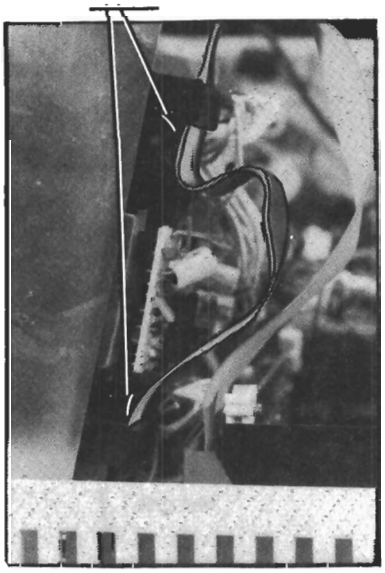
BANDED END OF 34-PIN CONNECTOR



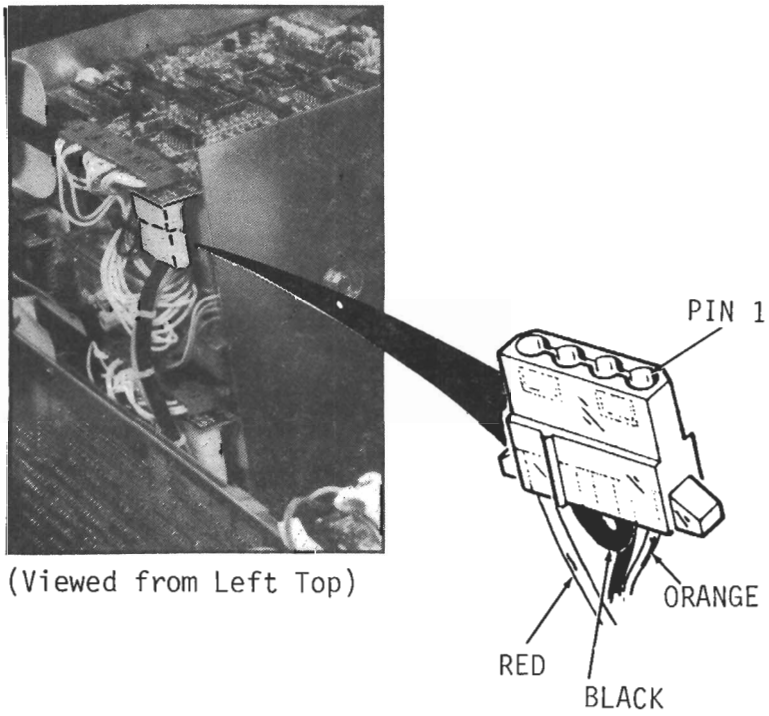
(Viewed from Top)

ALL-IN-ONE COMPUTER

BANDED END OF 34-PIN CONNECTOR

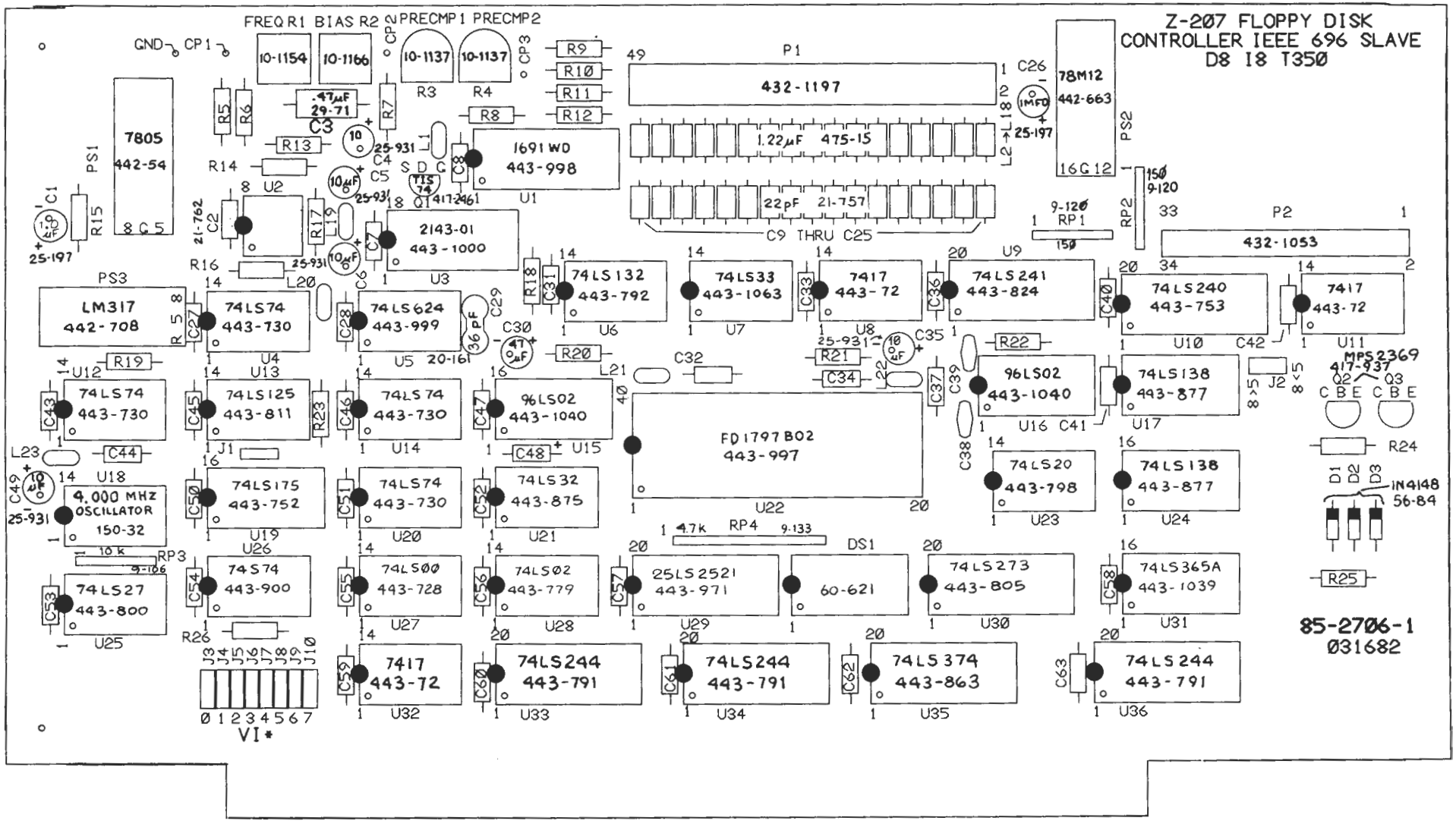


(Viewed from Right Side)



(Viewed from Left Top)

COMPONENT LOCATIONS AND VALUES



DISK CONTROLLER CIRCUIT BOARD (HE-181-3763-1)

ADJUSTMENTS

INTRODUCTION

In this section of the manual, instructions will be given on how to calibrate the Z-207 Disk Controller Board. By following the procedure below, adjustment of the VCO bias voltage and VCO center frequency are performed.

EQUIPMENT NEEDED

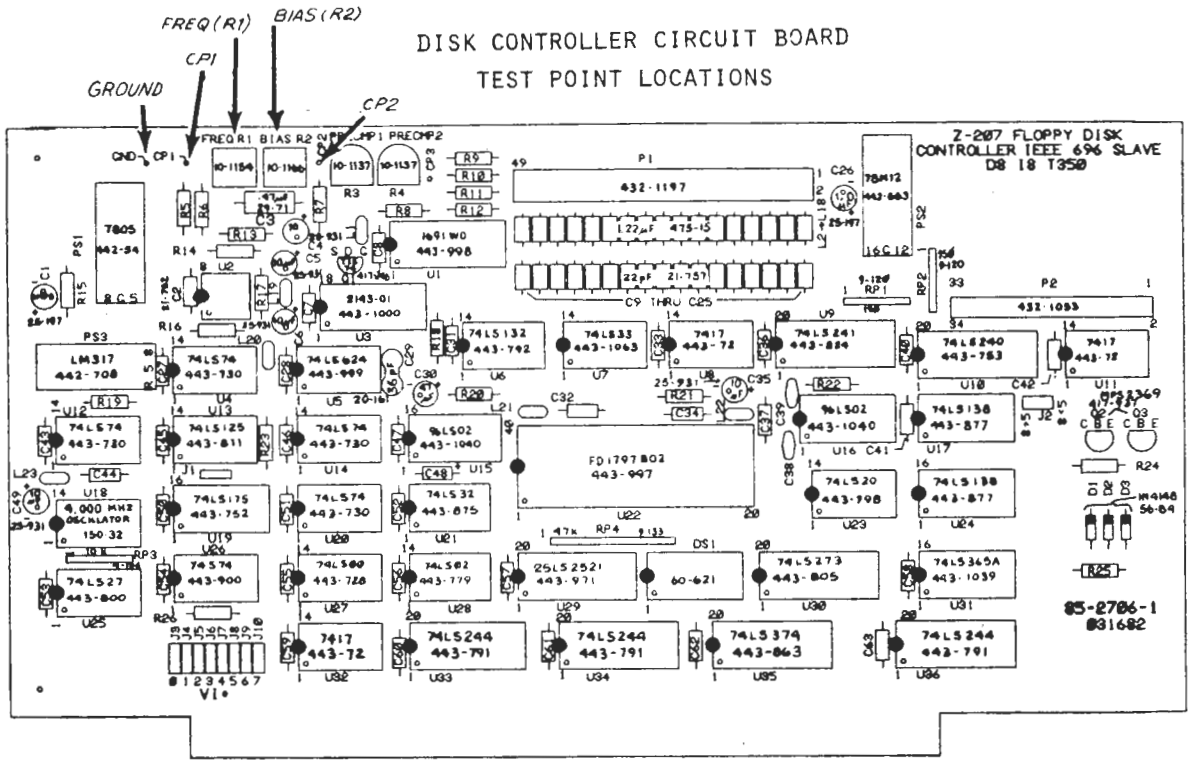
Frequency Counter	IM-2420 or equivalent.
Low Capacitance Probe	PKW-105 or equivalent.
Multimeter	IM-2202 or equivalent.

DATA SEPARATOR ADJUSTMENT

Perform the following steps to adjust the data separator.

-- Allow a fifteen minute warm-up of the board with the top cover of the computer in place.

-- Remove the top cover of the computer.



Refer to the illustration above for the location of the test points.

-- Connect the common test lead of the multimeter to the GND test point.

-- Connect the positive test lead to the CP2 test point.

-- Adjust the BIAS control (R2) until the multimeter display shows +1.40 VDC. You will want to switch the multimeter to lower ranges to perform this adjustment accurately. A reading of +1.40 VDC (±.05 volts) will result in proper operation.

-- Disconnect the multimeter.

-- Connect the common lead of the frequency counter to the GND test point.

-- Connect the test probe of the frequency counter to the CP1 test point.

-- Adjust the FREQ control (R1) until the frequency counter display shows 4.000 MHz.

-- Disconnect the frequency counter.

The adjustments to the Data Separator are now complete.

TROUBLESHOOTING

INTRODUCTION

The following procedure tests the ability of the Z-207 controller board to boot a 5-1/4" disk. Refer to the schematic for general logic states for troubleshooting the 8" portion of the board.

If there's a disk problem that only shows up after the disk is booted, you will need to use diagnostic programs. Check the Diagnostics section of this Manual for more comprehensive disk tests. As diagnostic programs become available, we will publish them for inclusion in the Diagnostics section of this manual. Also, if you develop any troubleshooting techniques or diagnostic programs that you'd like to share, send it to:

Heath Company
Service Publications and Training
Dept. 741
Benton Harbor, Mi. 49022

We will evaluate your submission and, when approved, publish it for inclusion in the Service Bulletins or Diagnostics sections of this manual. Be sure to include a complete description of the troubleshooting technique, symptoms caused by the failed component, and any special equipment needed to repair the problem. If submitting a diagnostic program, we will need a copy of the source listing; preferably on disk.

SETUP

-- Remove the disk controller board from a known-good H/Z-100 and install the H/Z-207 board to be tested into the H/Z-100.

-- Connect at least one 48 TPI, 5-1/4" disk drive to P1.

-- Refer to the configuration section and configure the system to 48 TPI, 5-1/4" soft-sector disk for the primary boot device. Set the configuration to defeat the auto-boot option.

-- Turn on the computer.

As you make the following measurements, press the (B)oot key and press RETURN. Logic states located inside parenthesis indicate that the probe pulses one or more times while "Read Completed" is being printed onto the screen. In the case of a (P) indication, the pulse rate (as indicated by the logic probe) will momentarily change during the "Read Completed" interval.

The schematic shows the logic states after a CTRL/RESET has been performed. Refer to these logic states for troubleshooting areas not covered in the following charts.

CHECKOUT PROCEDURE

In the following tests, you need only test the ICs in the left column indicated by an asterisk (*). If you don't get the suggested logic state, then check each IC listed immediately to the right. The logic states for these ICs are listed in the left column below the ICs with the asterisks.

Continue tracing backwards using this procedure until you test an IC that matches the suggested logic state. The previous IC that you tested is likely the bad IC.

Before you replace the suspected IC, check the other lines leading up to it. You must do this because this checkout procedure gives only the most likely causes to the problem. It doesn't cover such things as open ground foils, foil runs shorted together, open resistors, or missing power supplies.

To help you locate the IC on the schematic, the schematic number is shown in parenthesis to the right of the IC under test.

Unless instructed otherwise, perform these tests with the H/Z-100 configured for 5-1/4" drives (primary) and with auto-boot defeated. See the Configuration section. Also, unless noted otherwise, all logic states are those present after a hard reset.

Z-207 DISK CONTROLLER TEST

CHECK	IF NOT OKAY, CHECK
*Q3 Collector = Z	U21-8
*U1-16 = 2 MHz	U13-6
*U7-4 = L	U7-5 (Also press and release CTRL/RESET. U7-4 should remain low for about 18 seconds. If not, then replace U15.)
*U9-19 = L	U30 or the data bus is defective.
*U10-12 = H	U10 or U22 is defective.
*U10-14 = H	U10 or U22 is defective.
*U10-16 = H	U10 or U22 is defective.
*U11-4 = H	U11-3
*U11-6 = H	U11-5
*U11-8 = H	U11-9
*U11-10 = L	U11-11
*U11-12 = H	U11-13
*U22-2 = (H)	U21-11
*U22-3 = (H)	U21-3
*U22-23 = (H)	U15-7
*U22-24 = 1 MHz	U13-8
*U22-27 = P	U16-9
*U22-34 = L	U9 is defective.
*U22-35 = L	U9 is defective.
*U22-36 = H	U9 is defective.
*U31-1 = (H)	U27-8
*U31-15 = (H)	U17-14
*U32-6 = (H)	U32-5
*U35-11 = (P)	U28-4
*U36-1 = (H)	U27-8
*U36-19 = (H)	U27-8

End of test.

U4-3	= 4 MHz	U5-8
U4-5	= 2 MHz	U4-3
U4-9	= L	U4-11, U4-12
U4-11	= P	U4-5
U4-12	= L	U30 or the data bus is defective.
U5-8	= 4 MHz	U5 or U1 defective; R1 or R2 incorrectly adjusted.
U7-5	= H	U23-8
U7-11	= L	U30 or the data bus is defective.
U7-12	= L	U30 or the data bus is defective.
U7-13	= H	U7-11, U7-12
U10-3	= L	U10-17
U10-17	= H	U33-9
U11-3	= H	U16-7
U11-5	= H	U24-14
U11-9	= H	U24-12
U11-11	= L	U24-15
U11-13	= H	U24-13
U12-3	= 4 MHz	U18 is bad.
U12-5	= 2 MHz	U12-3
U12-9	= 1 MHz	U12-11
U12-11	= 2 MHz	U12-5
U13-4	= L	U4-9
U13-5	= 2 MHz	U4-5
U13-6	= 2 MHz	U13-4, U13-5
U13-8	= 1 MHz	U13-9, U13-10
U13-9	= 1 MHz	U12-9
U13-10	= L	U14-8
U14-8	= L	U14-11, U14-12
U14-11	= 1 MHz	U12-9
U14-12	= H	U7-13
U15-4	= H	U22 or the data bus is defective.
U15-7	= (H)	U15-4
U16-4	= L	U1 or U22 is defective.
U16-7	= H	U16-4
U16-9	= P	U16-11
U16-11	= P	U9 is defective.

U17-1 = P	U34-18
U17-2 = P	U34-16
U17-4 = (H)	U20-6
U17-6 = P	U34-14
U17-7 = L	U19-1
U17-14 = (H)	U17-1, U17-2, U17-4, U17-6
U17-15 = (H)	U17-1, U17-2, U17-4, U17-6
U19-1 = (L)	U26-8
U19-14 = L	U19-1
U20-1 = (L)	U28-13
U20-2 = (L)	U28-13
U20-3 = P	U27-6
U20-5 = (L)	U20-1, U20-2, U20-3
U20-6 = (H)	U20-1, U20-2, U20-3
U21-1 = (H)	U27-11
U21-2 = (H)	U27-8
U21-3 = (H)	U21-1, U21-2
U21-4 = (H)	U17-15
U21-5 = (P)	U33-12
U21-6 = (H)	U21-4, U21-5
U21-8 = L	U21-10
U21-10 = L	U22 of data bus is defective.
U21-11 = (H)	U21-12, U21-13
U21-12 = (H)	U27-11
U21-13 = (P)	U33-12
U22-39 = (L)	Check the data bus at pins 7 through 14. These lines pulse from a high impedance state while "Read Completed" is being printed. If not, then check the components along the data bus.
U23-2 = (L)	U30-16
U23-4 = P	U34-18
U23-5 = P	U34-16
U23-6 = (H)	U23-2, U23-4, U23-5
U23-8 = H	U23-13
U23-13 = L	U24-15

U24-1 = L	U30 or the data bus is defective.
U24-2 = L	U30 or the data bus is defective.
U24-3 = L	U30 or the data bus is defective.
U24-6 = H	U30 or the data bus is defective.
U24-12 = H	U24-1, U24-2, U24-3, U24-6
U24-13 = H	U24-1, U24-2, U24-3, U24-6
U24-14 = H	U24-1, U24-2, U24-3, U24-6
U24-15 = L	U24-1, U24-2, U24-3, U24-6
U25-1 = L	U19-7
U25-2 = L	U10-3
U25-3 = L	U10-3
U25-4 = (L)	U22-39
U25-5 = L	U19-14
U25-6 = (H)	U25-3, U25-4, U25-5
U25-12 = (H)	U25-1, U25-2, U25-13
U25-13 = (L)	U22-39
U26-2 = (H)	U23-6
U26-3 = (L)	U20-5
U26-4 = (H)	U25-12
U26-5 = (H)	U26-2, U26-3, U26-4
U26-8 = (L)	U26-10, U26-11, U26-12
U26-10 = (H)	U25-6
U26-11 = (L)	U20-5
U26-12 = (H)	U23-6
U27-1 = (L)	U22-39
U27-3 = (H)	U27-1
U27-4 = P	U33 defective.
U27-5 = P	U33 defective.
U27-6 = P	U27-5, U27-4
U27-8 = (H)	U27-9, U27-10
U27-9 = P	U33 defective.
U27-10 = (L)	U20-5
U27-11 = (H)	U27-12, U27-13
U27-12 = (L)	U28-10
U27-13 = (H)	U26-5
U28-1 = (H)	U28-2, U28-3
U28-2 = (L)	U33 defective.
U28-3 = (L)	U33 defective.
U28-4 = (P)	U28-6

U28-6 = (P)	U33-12
U28-8 = (H)	U20-6
U28-9 = P	U34-14
U28-10 = (L)	U28-8, U28-9
U28-11 = (P)	U29-19
U28-12 = (H)	U28-1
U28-13 = (L)	U28-11, U28-12
U29-19 = (P)	U29, U34, or DS1 defective.
U30-1 = H	U33-9
U30-11 = (H)	U21-6
U30-16 = (L)	U30-1, U30-11, or data bus problem.
U32-5 = (H)	U27-3
U33-9 = H	U33 defective.
U33-12 = (P)	U33 defective.
U34-14 = P	U34 defective.
U34-16 = P	U34 defective.
U34-16 = P	U34 defective.
U34-18 = P	U34 defective.

PARTS LIST

PARTS LIST

DISK CONTROLLER BOARD PART LIST
(Assembled HE 181-3763-1)

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CAPACITORS		
C1	1.0 uF tantalum	HE 25-197
C2	none	
C3	.47 uF polycarbonate	HE 29-71
C4	10 uF electrolytic	HE 25-931
C5	10 uF electrolytic	HE 25-931
C6	10 uF electrolytic	HE 25-931
C7	.1 uF ceramic	HE 21-762
C8	.1 uF ceramic	HE 21-762
C9	22 pF ceramic	HE 21-757
C10	22 pF ceramic	HE 21-757
C11	22 pF ceramic	HE 21-757
C12	22 pF ceramic	HE 21-757
C13	22 pF ceramic	HE 21-757
C14	22 pF ceramic	HE 21-757
C15	22 pF ceramic	HE 21-757
C16	22 pF ceramic	HE 21-757
C17	22 pF ceramic	HE 21-757
C18	22 pF ceramic	HE 21-757
C19	22 pF ceramic	HE 21-757
C20	22 pF ceramic	HE 21-757
C21	22 pF ceramic	HE 21-757
C22	22 pF ceramic	HE 21-757
C23	22 pF ceramic	HE 21-757
C24	22 pF ceramic	HE 21-757
C25	22 pF ceramic	HE 21-757
C26	1.0 uF tantalum	HE 25-197
C27	.1 uF ceramic	HE 21-762
C28	.1 uF ceramic	HE 21-762
C29	36 pF ceramic	HE 21-709
C30	47 uF electrolytic	HE 25-921
C31	.1 uF ceramic	HE 21-762
C32	.1 uF ceramic	HE 21-762
C33	.1 uF ceramic	HE 21-762
C34	.1 uF ceramic	HE 21-762
C35	10 uF electrolytic	HE 25-931
C36	.1 uF ceramic	HE 21-762
C37	.1 uF ceramic	HE 21-762
C38	180 pF ceramic	HE 21-746
C39	180 pF ceramic	HE 21-746

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CAPACITORS (CONTINUED)		
C40	.1 uF ceramic	HE 21-762
C41	.1 uF ceramic	HE 21-762
C42	.1 uF ceramic	HE 21-762
C43	.1 uF ceramic	HE 21-762
C44	.1 uF ceramic	HE 21-762
C45	.1 uF ceramic	HE 21-762
C46	.1 uF ceramic	HE 21-762
C47	.1 uF ceramic	HE 21-762
C48	1.0 uF tantalum	HE 25-197
C49	10 uF electrolytic	HE 25-931
C50	.1 uF ceramic	HE 21-762
C51	.1 uF ceramic	HE 21-762
C52	.1 uF ceramic	HE 21-762
C53	.1 uF ceramic	HE 21-762
C54	.1 uF ceramic	HE 21-762
C55	.1 uF ceramic	HE 21-762
C56	.1 uF ceramic	HE 21-762
C57	.1 uF ceramic	HE 21-762
C58	.1 uF ceramic	HE 21-762
C59	.1 uF ceramic	HE 21-762
C60	.1 uF ceramic	HE 21-762
C61	.1 uF ceramic	HE 21-762
C62	.1 uF ceramic	HE 21-762
C63	.1 uF ceramic	HE 21-762
INDUCTORS		
L1	35 uH	HE 235-229
L2	1.22 uH bead	HE 475-15
L3	1.22 uH bead	HE 475-15
L4	1.22 uH bead	HE 475-15
L5	1.22 uH bead	HE 475-15
L6	1.22 uH bead	HE 475-15
L7	1.22 uH bead	HE 475-15
L8	1.22 uH bead	HE 475-15
L9	1.22 uH bead	HE 475-15
L10	1.22 uH bead	HE 475-15
L11	1.22 uH bead	HE 475-15
L12	1.22 uH bead	HE 475-15
L13	1.22 uH bead	HE 475-15
L14	1.22 uH bead	HE 475-15

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INDUCTORS (CONTINUED)		
L15	1.22 uH bead	HE 475-15
L16	1.22 uH bead	HE 475-15
L17	1.22 uH bead	HE 475-15
L18	1.22 uH bead	HE 475-15
L19	35 uH	HE 235-229
L20	35 uH	HE 235-229
L21	35 uH	HE 235-229
L22	35 uH	HE 235-229
L23	35 uH	HE 235-229
RESISTORS		
R1	10 kilohm control	HE 10-1154
R2	100 kilohm control	HE 10-1180
R3	2 kilohm control	HE 10-1137
R4	2 kilohm control	HE 10-1137
R5	47 ohm 1/4 watt, 5%	HE 6-470-12
R6	none	
R7	47 kilohm 1/4 watt, 5%	HE 6-473-12
R8	jumper	
R9	1 megohm 1/4 watt, 5%	HE 6-105-12
R10	1000 ohm 1/4 watt, 5%	HE 6-102-12
R11	3900 ohm 1/4 watt, 5%	HE 6-392-12
R12	1800 ohm 1/4 watt, 5%	HE 6-182-12
R13	47 kilohm 1/4 watt, 5%	HE 6-473-12
R14	jumper	
R15	720 ohm 1/4 watt, 1%	HE 6-7200-12
R16	none	
R17	none	
R18	120 kilohm 1/4 watt, 5%	HE 6-124-12
R19	237 ohm 1/4 watt, 1%	HE 6-2370-12
R20	1 megohm 1/4 watt, 5%	HE 6-105-12
R21	3900 ohm 1/4 watt, 1%	HE 6-3901-12
R22	2200 ohm 1/4 watt, 1%	HE 6-2201-12
R23	1000 ohm 1/4 watt, 5%	HE 6-102-12
R24	120 kilohm 1/4 watt, 5%	HE 6-124-12
R25	1000 ohm 1/4 watt, 5%	HE 6-102-12
R26	1000 ohm 1/4 watt, 5%	HE 6-102-12

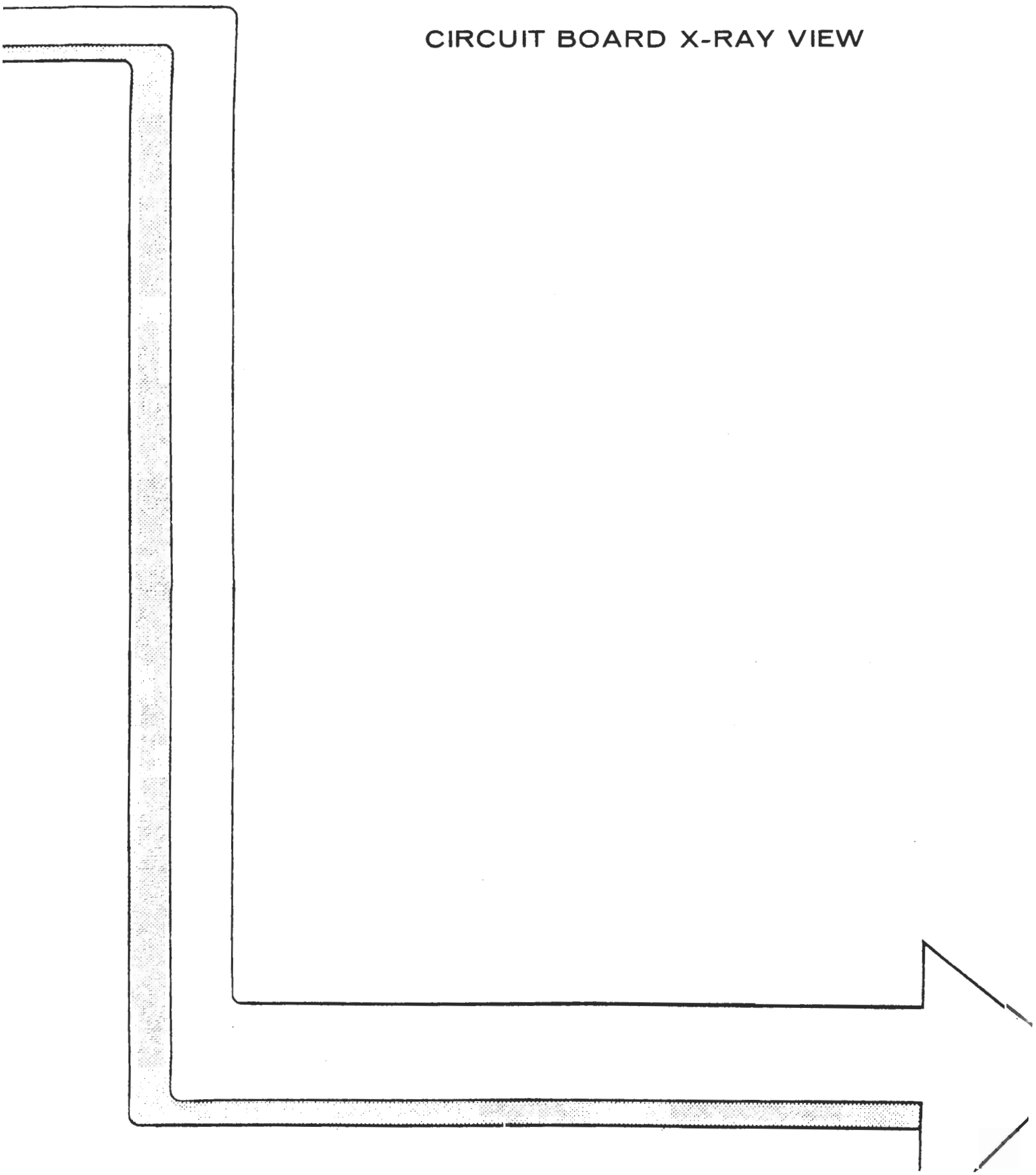
PARTS LIST

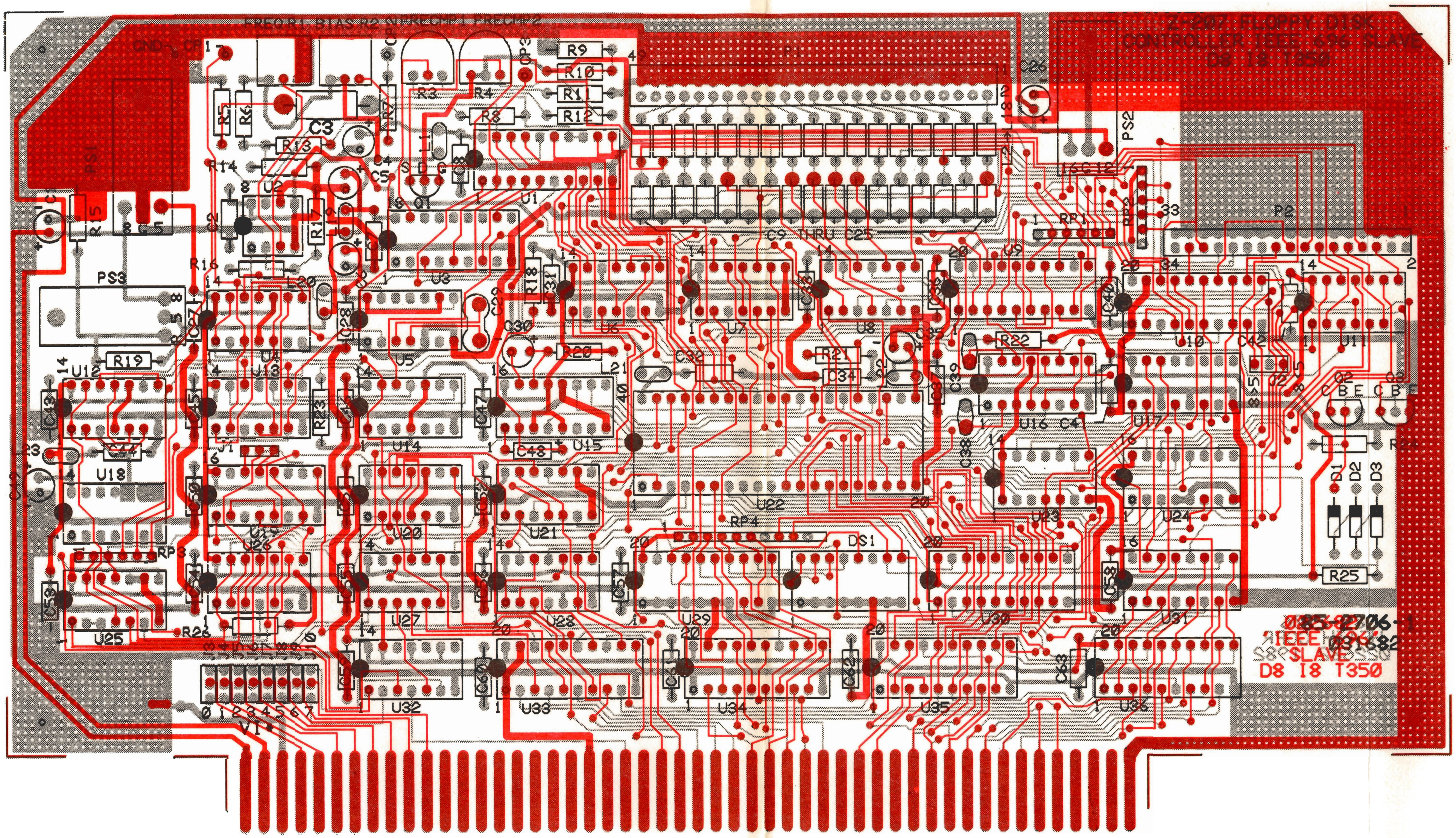
CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
RESISTOR PACKS		
RP1	150 ohm	HE 9-120
RP2	150 ohm	HE 9-120
RP3	10 kilohm	HE 9-106
RP4	4.7 kilohm	HE 9-133
INTEGRATED CIRCUITS		
PS1	7805 5V regulator	HE 442-54
PS2	78M12 +12V regulator	HE 442-663
PS3	LM317 +adj regulator	HE 442-708
U1	WD1691	HE 443-998
U2	none	
U3	2143-01	HE 443-1000
U4	74LS74	HE 443-730
U5	74LS624	HE 443-999
U6	74LS132	HE 443-792
U7	74LS33	HE 443-1063
U8	7417	HE 443-72
U9	74LS241	HE 443-824
U10	74S240	HE 443-753
U11	7417	HE 443-72
U12	74LS74	HE 443-730
U13	74LS125	HE 443-811
U14	74LS74	HE 443-730
U15	96LS02	HE 443-1040
U16	96LS02	HE 443-1040
U17	74LS138	HE 443-877
U18	4.000 MHz oscillator	HE 150-132
U19	74LS175	HE 443-752
U20	74LS74	HE 443-730
U21	74LS32	HE 443-875
U22	FD1797B02	HE 443-997
U23	74LS20	HE 443-798
U24	74LS138	HE 443-877
U25	74LS27	HE 443-800
U26	74S74	HE 443-900
U27	74LS00	HE 443-728
U28	74LS02	HE 443-779
U29	25LS2521	HE 443-971
U30	74LS273	HE 443-805
U31	74LS365A	HE 443-1039
U32	7417	HE 443-72
U33	74LS244	HE 443-791
U34	74LS244	HE 443-791
U35	74LS374	HE 443-863
U36	74LS244	HE 443-791

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
OTHER CIRCUIT COMPONENTS		
D1	1N4148 diode	HE 56-84
D2	1N4148 diode	HE 56-84
D3	1N4148 diode	HE 56-84
DS1	8-section slide switch	HE 60-621
Q1	TIS74 transistor	HE 417-246
Q2	MPS2369 transistor	HE 417-937
Q3	MPS2369 transistor	HE 417-937
CONNECTORS - SOCKETS		
	14-pin IC socket	HE 434-298
	16-pin IC socket	HE 434-299
	18-pin IC socket	HE 434-310
	20-pin IC socket	HE 434-311
	40-pin IC socket	HE 434-253
	1-pin connector	HE 432-121
P2	34-pin right-angle connector	HE 432-1053
P1	50-pin right-angle connector	HE 432-1197
HARDWARE		
	#4 lockwasher	HE 254-9
	4-40 nut	HE 252-2
	4-40 x 5/16" screw	HE 250-213
MISCELLANEOUS		
	Heat sink	HE 215-669
	PC board (Z-207, early)	HE 85-2706-1
	PC board (H-207 and later Z-207)	HE 85-2757-1
	S-100 circuit board extractor	HE 266-1203
	Wire, solid	HE 340-8

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.

CIRCUIT BOARD X-RAY VIEW





DISK CONTROLLER BOARD (#HE-181-3763-1)
(SHOWN FROM COMPONENT SIDE)

48 TPI DISK DRIVE DATA

SECTION I
INTRODUCTION TO THE TM-100-1 AND -2 DISK DRIVES, 48 TPI

1. INTRODUCTION

This section contains a description of the physical and functional specifications for the TM-100-1 and -2 disk drives, 48 tracks per inch (TPI), manufactured by Tandon Corporation.

1.1 PURPOSE OF THE DISK DRIVE

The disk drive is a "mini" disk memory designed for random access data entry, storage, and retrieval applications. These applications typically are intelligent terminal controllers, microcomputers, word processing systems, data communications systems, error logging, microprogram loading, and point-of-sale terminals.

The disk drive is capable of recording and reading digital data, using FM, MFM, M2FM or GCR techniques.

1.2 PHYSICAL DESCRIPTION OF THE DISK DRIVE

The disk drive can be mounted in any vertical or horizontal plane. However, when mounted horizontally, the logic circuit board must be up.

The spindle is belt driven by a DC motor with an integral tachometer. The servo control circuit, suitably sized pulleys, and the tachometer control the speed of the spindle. The Read/Write, double-sided head assembly is positioned by means of a stepper motor, split band, and a suitably sized pulley.

The Read/Write/Erase head assembly is a glass-bonded ferrite/ceramic structure. It has a life in excess of 20,000 hours.

For diskette loading, operator access is provided via a slot which is located at the front of the unit.

The electronic components of the disk drive are mounted on two Printed Circuit Board Assemblies (PCBA's), one of which (logic) is located above the chassis, the other of which (servo) is mounted at the rear of the unit. Power and interface signals are routed through connectors that plug directly into the logic PCBA.

1.3 FUNCTIONAL DESCRIPTION OF THE DISK DRIVE

The disk drive is fully self-contained. It requires no operator intervention during normal operation. The disk drive consists of a Spindle Drive system, a Head Positioning system, and a Read/Write/Erase system.

The TM-100-1 is a single-sided disk drive. The TM-100-2 is a double-sided disk drive. The only difference between the two units is the number of heads in the disk drive. The Logic PCB is identical in both models.

When the front door is opened, access is provided for the insertion of a diskette. The diskette is accurately positioned by plastic guides and by the front latch inhibitor. The in/out location is ensured by the backstop.

Closing the front door activates the cone/clamp system, resulting in centering of the diskette and clamping of the diskette to the drive hub. The drive hub is driven at a constant speed of 300 rpm by a servo-controlled DC motor. The magnetic head is loaded into contact with the recording medium whenever the front door is closed.

The magnetic head is positioned over the desired track by means of a stepper motor/band assembly and its associated electronics. This positioner employs a one-step rotation to cause a one-track linear movement. When a write-protected diskette is inserted into the disk drive, the Write Protect sensor disables the write electronics of the disk drive, and a Write Protect output signal is applied to the interface.

When performing a write operation, a 0.33 mm (0.013-inch) (nominal) data track is recorded. Then, this track is tunnel erased to 0.30 (0.012 inch) (nominal).

Data recovery electronics include a low-level read amplifier, a differentiator, a zero crossing detector, and digitizing circuits.

No data decoding ability is provided in the basic disk drive.

The disk drive is also supplied with the following sensor systems:

1. A Track 00 switch that senses when the Head/Carriage assembly is positioned at Track 00.

2. The Index sensor, which consists of a LED light source and phototransistor, is positioned such that a digital signal is generated when an index hole is detected. The Index sensor is a high resolution device that can distinguish holes placed close together, i.e., index sector holes in a hard-sectored diskette.

3. The Write Protect sensor disables the disk drive write electronics whenever a write-protect tab is applied to the diskette (see Section 1.13).

1.4 DISKETTES

The disk drive uses a standard 133.4 mm (5.25 inch) diskette. Diskettes are available with a single index hole or with index and sector holes.

Single index hole diskettes are used when sector information is pre-recorded on the diskette. Multiple index hole diskettes provide sector pulses by means of the Index sensor and electronics.

1.5 MECHANICAL AND ELECTRICAL SPECIFICATIONS

The mechanical and electrical specifications of the disk drive are listed in Table 1-1.

1.6 INTERFACE CIRCUIT SPECIFICATIONS

The interface circuits are designed so that a disconnected wire results in a false signal.

Levels:

True = +0.4 V (maximum)
False = +2.4 V (minimum)

TABLE 1-1
MECHANICAL AND ELECTRICAL SPECIFICATIONS

Media	Industry-Standard 5.25" diskette
Dimensions	
Height	85.85 mm (3.38 inches)
Width	149.1 mm (5.87 inches)
Length	203.2 mm (8.00 inches)
Weight	1.45 Kg (3.2 pounds)
Temperature (Exclusive of Media)	
Operating	10°C to 44°C (50°F to 112°F)
Nonoperating	-40°C to 71°C (-40°F to 160°F)
Relative Humidity (Exclusive of Media)	
Operating	20% to 80% (Noncondensing)
Nonoperating	5% to 95% (Noncondensing)
Head Settling Time	15 msec (Last Track Addressed)
Error Rates (Maximum)	
Soft Read	1 per 10^9 bits (Recoverable)
Hard Read	1 per 10^{12} bits (Nonrecoverable)
Head Life	20,000 Hours (Normal Use)
Media Life	3.6×10^6 Passes Per Track
Disk Speed	300 rpm ± 1.5% (Long Term)
Instantaneous Speed Variation	± 3%
Start/Stop Time	250/150 msec (Maximum)
Transfer Rate	FM: 125,000 BPS MFM: 250,000 BPS
Bits Per Disk (Unformatted)	2 Million (FM)
Recording Modes (Typical)	FM, MFM, MMFM
Power	+ 12 VDC ± 0.6 VDC @ 900 mA (Average Maximum) + 5 VDC ± 0.25 VDC @ 600 mA (Average Maximum) with 100 mv P/P Ripple

1.7 UNCRATING THE DISK DRIVE

The disk drive is shipped in a protective container which, when bulk packaged, minimizes the possibility of damage during shipment. The following procedure is the recommended method for uncrating the disk drive.

1. Place the shipping container on a flat work surface.
2. Remove the upper half of the inner container.
3. Remove the disk drive from the lower half of the inner container.
4. Check the model number and top assembly description against the packing slip.
5. Examine the contents of the shipping container for possible damage.
6. Notify the carrier immediately if any damage is noted.

1.8 PHYSICAL CHECKOUT OF THE DISK DRIVE

Before applying power to the disk drive, the following inspection procedure should be performed:

1. Remove the plastic bag.
2. Remove the cable harness from the door latch of the disk drive.
3. Check that the front latch opens and closes. Note that when the door is opened, the head arm raises.
4. Ensure that the front panel is secure.
5. Manually rotate the drive hub. The drive hub should rotate freely.
6. Check that the PCBA's are secure.
7. Check that the connectors are firmly seated.
8. Check for debris or foreign material between the heads.
9. Notify the carrier immediately if any damage is noted.

1.9 INTERFACE CONNECTIONS

Signal connections for the disk drive are made via a user-supplied 34-pin, flat ribbon connector (3M Part Number 3463-0001 or equivalent). This connector mates directly with the PCBA connector at the rear of the disk drive. The DC power connector is a four-pin connector (Amp Mate-N-Lok Part Number 1-480424-0), which mates with the connector on the logic PCBA at the top rear of the disk drive.

The signal connector harness should be of the flat ribbon or twisted pair type, have a maximum length of ten (10) feet, and have a 22-to-24 gauge conductor compatible with the connector that is to be used.

Power connections should be made with 18-AWG cable (minimum). In addition, the PCBA-mounted, DC power connector is keyed.

1.10 CHASSIS GROUND

To ensure proper operation of the disk drive, the chassis should be connected to earth ground. A 3/16-inch male QC lug, located at the rear of the chassis, is provided to facilitate this connection.

1.10.1 Isolated Ground

The power return of the disk drive is connected to the drive chassis. If a particular application does not require this, the mounting screw near the middle of the servo PCB may be replaced with a nylon screw. This isolates the power return from the chassis ground.

1.11 MOUNTING THE DISK DRIVE

The disk drive has been designed such that it can be mounted in any plane, i.e.: upright, horizontal, or vertical. The only restriction is that the logic PCBA side of the chassis must be uppermost when the disk drive is mounted horizontally. Eight (8) 6-32 tapped holes are provided for mounting: two (2) on each side and four (4) on the bottom of the housing (see Figure 1-1).

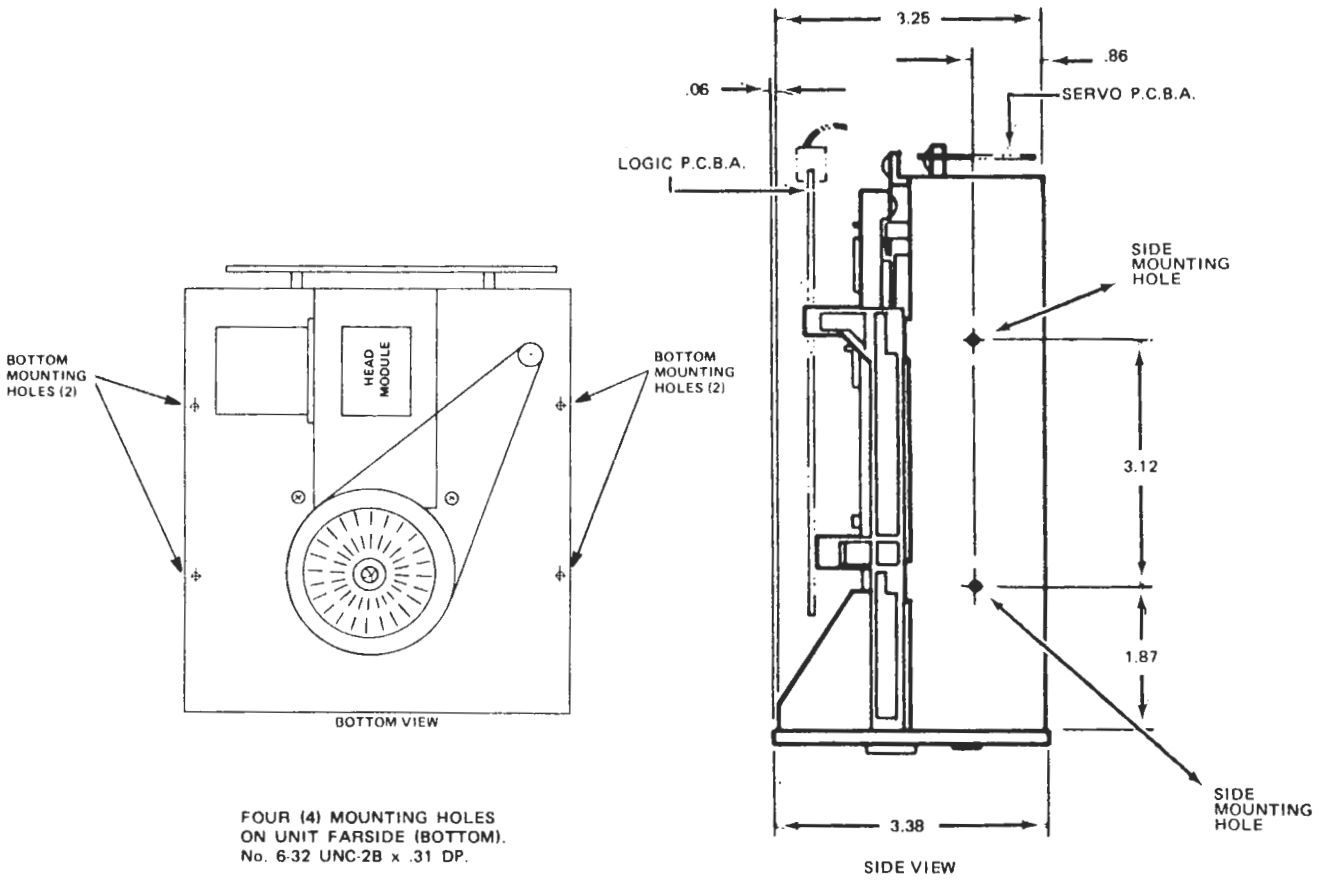


Figure 1-1
TM-100 Disk Drive Mounting Configuration

1.11.1 Hardware

The disk drive is manufactured with certain cricital internal alignments that must be maintained. Hence, it is important that the mounting hardware does not introduce significant stress on the disk drive.

Any mounting scheme in which the disk drive is part of the structural integrity of the enclosure may cause equipment operating problems and should be avoided.

Mounting schemes should allow for adjustable brackets or incorporate resilient members to accommodate tolerances.

1.11.2 Dust Cover

The design of an enclosure should incorporate a means to prevent contamination from loose items — e.g., dust, lint, paper chad — since the disk drive does not have a dust cover.

1.11.3 Cooling System Requirements

Heat dissipation from a single disk drive is normally 15 watts (51 Btu/Hr.) under high line conditions. When the disk drive is mounted so that the components have access to the free flow of air, normal convection cooling allows operation over the specified temperature range.

When the disk drive is mounted in a confined environment, air flow must be provided to maintain specified air temperatures in the vicinity of the motors, the PCBA's, and the diskette.

1.12 DISKETTE CARE, HANDLING, AND STORAGE

It is important that the diskette be cared for, handled, and stored properly so that the integrity of the recorded data is maintained. A damaged or contaminated diskette can impair or prevent recovery of data, and can result in damage to the Read/Write heads of the disk drive.

The following list contains information on how the diskette can optimally be cared for, handled, and stored.

1. Keep the diskette away from magnetic fields.
2. Do not touch the precision surface of the diskette with fingers.
3. Insert the diskette carefully into the disk drive until the backstop is encountered.
4. Do not bend or fold the diskette.
5. Put the diskette into its jacket when it is not in use.
6. Store the diskette at temperatures between 10°C and 52°C or 50°F and 125°F.

1.13 WRITE PROTECT

The disk drive is equipped with a Write Protect Switch Assembly. This sensor operates in conjunction with a diskette that has a slot cut in the protective jacket.

When the slot is covered with a self-adhesive tab, the diskette is write protected. The slot must be uncovered to write on the diskette.

1.14 OPERATION OF THE DISK DRIVE

The disk drive consists of the mechanical and electrical components necessary to record and to read digital data on a diskette. User-provided DC power at +12 V and +5 V is required for operation of the disk drive.

1.15 ORGANIZATION OF THE DISK DRIVE

All electrical subassemblies in the disk drive are constructed with leads that terminate in 4- to 5-pin connectors, enabling the individual assemblies to be removed.

The magnetic heads are connected to the PCBA via cables that terminate in 5-pin female connectors and their associated male sockets, which are located in close proximity to the Read/Write data electronics.

Interface signals and power are provided via connectors at the rear of the disk drive.

1.16 COMPONENTS OF THE DISK DRIVE

The disk drive consists of seven (7) functional groups:

1. Index Pulse Shaper
2. Write Protect Sensor
3. Track 00 Sensor
4. Spindle Drive Control
5. Carriage Position Control
6. Write/Erase Control
7. Read Amplifier and Digitizer

Figure 1-2 is a functional block diagram of the disk drive. It should be referred to in conjunction with the following sections. The data in the ensuing figures is primarily represented in simplified form.

1.16.1 Index Pulse

An index pulse is provided to the user system via the Index Pulse interface line. The index circuitry consists of an Index LED, an Index Photo Transistor, and a Pulse Shaping Network. As the index hole in the disk passes the Index LED/Photo Transistor combination, light from the LED strikes the Index Photo Transistor, causing it to conduct. The signal from the Index Photo Transistor is passed to the Pulse Shaping Network, which produces a pulse for each hole detected. This pulse is presented to the user on the Index Pulse Interface line.

1.16.2 Write Protect

A Write Protect signal is provided to the user's system via the Write Protect interface line. The Write Protect circuitry consists of a Write Protect sensor and circuitry that routes the signal that is produced.

When a write protected diskette is inserted in the disk drive, the sensor is activated and the logic disables the write electronics and supplies the status signal to the interface.

1.16.3 Track 00 Switch

The level on the Track 00 interface line is a function of the position of the magnetic head assembly. When the head is positioned at Track 00 and the stepper motor is at the home position, a true (low) level signal is generated at the interface.

1.16.4 Spindle Drive System

The Spindle Drive system consists of a spindle assembly driven through a drive belt by a DC motor/tachometer combination.

The servo electronics required for speed control are associated with the spindle drive motor.

The control circuitry also includes a current limiter and interface control line. When the Drive Motor Enable interface line is true, the drive motor is allowed to come up to speed. When the current through the drive motor exceeds 1.3 ampere, the current limit circuitry disables the motor drive.

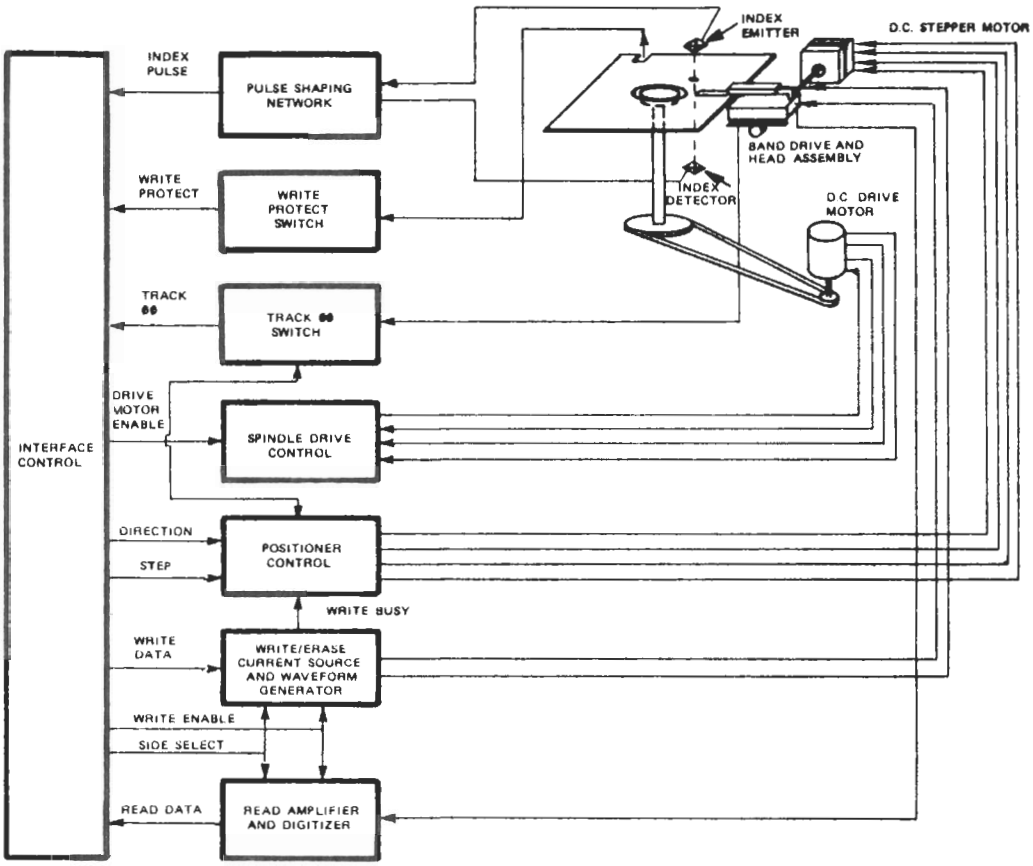


Figure 1-2
TM-100 Disk Drive Functional Block Diagram

1.16.5 Positioner Control

The Head Positioning system utilizes a four-phase stepper motor drive, which changes one phase for each track advancement of the Read/Write carriage. In addition to the logic necessary for motion control, a gate is provided which inhibits positioner motion during a write operation.

1.16.6 Data Electronics

Information can be recorded on the diskette by using a double-frequency code. Figure 1-3 illustrates the magnetization profiles in each bit cell for the number sequence shown for FM recording.

The erase gaps provide a guard band on either side of the recorded track. This provides flexibility in track positioning.

All signals required to control the data electronics are provided by the user system and are shown in the TM-100 disk drive functional block diagram (see Figure 1-2). These control signals are:

1. Select
2. Write Enable
3. Write Data
4. Side Select

The Read Data composite signal is sent to the user system via the interface.

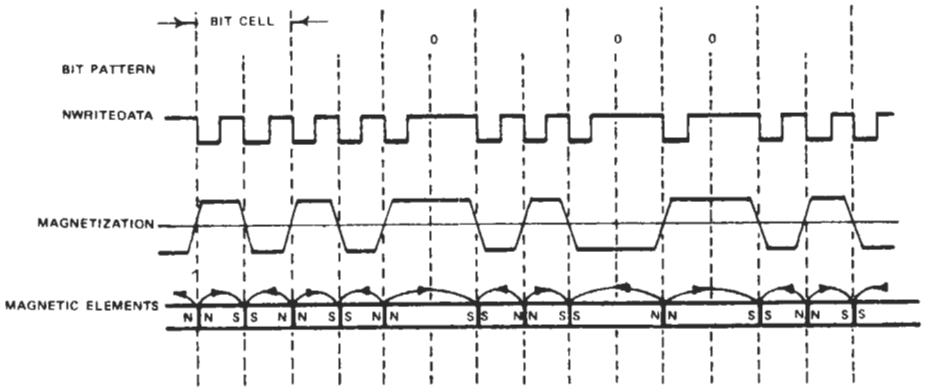


Figure 1-3
FM Recording Magnetization Profiles

1.16.6.1 Data Recording

The write electronics consist of a Write Current Source, a Write Waveform Generator, an Erase Current Source, the Trim Erase Control Logic, and the Head Select Logic (see Figure 1-2).

The read/write winding on the magnetic head is center-tapped. During a write operation, current from the Write Current Source flows in alternate halves of the winding, under control of the Write Waveform Generator.

The conditions required for recording, i.e., unit ready, must be established by the user system, as follows:

1. Drive speed stabilization occurs 250 msec after the drive motor is started.

2. Subsequent to any step operation, the positioner must be allowed to settle. This requires 20 msec after the last step pulse is initiated, i.e., 5 msec for the step motion and 15 msec for settling.

3. The foregoing operations can be overlapped, if required.

Figure 1-4 illustrates the timing diagram for a write operation. At t = 0, when the unit is ready, the Write Enable interface line goes true. This enables the Write Current Source.

The Trim Erase control goes true 390 msec after the Write Enable interface line since the trim erase gaps are behind the read/write gap. It should be noted that this value is optimized between the requirements at Track 00 and at Track 39, so that the effect of the trim erase gaps on previous information is minimized.

Figure 1-4 shows the information on the Write Data interface line and the output of the Write Waveform Generator, which toggles on the leading edge of every Write Data pulse.

Note that a minimum of 4 usec and a maximum of 8 usec between Write Enable going true and the first Write Data pulse is only required if faithful reproduction of the first Write Data Transition is significant.

At the end of recording, at least one additional pulse on the Write Data line must be inserted after the last significant Write Data pulse to avoid excessive peak shift effects.

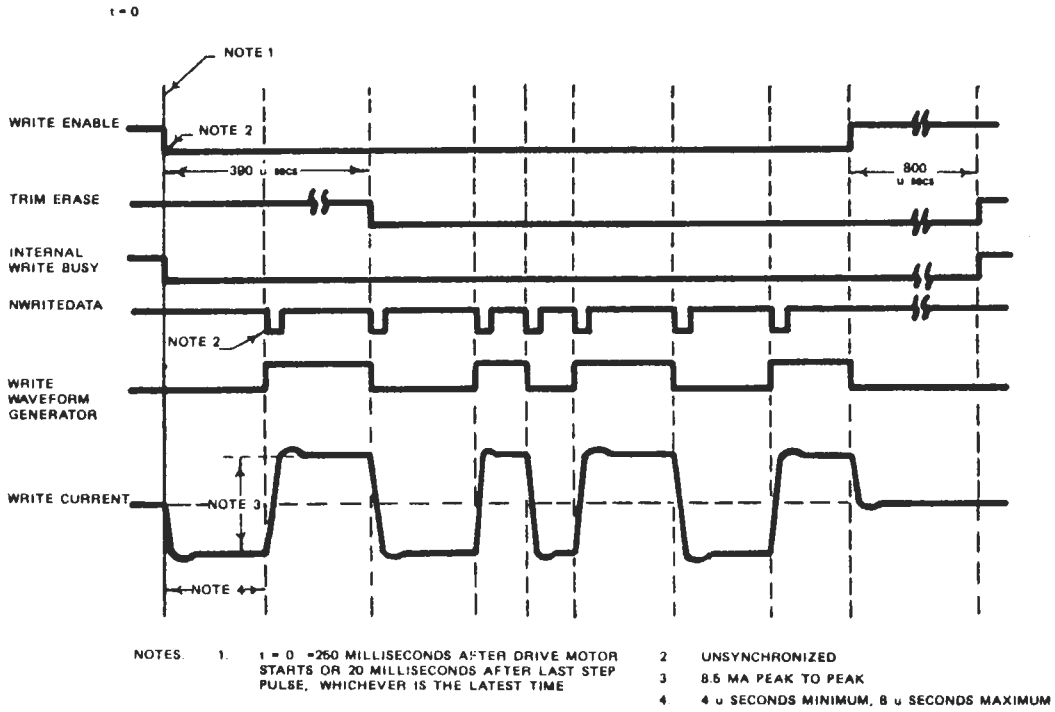


Figure 1-4
Write Operation Timing Diagram

The duration of a write operation is from the true going edge of Write Enable to the false going edge of Trim Erase. This is indicated by the internal Write Busy waveform shown (see Figure 1-4).

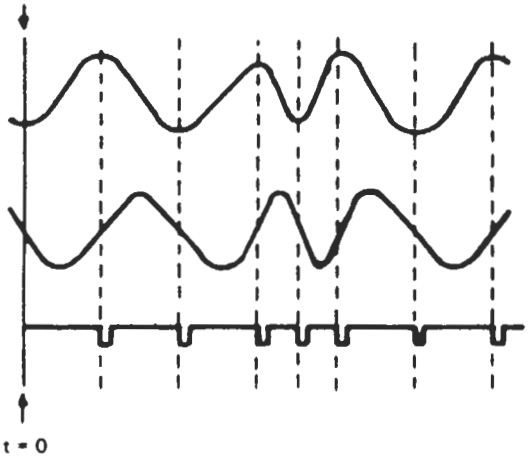
The Read electronics consist of:

1. Read Switch/Side Select
2. Read Amplifier
3. Filter
4. Differentiator
5. Comparator and Digitizer

The Read switch is used to isolate the Read Amplifier from the voltage excursion across the magnetic head during a Write operation. The side select is used to enable one of the Read/Write/Erase heads.

The disk drive must be in a ready condition before reading can begin. As with the data recording operation, this ready condition must be established by the user system. In addition to the requirements established in this section, a 100 usec delay must exist from the trailing edge of the Trim Erase signal to allow the Read Amplifier to settle after the transient caused by the Read switch returning to the Read mode.

The output signal from the Read/Write head is amplified by a Read Amplifier and filtered by a linear phase filter to remove noise (see Figure 1-5). The linear output from the filter is passed to the Differentiator, which generates a waveform whose zero crossovers correspond to the peaks of the Read signal. Then, this signal is fed to the Comparator and the Digitizer circuitry.



NOTES: t = 0 =250 MILLISECONDS AFTER DRIVE MOTOR STARTS, OR 20 MILLISECONDS AFTER STEP COMMAND, OR 100 u SECONDS AFTER TERMINATION OF WRITE BUSY, WHICHEVER IS THE LATEST TIME

Figure 1-5
Read Timing Diagram

The Comparator and the Digitizer circuitry generate a 1 usec Read Data pulse, corresponding to each peak of the Read signal. Then, the Composite Read Data signal is sent to the user system via the Read Data interface line.

1.17 INTERFACE ELECTRONICS

All interface signals are TTL-compatible. Logic true (low) is +0.4V (maximum); logic false (high) is +2.4V (minimum). The maximum interface cable length is ten (10) feet.

It is recommended that the interface cable be flat ribbon cable, having a characteristic impedence of 100 ohms, or equivalent twisted pairs.

1.17.1 Interface Connector Pin Assignments, J1/P1

The interface connector pin assignments, J1/P1, are listed in Table 1-2.

1.17.2 Power Connector Pin Assignments

The power connector pin assignments are listed in Table 1-3.

1.18 OPTION SELECT

1.18.1 Input Line Terminations

The disk drive has the capability of terminating the following input lines:

1. Motor On
2. Direction Select
3. Step
4. Write Data

TABLE 1-2
INTERFACE CONNECTOR PIN ASSIGNMENTS, J1/P1

CONTROLLER-TO-DISK DRIVE		
Ground	**Signal**	**Mnemonic Description**
1	2	Connector Clamp
3	4	Spare
5	6	Select 3 (NDS3)
9	10	Select 0 (NDS0)
11	12	Select 1 (NDS1)
13	14	Select 2 (NDS2)
15	16	Drive Motor Enable (N MOTOR ON)
17	18	Direction (DIR)
19	20	Step (N STEP)
21	22	Write Data (N WRITE DATA)
23	24	Write Gate (N WRITE ENABLE)
31	32	Side Select (N SIDE SELECT)
33	34	Connector Clamp

DISK DRIVE-TO-CONTROLLER		
Ground	**Signal**	**Mnemonic Description**
7	8	Index (N INDEX / SECTOR)
25	26	Track 00 (N TRK 00)
27	28	Write Protect (N WRITE PROTECT)
29	30	Read Data (N READ DATA)

TABLE 1-3
POWER CONNECTOR PIN ASSIGNMENTS

Pin	Supply Voltage
1	+12 VDC
2	Return (+12 VDC)
3	Return (+5 VDC)
4	+5 VDC

5. Side Select

6. Write Gate

These input lines are terminated through a 150 ohm resistor pack that is installed in the dip socket located at IC location 2F. In a single-drive system, this resistor pack should be kept in place to provide the proper terminations. In a multiple-drive system (Program Shunt position MX open), only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed (see Figure 1-6).

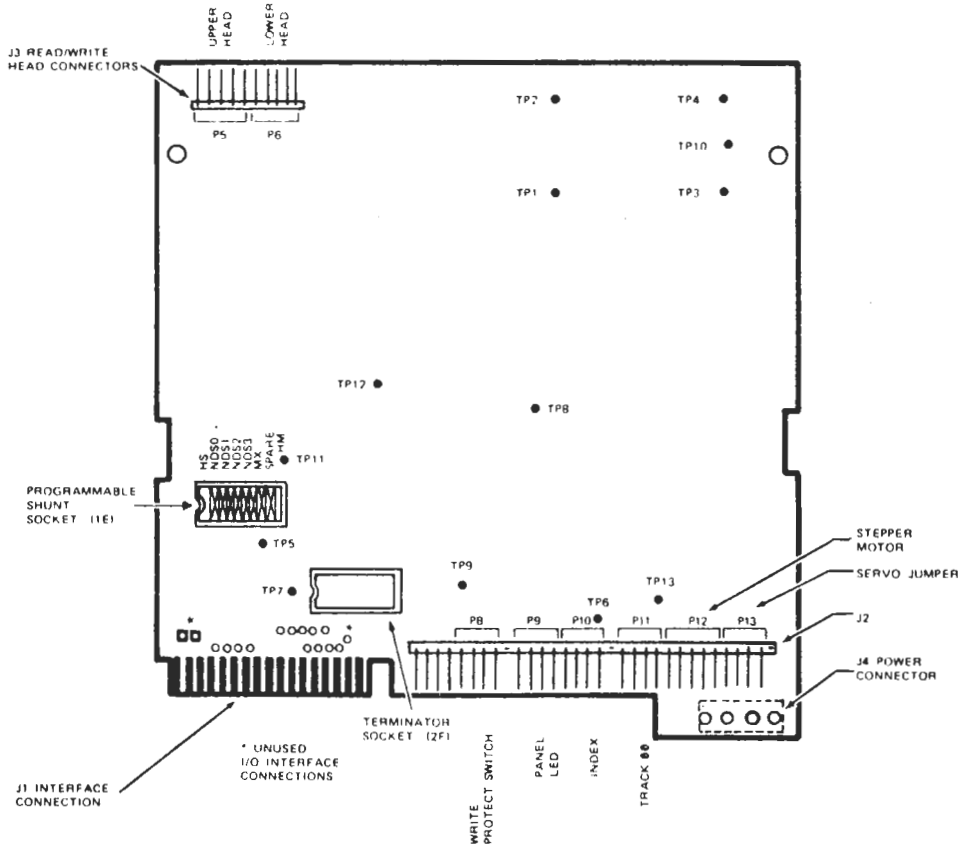


Figure 1-6
Logic Printed Circuit Board Assembly

1.18.2 Drive Select

As shipped from the factory, the disk drive is configured to operate in a single-drive system. The user can easily modify it to operate with other drives in a multiplexed, multiple-drive system. The user can activate the multiplex option by cutting the MX position of the programmable shunt, located at IC location 1E, which allows the input/output (I/O) lines to be multiplexed.

The Select lines provide a means of selecting and deselecting a disk drive. These four (4) lines — NDS0 through NDS3 — select one of the four (4) disk drives attached to the controller.

When the signal logic level is true (low), the disk drive electronics are activated and the disk drive is conditioned to respond to Step or to Read/Write commands. When the signal logic level is false (high), the Input Control lines and the Output Status lines are disabled.

A Select line must remain stable in the true (low) state until the execution of a Step or Read/Write command is completed.

The disk drive address is determined by a Select Shunt on the PCBA. Select lines zero-through-three (0-3) provide a means of daisy chaining a maximum of four (4) disk drives to a controller. Only one (1) line can be true (low) at a time. An undefined operation might result if two or more units are assigned the same address or if two or more Select lines are in the true (low) state simultaneously (see Figure 1-6).

The Program Shunt is AMP Part Number 435704-7. The Program Shunt positions can be cut using AMP's Part Number 435705. The Program Shunt is installed in a dip socket. At the user's option, the Program Shunt may be removed and replaced by a dip switch. In addition, the user may choose to have the Program Shunts preprogrammed and/or color coded by AMP. For this service, contact your local AMP representative.

1.19 POWER SAVE OPTION

As shipped from the factory, the disk drive is configured to operate in a single-drive system. Jumper (0 ohm resistor) R51 maintains the power to the stepper motor whether or not the disk drive is selected. However, the jumper in position R51 may be moved to position R50. R50 removes the power to the stepper motor when the disk drive is not selected, for a savings approximately equal to 3.8 watts per drive. When R50 is used, at the time the disk drive is reselected, the user must ensure the track location.

SECTION II
MAINTENANCE CHECKS AND ADJUSTMENTS

2. INTRODUCTION

This section is designed for the use of the OEM Repair Department. It contains the maintenance checks and adjustments that are used during the normal life of the disk drive.

Before applying power to the unit or doing any checks or adjustments, visually inspect the disk drive to ensure that it has no missing or broken parts.

The following equipment is required for checks and adjustments:

1. A dual-channel, wideband oscilloscope (HP 1740A or equivalent).
2. An exerciser or software routine capable of stepping the disk drive to any track, selecting the upper or lower head, and writing a 1F (all zeros if FM) or a 2F (all ones if FM) pattern.
3. A Phillips screwdriver.
4. A .050" Allen wrench.
5. A flat blade screwdriver.
6. A 3/16" nut driver.
7. A work diskette.
8. An alignment diskette (Dysan P/N 222/2A).

2.1 DRIVE MOTOR CHECKS AND ADJUSTMENTS

The long-term drive motor speed adjustment ensures that the motor's speed is within the range of tolerance specified. The motor speed specification is 300 rpm ± 1.5%.

2.1.1 Long-Term Drive Motor Speed Checks and Adjustment

2.1.1.1 Preliminary checks required:

Verify power: +12 VDC ±.6 V
+5 VDC ±.25 V

2.1.1.2 Apply power to the disk drive.

2.1.1.3 Activate the drive motor on the interface line.

2.1.1.4 Insert a work diskette.

2.1.1.5 Observe the speed disk on the spindle pulley under flourescent lighting (see Figure 2-1).

2.1.1.6 Adjust R4, located on the Servo PCBA, until the applicable pattern on the pulley appears stationary (see Figure 2-2).

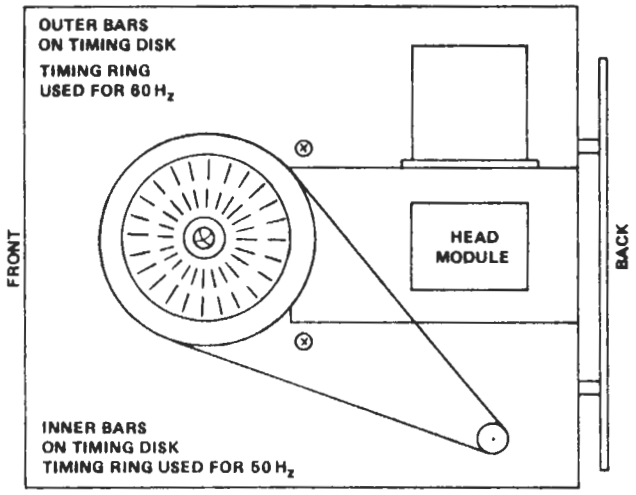


Figure 2-1
Bottom View of The TM-100 Disk Drive

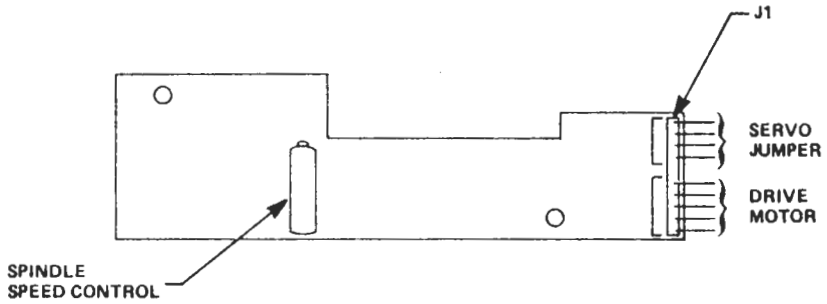


Figure 2-2
Location of R4 Speed Control Pot

2.1.2 Instantaneous Speed Variation Check

The Instantaneous Speed Variation (ISV) checks the smoothness of the spindle's rotation. This is determined by the disk drive system, which consists of the drive motor, drive belt, pulleys, hub, and hub bearings.

2.1.2.1 With the work diskette inserted, write a 2F (all ones) pattern on any track.

2.1.2.2 Connect a wideband oscilloscope to Test Point 5 on the logic PCBA, using Test Point 6 as a ground.

2.1.2.3 Set up a dual-channel, wideband oscilloscope, as follows:

Vertical: 2 Volts Per Division

Time Base: 1 usec Per Division

Internal Trigger: Positive Edge

2.1.2.4 Observe the following pattern (see Figure 2-3).

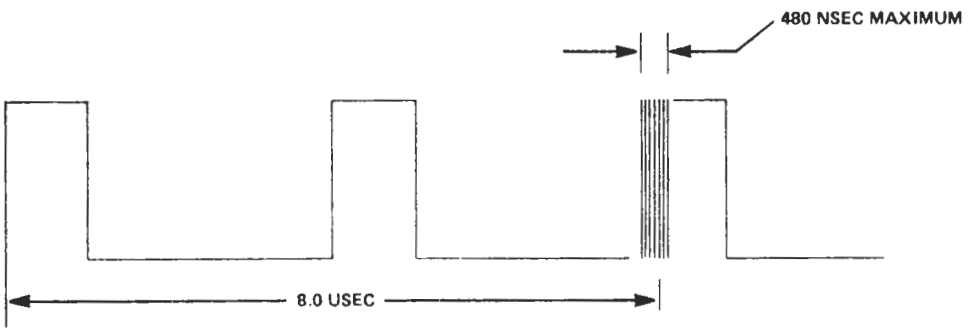


Figure 2-3
ISV Pulse Pattern

2.1.2.5 Measure the amount of jitter present on the leading edge of the third pulse (see Figure 2-3). The leading edge of the third pulse should start 8 usec ±240 nsec from the trigger pulse. Jitter on the third pulse of greater than ±240 nsec (480 nsec edge-to-edge) indicates excessive ISV.

2.1.2.6 Confirm the measurement (see Section 2.1.2.5) with a second work diskette.

2.1.2.7 If the ISV is excessive, replace the drive belt (see Section 5.1), and remeasure the Instantaneous Speed Variation (ISV) (see Section 2.1.2).

2.1.2.8 If the ISV is excessive, replace the drive motor (see Section 5.10), and remeasure the ISV (see Section 2.1.2).

2.1.2.9 If replacing the drive belt and the drive motor does not cure the excessive ISV, see Section IV (Troubleshooting Guide).

2.2 CATS EYE ALIGNMENT CHECK AND ADJUSTMENT

The Cats Eye (CE) alignment procedure locates the magnetic read/write head at the proper radial distance from the hub center line, thus ensuring that the track location is accurate (see Figure 2-4). This adjustment is necessary only after service or if diskette interchange problems are suspected.

2.2.1 CE Alignment Check

2.2.1.1 Set up a dual-channel, wideband oscilloscope, as follows:

Channel A: Test Point 1

Channel B: Test Point 2

Ground: Test Point 10

Read Differentially: A plus B, B inverted

Time Base: 20 msec Per Division

External Trigger: Test Point 7, Positive Edge

2.2.1.2 Apply power to the disk drive.

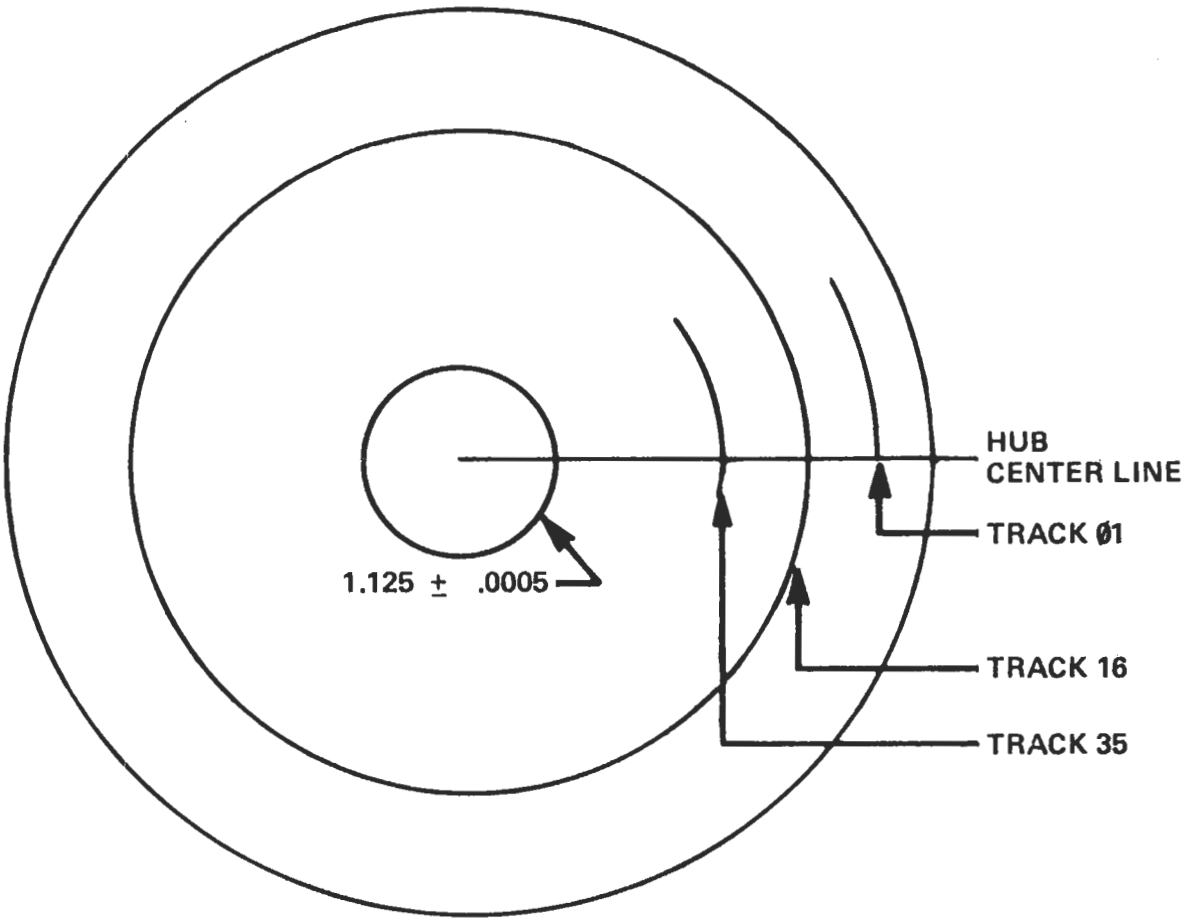


Figure 2-4
Hub Center Line and Track Locations

NOTES

The Track 16 radius is 1.9167. Other track locations are computed based upon 48 TPI.

2.2.1.3 Select the disk drive with the interface logic.

2.2.1.4 Insert a Cats Eye alignment diskette (Dysan alignment diskette number 800180) into the disk drive.

2.2.1.5 Select Head 00, the lower head.

2.2.1.6 Read Track 16 for Cats Eye alignment of the lower magnetic head.

2.2.1.7 Adjust the dual-channel, wideband oscilloscope to observe a Cats Eye pattern (see Figure 2-5).

2.2.1.8 Verify that the smaller of the two (2) Cats Eye patterns is not less than 75% in amplitude of the other one.

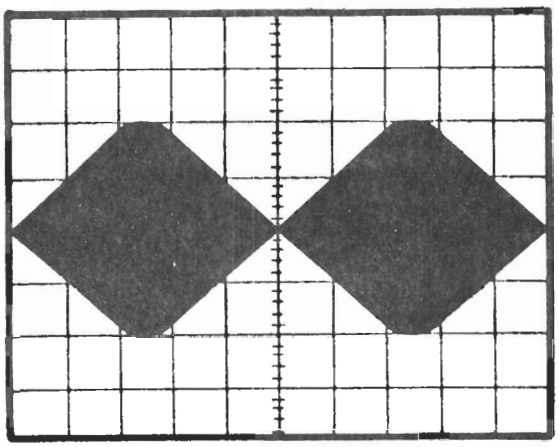


Figure 2-5
Cats Eye Pattern

NOTE

The 75% figure is for use with an alignment diskette that has been verified against a standard alignment diskette.

2.2.1.9 Step the disk drive to Track 00; then, step it back to Track 16.

2.2.1.10 Reverify the Cats Eye pattern.

2.2.1.11 Step the disk drive to Track 26 or a higher track; then, step it back to Track 16.

2.2.1.12 Reverify the Cats Eye pattern.

2.2.1.13 Switch to Head 01, the upper magnetic head.

2.2.1.14 Read Track 16 to verify the alignment of the upper magnetic head.

2.2.1.15 Verify the Cats Eye pattern.

2.2.1.16 Step the disk drive to Track 00; then, step it back to Track 16.

2.2.1.17 Reverify the Cats Eye pattern.

2.2.1.18 Step the disk drive to Track 26 or a higher track; then, step it back to Track 16.

2.2.1.19 Reverify the Cats Eye pattern.

2.2.1.20 If all of the checks listed above verify or reverify, the Cats Eye alignment of the magnetic head is acceptable.

2.2.1.21 If any of the checks listed above does not meet the conditions stated in Section 2.2.1.8, the corresponding magnetic head must be adjusted.

2.2.2 Head Adjustment

2.2.2.1 Turn the three (3) module retaining screws – two of which are located underneath and one of which is located at the back of the disk drive in the center – counterclockwise one-half (1/2) turn (see Figure 2-6) with a Phillips screwdriver.

2.2.2.2 Turn the cam screw (see Figure 2-6) counterclockwise with a flat blade screwdriver.

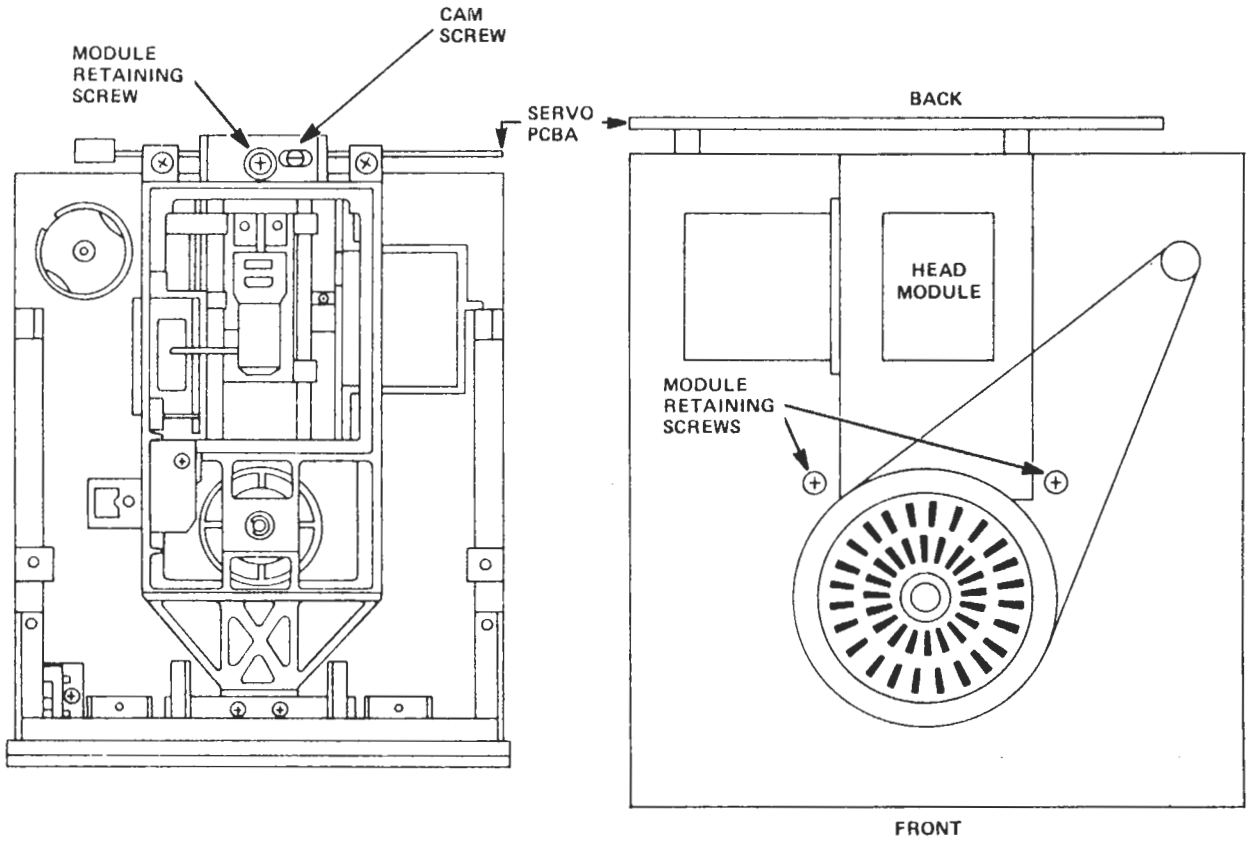


Figure 2-6
Head Module Retaining and Cam Screws

2.2.2.3 Observe the Cats Eye pattern at the magnetic head that is farthest out of alignment.

2.2.2.4 Using a flat blade screwdriver, turn the cam screw until the Cats Eye pattern meets the conditions stated in Section 2.2.1.8.

2.2.2.5 Tighten the three (3) module retaining screws (see Figure 2-6) with a Phillips screwdriver.

2.2.2.6 Reverify the Cats Eye alignment (see Section 2.2.1).

2.2.3 Track 00 Stop Adjustment

2.2.3.1 The Track 00 stop screw does not allow the carriage assembly to seek to a track lower than Track 00.

2.2.3.2 The Track 00 stop screw should be adjusted when the Cats Eye pattern is adjusted or the carriage seeks to a track lower than Track 00.

2.2.3.3 Apply power to the disk drive.

2.2.3.4 Select the disk drive with the control logic.

2.2.3.5 Monitor the output at Test Point 1.

2.2.3.6 Monitor the output at Test Point 2.

2.2.3.7 Set the dual-channel, wideband oscilloscope to read differentially, A and B, B inverted.

2.2.3.8 Insert an alignment diskette.

2.2.3.9 Read the information at Track 00.

2.2.3.10 Turn the Track 00 stop screw counterclockwise two (2) turns with a .050" Allen wrench (see Figure 2-7).

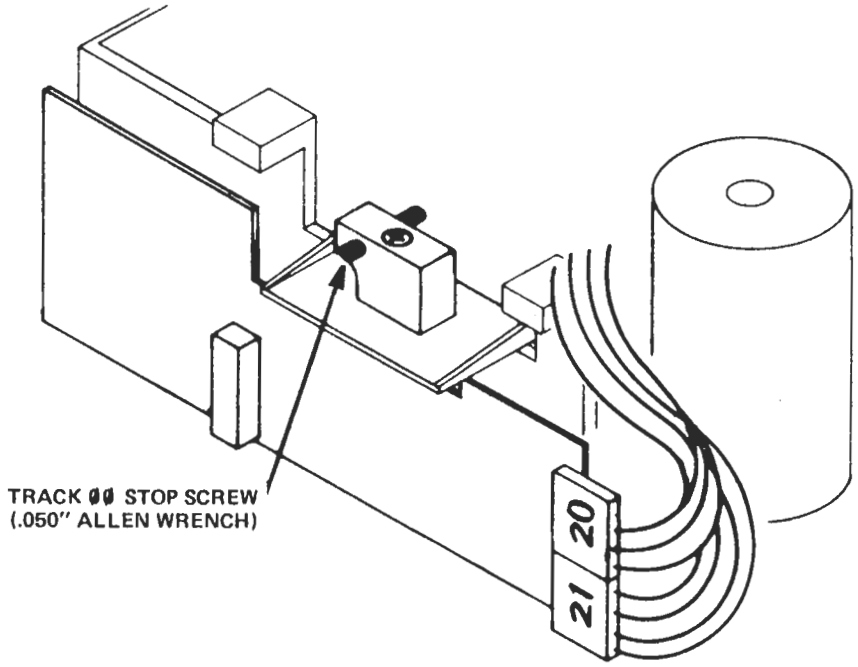


Figure 2-7
Track 00 Stop

2.2.3.11 Slowly turn the Track 00 stop screw clockwise until the output amplitude shown on the dual-channel, wideband oscilloscope begins to decrease.

2.2.3.12 Turn the Track 00 stop screw counterclockwise until the amplitude stops increasing.

2.2.3.13 Turn the Track 00 stop screw counterclockwise an additional one-eighth (1/8) turn.

2.3 INDEX CHECKS AND ADJUSTMENT

The index adjustment changes the time period from the index pulse to the start of the data. The adjustment should be checked after the disk drive has been aligned (see Section 2.1.1) or when diskette interchange errors are suspected.

2.3.1 Index Checks

2.3.1.1 Check the speed of the long-term drive motor.

2.3.1.2 Apply power to the disk drive.

2.3.1.3 Select the disk drive with the control logic.

2.3.1.4 Set up a dual-channel, wideband oscilloscope, as follows:

External Trigger: Test Point 7, Positive Edge

Read Differentially: A plus B, B inverted

Channel A to Test Point 1

Channel B to Test Point 2

Time Base: 50 usec Per Division

2.3.1.5 Insert an alignment diskette.

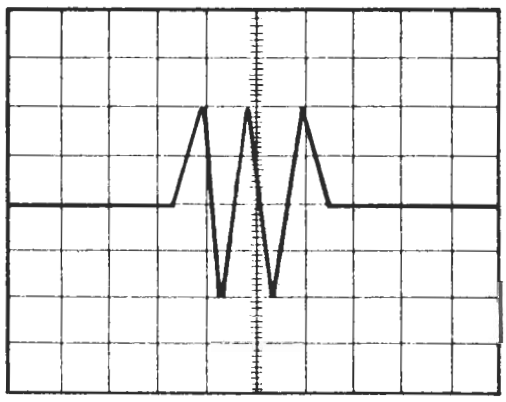
2.3.1.6 Select Track 01.

2.3.1.7 Select Head 00, the lower magnetic head.

2.3.1.8 Read the trigger point to the start of the first data pulse width (see Figure 2-8).

NOTE

The specification is 200 usec ± 100 usec.



TIME SCALE: 50 USEC PER DIVISION

Figure 2-8
Index-To-Data Pulse

2.3.1.9 For double-sided disk drives, if Head 00, the lower head, meets the specification, check Head 01, the upper head.

NOTE

Head 01 should meet the same specification.

2.3.1.10 If either Head 00 or Head 01 does not meet the specification, adjust the index sensor (see Section 2.3.2.1).

2.3.1.11 Recheck both indexes after they are adjusted.

2.3.1.12 When both index measurements on a double-sided disk drive or the one index measurement on a single-sided disk drive meet the specification, check the index on Track 34.

2.3.1.13 On a double-sided disk drive, check Heads 01 and 00, the upper and lower heads.

NOTES

If any index measurement does not meet the specification, the index sensor must be adjusted (see Section 2.3.2.1).

If the index measurements meet the specification, the index sensor does not need to be adjusted.

2.3.1.14 Recheck all indexes after each adjustment.

2.3.2 Index Adjustment

2.3.2.1 From the bottom of the chassis, lossen the index sensor's retaining screw counterclockwise one-quarter (1/4) turn (see Figure 2-9) with a Phillips screwdriver.

2.3.2.2 Adjust the index sensor with a flat blade screwdriver until the data pulse begins 200 usec ± 100 usec from the trigger point.

2.3.2.3 Tighten the index sensor's retaining screw with a Phillips screwdriver.

2.3.2.4 Verify the indexes.

2.4 COMPLIANCE CHECK AND ADJUSTMENT

Compliance is the maximized output of the magnetic head when the pressure of the felt pressure pad is centered over the read/write gap. For single-sided disk drives, a compliance check and adjustment can be made in the field. For double-sided disk drives, a compliance check and adjustment must be made at the factory.

2.4.1 Compliance Check

2.4.1.1 Rest the disk drive on its cast base.

2.4.1.2 Remove the two (2) screws that attach the Logic PCBA to the guide rails.

2.4.1.3 Lift out the Logic PCBA, and lay it on the disk drive.

NOTE

This allows the operator to reach inside the disk drive to move the magnetic head.

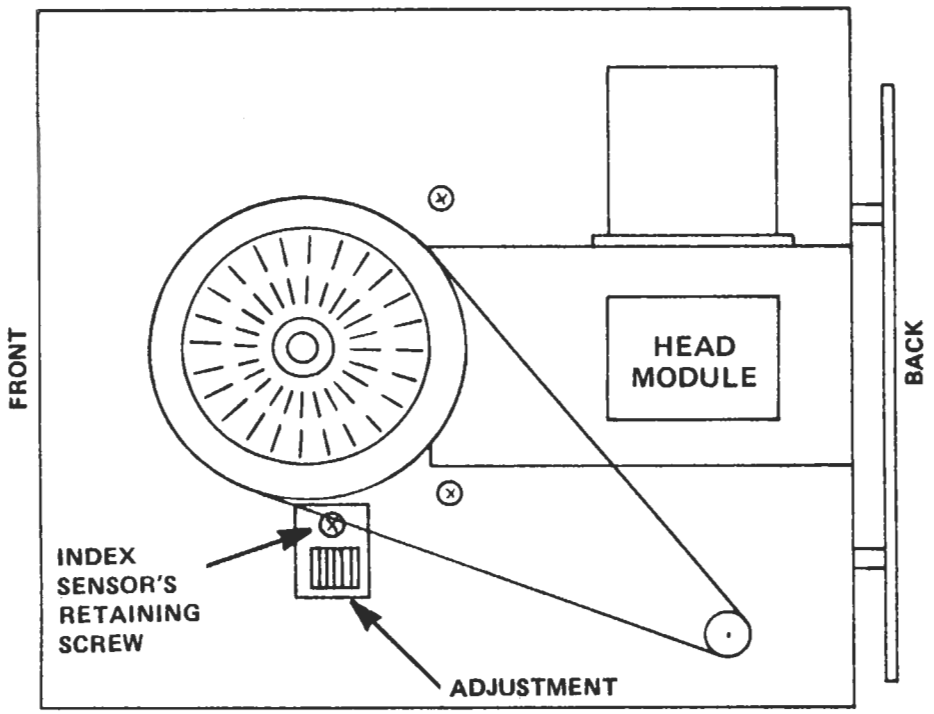


Figure 2-9
Index Sensor's Retaining Screw and Adjustment

2.4.1.4 Apply power to the disk drive.

2.4.1.5 Select the disk drive with the control logic.

2.4.1.6 Insert a work diskette.

2.4.1.7 Write information on Track 34.

2.4.1.8 Read the information on Track 34.

2.4.1.9 Set up a dual-channel, wideband oscilloscope, as follows:

Channel A: Test Point 1

Channel B: Test Point 2

Ground: Test Point 10

Read Differentially: A and B, B Inverted

Time Base: 10 msec per Division

External Trigger: Test Point 7, Positive Edge

2.4.1.10 Read the output voltage.

2.4.1.11 With a gram gauge, carefully apply fifteen (15) grams pressure to the upper arm, increasing the load force on the magnetic head.

Note

Fifteen grams is about the weight of a quarter.

2.4.1.12 If the output shown on the dual-channel, wideband oscilloscope increases by more than ten percent (10%), adjust the compliance.

2.4.2 Compliance Adjustment

The compliance is adjusted by using the same procedure as is used in the compliance check (see Section 2.4.1).

2.4.2.1 Turn the two (2) nuts that attach the upper arm to the carriage assembly (see Figure 2-10) counter-clockwise one-quarter (1/4) turn with a 3/16" nut driver.

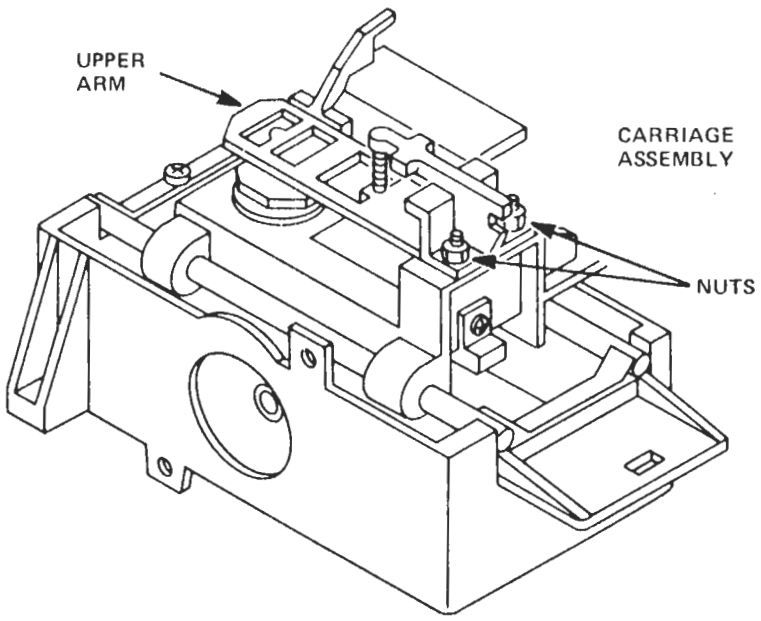


Figure 2-10
Upper Arm and Nuts

2.4.2.2 While monitoring the output, move the upper arm around the axis of the head until the output is the highest.

2.4.2.3 Turn the two (2) nuts that attach the upper arm to the carriage assembly clockwise with a 3/16" nut driver while holding the arm in the highest position.

2.4.2.4 Reverify the compliance of the magnetic head.

2.4.2.5 If the compliance cannot be adjusted, replace the upper arm (see Section 5.13).

2.5 WRITE PROTECT SWITCH ADJUSTMENT PROCEDURE

2.5.1 Connect the disk drive to an exercisor or computer with a direct monitor of write printed output (Pin 28 of J1) or, with no power to the disk drive, disconnect Plug 8, and check the continuity with an ohmeter.

2.5.2 With a non-write protected diskette inserted, verify that there is no continuity between the two (2) wires of Plug 8 or that there is a non-write protected output to the exercisor or computer, i.e., a high at Pin 28 of J1.

2.5.3 With a write protected diskette inserted, verify that there is continuity between the two (2) wires of Plug 8 or that there is a write-protect true output to the controller or exercisor (low at Pin 28 of J1).

Note

A defective circuit board can be responsible for a write protect problem. Test Point 9 should be high for a write-protected disk drive, and low for a non-write protected disk drive.

2.5.4 To adjust the write protect switch, loosen the screw that holds the switch to the bracket on the side farthest from the front of the disk drive. Move the switch up or down, as required, to satisfy the condition of Section 2.5.2 and Section 2.5.3 above (see Figure 2-11).

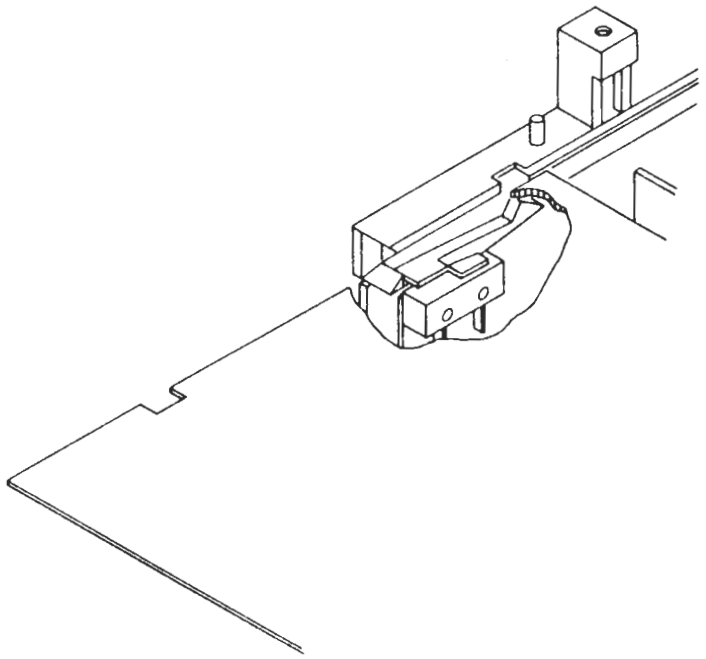


Figure 2-11
Write Protect Switch Adjustment

SECTION III
PRINTED CIRCUIT BOARD OPERATION

3. INTRODUCTION

This section contains the interface description and the mechanical and the electrical adjustments necessary for the TM-100-1 and -2 Disk Drives, 48 TPI. In addition, Section 3.2 and Section 3.3 contain schematic diagrams of the Logic Printed Circuit Board Assembly (PCBA) installed in the disk drive. Section 3.4 contains a schematic diagram of the Servo PCBA installed in the disk drive.

3.1 EXPLANATION OF SYMBOLS AND ABBREVIATIONS

Table 3-1 contains a list of all of the symbols and abbreviations found on the schematic diagrams in this section. In addition, in the functional and circuit descriptions, a specification line "N MOTOR ON" stands for the negative true motor on signal.

3.2 PHYSICAL DESCRIPTION OF THE LOGIC PCBA

The Logic PCBA is approximately 146 mm (5.75 inches) long by 146 mm (5.75 inches) wide. Figure 3-1 contains an illustration of the placement of test points and connectors.

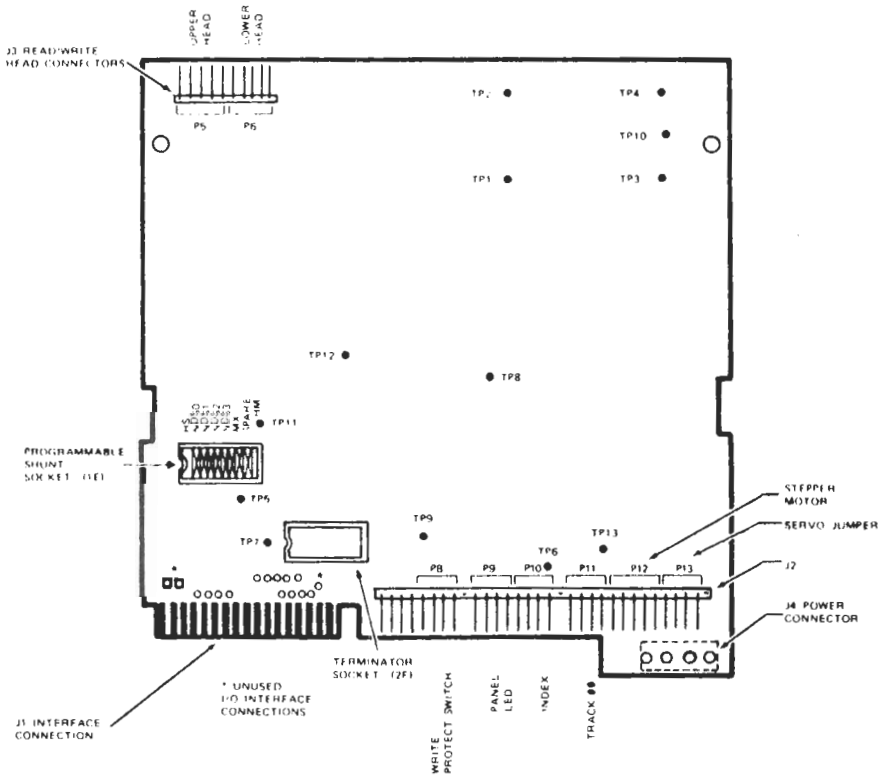


Figure 3-1
Logic PCBA

TABLE 3-1
SYMBOLS AND ABBREVIATIONS

Symbol	Meaning
	Erase Coils
	Read/Write Coils
	Normal Transistor
	Photo Transistor
	Driver
	Driver, Open Collector Output
	Driver, Inverted
	Inverter, Open Collector Output
	"AND" Gate, Open Collector Output
	"AND" Gate, Inverted

3.3 INTERFACE ELECTRONICS SPECIFICATIONS

All interface signals are TTL compatible. Logic true (low) is +0.4 V (minimum). Figure 3-2 illustrates the interface configuration. The maximum interface cable length is ten (10) feet.

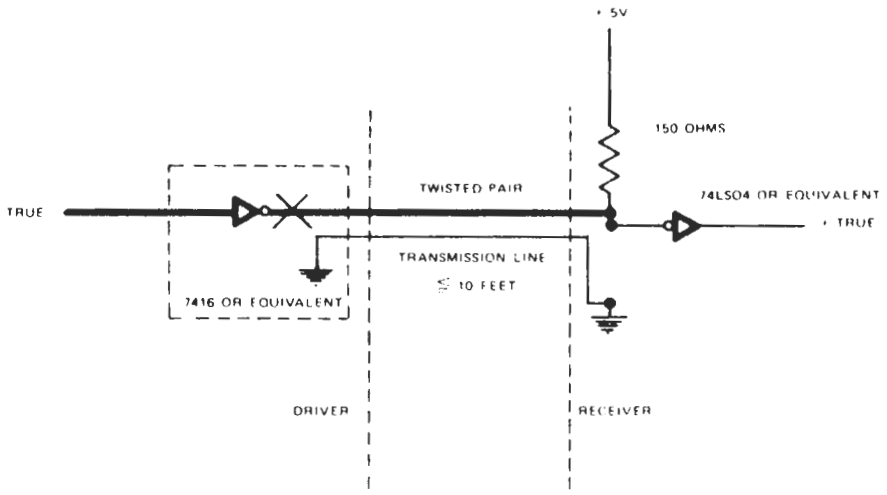


Figure 3-2
Interface Configuration

It is recommended that the interface cable be flat ribbon cable, with a characteristic impedance of 100 ohms (or equivalent twisted pairs).

Interface connector pin assignments and power connector pin assignments are given in Table 3-2 and Table 3-3.

3.3.1 Input Control Lines

TABLE 3-2
INTERFACE CONNECTOR PIN ASSIGNMENTS, J1/P1

CONTROLLER-TO-DISK DRIVE		
Ground	**Signal**	**Mnemonic Description**
1	2	Connector Clamp
3	4	Spare
5	6	Select 3 (NDS3)
9	10	Select 0 (NDS0)
11	12	Select 1 (NDS1)
13	14	Select 2 (NDS2)
15	16	Drive Motor Enable (N MOTOR ON)
17	18	Direction (DIR)
19	20	Step (N STEP)
21	22	Write Data (N WRITE DATA)
23	24	Write Gate (N WRITE ENABLE)
31	32	Side Select (N SIDE SELECT)
33	34	Connector Clamp

DISK DRIVE-TO-CONTROLLER		
Ground	**Signal**	**Mnemonic Description**
7	8	Index (N INDEX / SECTOR)
25	26	Track 00 (N TRK 00)
27	28	Write Protect (N WRITE PROTECT)
29	30	Read Data (N READ DATA)

TABLE 3-3
POWER CONNECTOR PIN ASSIGNMENTS

Pin	Supply Voltage
1	+12 VDC
2	Return (+12 VDC)
3	Return (+5 VDC)
4	+5 VDC

3.3.1.1 Select Lines (NDS0-NDS3)

Functional Description

The select lines (see Figure 3-3) provide a means of selecting and deselecting a disk drive. These four (4) lines (NDS0-NDS3 standard) select one (1) of the four (4) disk drives attached to the controller. When the signal logic level is true (low), the disk drive electronics are activated and the disk drive is conditioned to respond to Step or Read/Write commands. When the logic level is false (high), the input control lines and output status lines are disabled.

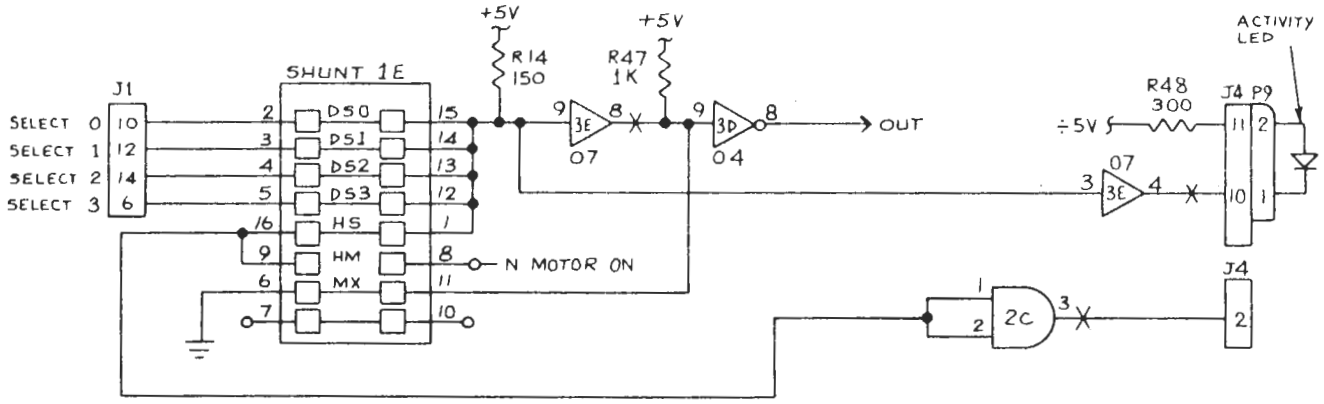


Figure 3-3
Select Lines Schematic Diagram

A select line must remain stable in the true (low) state until the execution of a Step or Read/Write command is completed.

The disk drive address is determined by a Select Shunt on the PCBA. Select lines 0-3 provide a means of daisy chaining a maximum of four (4) disk drives to a controller. Only one line can be true (low) at a time. An undefined operation might result if two or more units are assigned the same address or if two or more select lines are in the true (low) state simultaneously.

When the disk drive is selected, the activity (front panel) LED will be on.

In a multiple disk drive system, the MX jumper must be cut. If not, the disk drive will always be active.

Circuit Description

R14 holds the output of the appropriate select line high until the line is driven low. This is buffered through IC 3E 9-to-8 to IC 3D 9-to-8. IC 3D, Pin 8, is the output that enables the drive electronics. Note that when the MX jumper is not cut, the disk drive is always enabled (Pin 3D-8 high).

The front panel LED is driven by the select logic through IC 3E, Pin 3 to 4. Note that if the disk drive is not selected through the select jumpers, and the MX jumper is not cut, the drive electronics will be active but the front panel LED will not be on.

Normally, Tandon Corporation's disk drives have no head load solonoid. Hence, the HS and the HM jumpers are not used. In no case should both the HS and the HM jumpers be in since this would allow interaction between the Select signal and the Motor On signal. However, if the optional head load solonoid is installed, IC 2C, Pins 1, 2, & 3 drive it. This is selected by either the HS or the HM jumper. The HS jumper enables the head load solonoid driver when the unit is selected. the HM jumper enables the head load solonoid driver when the Motor On signal to the disk drive is true.

3.3.1.2 Drive Motor Enable (N MOTOR ON)

Functional Description

When the Drive Motor Enable signal line logic level goes true (low), the disk drive's motor accelerates to its nominal speed of 300 rpm and stabilizes in less than 250 msec. When the logic level goes false (high), the disk drive's motor decelerates to a stop.

Test Point 13 (see Figure 3-4) is low (true) for the Motor On condition.

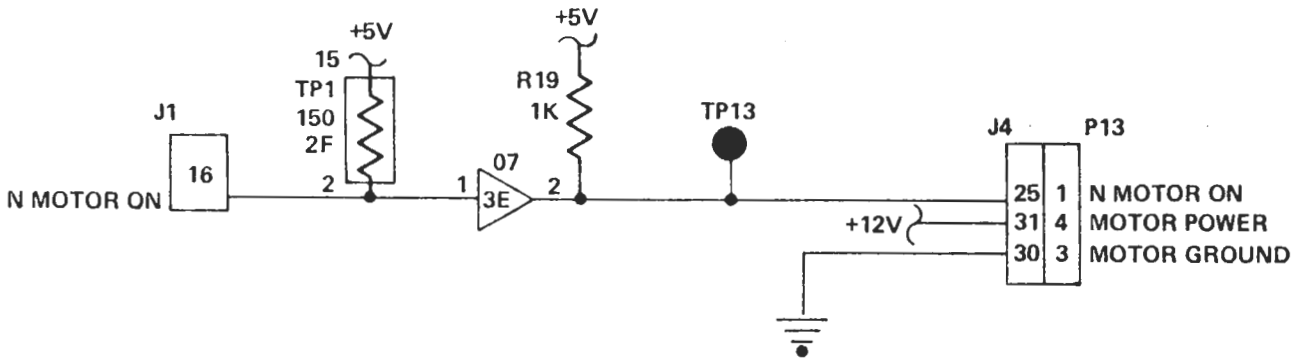


Figure 3-4
Drive Motor Enable Schematic Diagram

Circuit Description

The disk drive's Motor On signal comes in on Pin 16 and is buffered through IC 3E, Pin 1 and Pin 2 to the servo board.

3.3.1.3 Direction and Step Lines (Two Lines) (DIR) (N STEP)

Functional Description

When the disk drive is selected, a true (low) pulse with a time duration greater than 200 nsec on the Step line initiates the access motion. The direction of motion is determined by the logic state of the Direction line when a Step pulse is issued. The motion is toward the center of the disk drive if the Direction line is in the true (low) state when a Step pulse is issued. The direction of motion is away from the center of the disk drive if the Direction line is in the false (high) state when a Step pulse is issued. To ensure proper positioning, the direction line should be stable 100 usec (minimum) before the trailing edge of the corresponding Step pulse. The Direction line should remain stable until 100 usec after the trailing edge of the Step pulse. The access motion is initiated on the trailing edge of the Step pulse.

Test Point 8 (see Figure 3-5) is low (true) when the carriage is positioned at Track 00 and the step motor is at Phase 0.

When stepping in or out, Test Point 12 (see Figure 3-5) is a high going pulse for each step of the carriage (see Table 3-4).

TABLE 3-4
STEPPER LOGIC TRUTH

Step In (Toward Track 00)						**Step Out (Toward Track 40)**					
	Phase						**Phase**				
Pin No.	**0**	**3**	**2**	**1**	**0**	**Pin No.**	**0**	**1**	**2**	**3**	**0**
4C-5	0	1	1	0	0	4C-5	0	0	1	1	0
4C-6	1	0	0	1	1	4C-6	1	1	0	0	1
4C-9	0	0	1	1	0	4C-9	0	1	1	0	0
4C-8	1	1	0	0	1	4C-8	1	0	0	1	1

Circuit Description

The direction line comes in on Pin 18 of the interface connector. A high signal directs the step logic to step in toward Track 00. A low signal directs the stop logic to step out toward Track 39.

The direction line sets the proper phase to the exclusive OR gates of IC 5D. This signal is also buffered by IC 3D to gate IC 4F to inhibit stepping inward when the disk drive is already at Track 00. This is done at Pin 4 of IC 4B.

The step pulses come in at Pin 20 of the interface connector. They are buffered by 2E and gated at IC 4B by the unit select, the Not Write signal, and by the inward step inhibit at the Track 00 signal. Then, the step pulses go to the C inputs of the two (2) flip flops at IC 4C. The direction of the step, hence the selection of the flip flop to be toggled, is done by the two (2) exclusive OR gates of IC 5D. These gates are controlled by the step direction line and by the state of the two (2) flip flop outputs.

IC 3E, Pins 5 and 6, resets the two (2) flip flops after a Power On.

The output of the two (2) flip flops drives the stepper motor through the drivers of IC 4D. The diodes are for voltage spike elimination.

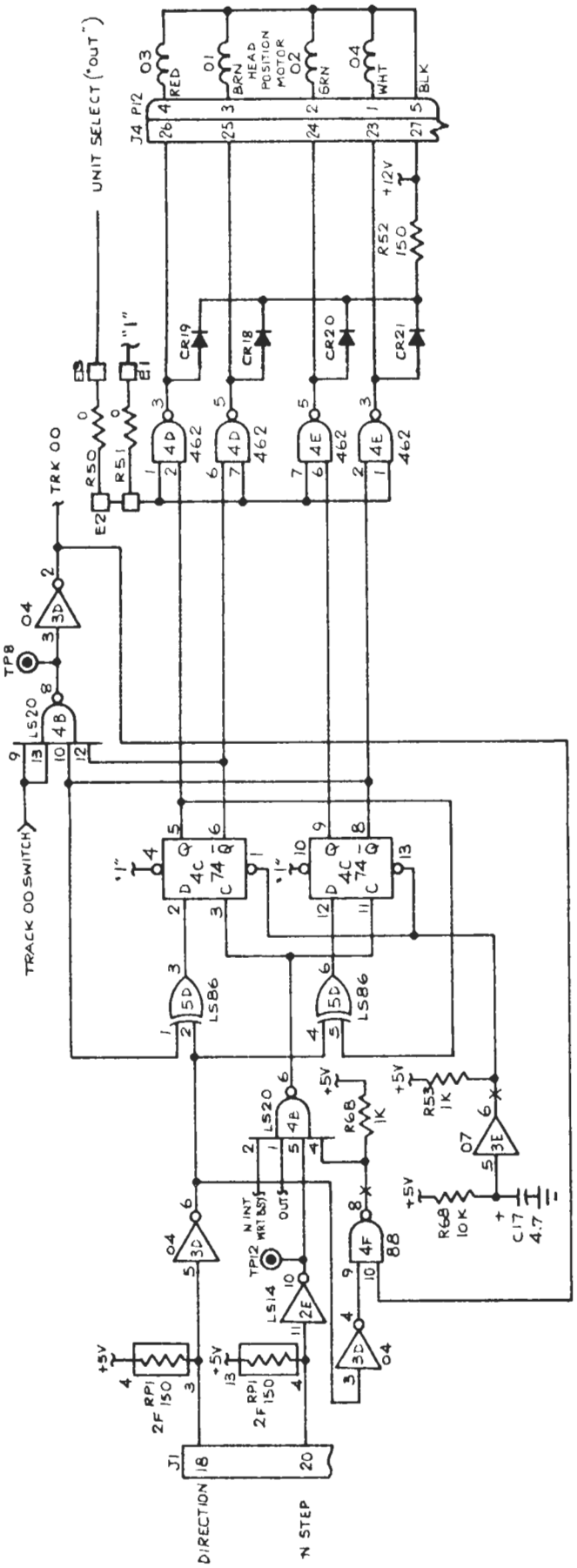


Figure 3-5
Direction and Step Lines Schematic Diagram

The disk drive is shipped with R50 in place and with R51 not in place. If the resistor is moved to position R51, the power is only on to the stepper motor when the disk drive is selected. 3.8 watts of power are saved because power is not applied to the stepper motor unless the disk drive is selected.

3.3.1.4 Write Enable (N WRITE ENABLE)

Functional Description

When the Write Enable signal is true (low), the write electronics are prepared for writing data (read electronics disabled). This signal turns on the write current in the read/write head. Data is written under control of the Write Data input line. It is generally recommended that changes of state on the Write Enable line occur before the first Write Data pulse. However, the separation between the leading edge of Write Enable and the first significant Write Data pulse should not be less than four (4) usec and not greater than eight (8) usec. The same restrictions exist for the relationship between the least significant Write Data pulse and the termination of the Write Enable signal. When the Write Enable line is false (high), all write electronics are disabled.

When a write-protected diskette is installed in the disk drive, the write electronics are disabled, irrespective of the state of the Write Enable line. Stepping is also disabled by a true (low) Write Enable (see Section 3.3.1.3).

Tandon Corporation recommends that the controller wait one (1) msec after the N WRITE ENABLE goes false before any step pulses are sent to the disk drive.

Circuit Description

The Write Gate signal comes in on Pin 24 of the interface connector. It is buffered through IC 3D, and gated at IC 3B by the Write Protect and the Unit Select signals, becoming the N WRITE signal. The N WRITE signal goes to Pin 9 of IC 3C, which is configured as a delay. The output at Pin 12 goes high 390 usec after the N WRITE signal goes true.

The N WRITE signal also goes to IC 3C, Pin 1, which is configured as a one-shot delay. The output at Pin 13 goes low only 900 usec after it stops getting pulses at Pin 2 (the pulse from the write data circuit), and the N WRITE goes high or false.

The N ERASE signal is gated through IC 3B. It is true 390 usec after a write true and 900 usec after a write false. This signal enables the erase driver IC 2C. R58 controls the erase current, which is approximately 80 mA.

Pin 4 of IC 3C is the Not Internal Write Busy signal. It enables Q5 through IC 3E, and gates twelve (12) volts to the selected head. This signal also disables the data output at IC 5E, Pin 11. The Not Internal Write Busy signal also enables the write flip flop IC 5C through IC 2E, Pin 12 and Pin 13.

Finally, the Not Internal Write Busy signal goes to driver 2B, Pin 10 and Pin 11, to disable the signal from the heads to the first-stage amplifier, using diodes CR11 and CR12 as gates.

3.3.1.5 Write Data (N WRITE DATA)

Functional Description

When the disk drive is selected, the write data line provides the bit-serial Write Data pulses that control the switching of the write current in the heads. The write electronics must be conditioned for writing by the Write Enable line (see Section 3.3.1.4).

For each high-to-low transition on the Write Data line, a flux change is produced at the head write gap. This causes a flux change to be stored on the disk drive. (See Figure 3-6.)

When the double-frequency type encoding technique is used (in which data and clock form the combined Write Data signal), it is recommended that the repetition of the high-to-low transitions, when writing all zeros, be equal to the nominal data rate ±0.1 percent. The repetition rate of the high-to-low transitions, when writing all ones, should be equal to twice the nominal data rate +0.1 percent. The data transfer rate is 125,000 Bits Per Second (BPS) at single density; it is 250,000 BPS at double density.

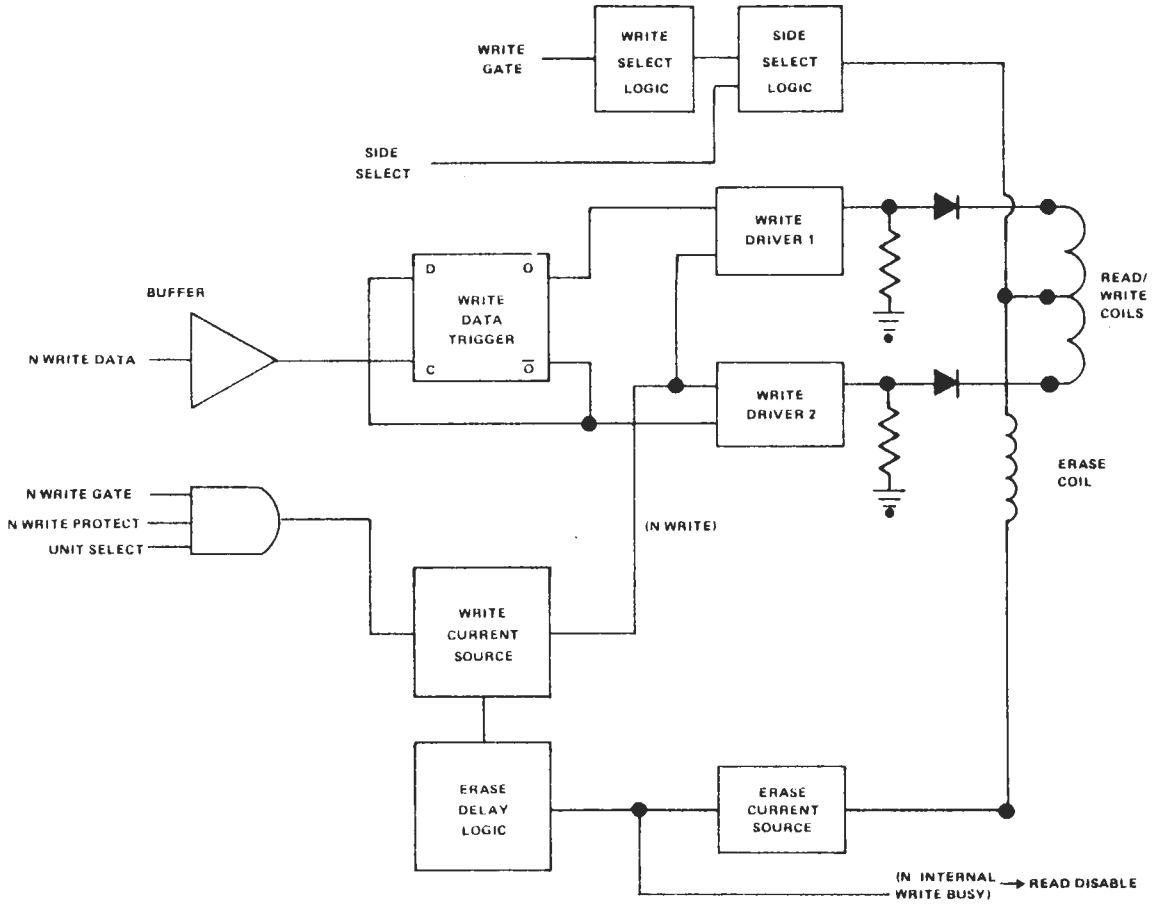


Figure 3-6
Write Data Circuit Block Diagram

Circuit Description

Data comes in on Pin 22 of the interface connector in pulse form. Subsequently it is buffered by IC 2E, then fed to a flip flop, IC 5C. The two outputs of the flip flop, through drive IC 2B, alternately turn on Q1 and Q2, which alternates the write current to the selected head. R31 controls the amount of write current. (See Figure 3-7.)

Q3 is activated by the write gate through IC 2B, IC 3B, and IC 3D (see Section 3.3.1.5).

Q4 is designed to allow write current to flow only after the five-volt line is high enough to forward-bias CR14, CR 15, and CR 16, which protects the disk from extraneous data being written when power is initially applied to the disk drive.

3.3.1.6 Side Select (N SIDE SELECT)

Functional Description

When the Side Select signal is true (low), Side 1 of the disk drive is selected for read/write operations. When this signal is false (high), Side 0 of the disk drive is selected (see Figure 3-10). The Side Select signal must be stable during an entire read or write operation. This signal is best implemented in synchronization with the Device Select line signal (see Section 3.3.1.1).

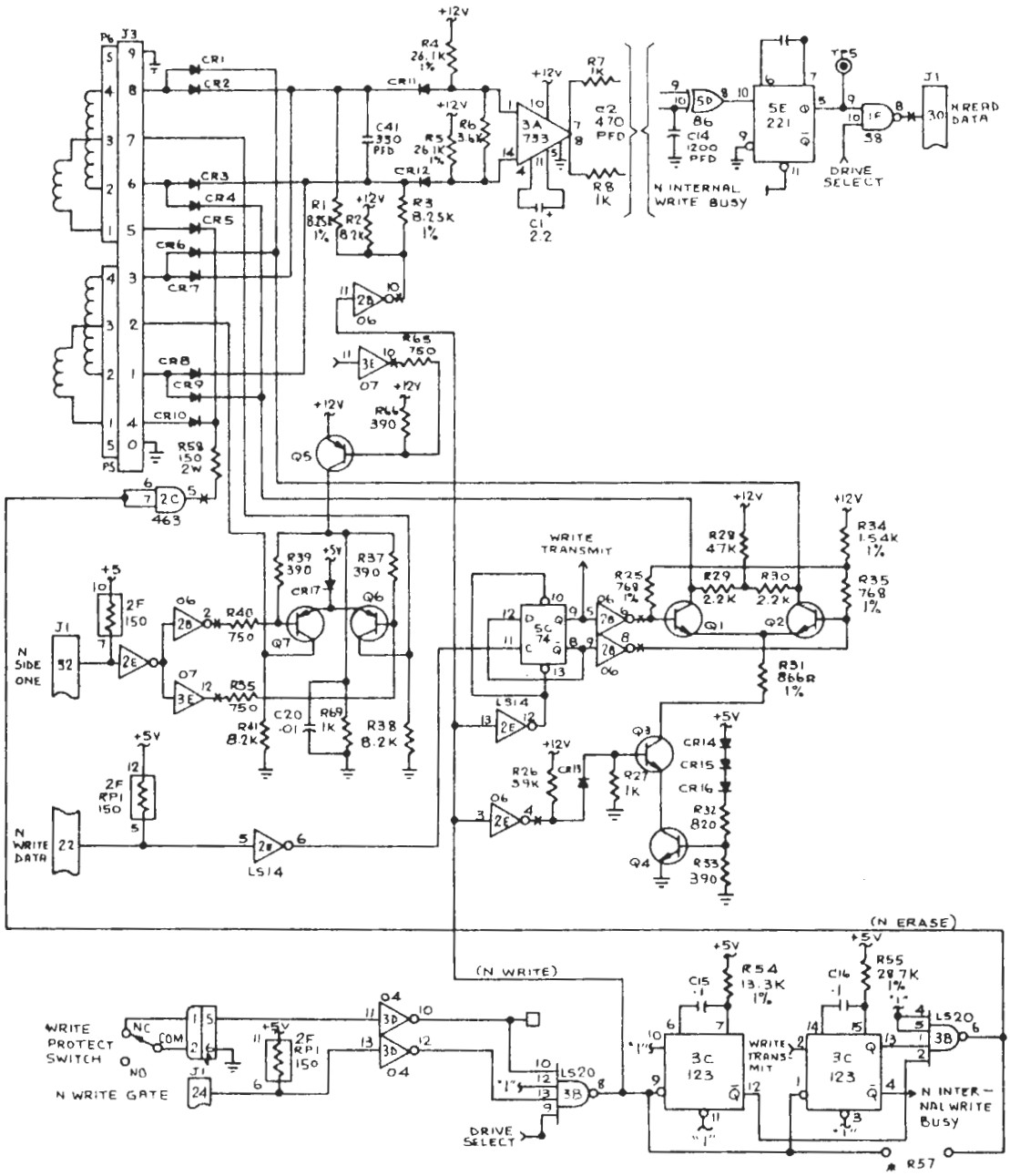


Figure 3-7
Write Data Schematic Diagram

Circuit Description

The Side Select signal comes in on Pin 32 of the interface connector. If this signal is high, Side 0 is selected. This signal is buffered through IC 2E (see Figure 3-8). From there, the Side Select signal is sent through IC 2B and IC 3E to Drive Q7 or Drive Q6. Drive Q7 sends current to the upper head (Head 1). Drive Q6 sends current to the lower head (Head 0).

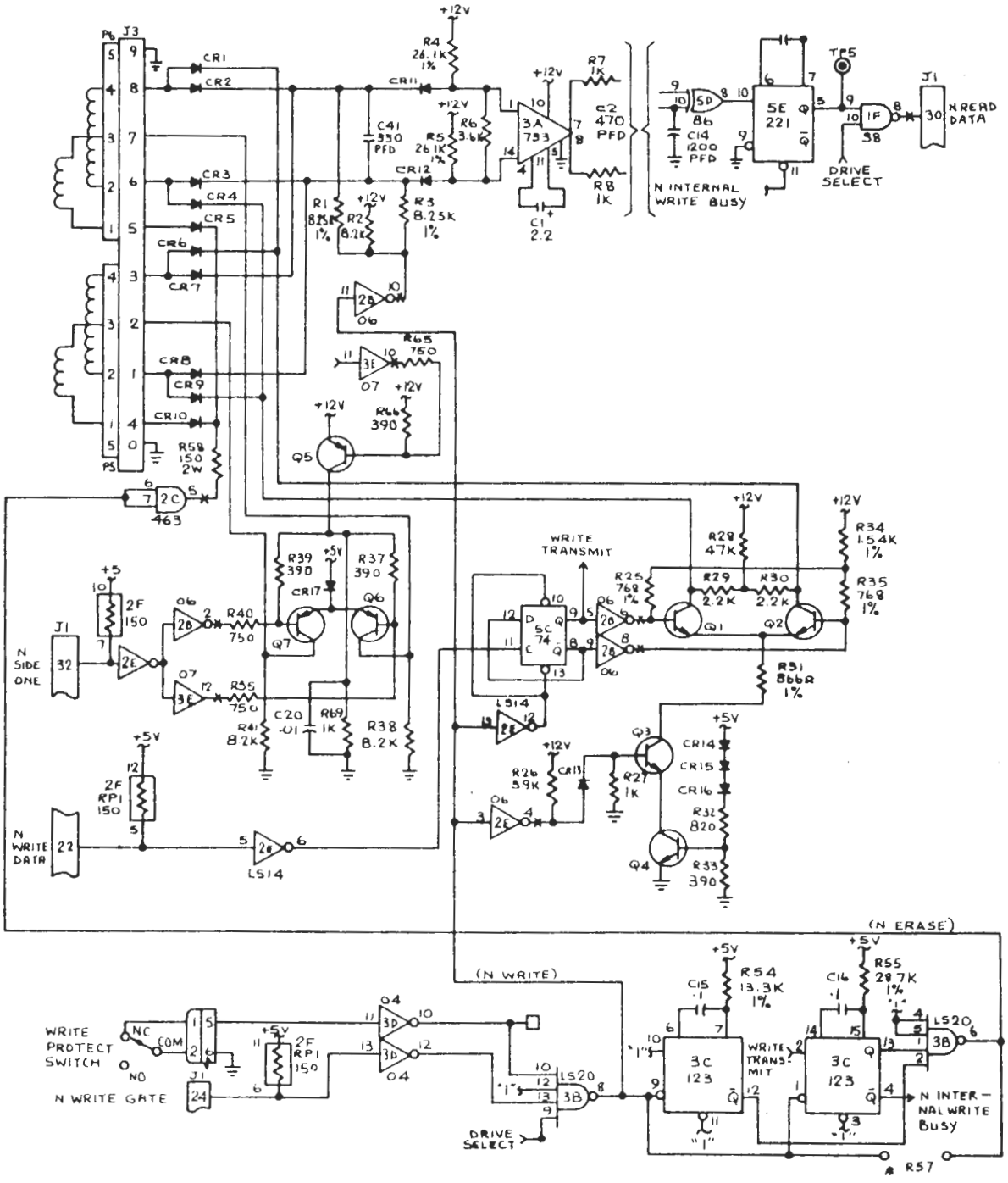


Figure 3-8
Side Select Schematic Diagram

3.3.2 Outputs

3.3.2.1 Index (N INDEX/SECTOR)

Functional Description

The Index signal is provided once each revolution (200 msec, nominal) to indicate the beginning of a track to the controller. The Index line remains in the true (low) state for the duration of the Index pulse. The duration of an Index pulse is nominally 4.0 msec.

The leading edge of an Index pulse must always be used to ensure diskette interchangeability between disk drives.

With a standard, soft-sectored diskette installed, Test Point 7 (see Figure 3-9 and Figure 3-10) is a high going pulse, nominally 4.5 msec in duration, every 200 msec.

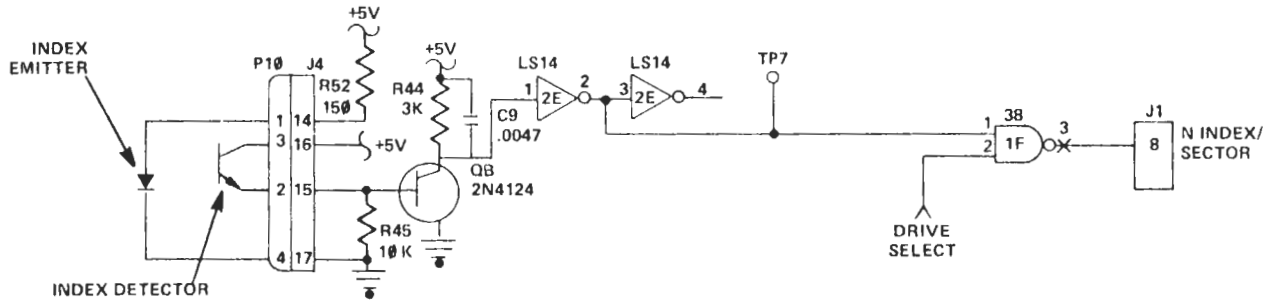


Figure 3-9
Index Schematic Diagram

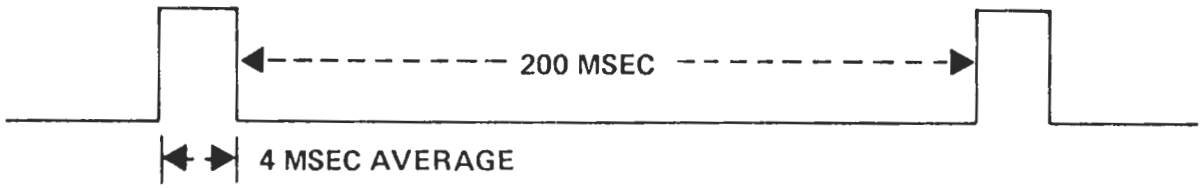


Figure 3-10
Waveform at Test Point 7 (Soft Sectored)

Circuit Description

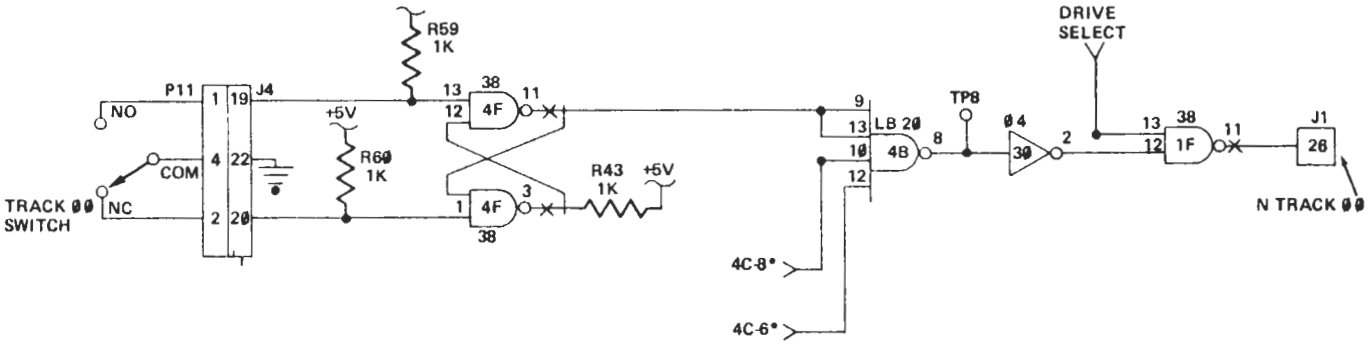
The Index signal from the disk drive comes in on J4, Pin 15. The Index signal is derived from an infrared LED and a photo-transistor detector. When the index hole in the disk drive allows the light to turn on the detector, Q8 is turned on, sending a signal through IC 2E to IC 1F to be gated by the Drive Select signal to produce a low output at Pin 8 of the interface connector.

3.3.2.2 Track 00 (N TRK 00)

Functional Description

When the disk drive is selected, the Track 00 Interface signal indicates, to the controller, that the read/write head is positioned at Track 00. The Track 00 signal remains true (low) until the head is moved away from Track 00. The Track 00 switch usually is deactivated between Track 1 and Track 2.

Test Point 8 (see Figure 3-11) is true (low) when the carriage is positioned at Track 00 and the Step Motor phase is correct.



*4C-8 and 4C-6 are high on Phase 0 only.

Figure 3-11
Track 00 Schematic Diagram

Circuit Description

The Track 00 switch is internal to the disk drive. Its signal comes in on Connector 11. 4F is a latch that debounces the switch noise. The Track 00 switch is activated between Track 00 and Track 3. The combination of the Track 00 switch being activated and the proper stepping motor phase (Phase 0), produces all "high" signals at IC 4B, Pins 9, 10, 12, and 13. This signal subsequently is buffered through IC 3D, Pin 1 and Pin 2. IC 1F Pins 11, 12, and 13 gate the Track 00 output with the disk drive select output, to give a Track 00 output to the controller at Pin 26 of the interface connector.

3.3.2.3 Write Protect (N WRITE PROTECT)

Functional Description

When the disk drive is selected and the diskette is write protected, the Write Protect signal line logic level goes true (low). The write electronics are internally disabled when the diskette is write protected.

It is recommended that the Write data line be inactive whenever Write Enable is false, i.e., in a Read state, J1, Pin 24.

When the level on this line is false (high), the write electronics are enabled and the write operation can be performed. It is recommended that the controller not issue a Write command when the Write Protect signal is true (low).

When a write protected diskette is installed in the disk drive, Test Point 9 (see Figure 3-12) is high.

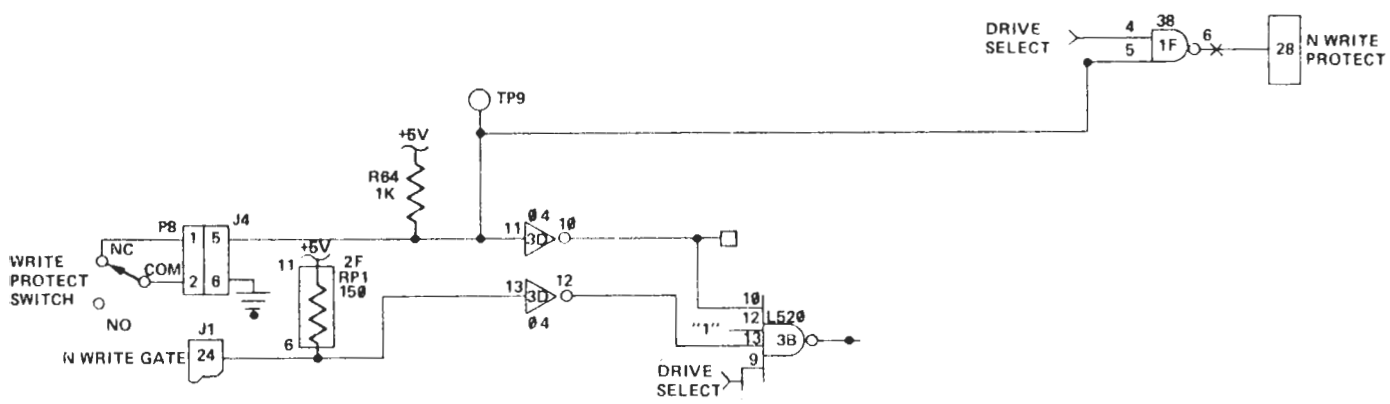


Figure 3-12
Write Protect Schematic Diagram

Circuit Description

The Write Protect signal comes in at Connector 8. Test Point 9 is held low when the switch is closed by a non-write protected diskette. The Write Protect output at Pin 28 of the interface is enabled at IC1F, Pins 4, 5, and 6, by the Drive Select signal.

3.3.2.4 Read Data (N READ DATA)

Functional Description

The Read Data interface line transmits the readback data to the controller when the disk drive is selected. It provides a pulse for each flux transition recorded on the media. The Read Data output line goes true (low) for a duration of one (1) usec for each flux change recorded.

The leading edge of the Read Data output pulse represents the true positions for the flux transitions on the diskette surface.

Test Point 1 and Test Point 2 (see Figure 3-13) are provided to observe the differential output of the first stage of Read signal amplification. Test Point 3 and Test Point 4 are provided to observe the differential output of the second stage amplifier and differentiated Read signal. Test Point 5 is the output of the single shot used in the Read section, nominally 1.0 usec for each flux transition detected. Test Point 10 is signal ground.

Circuit Description

The read signal comes from the selected head on the disk drive. It is gated to the first amplifier (IC 3A) by the N WRITE signal to IC 2B, Pin 11 and Pin 10, which forward-biases diodes CR11 and CR12. Then the Read signal passes through C2, L1, L2, C3, C4, and C5, which is a bandpass filter. The Read signal is then at the input IC 4A, the differentiator, which is also Test Point 1 and Test Point 2.

The output of IC 4A goes through DC blocking capacitors C7 and C8 to the crossover detector, IC 5B, which digitizes the AC signal. This puts the signal into a standard TTL format. IC's 5D, 5E, and 5C comprise a comparator circuit. Any pulses that occur outside of the normal duty cycle of IC 5B are eliminated. IC 5D is an edge detector. IC 5E acts as a one-shot. IC 5C is the actual comparator.

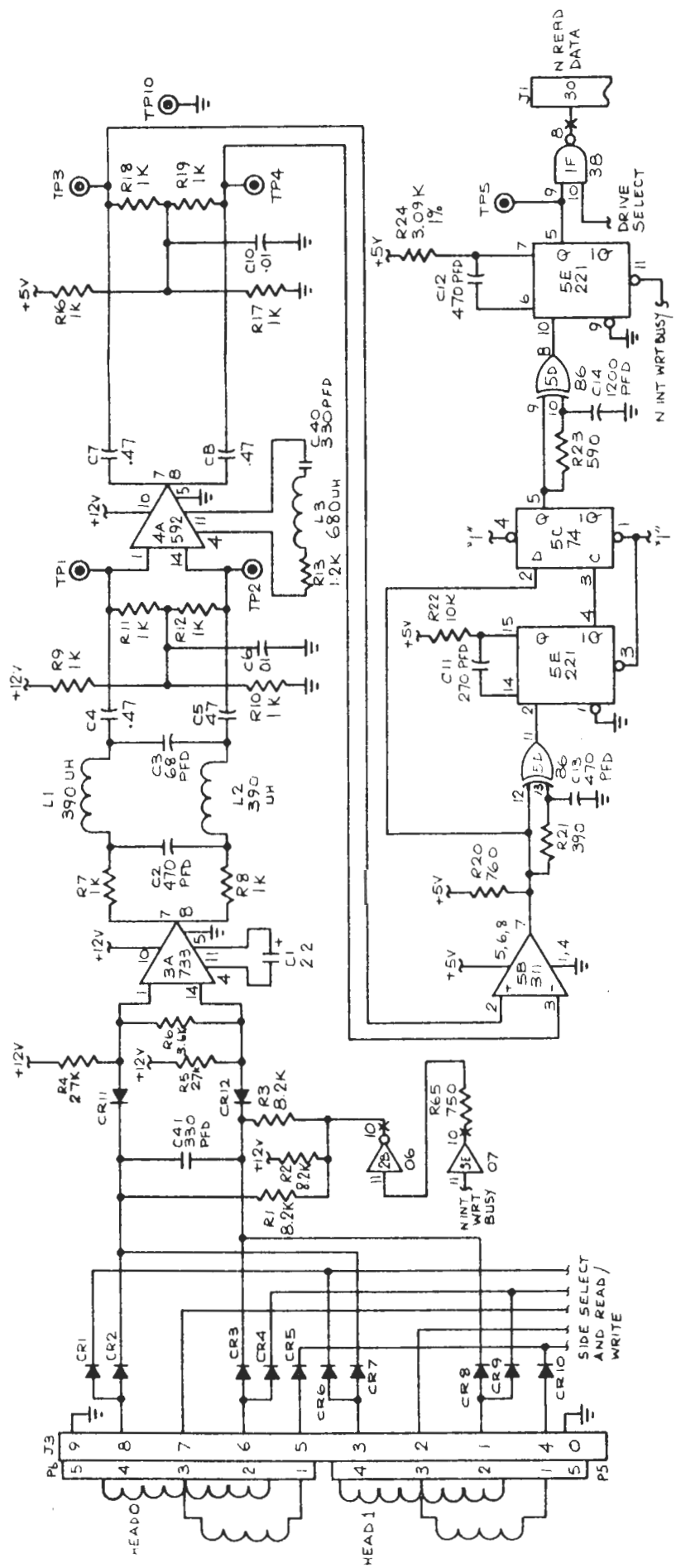


Figure 3-13
Read Data Schematic Diagram

The Read signal is presented to IC 5D, which is another edge detector, and then goes to IC 5E, where the pulses are shaped to 1 usec. This output is gated at IC 1F with the Unit Select signal to produce a digital output at Pin 30 of the interface connector (see Figure 3-14).

NOTE

IC 5E, the final one shot, is enabled only when the disk drive is in a Read state (Pin 11).

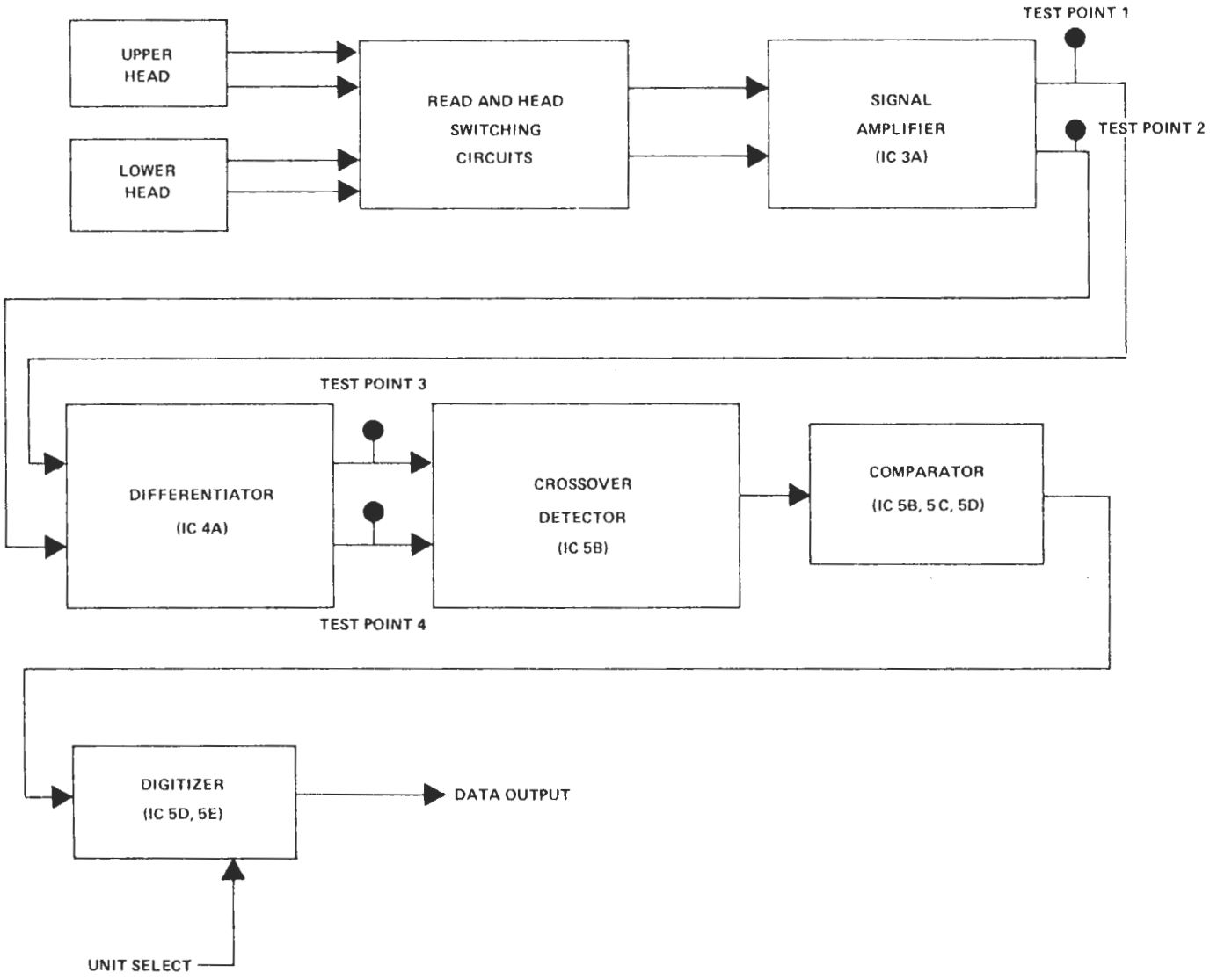


Figure 3-14
Read Circuit Block Diagram

3.4 PHYSICAL DESCRIPTION OF THE SERVO PCBA

The Servo PCBA is approximately 127 mm (5.0 inches) long by 38 mm (1.5 inches) wide. Figure 3-15 illustrates the placement of test points and connectors.

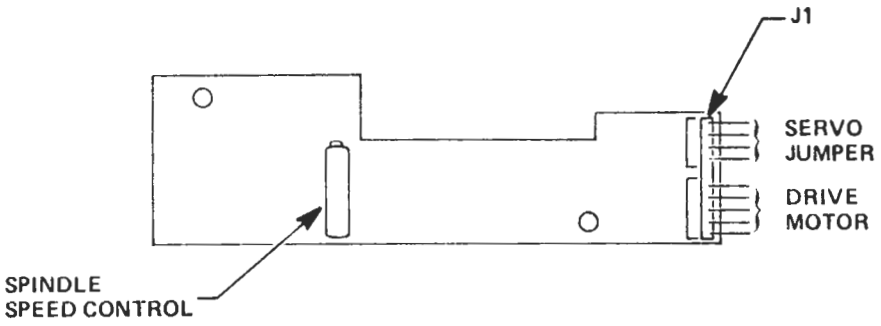


Figure 3-15
Servo PCBA

3.4.1 Input Control Lines

Functional Description

When the logic board receives a true (low) Motor On signal, a true (low) signal is sent to the servo board (N MOTOR ON) (see Figure 3-16). This signal turns on the regulator (Q1), and the motor's speed accelerates to 300 rpm (± 1.5%).

R4 is adjusted for a motor speed of 300 rpm.

The motor supplies a 12-volt AC tachometer signal to the servo board for regulation control.

Circuit Description

The Motor On signal comes in at Pin 7 of the servo board (see Section 3.3.1.2). This turns off Q2, allowing the signal to be sent to the base of Q1. The signal to the base of Q1 is the output of the regulator IC Pin 8. This is controlled by the tach input at Pin 1 and Pin 2 of the servo board. The tach signal is an AC signal of twelve (12) volts. The other input to the regulator is from the voltage divider R3, R4, and R5. This voltage is adjustable by R4, a potentiometer, to produce the proper amount of current through Q1 to the drive motor.

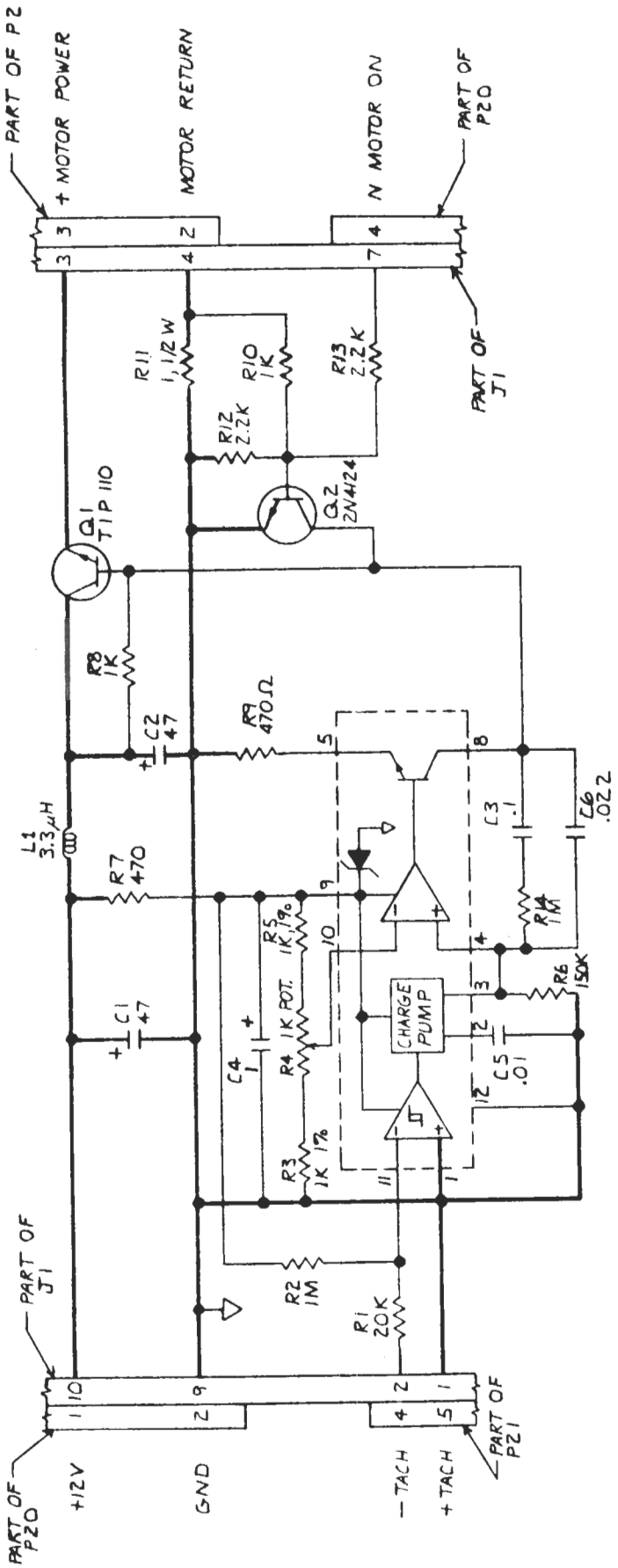
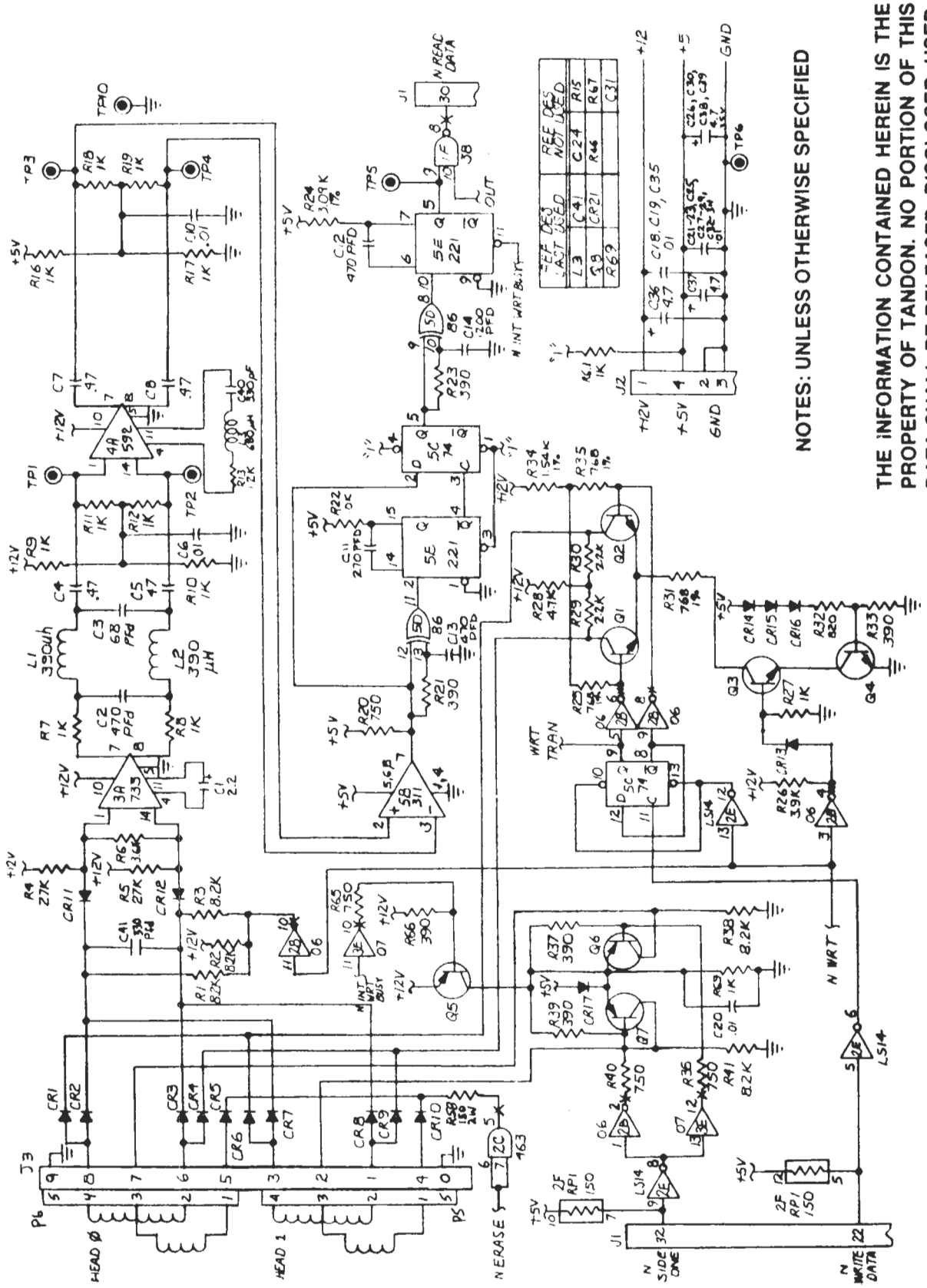


Figure 3-16
Servo Board Schematic Diagram

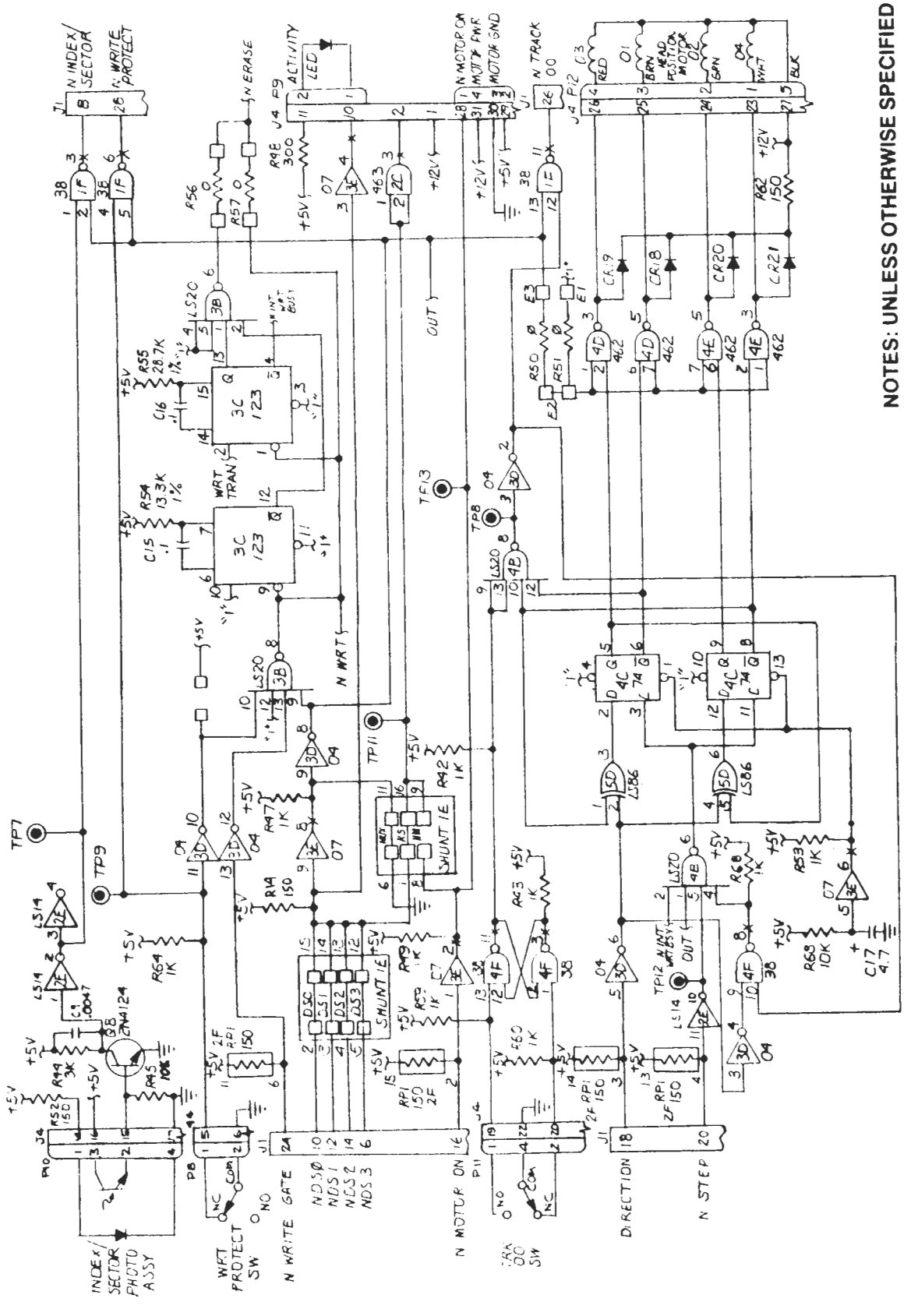
NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE IN OHMS, ±5%, 1/4 W.
2. 1% RESISTORS ARE 1/8 W.
3. CAPACITORS ARE IN uF, ±20%, 35V.



LOGIC SCHEMATIC

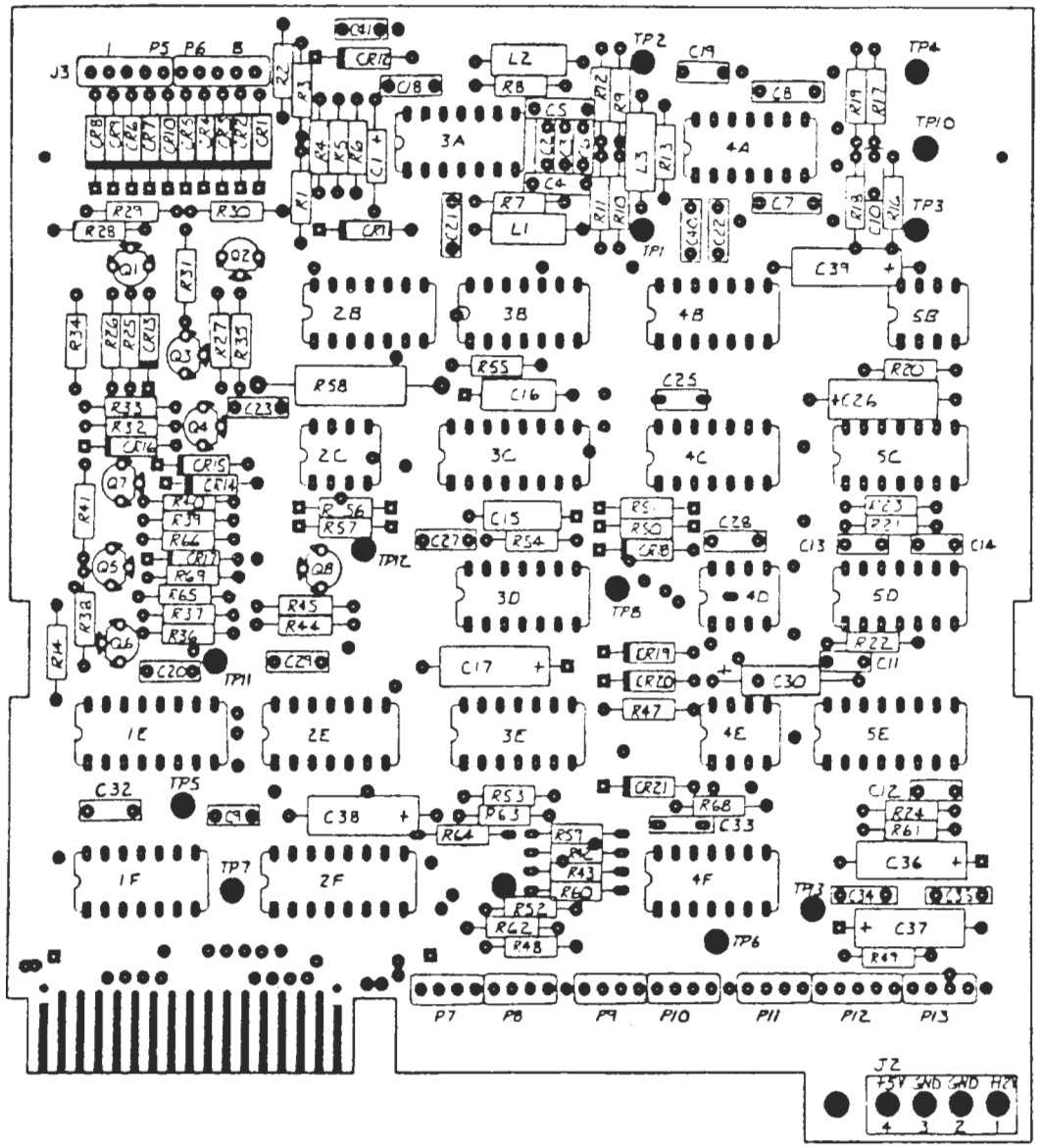
NOTES: UNLESS OTHERWISE SPECIFIED



LOGIC SCHEMATIC

NOTES: UNLESS OTHERWISE SPECIFIED

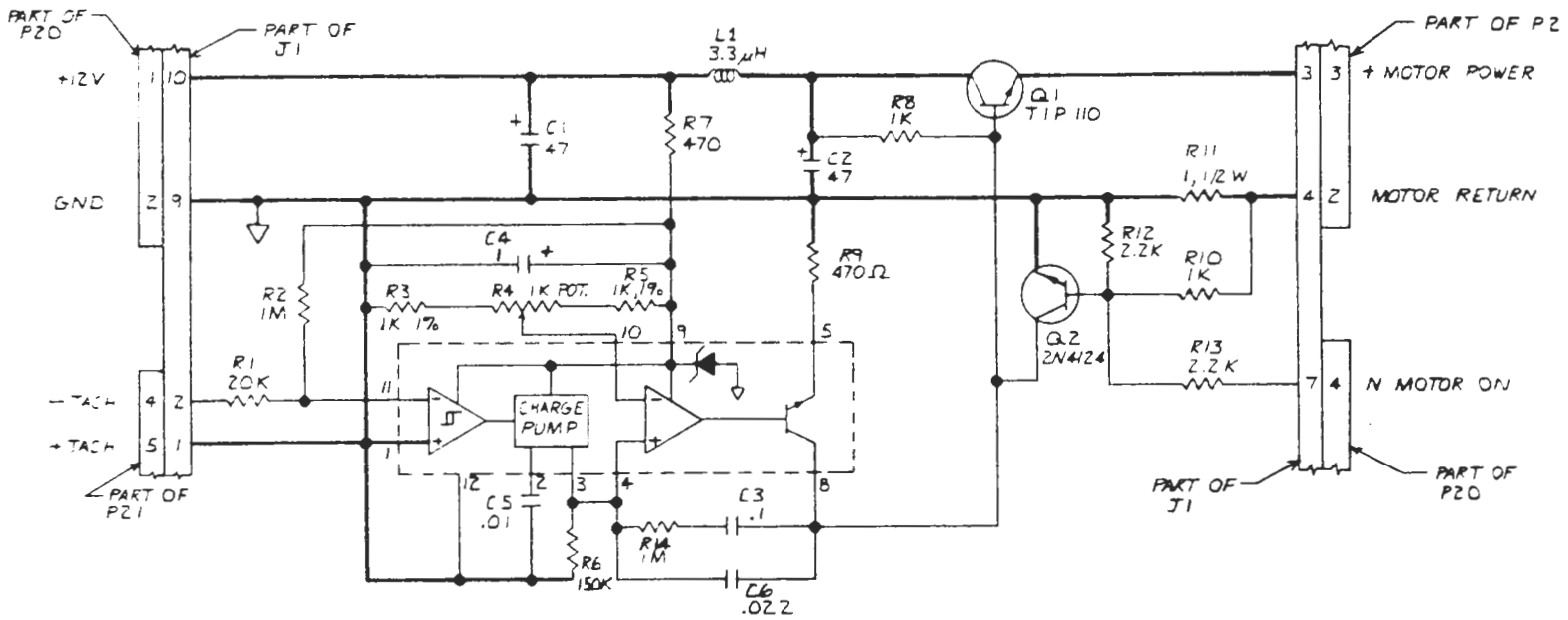
1. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%
2. ALL CAPS ARE IN uFD.
3. ALL DIODES ARE IN 4446.
4. ALL TRANSISTORS NPN ARE 2n4124 & PNP ARE 2N4125.



NOTES: UNLESS OTHERWISE SPECIFIED

1. COMPONENT HEIGHT NOT TO EXCEED .35 ABOVE P.C. BOARD.

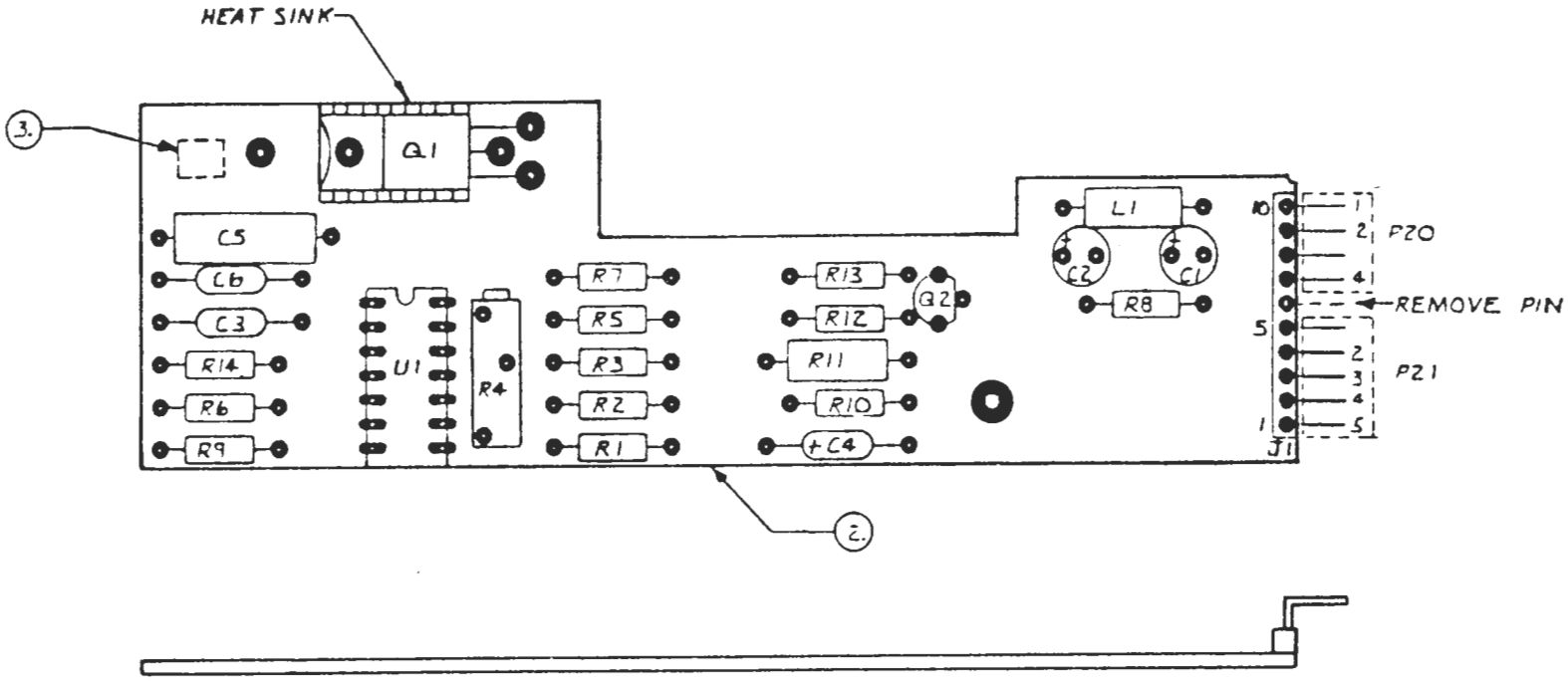
LOGIC PCBA ASSEMBLY DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED

1. **RESISTORS ARE IN OHMS, ±5%, 1/4 W.**
2. **1% RESISTORS ARE 1/8 W.**
3. **CAPACITORS ARE IN uF, ±20%, 35 V.**

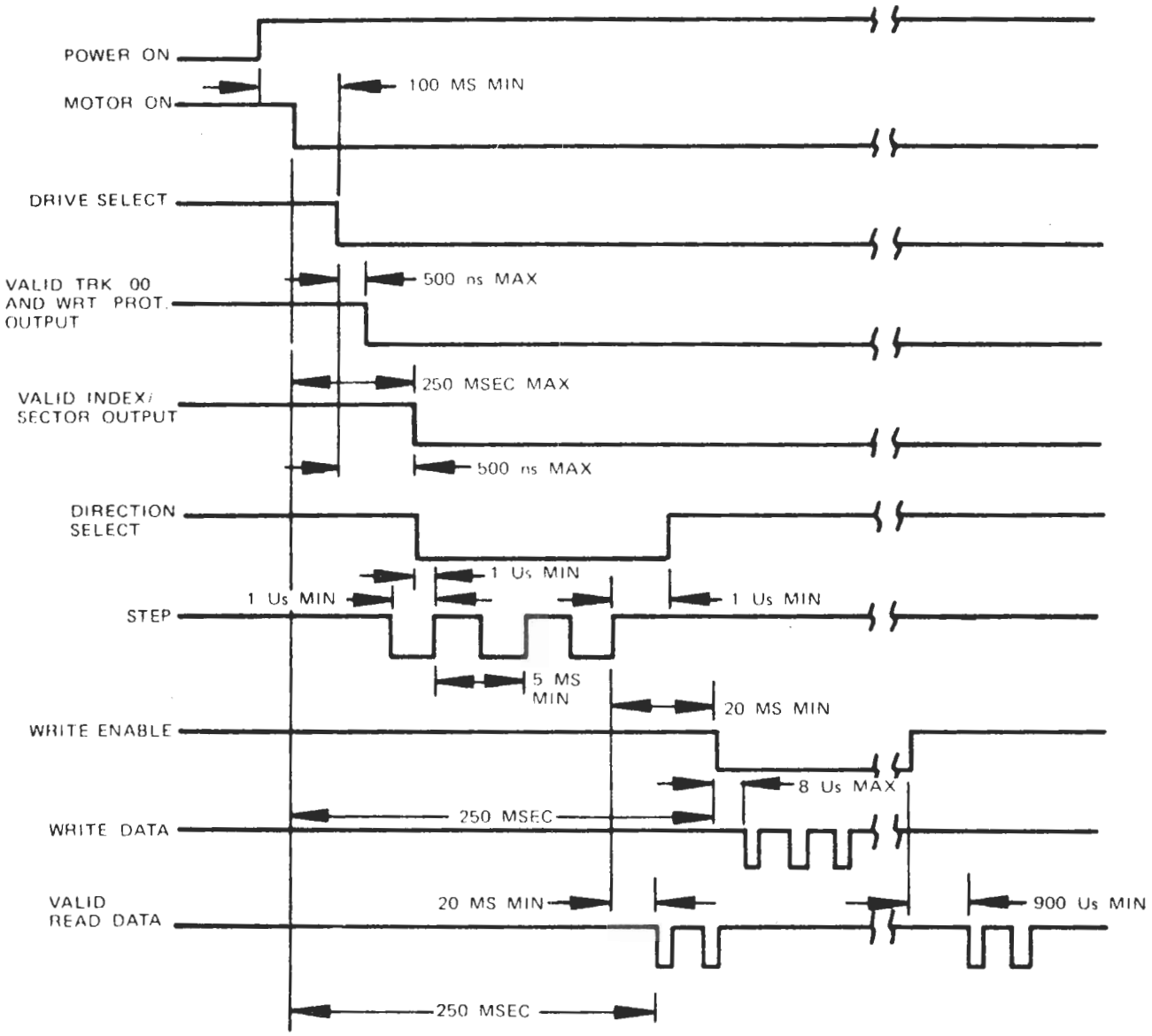
SERVO PCBA, LINEAR



NOTES: UNLESS OTHERWISE SPECIFIED

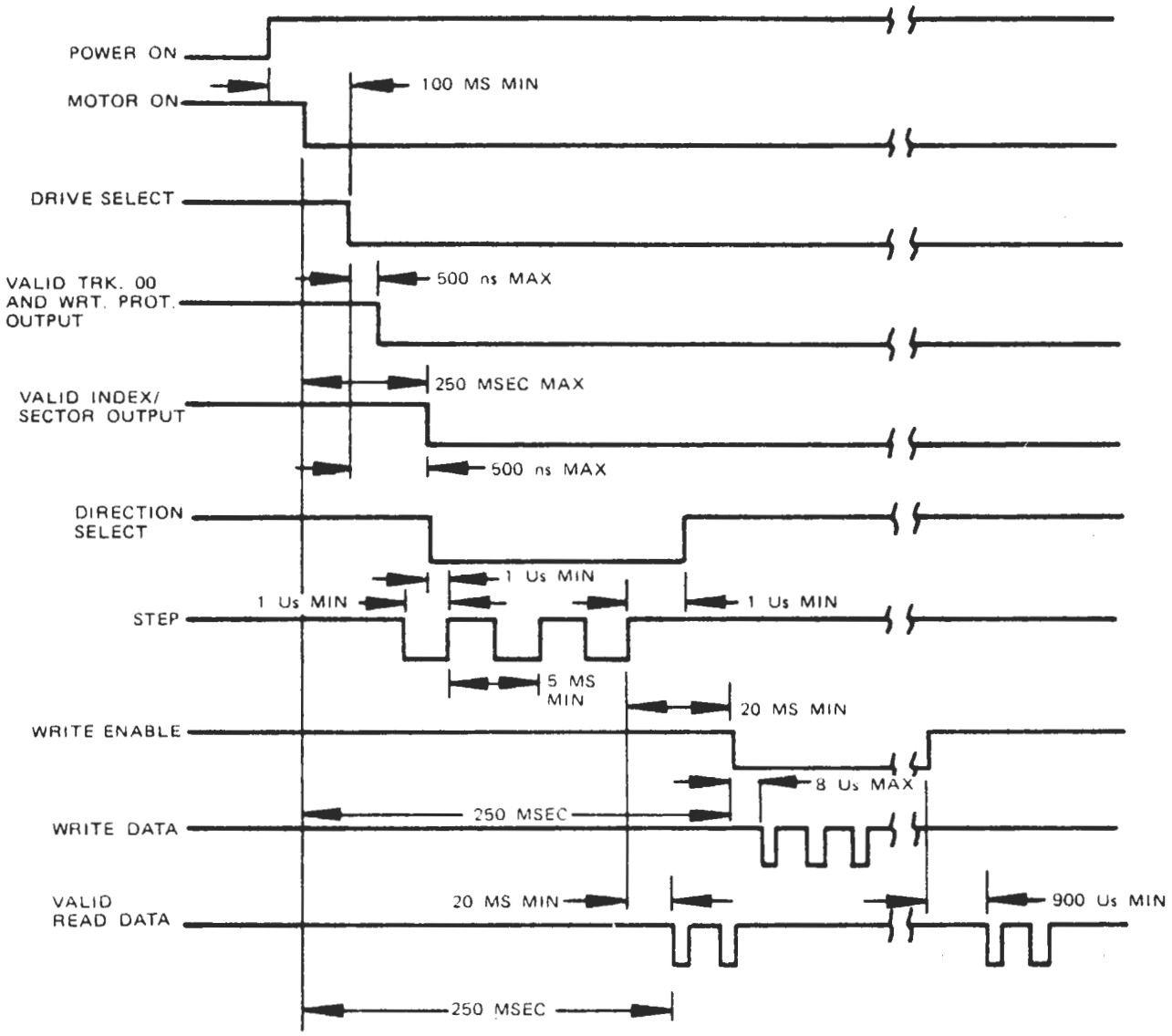
1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.
2. THIS ASSEMBLY SHALL BE MADE FROM PCB DETAIL 178901-001, REVISION A.

SERVO PCBA, LINEAR



MODEL TM-100 GENERAL CONTROL AND DATA TIMING REQUIREMENTS

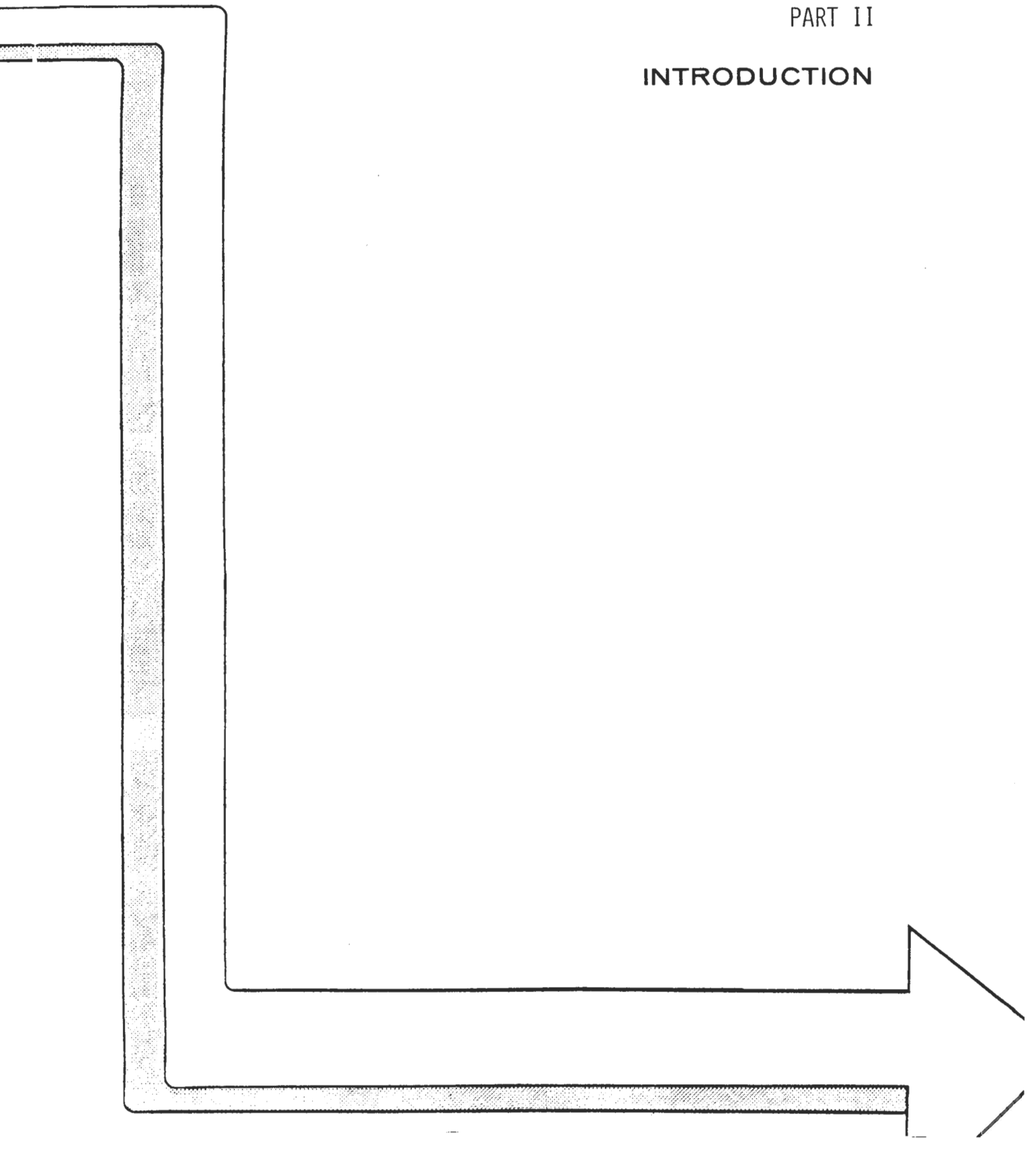
MODEL TM-100-1
PRODUCT SPEC.
MINI SINGLE-SIDED RECORDING
FLEXIBLE DISK DRIVE



MODEL TM-100 GENERAL CONTROL AND DATA TIMING REQUIREMENTS

PART II

INTRODUCTION



The H-207 is a floppy disk controller board. It functions as an intelligent interface between the CPU and the disk drives. The H-207 selects the correct drive in a multi-drive system and properly handles data transfer to and from the disk drives.

The H-207 operates as a slave processor. This means the disk controller board contains its own processor which is controlled by the master CPU. Thus, the disk controller board takes commands from the master CPU and converts them into the necessary signals required to control the drives. This type of system allows the master CPU to do other tasks while the disk controller board processor actually does the work of controlling the disk drives.

The H-207 is versatile. It can support up to four 5-1/4" and four 8" disk drives. User software selects the type of drive used and the density of the media. However, present Heath Company software limits the number of drives to three.

The H-207 can be operated in three different modes; Wait State, Polled I/O, or Interrupt. This allows the disk controller board to support almost all available soft-sectored disk formats. By using the Wait State mode, the board can be jumpered to operate at speeds up to 6 MHz.

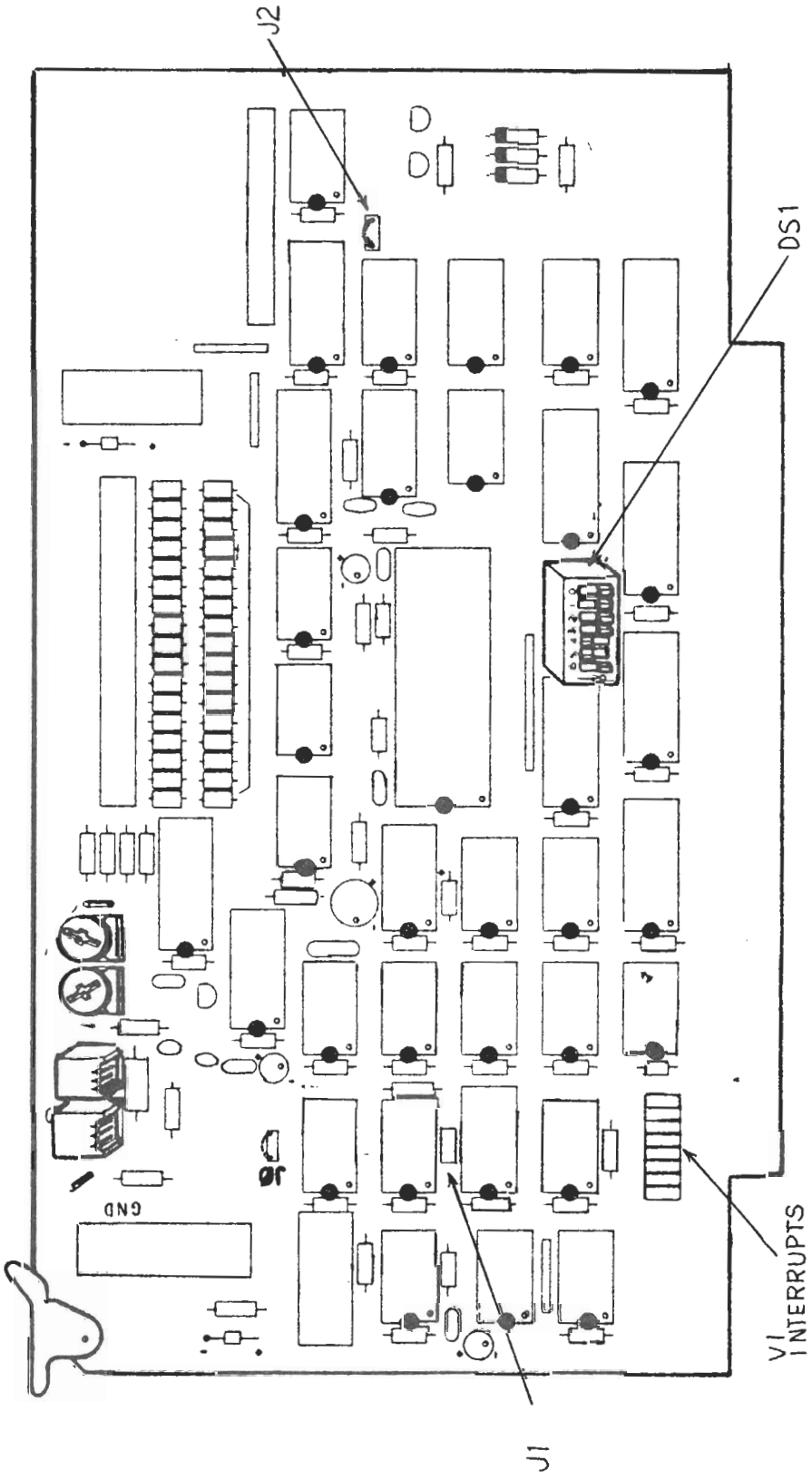
Because the H-207 is a IEEE 696 Standard S-100 compatible card, it can be installed in other makes of computers using the IEEE Standard. Additional features that make the controller board acceptable to other computers are: user selectable addressing, software controllable formatting, Shugart compatible 8" interface, and adjustable precompensation.

The information provided in this section of the manual will familiarize you with the operation and troubleshooting of the H-207. Using this information, you will be able to troubleshoot the disk controller board to the component level.

SPECIFICATIONS

Type	WD1797.
Drives Supported	Up to four each.
5-1/4"	Single/double-sided, 48/96 TPI, single/double density.
Capacity (formatted) ...	80K, 160K, 320K, or 640K; depending on the number of sides and density.
Track Format	4K, eight sectors of 512 bytes each.
Stepping Speed	6 milliseconds per track or faster.
8"	Single/double-sided, single/double density.
Interface type	Shugart 850 or equivalent.
Data Separator	Phase-locked loop.
Precompensation	Variable independently for both 5-1/4" and 8" sizes.
Data Transfer	Programmed using wait states, interrupt or polling.

OPERATION



H-207 CONTROLLER BOARD

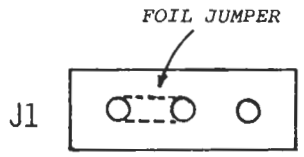
JUMPER AND SWITCH LOCATIONS

INTRODUCTION

To permit the H-207 to operate in many different types of computers, a number of jumpers and a slide switch are incorporated into the design of the board. These devices permit configuring the controller board for the computer environment in which the H-207 is installed. There are three main areas of concern: clock speed jumpering, selection of interrupt jumpers and the setting of the slide switch, DS1. Refer to the pictorial on the adjacent page for the location of the jumpers and the slide switch.

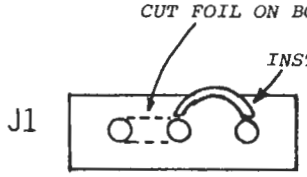
CLOCK SPEED

The host computer clock speed that the H-207 will operate with is determined by the jumpering at J1. As received, J1 is jumpered by a foil run on the bottom of the board. (See illustration below.) This jumpering enables the H-207 to operate in computers that have a CPU clock speed faster than 3 MHz. This jumpering is normal when the H-207 is installed in a H/Z-100.



J1 set for H/Z-100 Computer operation or for CPU clock speeds faster than 3 MHz.

For the H-207 to operate in a computer that has a CPU clock speed at or slower than 3 MHz, the jumpering of J1 must be altered. This is accomplished by cutting the foil jumper on the bottom of the circuit board and installing a 1" wire jumper from the middle hole of J1 to the rightmost hole. Refer to the illustration below when performing this alteration.



J1 setting for 3 MHz or slower CPU clock speed.

INTERRUPT JUMPERS

The Vectored Interrupt jumper locations, VI, are located on the lower left-hand corner of the controller board. The data request line, DRQ, from the 1797 is connected to holes J3 through J10 shown in the illustration below. The center row of holes numerically correspond with the S-100 interrupt lines VI0 through VI7. The interrupt request line, IRQ, from the 1797 is connected to holes 0 through 7. When jumpered, these locations route IRQ and/or DRQ from the 1797 controller to the S-100 interrupt lines.

No jumpers are installed in these locations when the H-207 is used in a H/Z-100. These jumper locations are only used when the H-207 is installed in computers that require interrupt protocol. The configuration of the jumpers is determined by the customer's computer documentation.

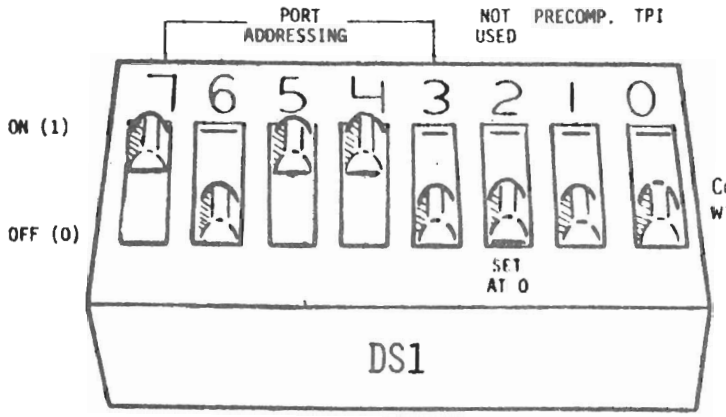
VI

VECTOR INTERRUPT JUMPER LOCATIONS
(No jumpers are installed for H/Z-100 operation.)

J3	J4	J5	J6	J7	J8	J9	J10	
0	0	0	0	0	0	0	0	← DRQ
0	0	0	0	0	0	0	0	← VIØ-VI7
0	0	0	0	0	0	0	0	
Ø	1	2	3	4	5	6	7	← IRQ

SLIDE SWITCH (DS1)

DS1, an 8-section slide switch, determines the port address and the condition of bits 3 and 4 of the status port. The sections of DS1 are defined as follows:



Configured for an H/Z-100 Computer with 48 TPI, 5-1/4" Drives

DS1

HEATH SOFTWARE DEFINED		HARDWARE DEFINED	
Section	Definition	Section	Definition
0	This bit determines the TPI of the 5-1/4" disk drive. 0 = 48 TPI. 1 = 96 TPI.	0	Status port bit 4.
		1	Status port bit 3.
		2	Not used. Leave at 0.
		3-4-5-6-7	Port addressing (MSB).
1	This bit determines whether precomp is on or off. 0 = precomp off. 1 = precomp on.		
2	Not used.		
3-4-5-6-7	Port addressing.		

The H-207 occupies a block of eight contiguous I/O port addresses. The three low-order bits in this block select 1797 registers, the control latch, or the status port. The H/Z-100 computer series place the H-207 at port address B0H. A map of the I/O port is shown below.

I/O ADDR. (Binary)	READ	WRITE	PORT DESIGNATION
SSSSS000*	•		1797 Status Register
SSSSS000		•	1797 Command Register
SSSSS001	•	•	1797 Track Register
SSSSS010	•	•	1797 Sector Register
SSSSS011	•	•	1797 Data Register
SSSSS100		•	Control Latch
SSSSS101	•		Status Port

* S = dip switch bit

The dip switch bits are simply defined from the binary equivalent of the switches. For example, the port address for the H/Z-100 is shown below.

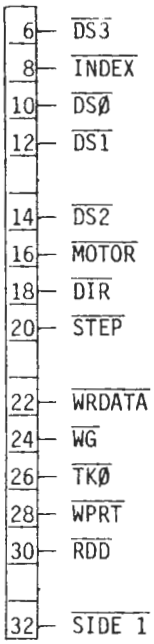
SSSSSXXX** = 10110XXX = Port B0 - B7.

** X = 1797 register, control latch, or status port.

OUTPUT CONNECTORS

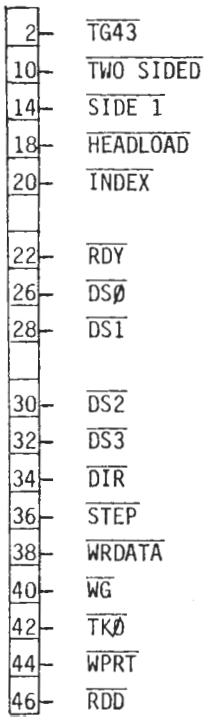
5" DISK DRIVE CONNECTOR (P2)

This 34-pin connector provides the necessary signals to drive a 5-1/4" disk drive. Refer to the pictorial at the left for a description of the pinouts of this connector. All numbered pins are grounded.

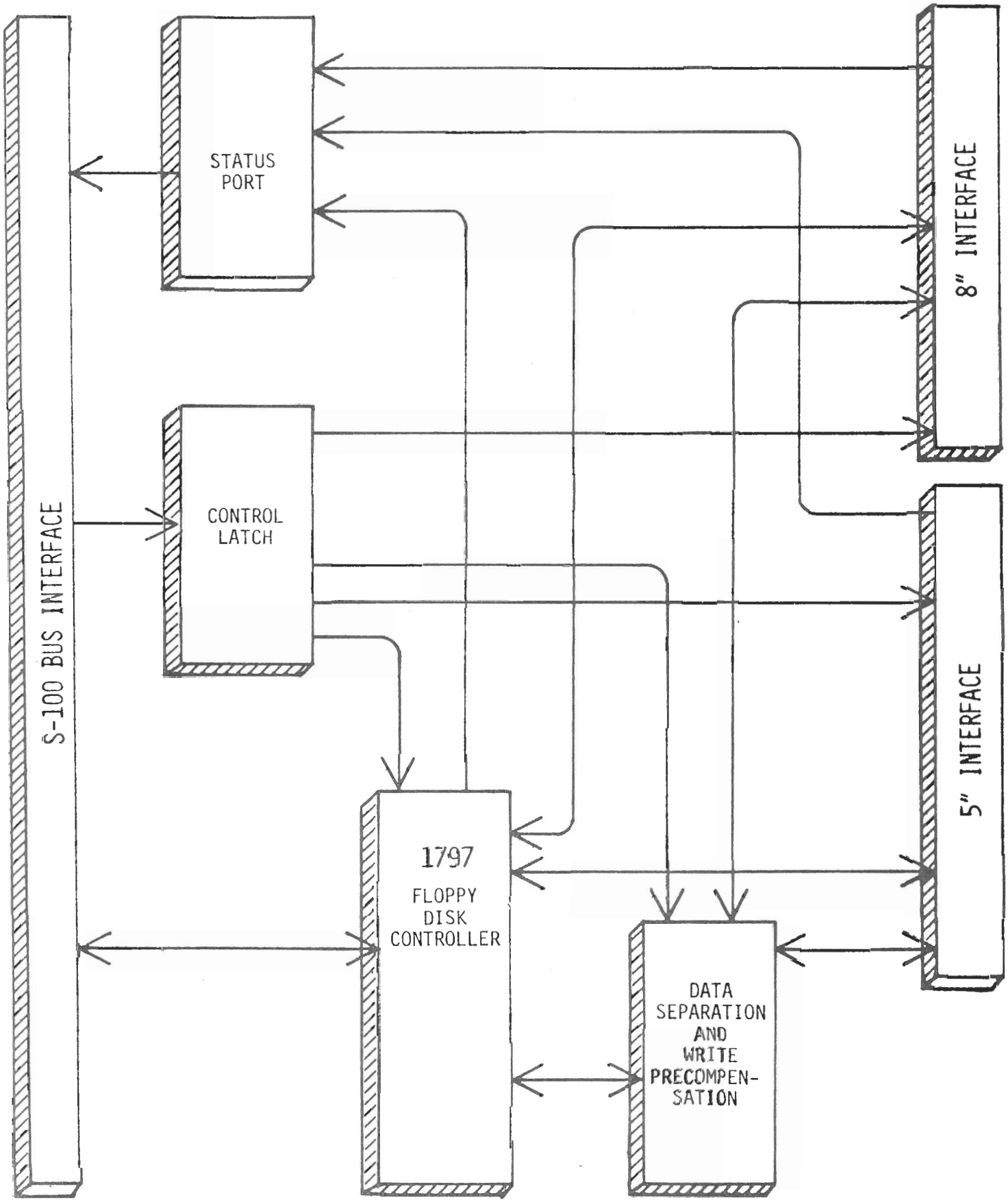


8" DISK DRIVE CONNECTOR (P1)

This 50-pin connector provides the necessary signals to drive an 8" Shugart compatible disk drive. Refer to the pictorial at the left for a description of the pinouts of this connector. All odd numbers pins are grounded.



CIRCUIT DESCRIPTION



H-207 BLOCK DIAGRAM

BLOCK DIAGRAM DESCRIPTION

Refer to the H-207 block diagram as you read the following.

The H-207 Floppy Disk controller board consists of seven major sections: the bus interface, the status port, the control latch, the 1797 floppy disk controller, the data separation & write precompensation circuits, and the two drive interfaces.

The bus interface is made up of two octal bus buffers, an octal tri-state latch, an address comparator, and some miscellaneous enabling circuitry. These components interface the H-207 to the S-100 bus in the H/Z-100.

The status port is a read-only device that tells the CPU the status of the disk drives and the controller. This includes track density, number of recording sides to the disk, and if precompensation is being used.

The control latch accepts commands to the disk drives such as DRIVE SELECT, 5" FASTEP, and others that have to do with the selection and mode of the drives.

The 1797 controller controls the placement of information on the diskette. That is, the movement of the drive head, the formation of written data, and the separation of the read data is controlled by the 1797.

The data separation and write precompensation circuitry control how the data is read to or written from the diskette. It does this by separating the data from the clock signal during read operations and precompensating data during the double-density write operations.

The 8" and 5.25" drive interfaces include buffers and filter circuitry. Up to four drives can be connected to each interface.

DETAILED CIRCUIT DESCRIPTION

S-100 BUS INTERFACE

The S-100 Bus Interface is compatible with any IEEE 696-standard S-100 Bus. See the S-100 specification sheets in the appendices of this manual for definitions of the lines.

DATA IN

Data into the bus (out from the controller board) travels through signal lines 91-95 and signal lines 41-43 on the bus interface. These pins are used in read operations from the status latch or from the 1797 controller. The data is buffered from the board's internal data bus to the S-100 bus by means of U36, a 74LS244 buffer.

DATA OUT

Data out from the bus (into the controller board) travels through pins 35, 36, 38, 39, 40, 88, 89, and 90 on the bus interface plug. This data is latched by tri-state latch U35. The latch is used because data on the S-100 bus is not present long enough for the 1797 to receive properly. The tri-state latch holds the data on the board's internal data bus so that the 1797 can read it. Valid data is latched in U35 on every write cycle. The latch is enabled through pin 1 when the ALE (Address Latch Enable) signal latches an asserted sOUT (Status Out) signal via U20.

ADDRESS LINES

The address lines from the bus enter the board through pins 29, 30, 31, 79, and 80 through 83 of the bus interface. They are buffered by the 74LS244 chip, U34.

CONTROL LINES

The control lines from the S-100 bus enter the board through pins 24, 25, 45, 46, and 75 through 78 of the bus interface. These lines are buffered by U33.

VECTOR INTERRUPT LINES

The vector interrupt lines from the bus enter the board at pins 4 through 11 of the bus interface. They may be driven by U32.

READY LINE

The ready line, RDY, enters through pin 72 of the bus interface. It is driven by U32. The controller board uses this line to put the CPU in a wait state during some operations to give the controller time to finish the operation.

RESET CIRCUITS

POWER-UP/RESET

On power up, the CPU sends RESET* through the S-100 bus to the H-207 board. This places the 1797 controller, the control latch, the write precompensation control, and the U26 flip-flops in a known state before the CPU accesses the board.

In the 1797, the reset line sets the command register at 03H, the sector register to 01H, and bit 7 of the status register (Not Ready bit) to logic zero.

After the reset line goes high, the 1797 executes the restore command. The drive read/write head seeks track 0 and sends an interrupt to the computer once the track is found. See the 1797 IC data sheets for more details.

The reset line connects to pin 1 of the control latch, U30, to clear all of the outputs.

The reset state of the phase lock loop control, U1, makes the phase four (ø4) input equal to 0 (see the 1691 IC data sheets).

Finally, the U26 Q-outputs are made equal to 1; pin 9 sends an RDY (ready) signal to the CPU and pin 5 provides part of the qualification needed for read/write enabling through U27-11.

POWER-UP WRITE PROTECTION

On power up, the TTL circuits will be at an undefined state until the power supply voltage rises above 4 volts. This could generate a write command in the drives and damage any disks that may be installed.

To protect the disk, the WG (write gate) output from the 1797 is coupled to the 5" and 8" drives through Q3 and Q2. These transistors are biased by R25, D3-D1, and R24 to remain cut off until the power supply voltage is at or above 4 volts. When the supply reaches this value, Q2 and Q3 are biased near their operating region and will conduct whenever WG is asserted.

CPU/CONTROLLER LOGIC

Reading and writing in the H-207 board involves three types of information: data which can be read or written, status signals, and control signals. Status signals can only be read and control signals can only be written.

READ STATUS LATCH (U31)

Assume a status signal needs to be read. There are two sources of status information for the S-100 bus, the status port at U31 and the 1797 status register in U22.

To read from the status port, the CPU selects the H-207 by placing the address of the board on the address lines, A0-A7. Lines A3-A7 are checked by the address comparator, U29, for the proper address. The proper address is defined by the user by setting DIP switch DS1. If the address is correct, the EOUT signal pin 19 asserts.

The EOUT signal is gated through U28-13 by I/O at pin 12. I/O asserts on a data transfer between the CPU and an I/O port. If I/O is low, indicating that the sINP signal or sOUT signal is asserted, then the simultaneous assertion of EOUT and I/O signals sends a logic one to U20-2. This logic one is latched onto pin 5 when ALE (address latch enable) asserts. ALE, derived from pSTVAL* and pSYNC, goes high when the H-207 port address is stable.

The Q output of U20 is NANDed with pDBIN from the S-100 bus to form $\overline{\text{RDME}}$ at U27-8. This line goes low to indicate that the H-207 board is being read by the CPU, and activates the status latch, U31-1.

The status latch still can not be read until the status port select line (STPS) is asserted at pin 15 of U31. This line comes from U17-14, the I/O address decoder.

The I/O address decoder activates STPS by decoding the address lines A0, A1, and A2. If A0 and A1 are low and A2 is high, and if BDSEL or board select is active, then U17's Y1 line goes low. This causes U31 to place the status word onto the board's internal data bus, where it is buffered by U36 to the S-100 bus.

The organization of the status latch is as follows:

BIT	SIGNAL NAME	FUNCTION	
0	INTRQ	0 = no interrupt request	1 = interrupt request from 1797
1	MOTORON (5")	0 = spindle motor not running	1 = spindle motor running
3	96TP1	0 = 5.25" drives are 48 TPI	1 = 5.25" drives are 96 TP1
4	PRECOMP	0 = 5.25" drives do not need precomp	1 = 5.25" drives need precomp
6	TWOSIDED	0 = 8" diskette not two sided	1 = 8" diskette two sided
7	DRQ	0 = not ready for data transfer	1 = ready for data transfer

READ STATUS REGISTER OF 1797 (U22)

Assume now that the 1797's status register is to be read. The procedure is the same as described previously, except that address lines A0, A1, and A2 are low. Because the address bits A0-A2 are different, the I/O address decoder, U17, does not enable the status latch, U31. Instead the status register of the 1797 is selected and read onto the data bus.

WRITE CONTROL LATCH (U30)

The control latch, U30, is written at the falling edge of CLEN, which is the simultaneous assertion of pWR and the Y0 output of the I/O address decoder. The pWR signal comes directly from the CPU, and the Y0 signal occurs when A0, A1, and A2 are high, low, and high, respectively. The Y0 and pWR signals are ORed at U21-6 to form CLEN.

The organization of each bit in the control latch is as follows:

BIT	SIGNAL NAME	FUNCTION	
0,1	DSA, DSB	00 = select drive 1 01 = select drive 2	10 = select drive 3 11 = select drive 4
2	8"/5"	0 = select 5.25"	1 = select 8"
3	DSEN	0 = deselect all drives	1 = select drive specified by bits 0, 1, and 2
4	PRECOMP*		
	5.25" DDEN	0 = precomp all tracks	1 = disable precomp
	8" DDEN	0 = precomp all tracks	1 = precomp tracks 44-76
5	5" FASTEP	0 = 1797 operates as specified by bit 2	1 = 1797 operates in 8" mode
6	WAITEN	0 = wait state enable	1 = wait state enable
7	SDEN	0 = double density	1 = single density

*(Note: Precomp is disabled in single density.)

When the WAITEN bit in the control latch is asserted, a wait state is intitiated on the next read or write of the data register. WAITEN couples through U23, U26, and U32 to the S-100 RDY line. RDY goes low to put the CPU in a wait state until the disk controller asserts DRQ at U22-38.

Upon DRQ becoming active, an additional delay is needed to fulfill the access time requirements of the 1797 Controller. The access delay and synchronization to the S-100 Bus are both accomplished by counting system clocks. An on-board jumper selects whether one system clock is counted (for systems with clocks up to 3 MHz) or two system clocks are counted (for systems with clocks up to 6 MHz). For operation at less than 3 MHz, jumper J1 (near U19) should be jumpered between F and G. For operation between 3 and 6 MHz, this jumper should be between F and E (normal position for the H/Z-100).

At the completion of the access delay, the wait state is cleared. RDY is asserted, and the CPU completes the read or write of the data register in the 1797. A RESET or an INTRQ signal also clears the wait state, so that the CPU does not hang up after an error during a disk access.

WRITE COMMAND REGISTER IN THE 1797 (U22)

The command register in the 1797 can be written when A0, A1, and A2 are all low. The FDWR signal at U22-2 is asserted when both FDEN and pWR* are logic zero. The signal pWR comes directly from the CPU, while FDEN is a composite signal made up of FDSEL and U26-5. The output of U26-5 is the signal that starts the access of the 1797 controller at the end of the wait state.

DATA READ/WRITE OPERATIONS

During a data write operation, the controller board is enabled by the proper address and by pWR*. After the proper control words are sent to select the proper drive, address lines A0 and A1 are made high and A2 is made low. This connects the data register of the 1797 to the internal data bus. As long as A0 and A1 are high and A2 and FDWR are low, the data from the S-100 bus will go to the 1797 data register and be shifted out serially on pin 31, the write output line. Also, on pin 31, clock pulses are inserted between each bit.

The track and sector registers in the 1797 determine where the data is to be written to on the disk. Whenever a sector is filled with data, software determines the next sector to be written to by making the A0 and A1 signals equal to 0 and 1, A2 equal to 0. Software then writes the sector number to the sector register and the track number to the track register.

The 1797 translates the track numbers into the proper step and direction commands to the drive.

A read operation requires the board to be enabled as described earlier. However, the I/O address decoder does not enable the status latch because the address provided by the CPU is not correct for a status read from the latch. Instead, the address lines causes the 1797 to dump the bits in its data register onto the internal data bus of the H-207, which connects to the U36 buffer and the S-100 bus.

The 1797 fills its data register from the data shift register, which fills serially from the RAWREAD data stream at U22-27. See "Data Separation and Precompensation" for a discussion on RAWREAD data processing.

RDY DELAY

U19 is a quad flip-flop that acts as a delay line for the DRQ signal from the 1797 to the S-100 RDY line. The input at U19-4, D1, is output at Q1 after one clock cycle. Q1 is tied to D2 and is output to Q2 after another clock cycle. Q2 is also tied to U25-1 and D3.

From U25-12, the D2 signal presets flip-flop U26. Flip-flop U26 qualifies the FDSEL signal to enable read/write operations in anticipation of the RDY line being made active.

From D3 of U19, the delayed DRQ signal is output to Q3, which is connected to D4 and to jumper J1, post G. Post G is connected to post F in 3 MHz operations, which do not need additional delay of the DRQ signal. Instead, the output of Q4, which contains the DRQ signal delayed by three to four clock cycles, is connected to jumper J1, post E. For 6 MHz operation, J1 is connected between post E and post F.

INTERRUPTS

There are two interrupts that the H-207 board can make. They are the interrupt request (INTRQ) and the data request (DRQ). Both of these interrupts originate from the 1797. The INTRQ signal is sent to indicate a command completion or an error. The DRQ signal is sent to indicate data will be accepted in response to a disk read or write command.

The interrupts can be detected two ways, as either a vectored interrupt on any of the bus interface pins from 4 to 11, or as a bit set in the status port, U31, which can then be polled by the CPU.

The INTRQ signal pulls the bus out of a wait state caused by a logic zero at U26-9. When pin 39 of the 1797 asserts, it is inverted at U25-6 to set pin 9 of U26.

CONTROLLER/DISK-DRIVE LOGIC

DATA SHAPING

Data pulses to the drive are reshaped by U16, a one-shot multivibrator, to 400 ns. Raw data from the drive are reshaped to 250 ns.

DATA SEPARATION AND PRECOMPENSATION

Data separation and precompensation are performed primarily by U1, U3, U4, U5, and U22. The data separation circuits are used when the controller is receiving data from the disk drive, while the precompensation circuits are used when the controller is writing data to the disk.

DATA SEPARATION

$\overline{\text{READDATA}}$ ($\overline{\text{RDD}}$) from the drive couples through U9 and U16 to U1-11 and U22-27 ($\overline{\text{RAWREAD}}$). $\overline{\text{RDD}}$ contains both data bits and clock bits. U1 extracts the clock bits and sends them to U22-26 as RCLK. These pulses are synchronized with RDD. The 1797 uses the RCLK signal to extract the data bits from the $\overline{\text{RAWREAD}}$ stream. U22 then formats the data and sends it to the CPU.

U1 uses a phase-locked loop to keep RCLK in phase with the incoming data stream. The phase-locked loop consists of U5, U4, U13, and U1. U5 is a 4-MHz voltage-controlled oscillator that drives U4 and U13. U4 and U13 select either 4 MHz or 2 MHz, depending on the disk size. If a 5-1/4" disk is being read, U4-9 is low. This couples the 2-MHz signal to U1-16. Four megahertz is coupled to U1 for 8" drives.

If the phase of RCLK should drift with respect to the incoming $\overline{RDD}$ signal, U1 will send feedback pulses from U1-13 or U1-14 to the VCO at U5. These pulses will increase or lower the VCO frequency. In turn, the VCO frequency will increase or decrease the RCLK frequency until it again in phase with RDD. Here's how:

> If the frequency of $\overline{RDD}$ is higher than RCLK, then $\overline{RDD}$ will go low at the beginning of RCLK. The pump-up output (PU) at U1-13 will go from a high-impedance state to a logic one. This increases the VCO frequency which increases frequency of RCLK.
>
> If the frequency of $\overline{RDD}$ is lower than RCLK, then $\overline{RDD}$ will go low at the end of RCLK. The pump-down output ($\overline{PD}$) responds by going from a high-impedance state to logic zero. This decreases the VCO frequency and thus decreases the frequency of RCLK.
>
> If RCLK and $\overline{RDD}$ are in phase, then PU and $\overline{PD}$ are in a high-impedance state and the VCO frequency remains constant.

Pins 5, 7, and 8 of U1 allow the 1797 to control clock separation and data recovery. When pins 7 and 8 are low, the data recovery circuits are enabled. If pin 7 is high, which happens during a write operation, then the data recovery circuits are disabled.

Pin 15, DDEN, controls the frequency of RCLK. When pin 15 is logic one, the frequency of RCLK is equal to the VCO frequency divided by 16. When pin 15 is logic zero, RCLK is equal to the VCO frequency divided by 8.

DATA PRECOMPENSATION

Precompensation, used for 80-track double-density disk write operations, places data properly on the disk so that it can be read back with minimum error. Error is introduced by the shifting of old data that is adjacent to new data being written. This shifting is due to the nature of the magnetic fields on the disk (like fields repel).

The precompensation circuits consist of U22, U1, and U3. U22 sends the write data from pin 31 to U1-1. U3 provides delay timing for the write data in U1. U22 selects the amount of precompensation by setting the logic levels on pin 18 (LATE) and pin 17 (EARLY).

Here's what happens...

When the 1797 sends a data bit to U1-1, the strobe line at U1-5 latches high. This triggers U3-11 and causes a negative-going pulse to ripple through $\overline{\phi 1}$, $\overline{\phi 2}$, $\overline{\phi 3}$, and $\overline{\phi 4}$. R3 sets the pulse width of these signals and, therefore, the amount of precompensation.

With no precompensation (EARLY = LATE = 0), the data pulse is coupled to U1-6 at $\overline{\phi 2}$ time. If LATE precompensation is selected, the data bit leaves U1-6 at $\overline{\phi 3}$ time. EARLY precompensation synchronizes the data bit to $\overline{\phi 1}$.

When $\overline{\phi 4}$ pulses low, it couples through U7 to U1-19 to clear the strobe at U1-5 in anticipation of the next write data pulse.

Precompensation must be enabled for double-density operation. The CPU does this by setting U30-19 to logic one and sending it to the DDEN input at U1-15. The CPU also asserts the $\overline{\text{PRECOMP}}$ line at U30-12. This couples through U6-8 to TG43 at U1-9. TG43 must be high before precompensation can take place.

Even if $\overline{\text{PRECOMP}}$ isn't asserted, the write data should be precompensated on the inner tracks, where the data is packed closer together. This condition is taken care of by U22-29, which asserts on tracks greater than 43. The TG43 signal couples through U6-8 to the TG43 input of U1.

HEAD LOAD TIMING

The single-shot multivibrator at U15 provides read/write head-load timing. When the 1797 sends a head-load command, pin 28 goes high to load the drive head and to trigger U15.

U15-7 goes low for about 50 mS. This signal couples to U22-23 to prevent a data read or write until U15 times out. This delay compensates for bounce when the read/write head contacts the disk surface.

1797 TIMING

U18, U12, U14, and U30 provide timing and control of timing to the 1797. Depending on the state of U14, the clock frequency to U22-24 will be either 1 MHz or 2 MHz.

The operating frequency of the 1797 is automatically switched from 1 MHz to 2 MHz when changing from 5-1/4" drives to 8" drives. This is done by U30-6 and is coupled through U7-11 to the latch at U14.

One drawback of the 1797 is that it won't allow 5-1/4" drives to step at a 3-mS rate during track seek. To circumvent this problem, U30-15 sets the 5" FASTSTEP signal. This signal couples through U7-12 to U14. U14 increases the operating frequency to 2 MHz to speed up the step rate. At the end of the track-seek function, the clock frequency is reduced to 1 MHz again for normal 5-1/4" operation.

8" DRIVE INTERFACE

The 8" drive interface is through P1. All output signals to the drives are buffered through U8 and U10 except WG and HLD. The WG signal is sent through transistor Q2, as described previously. The HLD signal is inverted by U7-10 before being transmitted to the drives.

All input signals except READY and TWOSIDED are buffered through the upper section of U9 when enabled by a high on the 8"/$\overline{5}$" line. The READY signal is inverted at U6-6, while the TWOSIDED signal is inverted at U6-11.

5" DRIVE INTERFACE

The 5" drive interface is through P2. All output signals to the drives are buffered through U10 and U11 except WG and MOTOR. The WG signal is sent through transistor Q3, as described previously. The MOTOR signal turns on the disk drive motor whenever a logic zero is present at pins 9, 10, 12, and 13 of U23. The single-shot at U15 keeps the drive motor on for about 20 seconds after the disk access is complete. This provides a proper turn-off delay.

All input signals are buffered through the lower section of U9, which is enabled by a low on the 8"/$\overline{5}$" line.

CALIBRATION CIRCUIT BOARD

The calibration circuit compares the end of the write pulse with a narrow pulse of a known delay. When the two happen simultaneously, the LED on the calibration board is latched on. This indicates that the length of the write pulse is properly adjusted.

The write pulse coming from CP3 is applied to NAND gate U501D. U501D inverts the pulse and applies it to inverter U501C and to delay line DL501. Within DL501 the pulse is delayed 120 nS between pins 1 and 10 and 160 nS between pins 1 and 6. These two delayed pulses are then compared by NAND gates U501A and U501B. The result of the comparison is a pulse 40 nS wide and 120 nS delayed in reference to the write pulse.

If the write pulse has been adjusted for a 120 nS pulse width, the write pulse at the D flip-flop U502B-11 will go high when the 40 nS delayed pulse is low. This condition causes U502B to latch a low on the Q output, U502B-9. A low at this point turns on the LED, D501.

By adjusting the precompensation controls into this 40 nS "window", it is possible to "tune" write precompensation to be not only between 120 and 160 nS, but also much closer to 120 nS than 160 nS.

To gain additional delay for greater write precompensation, DL502 (optional HE 41-10) can be added to the circuit. DL502 provides four additional delay taps with an additional 40 nS of delay per tap.

H-207 FLOPPY DISK CONTROLLER BOARD DEFINITIONS

A0-A7	Address bits.
ALE	Address latch enable. Data and address lines from the CPU have valid information.
BDSEL	Board select. The H-207 board is selected (enabled).
CLK	Clock signal.
CS	Chip select. When asserted, the 1797 chip is enabled.
DØ-D7	Data bits on the H-207 board's internal data bus.
DDEN	Double density enable.
D1Ø-D17	Data-in bits on the S-100 bus ("in" with respect to the CPU, not the Controller).
DIR	Direction of drive head. When high, the drive head is stepping in. When low, the drive head is stepping out.
DOØ-DO7	Data-out bits on the S-100 bus ("out" with respect to the CPU, not the Controller).
DRQ	Data request. The 1797 data register needs data for write operations or the register has data for read operations.
DSA	Drive select A. Used with DSB to address the drives.
DSB	Drive select B. Used with DSA to address the drives.
EARLY	Write data bit early to disk drive (used for precompensation).
HLD	Head load.

HLT	Head load timing. The drive head is engaged when this signal is high.
INDEX	The index hole on the diskette has been detected.
INTRQ	Interrupt request. H-207 board has input for the CPU.
LATE	Write data bit late for drive precompensation.
MR	Master reset pin on the 1797 Controller chip that sets all registers in the chip to a known state.
pSTVAL*	Status valid.
pSYNC	New bus cycle may begin.
PD	Pump down. Decreases the frequency of the raw read data tracking clock.
PRECOMP	Enables precompensation when low.
PU	Pump up. Increases frequency of the raw read data tracking clock.
pWR	Valid data is on data-out bus (write bus).
RAWREAD	Unprocessed data from the drive.
RCLK	Clock that separates data from drive data and clock stream.
RDD	Data and clock stream from the drive.
RDME	Data or status signals input for the bus are enabled.
RDY	Slave aboard is ready. (H-207 board is a slave board.)
RE	Read enable. Enables the 1797 chip for read operations when low.
READY	The 8" disk drive is ready.

RESET	Reset signal.
SIDE1	Otherwise known as side select output. When high side 1 is selected in the drive. When low, side 0 is selected.
sINP	Status signal signifying data input to the bus (read cycle) may occur.
sOUT	Status signal signifying data output from the bus (write cycle) may occur.
STEP	Steps the drive head one step per pulse.
STB	Strobe output from the 1691 (U1) phase lock loop control.
TG43	Track greater than 43. The drive read/write head is over or past track 43 (track of mandatory precompensation in double density 8" drive.
TKØ	Track 0. The drive read/write head is over track 0 on the diskette.
TWOSIDED	The 8" drive is set for two-sided operation with a two-sided diskette.
VFOE/WF	VFO enable/write fault. When WG is asserted, VFOE/WF flags write faults when deasserted, terminating any write commands. When WG is deasserted, VFDE/WF enables the data separator in the 1691.
VIØ*-V17*	Vector interrupts.
WAIT	RDY line is low (not ready).
WAITEN	Wait enable. Set RDY line low on all accesses of the 1797 data register.
WD	Write data. Contains the data to be written onto the diskettes as well as the clock signals.
WDIN	Write data into the 1691 phase lock loop control.

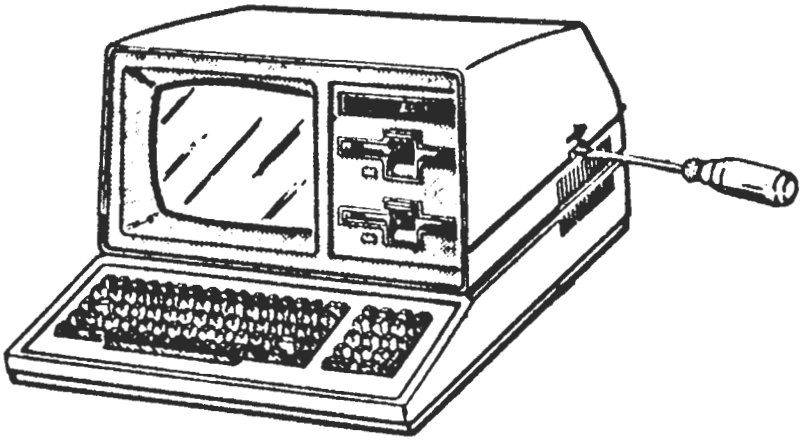
WDOUT	Write data out of the 1691 phase lock loop and precompensation controller.
WG	Write gate. Output to the disk drive is valid.
WE	Write enable. Enables the 1797 chip for write operations.
WPRT	Write protect. When this signal is received, no write command can take place and write protect bit in the status register is set.
WRDATA	Precompensated write data pulses that have been reshaped by U16.
5DSØ-5DS3	Five-inch drive select signals.
5"FASTEP	Enables fast stepping in the 5.25" drives.
8"/$\overline{5}$"	Selects between the 8" and the 5.25" drives.
8DSØ-8DS3	Eight-inch drive select signals.
CLOCK	Master clock signal.
$\phi 1$ - $\phi 4$	Precompensation phase signals.

DISASSEMBLY

INTRODUCTION

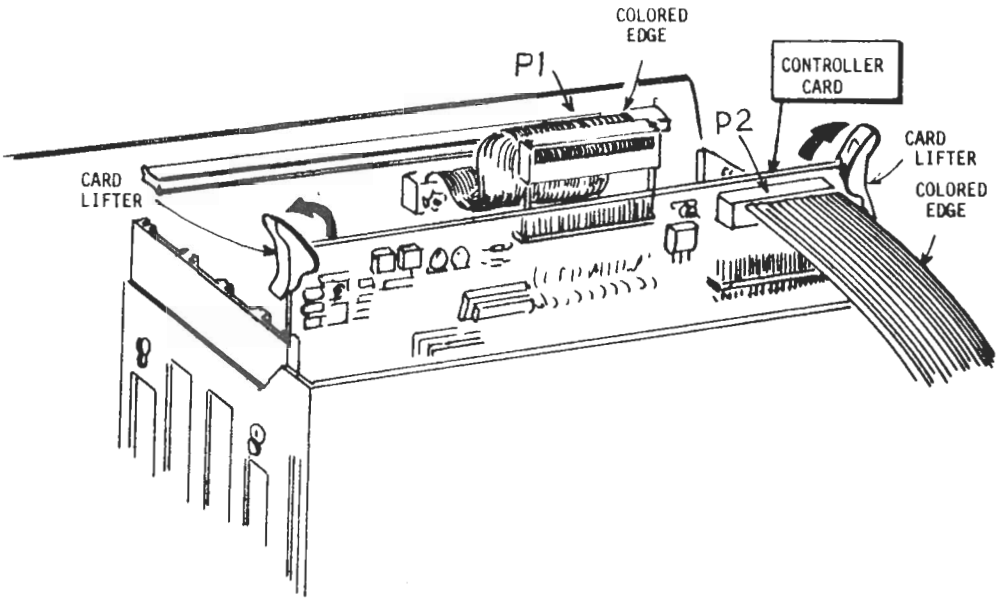
The procedures on the following pages show you how to remove the H-207 Floppy Disk Controller Board from the two different models of the H/Z-100. Find the appropriate procedure and follow the instructions.

ALL-IN-ONE



-- With a flat-blade screwdriver, slide the latch bracket to the center of the slot in the cabinet top. The latch bracket is spring loaded, so you will have to work with one side of the cabinet top at a time. While holding the latch in the center position, lift that side of the cabinet top. After one side is freed, perform the procedure on the other side. Be sure to hold the freed side up, so it will not snap back down.

-- Remove the cabinet top and set it aside in a safe place.



-- Disconnect the 50-conductor cable at P1 and the 34-conductor cable at P2 from the H-207 board.

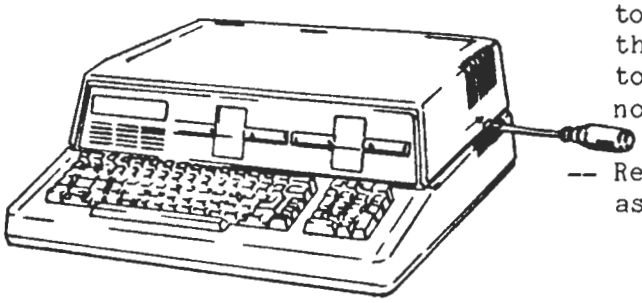
-- Lift up on the H-207 board extractors to pop the board free from the S-100 bus connector.

-- Now lift the H-207 board from the card cage.

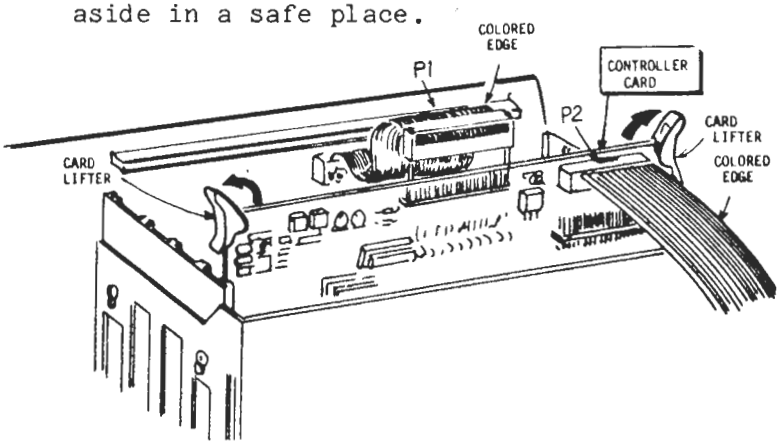
This completes the removal of the H-207 board from the H/Z-100 All-in-One computer. Reverse the procedure to install the board into the computer.

LOW PROFILE

-- With a flat-blade screwdriver, slide the latch bracket to the center of the slot in the cabinet top. The latch is spring loaded, so you will have to work with one side of the cabinet top at a time. While holding the latch in the center position, lift that side of the cabinet top. After one side is freed, perform the procedure on the other side. Be sure to hold the freed side up, so it will not snap back down.



-- Remove the cabinet top and set it aside in a safe place.



-- Disconnect the 50-conductor cable at P1 and the 34-conductor cable at P2 from the H-207 board.

-- Lift up on the H-207 board extractors to pop the board free from the S-100 bus connector.

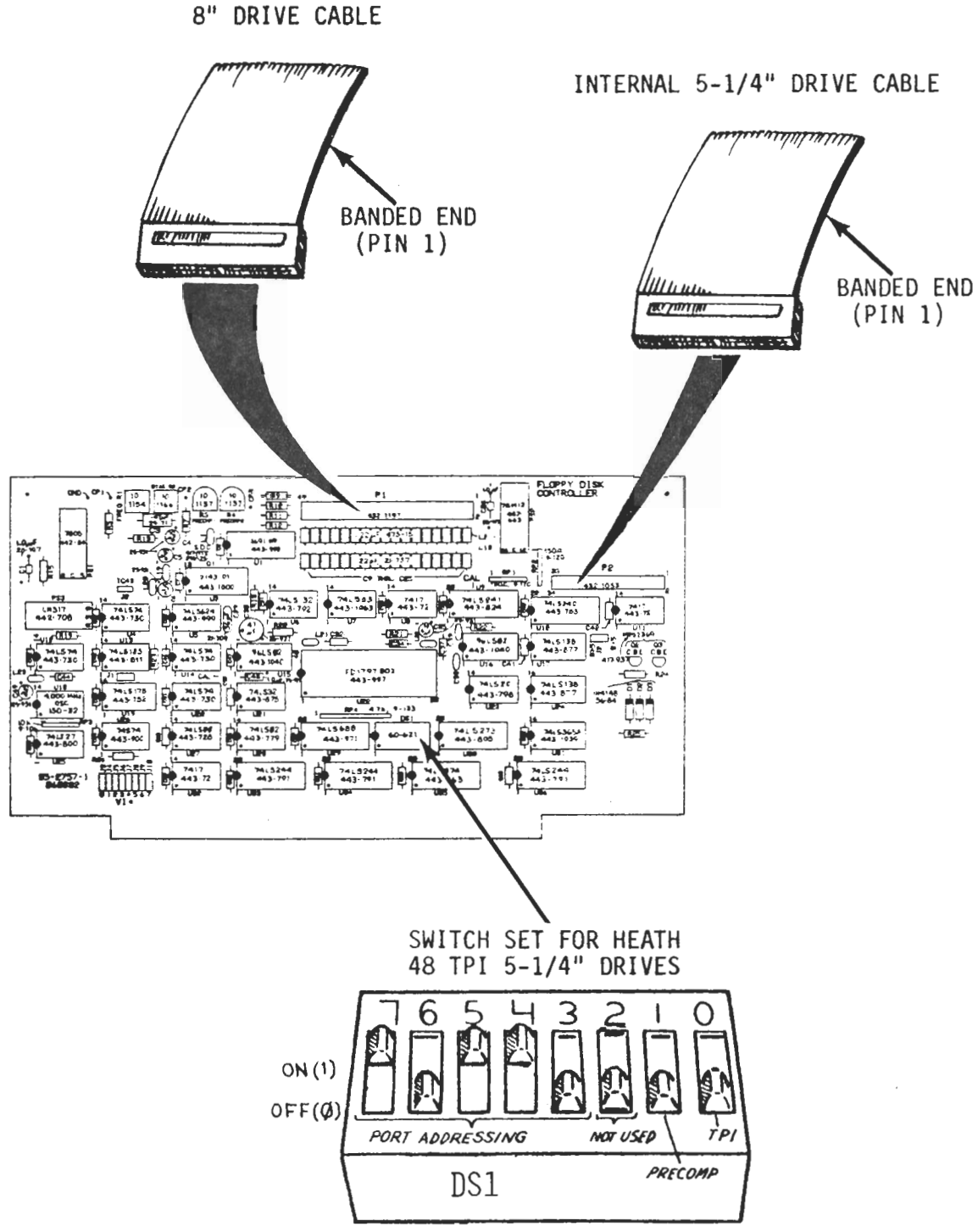
-- Now lift the H-207 board from the card cage.

This completes the removal of the H-207 board from the H/Z-100 Low-Profile computer. Reverse the procedure to install the board into the computer.

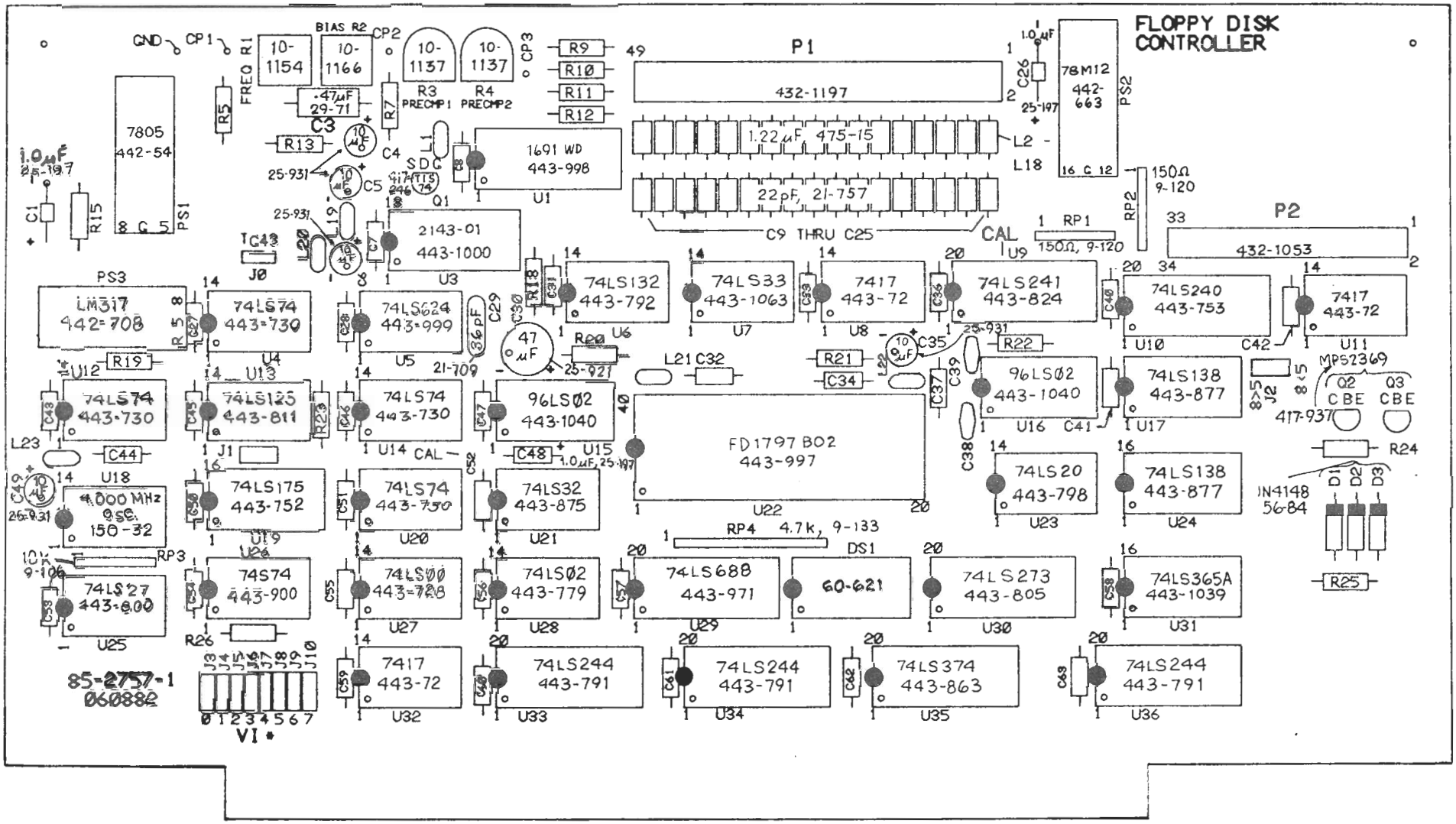
TECHNICIAN NOTES:

VISUAL CHECKS

DISK CONTROLLER BOARD CABLE CONNECTIONS AND SWITCH POSITIONS (IN AN H/Z-100 ENVIRONMENT)

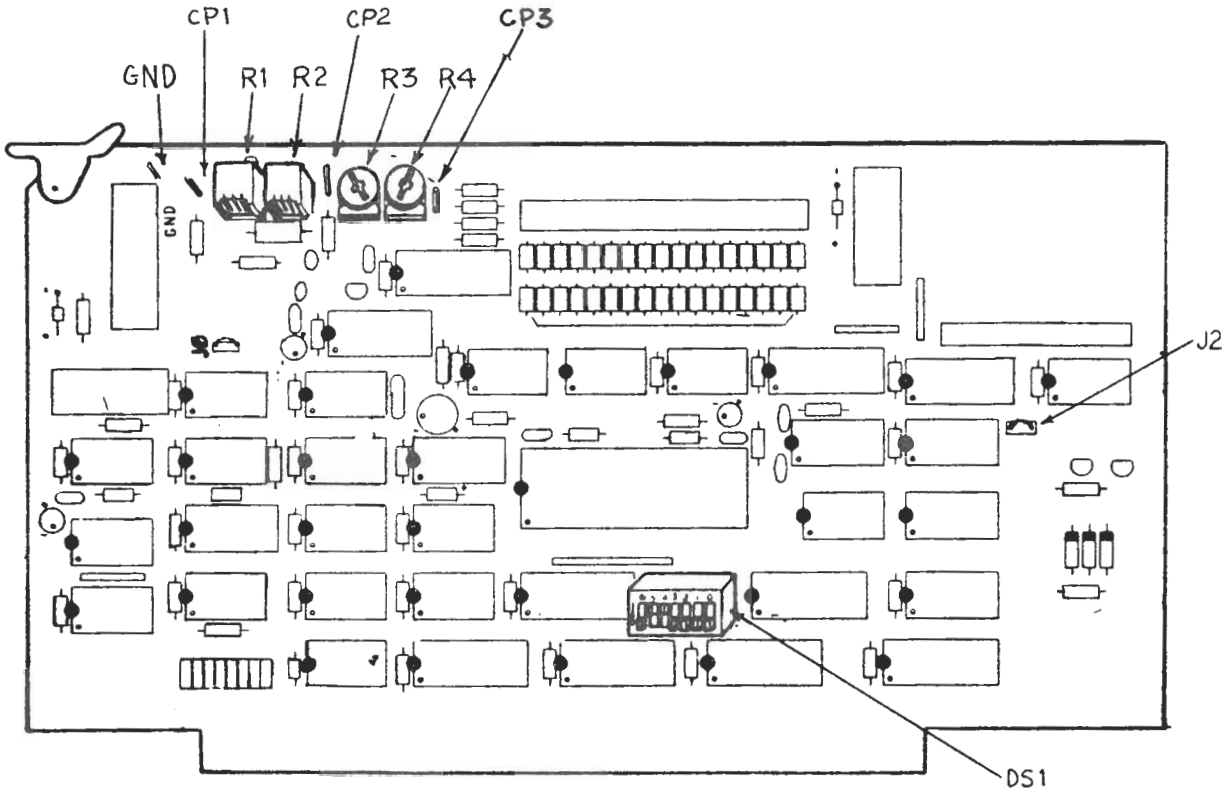


CIRCUIT COMPONENT LOCATIONS AND VALUES



H-207 FLOPPY DISK CONTROLLER

ADJUSTMENTS



H-207 CONTROLLER BOARD

CONTROLS AND JUMPER LOCATIONS

INTRODUCTION

In this section of the manual, instructions will be given on how to calibrate the H-207 Disk Controller Board. There are two adjustments that the controller board may require. These are Data Separator adjustments and Write Precompensation adjustments. Follow the procedures below to perform these two adjustments.

EQUIPMENT NEEDED

Frequency Counter	IM-2420 or equivalent (optional).
Low Capacitance Probe	PKW-105 or equivalent.
Multimeter	IM-2202 or equivalent.
Oscilloscope	IO-4510 or equivalent.
H-207 Calibration Board	See H-207 assembly manual (HE 595-2909) for parts list and assembly details.

DATA SEPARATOR ADJUSTMENT

Located on the following pages are two methods to adjust the data separator. The first procedure is the preferred method because of its ease and accuracy. The second procedure is the same method given to kitbuilders of the H-207. Locate the procedure you wish to use and follow the steps in that procedure.

FREQUENCY COUNTER METHOD

-- Allow a fifteen minute warm-up of the board with the top cover of the computer in place.

-- Remove the top cover of the computer.

-- Connect the common test lead of the multimeter to the GND test point at the upper left side of the controller board. Refer to the H-207 Controls and Jumper Locations pictorial.

-- Connect the positive test lead to the CP2 test point.

-- Adjust the BIAS control (R2) until the multimeter display shows +1.40 VDC (±.05 volts). Switch the multimeter to lower ranges to perform this adjustment accurately.

-- Disconnect the multimeter.

-- Connect the common lead of the frequency counter to the GND test point.

-- Connect the test probe of the frequency counter to the CP1 test point.

-- Adjust the FREQ control (R1) until the frequency counter display shows 4.000 MHz.

-- Disconnect the frequency counter.

The adjustments to the Data Separator are now complete. Proceed to WRITE PRECOMPENSATION ADJUSTMENTS.

KIT BUILDER METHOD

-- Remove the controller board from the computer.

-- Remove U9, U22, and U30 from their sockets.

-- Tack solder a length of wire between pins 1 and 20 of the socket for U9.

-- Tack solder wires to interconnect pins 30, 33, 37, and 20 of the socket for U22.

-- Set the PRECMP 2 control (R4) to a fully clockwise position.

-- Set the PRECMP 1 control (R3) to a fully counterclockwise position.

-- Connect the common test lead of the multimeter to the GND test point.

-- Reinstall the controller board into the computer.

-- Connect the positive test lead to the CP2 test point and apply power to the computer.

-- Adjust the BIAS control (R2) until the multimeter display shows +1.40 VDC (±.05 volts). You will want to switch the multimeter to lower ranges to perform this adjustment accurately.

-- Allow a period of 15 minutes for drifting; then perform the R2 adjustment again.

-- Power down the computer and remove the controller board.

-- Tack solder a length of wire between the two holes marked CAL.

-- Reinstall the controller board and apply power to the computer.

-- Adjust the FREQ control (R1) for a multimeter display of +1.40 VDC (±0.05 volts) at test point CP2.

-- Power down the computer and remove the controller board.

-- Remove all the temporarily installed jumper wires.

-- Install U9, U22, and U30 in their respective sockets.

-- Reinstall the controller board into the computer.

The adjustments to the Data Separator are now complete. Proceed to WRITE PRECOMPENSATION ADJUSTMENTS.

WRITE PRECOMPENSATION ADJUSTMENTS

Located on the following pages are two methods to adjust write precompensation. The first method uses the calibration circuit board that is included in the H-207 kit. The second method requires the use of an oscilloscope and precompensation data about the drives that are used with the controller board. The first method is the preferred method because of its ease. The second method is required, however, when precompensation values not included on the calibration circuit board are needed for a particular drive. Locate the procedure you wish to use and follow the steps in that procedure.

CALIBRATION CIRCUIT BOARD METHOD

The calibration circuit board method is primarily used to adjust the H-207 for use within a H/Z-100. By using this method, the 5-1/4" drive section of the controller board is set for a write precompensation value of 120 nS. This is the value used for Heath/Zenith 48 TPI, 5-1/4" disk drives that are included in the H/Z-100s. The jumpers at J0 and J2 remain at the stock position. That is, J0 is out and J2 is in the 8 < 5 position (foil bridge).

You may use the calibration circuit board for other values of precompensation. By installing DL502, you may choose from five values of precompensation. These being 120 nS, 160 nS, 200 nS, 240 nS, and 280 nS. However, you may have a customer application that requires a precompensation value not mentioned above. In this case, proceed to Oscilloscope Method of Write Precompensation.

You may also use the calibration circuit board for setting write precompensation for 8" disk drives. Again, if the precompensation value needed is not obtainable with the calibration board, use the Oscilloscope Method. Remember when setting precompensation for 8" drives, you will have to determine if the 8" value is greater than the 5-1/4" value. If it is, you will have to jumper J2 so it is in the 8 > 5 position. Also remember, that R4 is the control that needs to be adjusted instead of R3.

PROCEDURE

-- Obtain a calibration circuit board (see H-207 manual HE 595-2909 for construction).

-- Connect the alligator clip of the calibration board to a source of +5 volts on the H-207 controller board. The positve end of any .1 uF glass capacitor is a good source.

-- Connect the black wire from the calibration board to the GND test point on the H-207 board.

-- Connect the yellow wire from the calibration board to the CP3 test point of the H-207 board.

-- If not already done, set R3 fully counterclockwise and R4 fully clockwise.

-- Set the jumper select wire of the calibration board to 120 nS. If the drive requires more precompensation, set the jumper to the desired position.

-- Turn on the computer.

-- Boot up a system disk. Refer to the appropriate operating system manual and start the disk format program.

-- While the format program is running, adjust R3 on the H-207 board until the LED on the calibration board just turns on.

-- Turn off the computer and disconnect the calibration circuit board.

This completes write precompensation adjustment.

NOTE: All diskettes should be reformatted before being used.

OSCILLOSCOPE METHOD

The oscilloscope method of write precompensation adjustment is primarily used to adjust the H-207 for non Heath/Zenith disk drives. To understand the relationship that exists between the PRECOMP switch setting of DS1 and jumper J0, refer to the table below. This table shows how to set the PRECOMP switch of DS1 and J0 for the particular system you are working on. Now perform the following steps to adjust write precompensation. Refer to the illustration at the beginning of this section for the locations of the test points.

	DESIRED RESULTS		
TYPE OF DRIVE	Precomp no tracks	Precomp all tracks	Precomp tracks >43
8" Double-Density	N/A	$\overline{\text{Precomp}}$* = Ø J0 = X	$\overline{\text{Precomp}}$ = 1 J0 - X
5-1/4", 48 TPI, Double-Density	$\overline{\text{Precomp}}$ = 1 J0 = X	$\overline{\text{Precomp}}$ = 0 J0 = X	N/A
5-1/4", 96 TPI, Double-Density	$\overline{\text{Precomp}}$ = 1 J0 = IN	$\overline{\text{Precomp}}$ = 0 J0 = X	$\overline{\text{Precomp}}$ = 1 J0 = OUT

*$\overline{\text{Precomp}}$ is bit 4 in the control latch

X = Don't Care

NOTE: Precomp is automatically disabled in single-density operation.

-- Set the PRECMP 2 control (R4) to a fully clockwise position.

-- Set the PRECMP 1 control (R3) to a fully counterclockwise position.

The position of J2 will determine which of the two following procedures you will use when adjusting write precompensation. Refer to the manufacturer's suggested write precompensation value for the type of drives in the system. If the system has only 8" disk drives, or only 5-1/4" disk drives, or the 8" write precompensation figure is less than the 5-1/4" write precompensation figure, use the procedure under "J2 = 8 < 5". If the system has disk drives where the 8" write precompensation figure is greater than the 5-1/4" write precompensation figure, use the procedure under "J2 = 8 > 5".
Typical values of precompensation are:

5-1/4" disk drives	125 to 200 nS	typical 150 nS.
8" disk drives	125 to 175 nS	typical 135 nS

J2 = 8 < 5 PROCEDURE

-- Connect the oscilloscope probe to GND and CP3. Set the probe to X10 and set the oscilloscope at 50 nS/division to display a 100 to 300 nS negative going pulse.

-- Apply power to the computer.

-- If the system has 8" disk drives, start the format routine on an 8" diskette. While format is running, adjust the PRECMP 1 control (R3) until the pulse width displayed on the oscilloscope corresponds to the manufacturer's suggested write precompensation for that type of drive.

-- If there are 5-1/4" disk drives in addition to 8" disk drives in the system, start the format routine on a 5-1/4" diskette. While format is running, adjust the PRECMP 2 control (R4) until the pulse width displayed on the oscilloscope corresponds to the manufacturer's suggested write precompensation for that type of drive.

-- If the system only has Heath/Zenith 5-1/4" 96 TPI disk drives or non Heath/Zenith disk drives that require write precompensation adjustment, start the format routine on a 5-1/4" diskette. While format is running, adjust the PRECMP 1 control (R3) until the pulse width displayed on the oscilloscope corresponds to the manufacturer's suggested write precompensation value for that drive.

-- Power down the computer.

-- Disconnect the oscilloscope probe.

This completes write precompensation adjustment.

NOTE: All diskettes should be reformatted before being used.

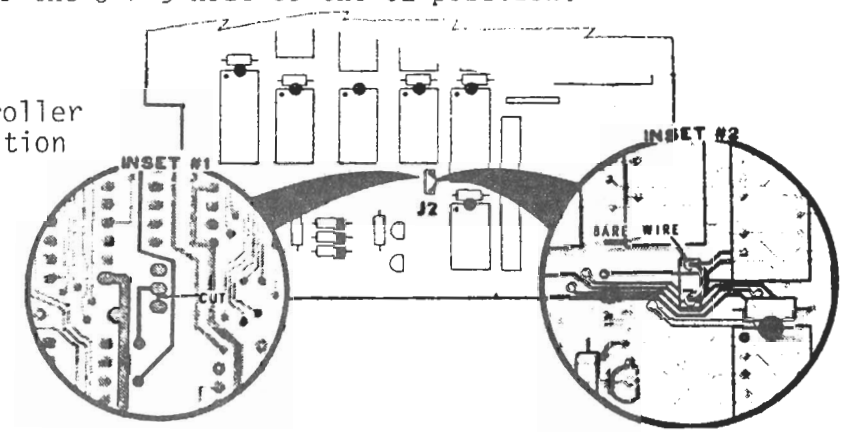
J2 = 8 > 5 PROCEDURE

-- Remove the controller board from the computer.

-- Refer to the H-207 J2 location pictorial and cut the foil that connects the middle of the J2 position to the 8 < 5 position of J2.

-- Install a jumper wire connecting the middle hole of the J2 position to the 8 > 5 hole of the J2 position.

H-207 Controller Board J2 Location



-- Install the floppy board into the computer.

-- Connect the oscilloscope probe to GND and CP3. Set the probe to X10 and set the oscilloscope at 50 nS/division to display a 100 to 300 nS negative going pulse.

-- Apply power to the computer.

-- While formatting a 5-1/4" diskette, adjust the PRECMP 1 control (R3) until the pulse width displayed on the oscilloscope corresponds with the manufacturer's suggested write precompensation value.

-- While formatting an 8" diskette, adjust the PRECMP 2 control (R4) until the pulse width displayed on the oscilloscope corresponds with the manufacturer's suggested write precompensation value.

-- Power down the computer.

-- Disconnect the oscilloscope probe.

This completes the write precompensation adjustment.

NOTE: All diskettes should be reformatted before being used.

TROUBLESHOOTING

INTRODUCTION

To troubleshoot the H-207 Floppy Disk Controller, use this section of the manual in conjunction with the schematic. Located in this section of the manual are service hints that will aid you in servicing the board. The schematic contains voltages and logic levels of a normally functioning board after a hard reset. By using standard troubleshooting techniques, most problems can be quickly located and corrected.

EQUIPMENT NEEDED

Frequency Counter	IM-2420 or equivalent.
Logic Probe	IT-4710 or equivalent.
Low Capacitance Probe	PKW-105 or equivalent.
Multimeter	IM-2260 or equivalent.
Oscilloscope	IO-4510 or equivalent.

H/Z-100 TEST FIXTURE

The H/Z-100 test fixture is set up so that the 5-1/4", 48 TPI disk drives are the primary boot device. Also, auto boot is defeated (See "Configuration").

It is assumed that the H-207 board is configured for operation within the H/Z-100. That is, J1 is jumpered for a 3 MHz or greater clock speed and DS1 is configured for port B0 (Hex), 48 TPI, and precompensation disabled.

PREWORK

Once you have received a H-207 Floppy Controller Board in for service, use the checkout procedure below. Included in the procedure are problems that may be identified before power is applied to the circuit board. Many of the checks below may have already been implemented in your preworking.

CHECKOUT PROCEDURE

Check the H-207 Controller Board for:

- Polarized capacitors installed backwards.
- Q1, Q2, or Q3 installed incorrectly.
- D1, D2, or D3 installed backwards.
- ICs installed backwards.
- Dirty S-100 board contacts.
- Solder bridges.
- Cold solder joints.
- Resistor packs installed backwards.
- Correct jumpering.
- Switch settings of DS1.
- Correct voltage regulator for location:

  7805 at PS1.
  78M12 at PS2.
  LM317 at PS3.

After making these checks, install the H-207 into your H/Z-100 test fixture and confirm the customer's complaint. If the board appears to operate properly, align the controller board using the procedure in the Alignment and Adjustments section of this manual.

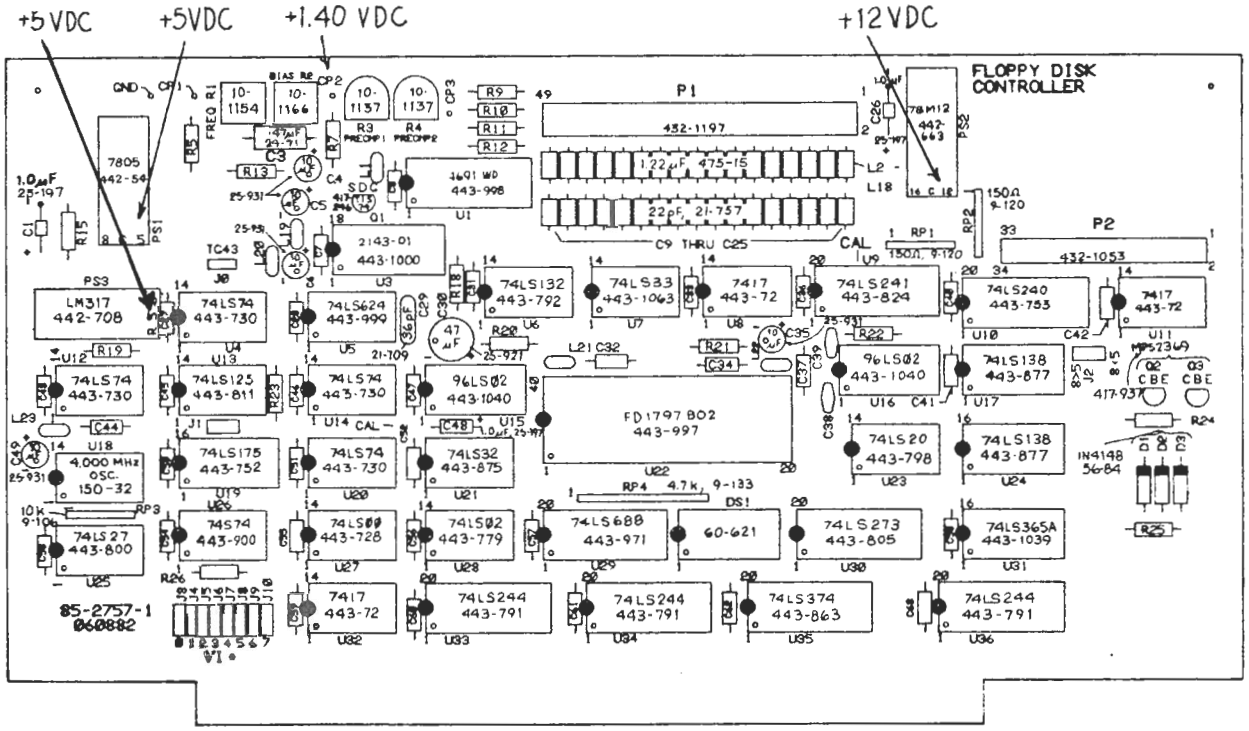
If the problem still exists, proceed to Service Hints.

SERVICE HINTS

VOLTAGE CHECKS

With the H-207 installed in your test fixture, perform the following voltage checks with your multimeter. The GND test point is a good place to connect the common lead of the multimeter. It is assumed that the disk drive cables are disconnected from the controller board.

- The voltage at PS1-5 is +5 VDC.
- The voltage at PS2-12 is +12 VDC.
- The voltage at PS3-5 is +5 VDC.
- The voltage at CP2 is +1.40 VDC.



If the voltages at these test points are within 5% of the values stated, it can be safely assumed U1, U5, and the voltage regulators are operating properly. Assuming the problem still exists, further aid can be found in Logic Level Checks and Waveforms. Otherwise, proceed to the Alignment and Adjustments.

LOGIC LEVEL CHECKS

On the following pages is a logic probe analysis of the H-207 board. When performing the tests, you need only to test the ICs in the left column indicated by an asterisk (*). If you don't get the suggested logic state, then check each IC listed immediately to the right. The logic states for these ICs are listed in the left column below the ICs with the asterisks.

Continue tracing backwards using this procedure until you test an IC that matches the suggested logic state. The previous IC that you tested is likely the bad IC.

Before you replace the suspected IC, check the other lines leading up to it. You must do this because this checkout procedure gives only the most likely causes to the problem. It doesn't cover such things as open ground foils, shorted foil runs, or open resistors.

As you make the following checks, press the (B)oot key and press RETURN. Logic states located inside parenthesis indicates that the probe pulses one or more times while "Read Completed" is printed on the screen. In the case of a (P) indication, the pulse rate (as indicated by the logic probe) will momentarily change during the "Read Completed" interval.

The schematic shows the logic states after a CTRL/RESET has been performed. Refer to these logic states for troubleshooting areas not covered in the following tests.

To setup the H-207 for the following test, connect at least one 48 TPI, 5-1/4" disk drive to P1 and turn on the computer.

H-207 DISK CONTROLLER TEST

CHECK	IF NOT OKAY, CHECK
*Q3 Collector = Z	U21-8
*U1-16 = 2 MHz	U13-6
*U7-4 = L	U7-5 (Also press and release CTR/RESET. U7-4 should remain low for about 18 seconds. If not, then replace U15.)
*U9-19 = L	U30 or the data bus is defective.
*U10-12 = H	U10 or U22 is defective.
*U10-14 = H	U10 or U22 is defective.
*U10-16 = H	U10 or U22 is defective.
*U11-4 = H	U11-3
*U11-6 = H	U11-5
*U11-8 = H	U11-9
*U11-10 = L	U11-11
*U11-12 = H	U11-13
*U22-2 = (H)	U21-11
*U22-3 = (H)	U21-3
*U22-23 = (H)	U15-7
*U22-24 = 1 MHz	U13-8
*U22-27 = P	U16-9
*U22-34 = L	U9 is defective.
*U22-35 = L	U9 is defective.
*U22-36 = H	U9 is defective.
*U31-1 = (H)	U27-8
*U31-15 = (H)	U17-14
*U32-6 = (H)	U32-5
*U35-11 = (P)	U28-4
*U36-1 = (H)	U27-8
*U36-19 = (H)	U27-8

End of test.

U4-3 = 4 MHz	U5-8
U4-5 = 2 MHz	U4-3
U4-9 = L	U4-11, U4-12
U4-11 = P	U4-5
U4-12 = L	U30 or the data bus is defective.
U5-8 = 4 MHz	U5 or U1 defective; R1 or R2 incorrectly adjusted.
U7-5 = H	U23-8
U7-11 = L	U30 or the data bus is defective.
U7-12 = L	U30 or the data bus is defective.
U7-13 = H	U7-11, U7-12
U10-3 = L	U10-17
U10-17 = H	U33-9
U11-3 = H	U16-7
U11-5 = H	U24-14
U11-9 = H	U24-12
U11-11 = L	U24-15
U11-13 = H	U24-13
U12-3 = 4 MHz	U18 is bad.
U12-5 = 2 MHz	U12-3
U12-9 = 1 MHz	U12-11
U12-11 = 2 MHz	U12-5
U13-4 = L	U4-9
U13-5 = 2 MHz	U4-5
U13-6 = 2 MHz	U13-4, U13-5
U13-8 = 1 MHz	U13-9, U13-10
U13-9 = 1 MHz	U12-9
U13-10 = L	U14-8
U14-8 = L	U14-11, U14-12
U14-11 = 1 MHz	U12-9
U14-12 = H	U7-13
U15-4 = H	U22 or the data bus is defective.
U15-7 = (H)	U15-4
U16-4 = L	U1 or U22 is defective.
U16-7 = H	U16-4
U16-9 = P	U16-11
U16-11 = P	U9 is defective.

U17-1 = P	U34-18
U17-2 = P	U34-16
U17-4 = (H)	U20-6
U17-6 = P	U34-14
U17-7 = L	U19-1
U17-14 = (H)	U17-1, U17-2, U17-4, U17-6
U17-15 = (H)	U17-1, U17-2, U17-4, U17-6
U19-1 = (L)	U26-8
U19-14 = L	U19-1
U20-1 = (L)	U28-13
U20-2 = (L)	U28-13
U20-3 = P	U27-6
U20-5 = (L)	U20-1, U20-2, U20-3
U20-6 = (H)	U20-1, U20-2, U20-3
U21-1 = (H)	U27-11
U21-2 = (H)	U27-8
U21-3 = (H)	U21-1, U21-2
U21-4 = (H)	U17-15
U21-5 = (P)	U33-12
U21-6 = (H)	U21-4, U21-5
U21-8 = L	U21-10
U21-10 = L	U22 of data bus is defective.
U21-11 = (H)	U21-12, U21-13
U21-12 = (H)	U27-11
U21-13 = (P)	U33-12
U22-39 = (L)	Check the data bus at pins 7 through 14. These lines pulse from a high impedance state while "Read Completed" is being printed. If not, then check the components along the data bus.
U23-2 = (L)	U30-16
U23-4 = P	U34-18
U23-5 = P	U34-16
U23-6 = (H)	U23-2, U23-4, U23-5
U23-8 = H	U23-13
U23-13 = L	U24-15

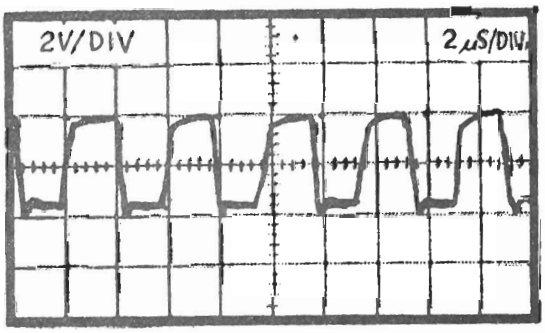
U24-1 = L	U30 or the data bus is defective.
U24-2 = L	U30 or the data bus is defective.
U24-3 = L	U30 or the data bus is defective.
U24-6 = H	U30 or the data bus is defective.
U24-12 = H	U24-1, U24-2, U24-3, U24-6
U24-13 = H	U24-1, U24-2, U24-3, U24-6
U24-14 = H	U24-1, U24-2, U24-3, U24-6
U24-15 = L	U24-1, U24-2, U24-3, U24-6
U25-1 = L	U19-7
U25-2 = L	U10-3
U25-3 = L	U10-3
U25-4 = (L)	U22-39
U25-5 = L	U19-14
U25-6 = (H)	U25-3, U25-4, U25-5
U25-12 = (H)	U25-1, U25-2, U25-13
U25-13 = (L)	U22-39
U26-2 = (H)	U23-6
U26-3 = (L)	U20-5
U26-4 = (H)	U25-12
U26-5 = (H)	U26-2, U26-3, U26-4
U26-8 = (L)	U26-10, U26-11, U26-12
U26-10 = (H)	U25-6
U26-11 = (L)	U20-5
U26-12 = (H)	U23-6
U27-1 = (L)	U22-39
U27-3 = (H)	U27-1
U27-4 = P	U33 defective.
U27-5 = P	U33 defective.
U27-6 = P	U27-5, U27-4
U27-8 = (H)	U27-9, U27-10
U27-9 = P	U33 defective.
U27-10 = (L)	U20-5
U27-11 = (H)	U27-12, U27-13
U27-12 = (L)	U28-10
U27-13 = (H)	U26-5
U28-1 = (H)	U28-2, U28-3
U28-2 = (L)	U33 defective.
U28-3 = (L)	U33 defective.
U28-4 = (P)	U28-6

U28-6 = (P)	U33-12
U28-8 = (H)	U20-6
U28-9 = P	U34-14
U28-10 = (L)	U28-8, U28-9
U28-11 = (P)	U29-19
U28-12 = (H)	U28-1
U28-13 = (L)	U28-11, U28-12
U29-19 = (P)	U29, U34, or DS1 defective.
U30-1 = H	U33-9
U30-11 = (H)	U21-6
U30-16 = (L)	U30-1, U30-11, or data bus problem.
U32-5 = (H)	U27-3
U33-9 = H	U33 defective.
U33-12 = (P)	U33 defective.
U34-14 = P	U34 defective.
U34-16 = P	U34 defective.
U34-18 = P	U34 defective.

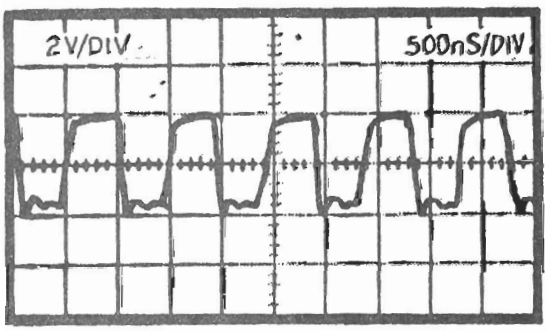
WAVEFORMS

The waveforms shown in this section are generated by a normally functioning controller board in an idle state. Use these waveforms as a reference when checking waveforms on the board you are servicing.

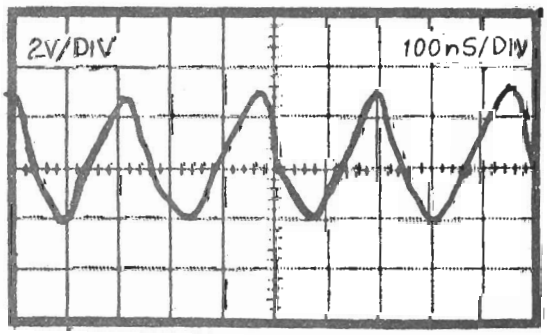
The waveform at the right was taken from U22-26. This is the RCLK signal that originates at U1-12. In an idle state the frequency of RCLK is around 250 kHz.



The waveform at the right was taken from U22-24. This is the CLK signal that originates from the oscillator circuits. The frequency of this signal is 1 MHz when the board is in an idle state.



The waveform at the right was taken from CP1. This is the VCO signal that originates from the VCO, U5-8. The frequency of this signal is 4 MHz when the board is in an idle state.



PARTS LISTS

PARTS LIST

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.

DISK CONTROLLER CIRCUIT BOARD

CAPACITORS

C1	1.0 uF tantalum	HE 25-197
C2	none	
C3	.47 uF polycarbonate	HE 29-71
C4	10 uF tantalum	HE 25-220
C5	10 uF tantalum	HE 25-220
C6	10 uF tantalum	HE 25-220
C7	.1 uF ceramic	HE 21-762
C8	.1 uF ceramic	HE 21-762
C9	22 pF ceramic	HE 21-757
C10	22 pF ceramic	HE 21-757
C11	22 pF ceramic	HE 21-757
C12	22 pF ceramic	HE 21-757
C13	22 pF ceramic	HE 21-757
C14	22 pF ceramic	HE 21-757
C15	22 pF ceramic	HE 21-757
C16	22 pF ceramic	HE 21-757
C17	22 pF ceramic	HE 21-757
C18	22 pF ceramic	HE 21-757
C19	22 pF ceramic	HE 21-757
C20	22 pF ceramic	HE 21-757
C21	22 pF ceramic	HE 21-757
C22	22 pF ceramic	HE 21-757
C23	22 pF ceramic	HE 21-757
C24	22 pF ceramic	HE 21-757
C25	22 pF ceramic	HE 21-757
C26	1.0 uF tantalum	HE 25-197
C27	.1 uF ceramic	HE 21-762
C28	.1 uF ceramic	HE 21-762
C29	36 pF ceramic	HE 21-709
C30	47 uF electrolytic	HE 25-921
C31	.1 uF ceramic	HE 21-762
C32	.1 uF ceramic	HE 21-762
C32a	10 uF tantalum	HE 25-220
C33	.1 uF ceramic	HE 21-762
C34	.1 uF ceramic	HE 21-762
C35	10 uF tantalum	HE 25-220
C36	.1 uF ceramic	HE 21-762
C37	.1 uF ceramic	HE 21-762
C38	180 pF ceramic	HE 21-746
C39	180 pF ceramic	HE 21-746
C40	.1 uF ceramic	HE 21-762
C41	.1 uF ceramic	HE 21-762
C42	.1 uF ceramic	HE 21-762
C43	.1 uF ceramic	HE 21-762
C44	.1 uF ceramic	HE 21-762
C45	.1 uF ceramic	HE 21-762

CAPACITORS (CONTINUED)

C46	.1 uF ceramic	HE 21-762
C47	.1 uF ceramic	HE 21-762
C48	1.0 uF tantalum	HE 25-197
C49	10 uF tantalum	HE 25-220
C50	.1 uF ceramic	HE 21-762
C51	.1 uF ceramic	HE 21-762
C52	.1 uF ceramic	HE 21-762
C53	.1 uF ceramic	HE 21-762
C54	.1 uF ceramic	HE 21-762
C55	.1 uF ceramic	HE 21-762
C56	.1 uF ceramic	HE 21-762
C57	.1 uF ceramic	HE 21-762
C58	.1 uF ceramic	HE 21-762
C59	.1 uF ceramic	HE 21-762
C60	.1 uF ceramic	HE 21-762
C61	.1 uF ceramic	HE 21-762
C62	.1 uF ceramic	HE 21-762
C63	.1 uF ceramic	HE 21-762

INDUCTORS

L1	35 uH	HE 235-229
L2	1.22 uH bead	HE 475-15
L3	1.22 uH bead	HE 475-15
L4	1.22 uH bead	HE 475-15
L5	1.22 uH bead	HE 475-15
L6	1.22 uH bead	HE 475-15
L7	1.22 uH bead	HE 475-15
L8	1.22 uH bead	HE 475-15
L9	1.22 uH bead	HE 475-15
L10	1.22 uH bead	HE 475-15
L11	1.22 uH bead	HE 475-15
L12	1.22 uH bead	HE 475-15
L13	1.22 uH bead	HE 475-15
L14	1.22 uH bead	HE 475-15
L15	1.22 uH bead	HE 475-15
L16	1.22 uH bead	HE 475-15
L17	1.22 uH bead	HE 475-15
L18	1.22 uH bead	HE 475-15
L19	35 uH	HE 235-229
L20	35 uH	HE 235-229
L21	35 uH	HE 235-229
L22	35 uH	HE 235-229
L23	35 uH	HE 235-229

RESISTORS

R1	10 kilohm control		HE 10-1154
R2	100 kilohm control		HE 10-1180
R3	2 kilohm control		HE 10-1137
R4	2 kilohm control		HE 10-1137
R5	47 ohm	1/4 watt, 5%	HE 6-470-12
R6	none		
R7	47 kilohm	1/4 watt, 5%	HE 6-473-12
R8	jumper		
R9	1 megohm	1/4 watt, 5%	HE 6-105-12
R10	1000 ohm	1/4 watt, 5%	HE 6-102-12
R11	3900 ohm	1/4 watt, 5%	HE 6-392-12
R12	1800 ohm	1/4 watt, 5%	HE 6-182-12
R13	47 kilohm	1/4 watt, 5%	HE 6-473-12
R14	jumper		
R15	720 ohm	1/4 watt, 1%	HE 6-7200-12
R16	none		
R17	none		
R18	120 kilohm	1/4 watt, 5%	HE 6-124-12
R19	237 ohm	1/4 watt, 1%	HE 6-2370-12
R20	1 megohm	1/4 watt, 5%	HE 6-105-12
R21	3900 ohm	1/4 watt, 1%	HE 6-3901-12
R22	2200 ohm	1/4 watt, 1%	HE 6-2201-12
R23	1000 ohm	1/4 watt, 5%	HE 6-102-12
R24	120 kilohm	1/4 watt, 5%	HE 6-124-12
R25	1000 ohm	1/4 watt, 5%	HE 6-102-12
R26	1000 ohm	1/4 watt, 5%	HE 6-102-12

RESISTOR PACKS

RP1	150 ohm	HE 9-120
RP2	150 ohm	HE 9-120
RP3	10 kilohm	HE 9-106
RP4	4.7 kilohm	HE 9-133

DISK CONTROLLER CIRCUIT BOARD (CONTINUED)

INTEGRATED CIRCUITS

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
PS1	7805 5V regulator	HE 442-54
PS2	78M12 +12V regulator	HE 442-663
PS3	LM317 +adj regulator	HE 442-708
U1	WD1691	HE 443-998
U2	none	
U3	2143-01	HE 443-1000
U4	74LS74	HE 443-730
U5	74LS624	HE 443-999
U6	74LS132	HE 443-792
U7	74LS33	HE 443-1063
U8	7417	HE 443-72
U9	74LS241	HE 443-824
U10	74S240	HE 443-753
U11	7417	HE 443-72
U12	74LS74	HE 443-730
U13	74LS125	HE 443-811
U14	74LS74	HE 443-730
U15	96LS02	HE 443-1040
U16	96LS02	HE 443-1040
U17	74LS138	HE 443-877
U18	4.000 MHz oscillator	HE 150-132
U19	74LS175	HE 443-752
U20	74LS74	HE 443-730
U21	74LS32	HE 443-875
U22	FD1797B02	HE 443-997
U23	74LS20	HE 443-798
U24	74LS138	HE 443-877
U25	74LS27	HE 443-800
U26	74S74	HE 443-900
U27	74LS00	HE 443-728
U28	74LS02	HE 443-779
U29	74LS688	HE 443-971
U30	74LS273	HE 443-805
U31	74LS365A	HE 443-1039
U32	7417	HE 443-72
U33	74LS244	HE 443-791
U34	74LS244	HE 443-791
U35	74LS374	HE 443-863
U36	74LS244	HE 443-791

OTHER CIRCUIT COMPONENTS

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
D1	1N4148 diode	HE 56-84
D2	1N4148 diode	HE 56-84
D3	1N4148 diode	HE 56-84
DS1	8-section slide switch	HE 60-621
Q1	TIS74 transistor	HE 417-246
Q2	MPS2369 transistor	HE 417-937
Q3	MPS2369 transistor	HE 417-937

CONNECTORS - SOCKETS

	1-pin connector	HE 423-121
	8-pin inline IC socket	HE 434-230
	14-pin IC socket	HE 434-298
	16-pin IC socket	HE 434-299
	18-pin IC socket	HE 434-310
	20-pin IC socket	HE 434-311
	40-pin IC socket	HE 434-253
P2	34-pin right-angle connector	HE 432-1053
P1	50-pin right-angle connector	HE 432-1197

HARDWARE

	#4 lockwasher	HE 254-9
	4-40 nut	HE 252-2
	4-40 x 5/16" screw	HE 250-213

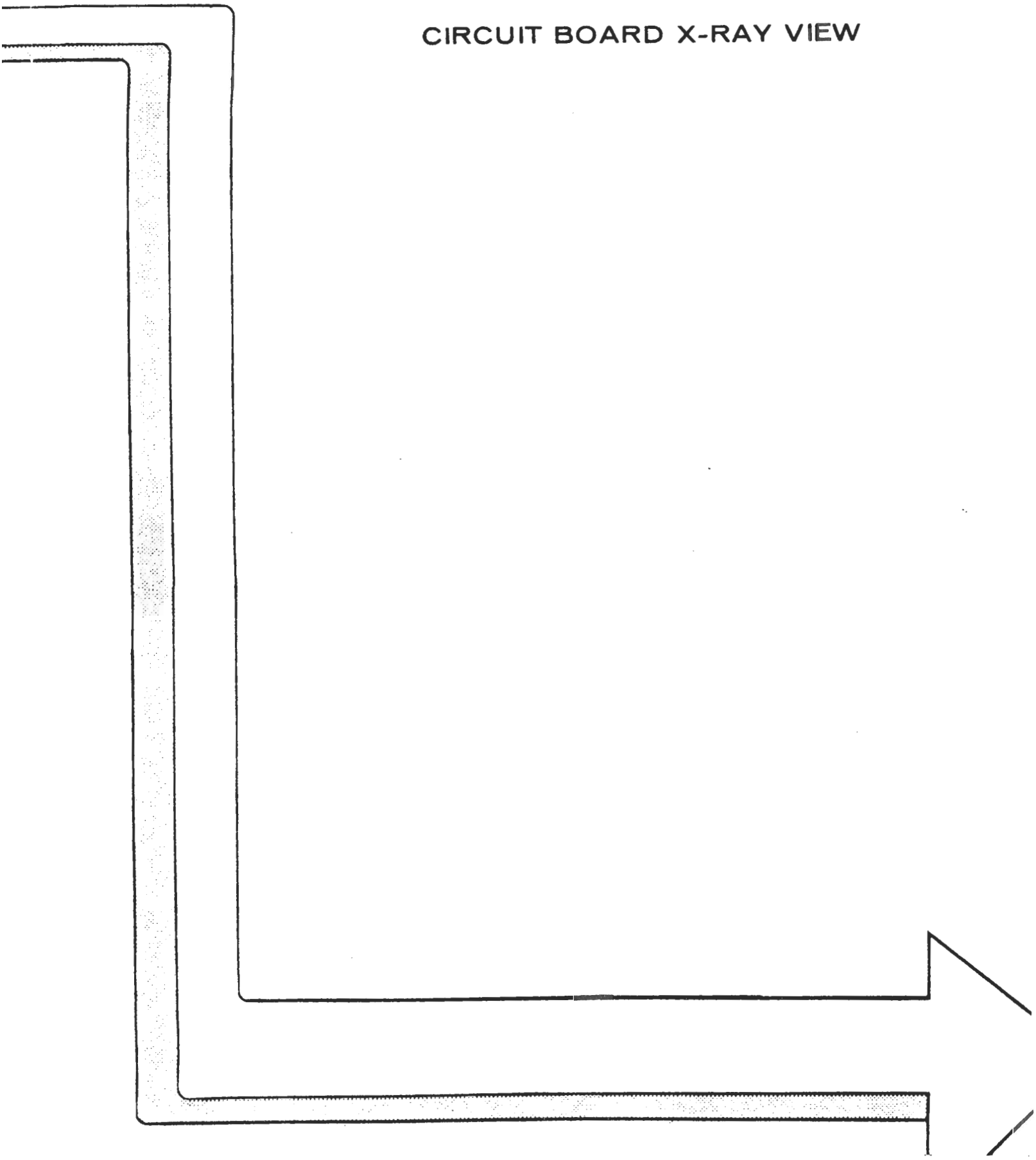
MISCELLANEOUS

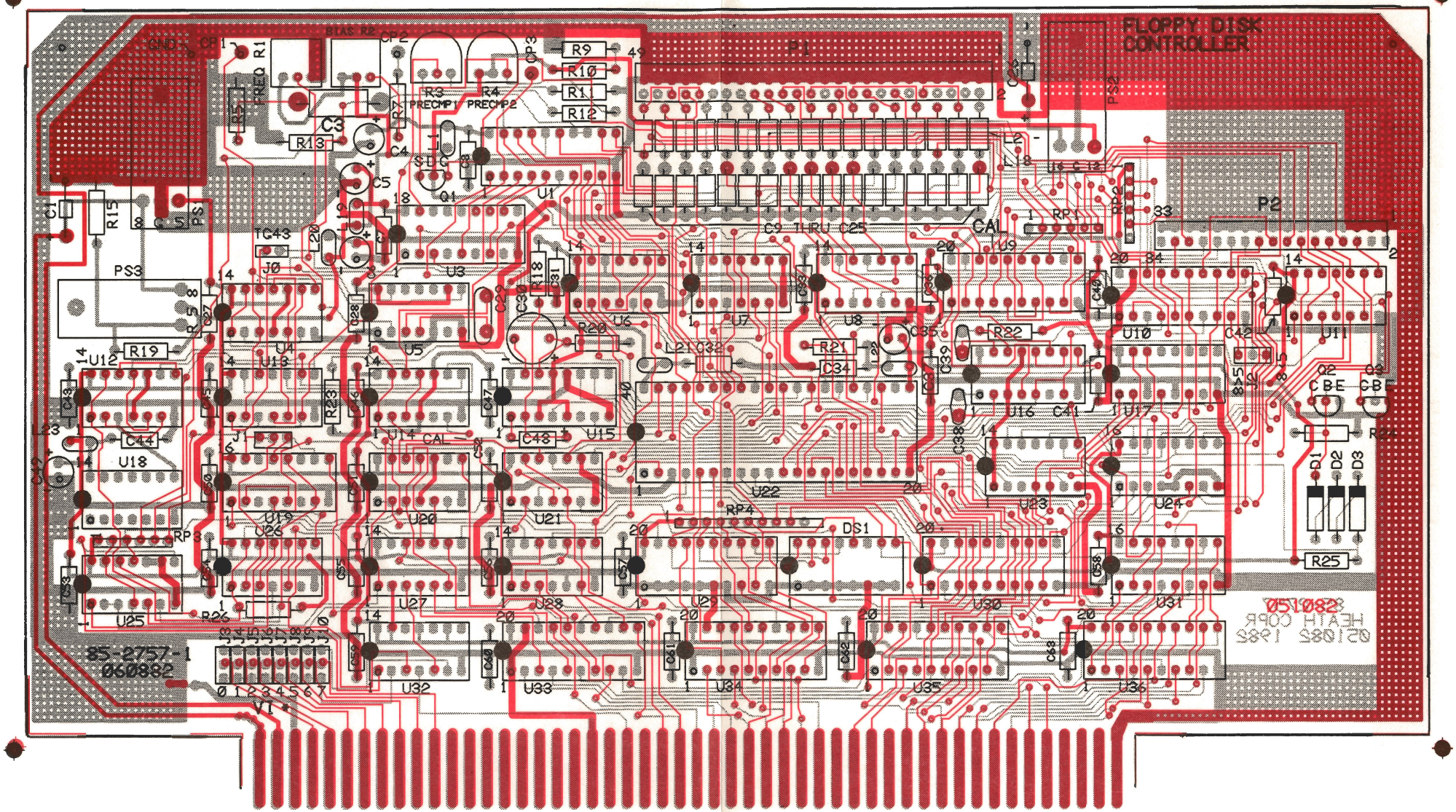
	Heat sink	HE 215-669
	H-207 manual	HE 595-2909
	PC board	HE 85-2757-2
	Silicone grease	HE 352-13
	S-100 circuit board extractor	HE 266-1203
	Wire, solid	HE 340-8
	Wire, white solid	HE 344-59

CALIBRATION CIRCUIT BOARD

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
R501	10 kilohm 1/4 watt, 5%	HE 6-103-12
R502	330 ohm 1/4 watt, 5%	HE 6-331-12
C501	.1 uF ceramic	HE 21-762
DL501	Delay line	HE 41-10
	Alligator clip insulator	HE 73-34
	PC board	HE 85-2800-1
	Alligator clip	HE 260-16
	Wire, black stranded	HE 344-90
	Wire, red stranded	HE 344-92
	Wire, white stranded	HE 344-94
D501	LST5053 LED	HE 412-640
	1-pin socket	HE 432-120
	14-pin IC socket	HE 434-298
U501	74LS00	HE 443-728
U502	74LS74	HE 443-730

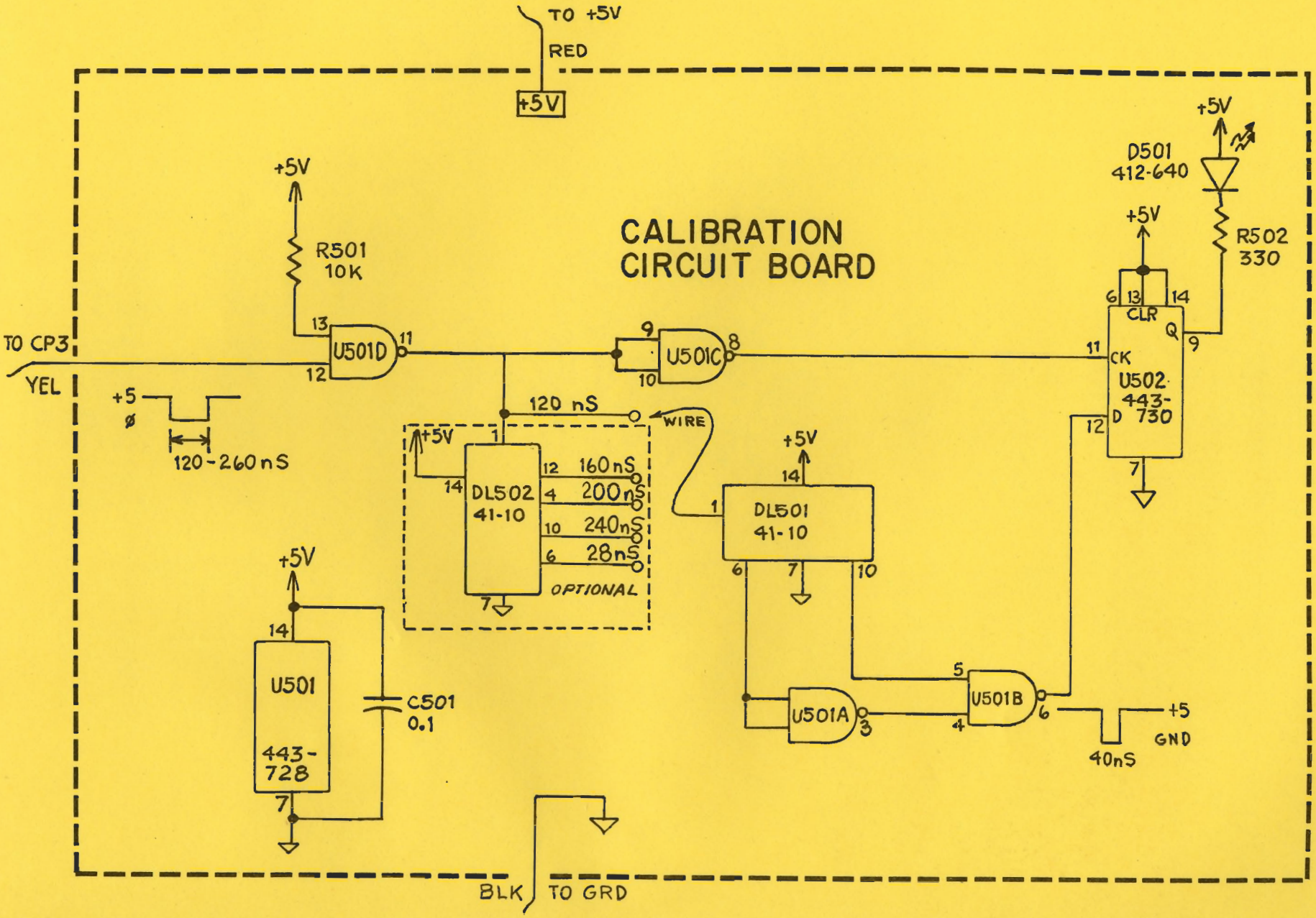
CIRCUIT BOARD X-RAY VIEW





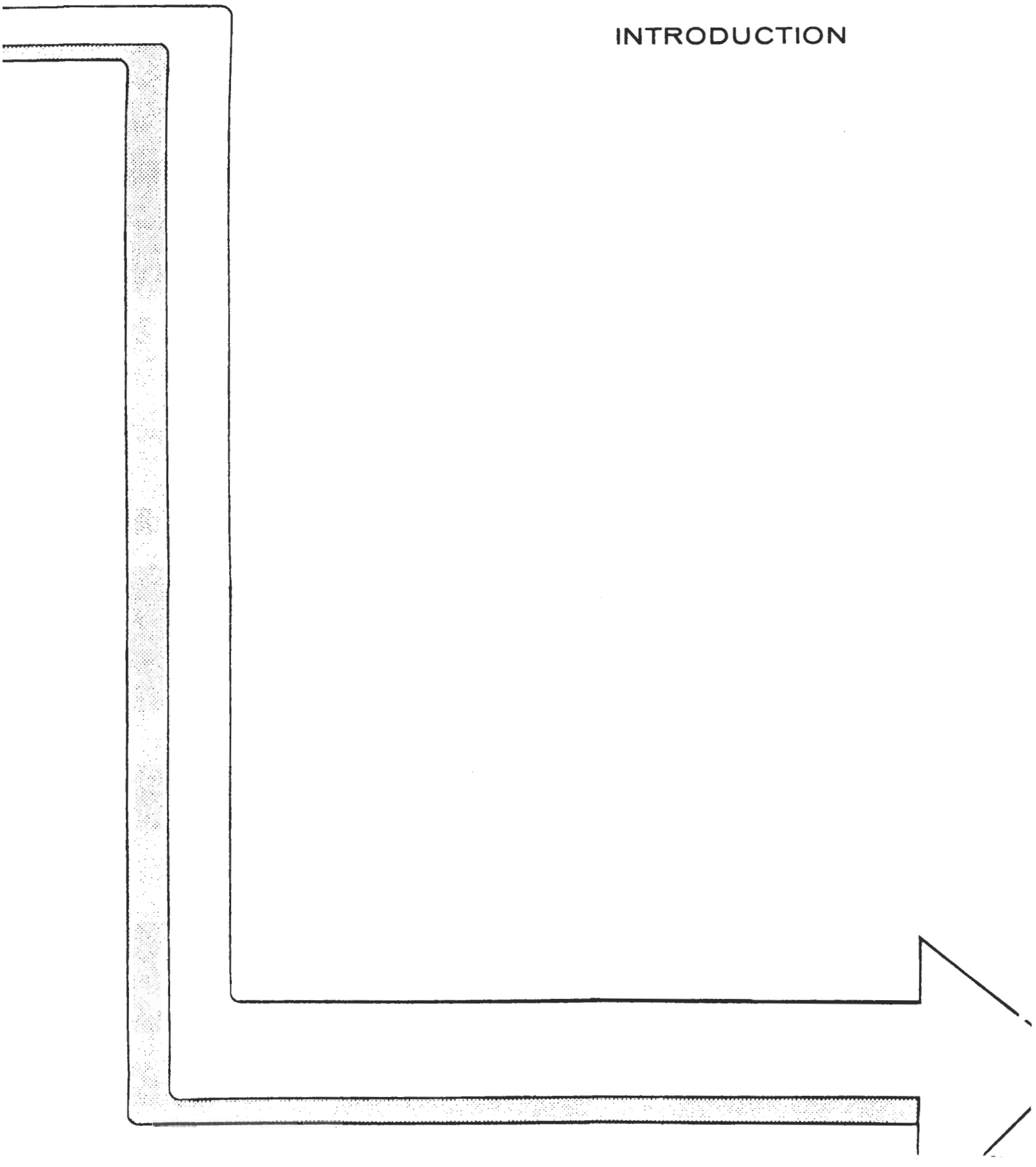
DISK CONTROLLER CIRCUIT BOARD (#HE-85-2757-1)

(SHOWN FROM COMPONENT SIDE)


TO +5V
RED
+5V
CALIBRATION
CIRCUIT BOARD
+5V
R501
10K
TO CP3
YEL
U501D
U501C
+5
ø
120-260nS
120 nS
WIRE
+5V
DL502
41-10
12 160nS
4 200nS
10 240nS
6 28nS
OPTIONAL
+5V
DL501
41-10
+5V
U501
443-
728
C501
0.1
U501A
U501B
40nS
+5
GND
+5V
D501
412-640
R502
330
CLR
CK
U502
443-
730
BLK
TO GRD

VIDEO MONITOR

INTRODUCTION



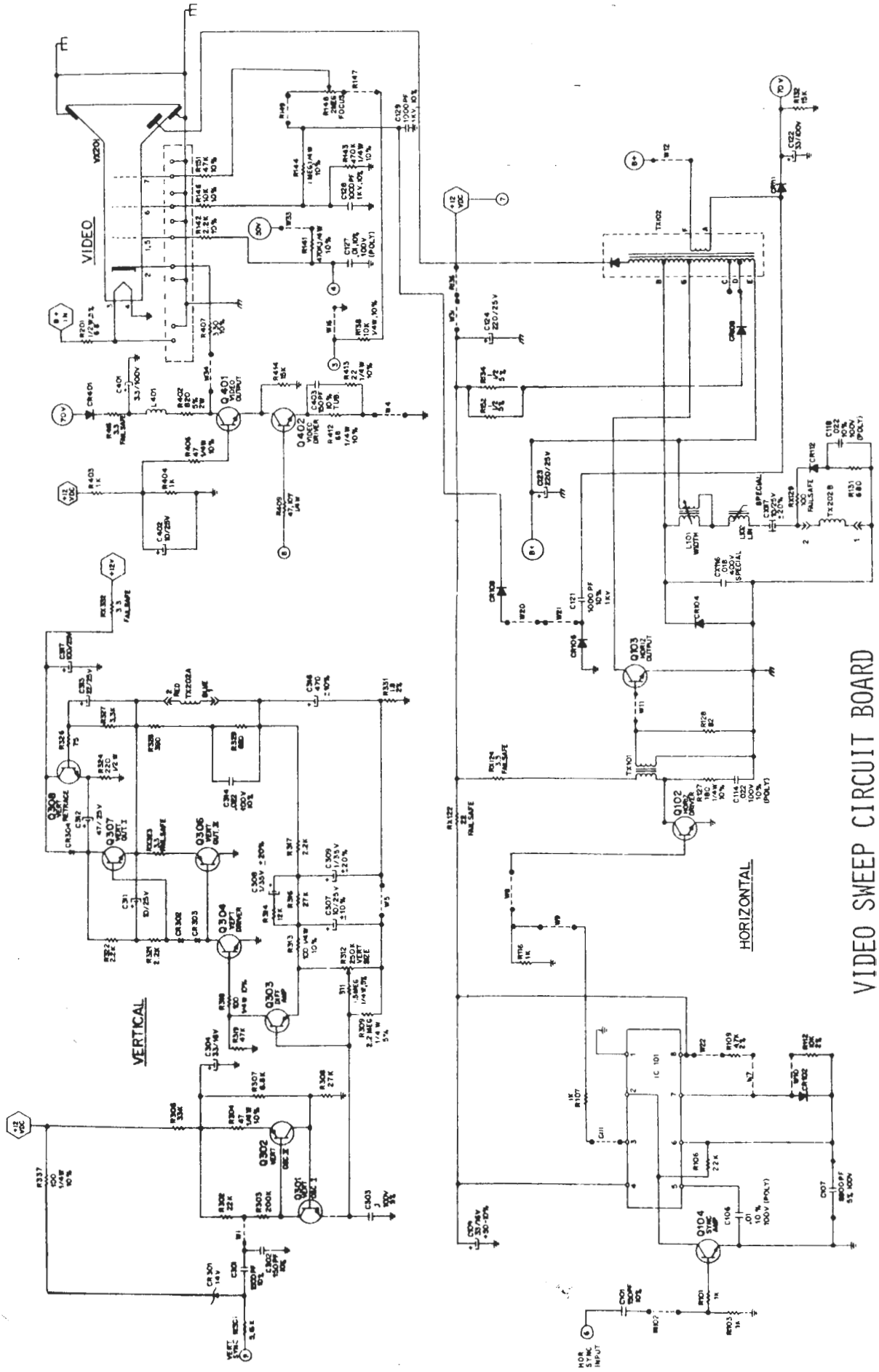
The video monitor in the All-in-One computer processes signals from the video board to produce a display on the CRT. This video monitor consists of two main parts: a high-resolution CRT and a sweep board.

The high-resolution CRT is necessary to transform the wide-band video information from the video board into a high-resolution display. A choice of three different CRT phosphors are available: green, amber, or white. Green phosphor is standard in the All-in-One computer, while amber and white are optional.

The sweep board in the video monitor produces vertical and horizontal sweep signals, high voltage to operate the CRT, and video drive for the CRT.

The information in this section will aid you in isolating and correcting problems that exist in the CRT and the sweep board.

CIRCUIT DESCRIPTION


VIDEO
VERTICAL
HORIZONTAL
VIDEO SWEEP CIRCUIT BOARD

OVERVIEW

The video sweep board is used in the All-In-One version H/Z-100 to convert the TTL signals from the video board to the voltages necessary to drive the CRT. The sweep board contains the vertical circuits, the horizontal circuits, the video amplifier, and the high-voltage power supply.

VERTICAL CIRCUITS

The vertical sync signal couples through C301 to synchronize the vertical oscillator, Q301 and Q302. The oscillator output is at the emitter of Q301; C303 helps shape this signal for a linear sweep.

The oscillator signal couples to the base of Q303, which is wired as a differential amplifier. The base acts as the inverting input; the emitter as the non-inverting input. The vertical amplifier output feeds back to the emitter to ensure good linearity. The RC network between R312 and R317 set the gain and frequency response.

The output of Q303 drives the vertical driver and amplifier, Q304 through Q307. This stage develops the sweep current through the vertical deflection yoke at TX202A. Q308 ensures a fast vertical retrace.

HORIZONTAL CIRCUITS

The horizontal sync pulse couples through C101 and is amplified by Q104. Q104 passes the signal on to IC101. This IC shapes and retimes the signal before coupling it to the horizontal driver, Q102.

Q102 couples the signal through TX101 to Q103. R127 and C114 shape the signal while R128 dampens any ringing that may occur. The collector current of Q103 couples through the flyback transformer, the width coil, and the linearity coil to drive the horizontal deflection yoke at TX202B.

HIGH VOLTAGE POWER SUPPLY

The flyback transformer uses the signal from Q103 to generate the acceleration voltage for the CRT. This voltage is rectified before leaving the transformer. The secondary of TX102 also develops focus, blanking, and bias voltages for the CRT. This is taken care of through C121, CR106, and CR108.

In addition, the secondary of T102 develops bias voltages for the horizontal circuits (B+) and the video amplifier (70 V).

VIDEO AMPLIFIER

The video amplifier is a cascode amplifier consisting of Q401 and Q402. This circuit is characterized by its high gain, low noise, and low input and output capacitances.

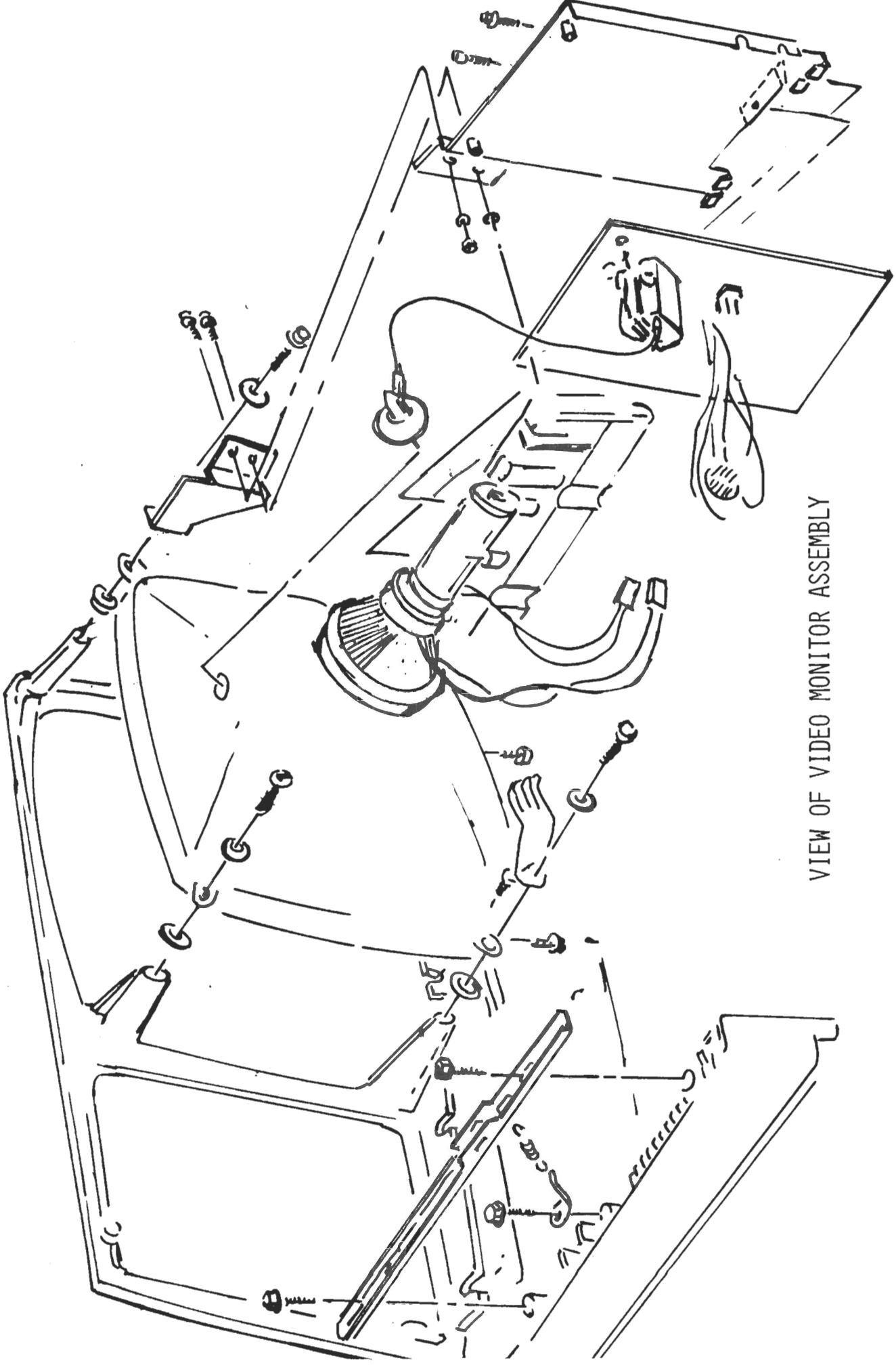
The video signal enters at the base of Q402. A positive voltage at this point is white information; Q401 and Q402 conduct to make the CRT cathode more negative.

The 68-ohm resistor in the emitter of Q402 sets the overall stage gain while C403, R413, and L401 set the frequency response.

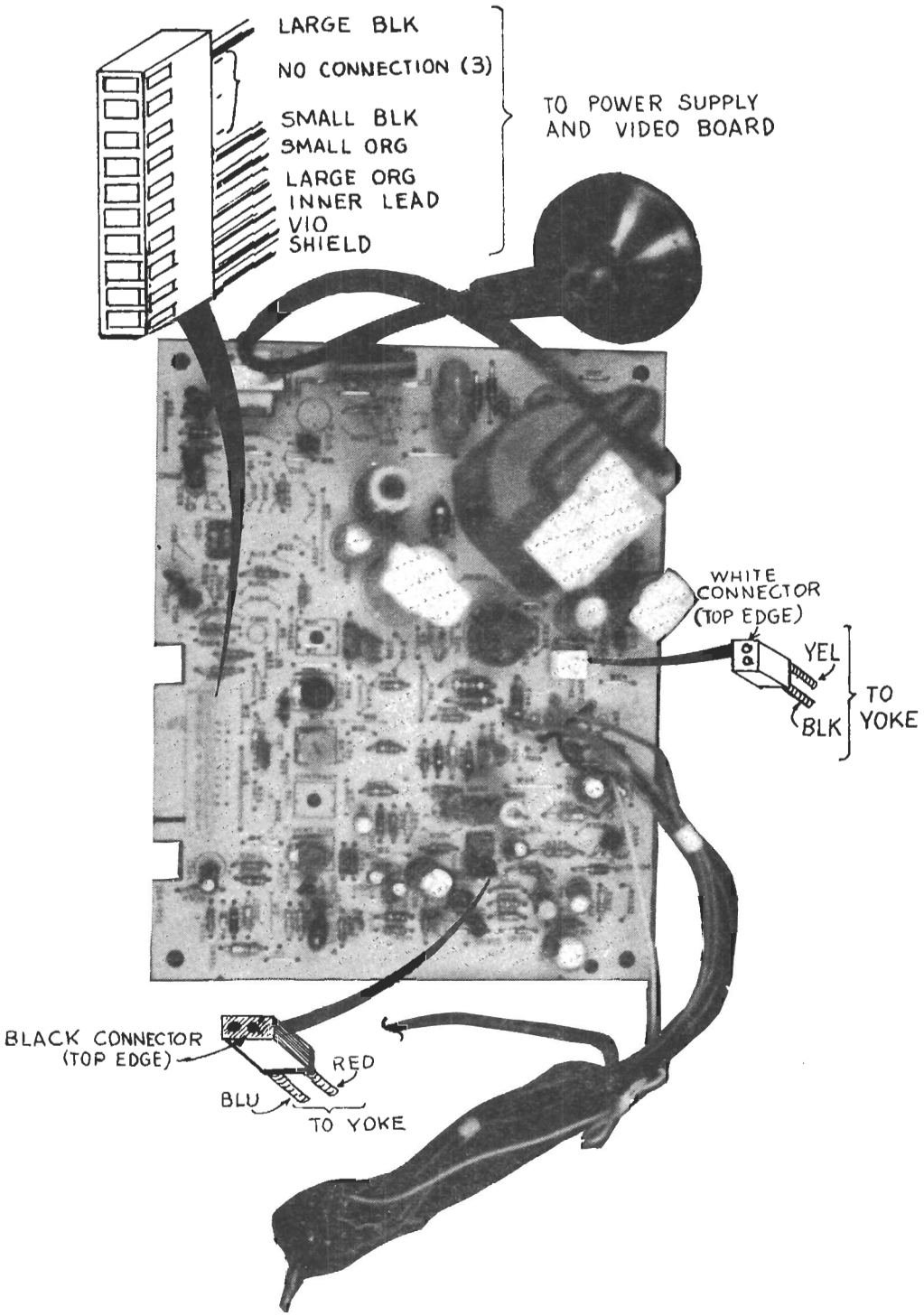
POWER SUPPLY

Power for the video sweep board is a single 12-volt source from the H/Z-100 power supply.

VISUAL CHECKS



VIEW OF VIDEO MONITOR ASSEMBLY



SWEEP BOARD CONNECTIONS

ALIGNMENT AND ADJUSTMENTS

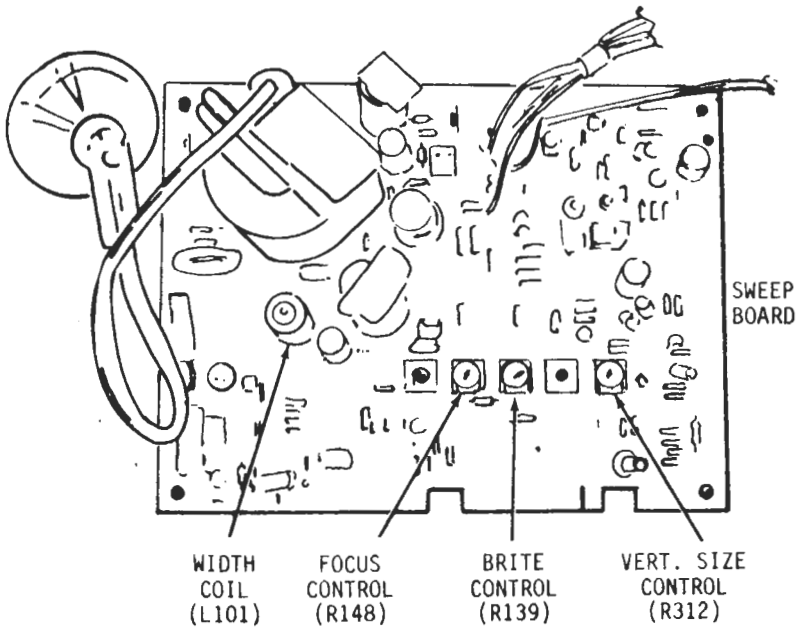
Adjusting the sweep board in the H/Z-100 All-in-One computer is a simple process. The only tools required are an adjusting tool (HE 490-1), a small insulated screwdriver, a short 3/16" nutdriver, and a bootable disk containing Z-BASIC. To reach the controls, the cabinet top will have to be removed. Follow the procedure below to adjust the controls on the sweep board.

-- Set section 3 of the motherboard configuration switch (S101) to the 0 position. This will disable the auto-boot.

-- Refer to the pictorial below and set the following controls of the sweep circuit board to the center of their rotation:

FOCUS (R148)
VERT. SIZE (R312)
BRIGHTNESS CONTROL (on back panel)

-- Set the BRITE control (R139) fully clockwise.



-- Apply power to the computer. A hand prompt, cursor and raster should appear in 20 to 30 seconds. If not, adjust the BRIGHTNESS CONTROL on the back panel until a raster appears.

-- If the display is tilted, loosen the yoke clamp with the 3/16" nutdriver and rotate the yoke to obtain a level display.

-- Adjust the VERT. SIZE control (R312) until the display is about 6.5" high.

-- Rotate the ring magnets on the back of the yoke to center the display on the screen.

-- Now boot the diskette containing Z-BASIC.

-- Load Z-BASIC and enter the following program:

```
10 FOR I = 1 TO 2000
20 PRINT "H";
30 NEXT I
40 GOTO 40
```

-- Run the program. It will fill the screen with H's.

-- Dim the room lighting and turn the BRITE control (R139) until the raster just disappears.

-- Adjust the WIDTH COIL (L101) for a display width of about 8-1/2".

-- Adjust the FOCUS control (R148) for best focus.

-- Recheck the display for proper alignment of the screen and then tighten the yoke clamp screw only enough to keep the yoke from turning.

-- Touch up the controls as necessary to obtain a good display.

-- Control C out of the BASIC program and dismount the disk.

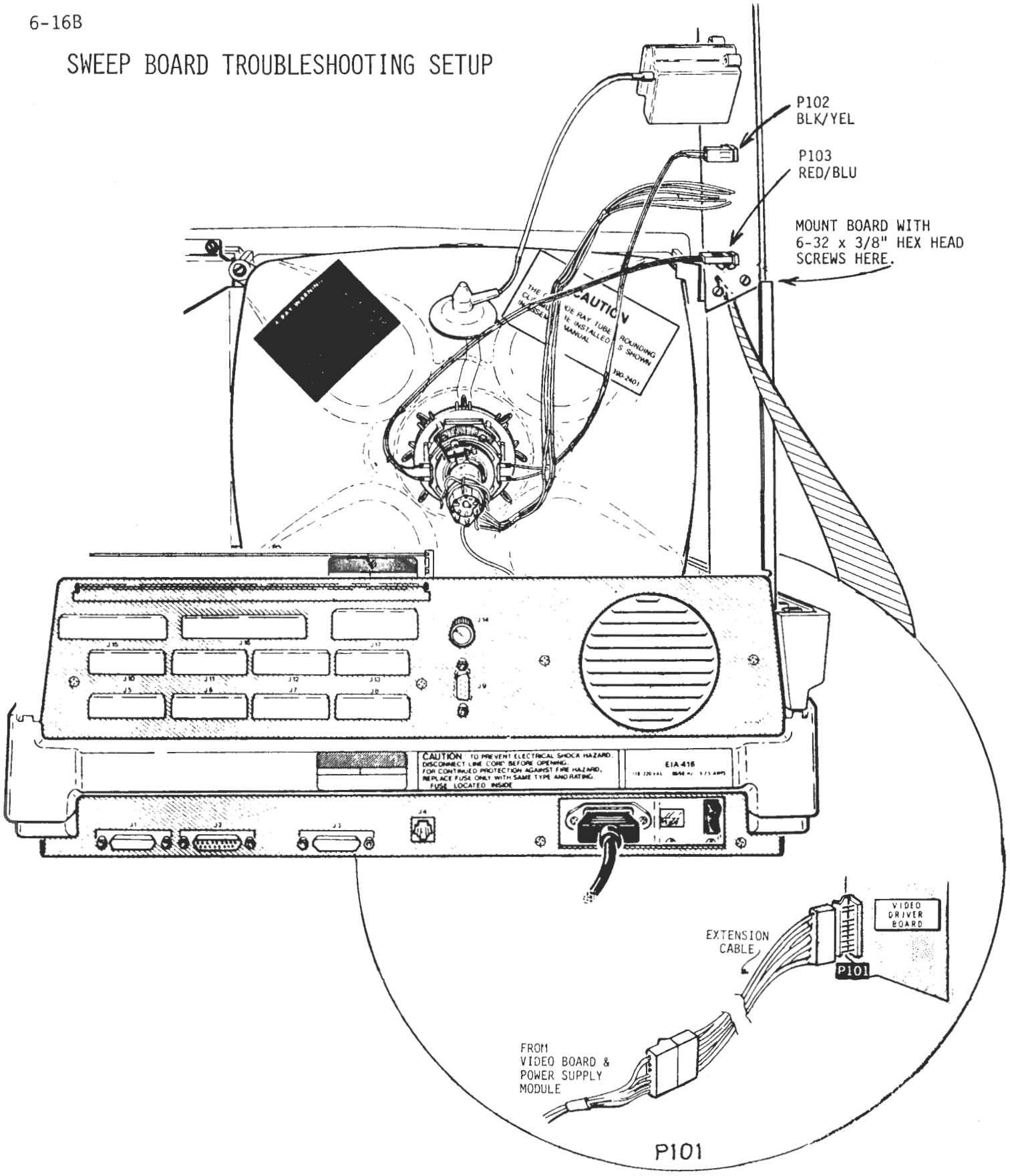
-- Turn off the computer.

-- Reset section 3 of S101 (on the motherboard) to its original position.

This completes alignment of the sweep circuit board.

TROUBLESHOOTING

SWEEP BOARD TROUBLESHOOTING SETUP



INTRODUCTION

The following service information applies only to the video sweep board used in the HS-120 All-In-One kit computer. Foil patterns and schematics for the ZF-120 series wired computers may be different.

INITIAL SETUP

This section describes two setup procedures: the preferred setup procedure and the alternate setup procedure. The preferred procedure allows you easy access to both sides of the video sweep board. On some units, however, the factory-wired cables may be too short to reach their connectors. If this is the case, use the alternate setup procedure. This second procedure requires fewer steps to set up, but doesn't allow you as easy access to all the components as does the first.

PREFERRED SETUP PROCEDURE

Refer to the Sweep Board Troubleshooting Setup illustration as you perform the following steps.

-- Unplug P101, P102, and P103.

-- Remove the two 6-32 x 3/8" hex-head screws from the top of the video sweep board.

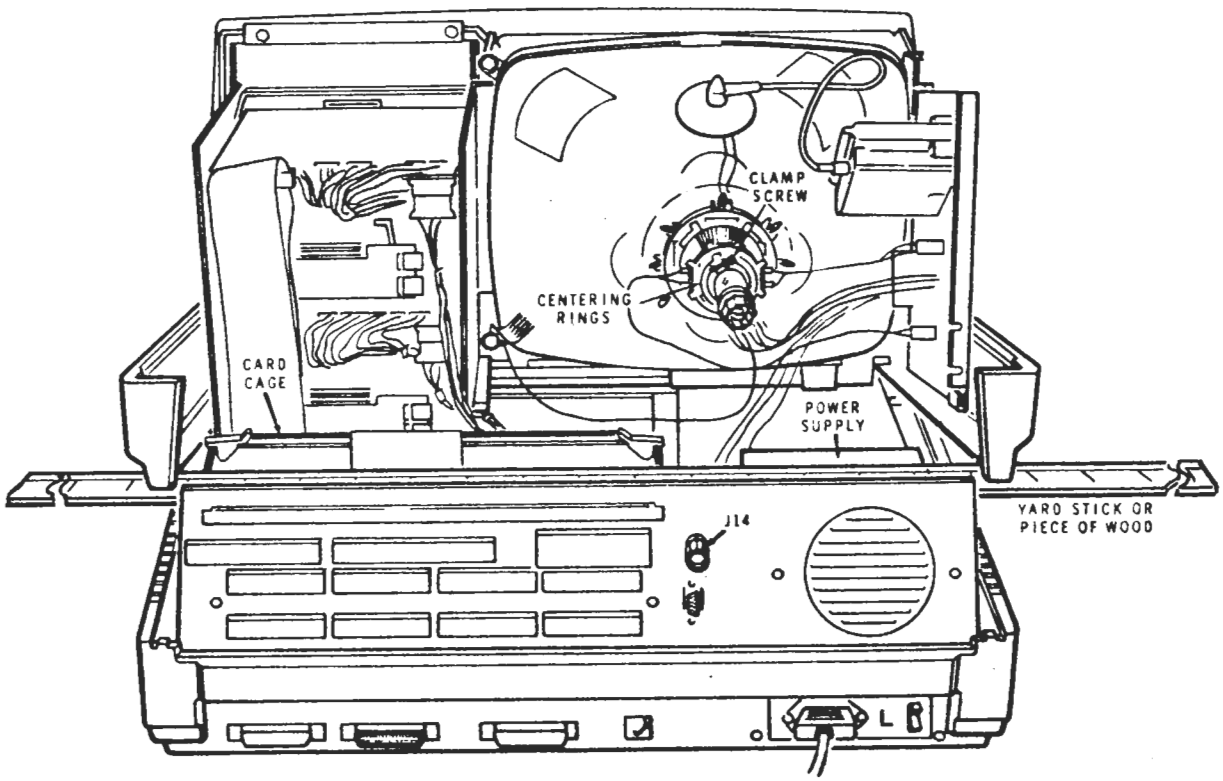
-- Position the sweep board so that the bottom holes on the circuit board line up with the two threaded spacers on the shield. Secure the sweep board with the two 6-32 x 3/8" hex-head screws.

-- Reinstall the horizontal and vertical yoke connectors. The black/yellow cable goes to P102 and the red/blue cable goes to P103.

-- Use the video board extender cable (see page 2-101 for construction details) to connect the video signal and power to P101.

ALTERNATE SETUP PROCEDURE

Perform the following if the yoke and CRT cables are too short to permit using the preferred setup procedure.



-- Remove the hardware holding the CRT/disk drive assembly to the bottom cover (See page 2-72 for disassembly instructions).

To perform the following step, you may have to unplug the ribbon cable to the 5-1/4" floppy drive controller board.

-- Position the CRT/disk drive assembly as shown and slide a wooden yardstick (or other nonconducting rod) between the top and bottom halves of the computer.

SERVICE INFORMATION

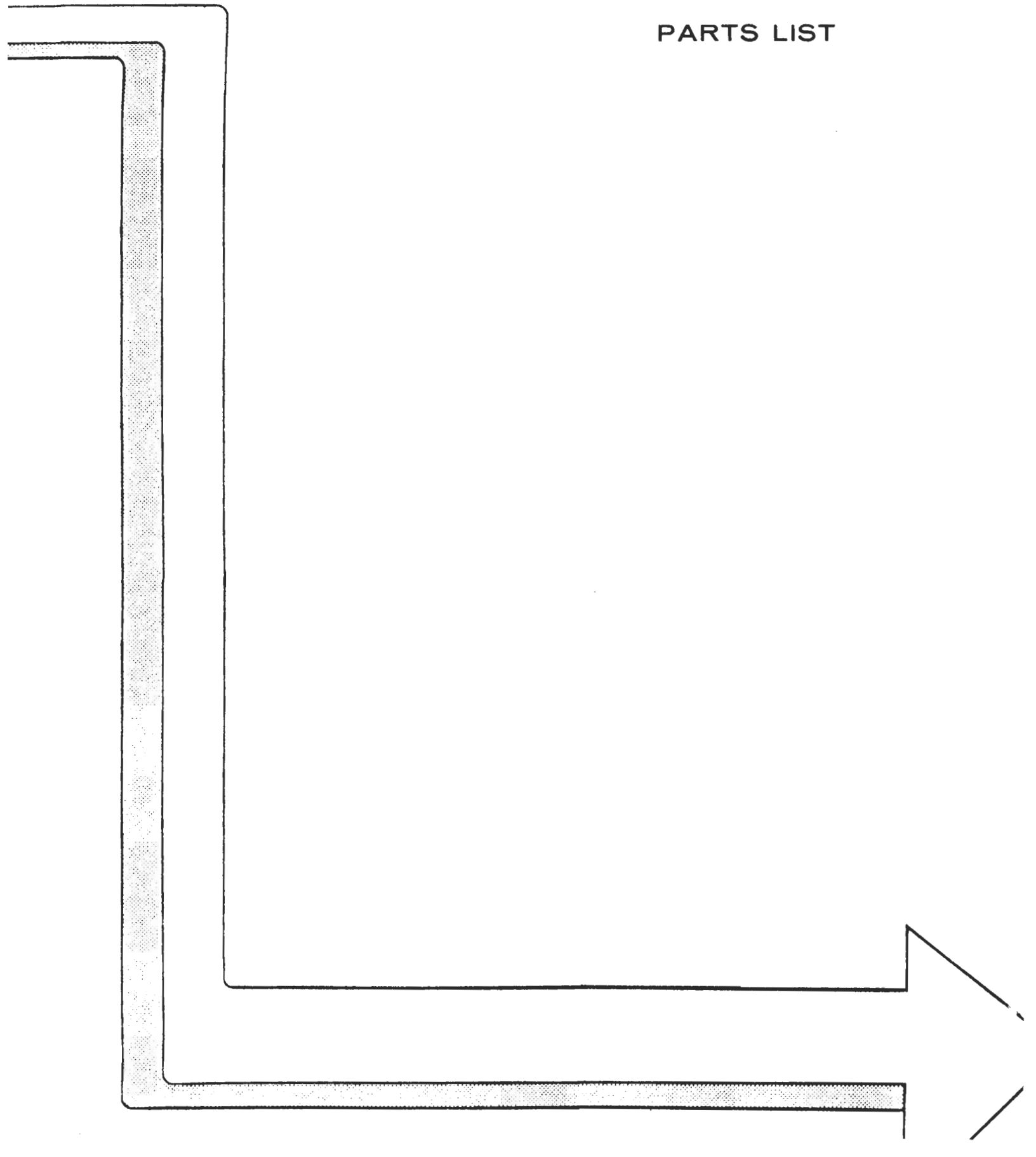
To troubleshoot the HS-120 sweep board, disable the auto-boot feature, turn on the computer, and perform a hard reset. Adjust the brightness control on the rear panel for a viewable "hand" prompt. Refer to the HS-120 schematic, waveforms, and x-ray view for voltage and parts location information.

Note that the voltages at the potentiometers will depend on the setting of the control. The values shown are for a properly adjusted unit. Also, the waveforms for the video circuits are those present when the rear panel brightness control, J14, is turned full clockwise.

High voltages are present at several locations on this circuit board. Be careful when taking a measurement.

When you've finished servicing and aligning the board, perform the final checks listed on page 2-117.

PARTS LIST



PARTS LIST

SWEEP BOARD

CIRCUIT Comp. No.	DESCRIPTION	ZENITH Part No.
ASSEMBLIES		
	Deflection Yoke Assembly	A-8337
	PC Board Assembly	A-10520
CRTS1	CRT Socket Assembly	F-11943
Q103	Transistor & Heat Sink Assy	F-10173
CAPACITORS		
C101	150 PFD 10% 50V ceramic	22-7742
C106	0.01 MFD 10% 100V Polyester	22-7774-12
C107	.0068 MFD 5% 100V Polyester	22-7773-10
C109	33 MFD +50-10% 16V electro	22-7707-07
C114	0.022 MFD 10% 100V poly	22-7774-16
C118	0.022 MFD 10% 100V poly	22-7774-16
C119	1000 PFD 10% 1000V ceramic	22-3748
C121	1000 PFD 10% 1000V ceramic	22-3748
C122	3.3 MFD +50-10% 100V electr	22-7712-07
C123	220 MFD +50-10% 25V electro	22-7708-10
C124	220 MFD +50-10% 25V electro	22-7708-10
C126	0.01 MFD 10% 100V Polyester	22-7774-12
C127	0.01 MFD 10% 100V Polyester	22-7774-12
C128	1000 PFD 10% 1000V ceramic	22-3748
C129	1000 PFD 10% 1000V ceramic	22-3748
C301	1500 PFD 10% 50V ceramic	22-7742-12
C302	150 PFD 10% 50V ceramic	22-7742
C303	0.1 MFD 5% 100V Polyester	22-7773-24
C304	33 MFD +50-10% 16V electro	22-7707-07
C307	10 MFD 10% 25V electrolytic	22-7389-14
C308	1 MFD 20% 35V electrolytic	22-7713-02
C309	1 MFD 20% 35V electrolytic	22-7713-02
C311	47 MFD +50-10% 25V electro	22-7708-08
C312	47 MFD +50-10% 25V electro	22-7708-08
C313	33 MFD +50-10% 25V electro	22-7708-05
C314	0.022 MFD 10% 100V polyest	22-7774-16
C316	470 MFD 10% 16V electrolyt	22-7579-12
C317	220 MFD +50-10% 25V electr	22-7708-10
C401	3.3 MFD +50-10% 100V elect	22-712-03
C402	33 MFD +50-10% 25V electro	22-7708-05
C403	150 PFD 10% 50V ceramic	22-7742
CX116	0.022 MFD 5% 400V polyprop	22-7798-04
CX117	10 MFD 20% 25V nonplzo ele	22-7313

CIRCUIT Comp. No.	DESCRIPTION	ZENITH Part No.
DIODES		
CR102	Low Voltage General Silicon	103-142-01
CR104	Low Voltage General Silicon	103-298-03
CR106	Low Voltage General Silicon	103-323-04
CR107	Low Voltage General Silicon	103-295-03
CR109	Low Voltage General Silicon	103-339-02
CR111	Low Voltage General Silicon	103-323-04
CR112	Low Voltage General Silicon	103-254-01
CR301	Zener 14V 0.5W	103-279-23
CR302	Low Voltage General Silicon	103-142-01
CR303	Low Voltage General Silicon	103-142-01
CR304	Low Voltage General Silicon	103-254-01
CR401	Low Voltage General Silicon	103-254-01
INDUCTORS		
L101	RCF Tunable Width Control	20-3943-02
L102	RCF Linearity	20-3906
L401	RCF	20-3907-10
TRANSISTORS		
Q102	NPN Silicon	121-819
Q103	Transistor & Heat Sink Assy	F-10173
Q301	NPN Silicon	121-895
Q302	PNP Silicon	121-699
Q303	PNP Silicon	121-699
Q304	NPN Silicon	121-819
Q306	PNP Silicon	121-1036
Q307	NPN Silicon	121-1035
Q308	NPN Silicon	121-819
Q401	NPN Silicon	121-1058
Q402	NPN Silicon	121-895

CIRCUIT Comp. No.	DESCRIPTION	ZENITH Part No.
RESISTORS		
Future	68K ohm 10% 1/4W Carbon	63-10184-16
R101	1K ohm 5% 1/4W Film	63-10235-72
R103	1K ohm 5% 1/4W Film	63-10235-72
R106	22K ohm 5% 1/4W Film	63-10236-04
R107	1K ohm 5% 1/4W Film	63-10235-72
R108	22K ohm 10% 1/4W Carbon	63-10184-04
R109	4.7K ohm 2% 1/4W Film	63-10233-88
R112	10K ohm 2% 1/4W Film	63-10233-96
R116	1K ohm 5% 1/4W Film	63-10235-72
R122	22 ohm 5% 1/4W Film	63-10559-32
R127	180 ohm 10% 1/4W Carbon	63-10183-54
R128	82 ohm 5% 1/4W Film	63-10235-46
R131	680 ohm 5% 1/4W Film	63-10235-68
R132	15K ohm 5% 1/4W Film	63-10236
R137	10K ohm 10% 1/4W Carbon	63-10183-96
R138	10K ohm 10% 1/4W Carbon	63-10183-96
R139	Single rotary control	63-10651-12
R142	2.2K ohm 10% 1/2W Carbon	63-7799
R144	270K ohm 10% 1/4W Carbon	63-10184-30
R146	10K ohm 10% 1/2W Carbon	63-7827
R148	Single rotary control	63-1065-14
R149	270K ohm 10% 1/4W Carbon	63-10184-30
R151	47K ohm 10% 1/2W Carbon	63-7855
R301	5.6K ohm 5% 1/4W Film	63-10235-90
R302	22K ohm 5% 1/4W Film	63-10236-04
R303	200K ohm 5% 1/4W Film	63-10236-27
R304	47 ohm 10% 1/4W Carbon	63-10183-40
R306	27K ohm 5% 1/4W Film	63-10236-06
R307	6.8K ohm 5% 1/4W Film	63-10235-92
R308	27K ohm 5% 1/4W Film	63-10236-06
R309	2.2M ohm 5% 1/4W Carbon	63-10182-52
R311	1.5M ohm 5% 1/4W Carbon	63-10182-48
R313	100 ohm 10% 1/4W Carbon	63-10183-48
R314	12K ohm 5% 1/4W Film	63-10235-98
R316	27K ohm 5% 1/4W Film	63-10236-06
R317	2.2K ohm 5% 1/4W Film	63-10235-80
R318	100 ohm 10% 1/4W Carbon	63-10183-48
R319	47K ohm 5% 1/4W Film	63-10236-12

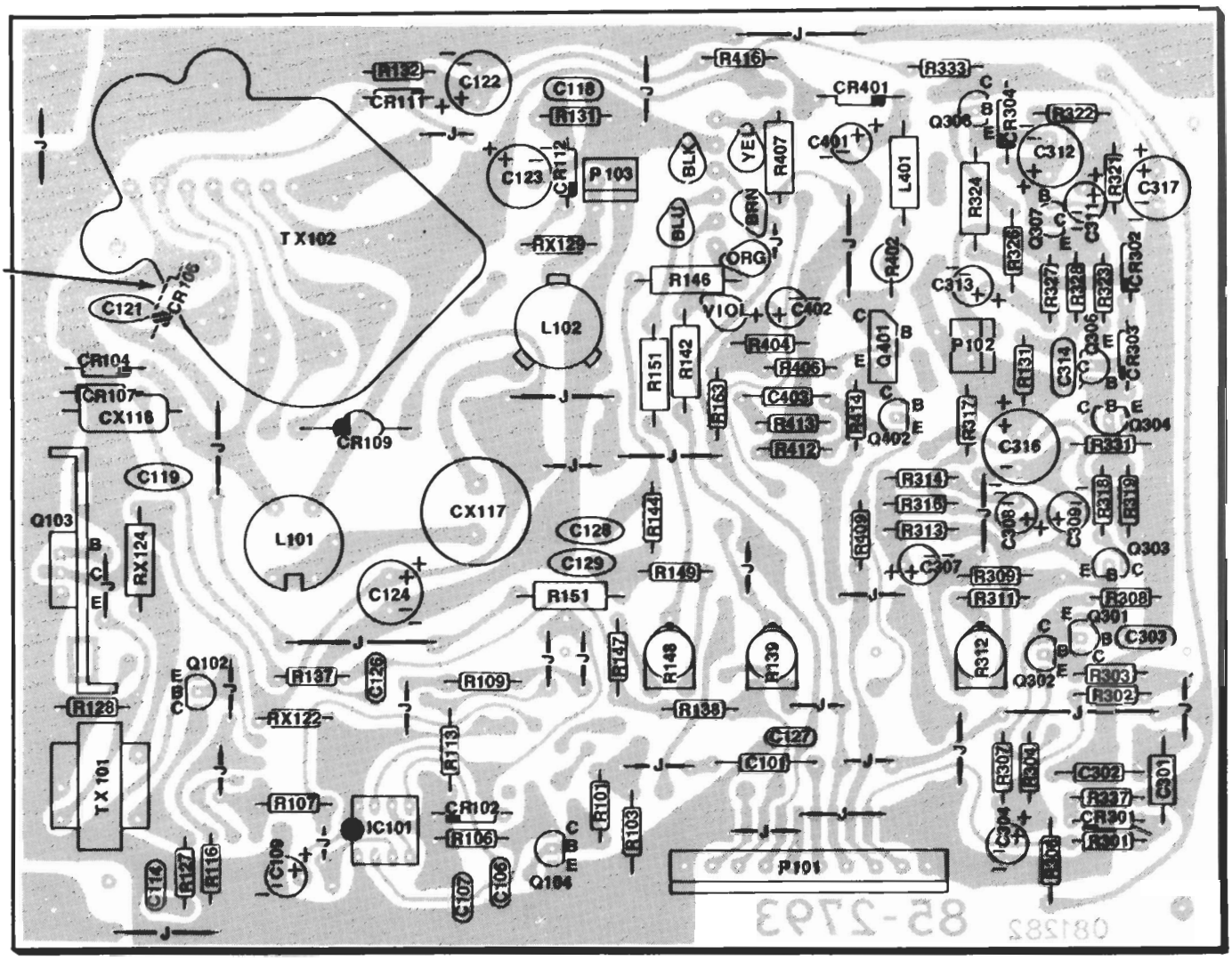
PARTS LIST

CIRCUIT Comp. No.	DESCRIPTION	ZENITH Part No.
RESISTORS (CONTINUED)		
R321	2.2K ohm 5% 1/4W Film	63-10235-80
R322	2.2K ohm 5% 1/4W Film	63-10235-80
R324	220 ohm 5% 1/2W Film	62-10243-56
R326	75 ohm 5% 1/4W Film	63-10235-45
R327	3.3K ohm 5% 1/4W Film	63-10235-84
R328	390 ohm 5% 1/4W Film	63-10235-62
R329	680 ohm 5% 1/4W Film	63-10235-68
R331	2.7 ohm 5% 1/4W Film	63-10235-10
R333	22 ohm 5% 1/4W Film	63-10559-32
R337	100 ohm 10% 1/4W Carbon	63-10183-48
R402	820 ohm 5% 2W Film	63-10836-70
R403	1K ohm 5% 1/4W Film	63-10235-72
R404	1K ohm 5% 1/4W Film	63-10235-72
R406	47 ohm 10% 1/4W Carbon	63-10183-40
R407	330 ohm 10% 1/2W Carbon	63-7764
R409	47 ohm 10% 1/2W Carbon	63-10183-40
R412	47 ohm 10% 1/2W Carbon	63-10183-40
R413	22 ohm 10% 1/4W Carbon	63-10183-32
R414	15K ohm 5% 1/4W Film	63-10236
R416	22 ohm 5% 1/4W Film	63-10559-32
RX124	10 ohm 5% 1/2W Film	63-10565-24
RX129	100 ohm 5% 1/4W Film	63-10559-48
RX323	3.3 ohm 5% 1/4W Film	63-10559-12
MISCELLANEOUS		
	Cable Retainer, Strap Tie 4"	19-773-01
	Cable Retainer, Strap Tie 7-1/2"	19-773-04
	Nut	54-986
	CRT Ground Spring	80-2377
	Terminal Strip, 10 position Male	83-9013-13
	Terminal Strip, Male	83-9013-03
	Label: X-Ray Hazard	101-6313
	Label: DAG Ground	101-6338
	Label: CSA	101-6339
	Label: X-Ray Emission	101-6583
	Label: X-Ray Emission	101-6583-01
	Hex Head Screw with Washer	114-976
IC101	CMOS I/C, Timer/Oscillator	221-217
TX101	Horizontal Driver Trans	95-3136-01
TX102	Sweep Transformer	95-3574-01

CIRCUIT Comp. No.	DESCRIPTION	ZENITH Part No.

CIRCUIT Comp. No.	DESCRIPTION	ZENITH Part No.

CR106
ON
FOIL SIDE

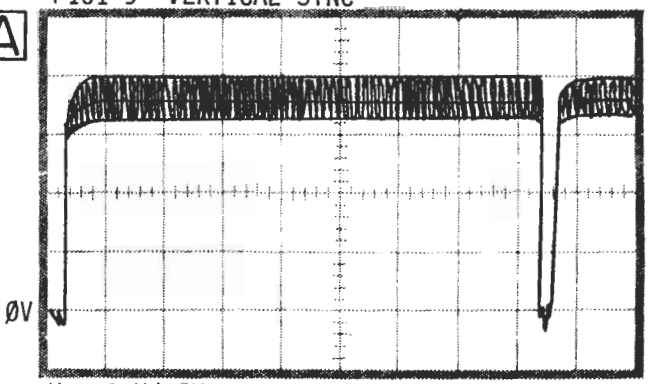


Video Board

(Shown from the component side.)

P101-9 VERTICAL SYNC

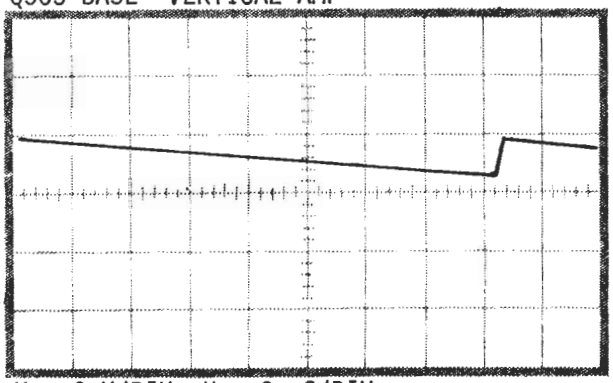
A



V = 1 V/DIV H = 2 mS/DIV

Q303 BASE VERTICAL AMP

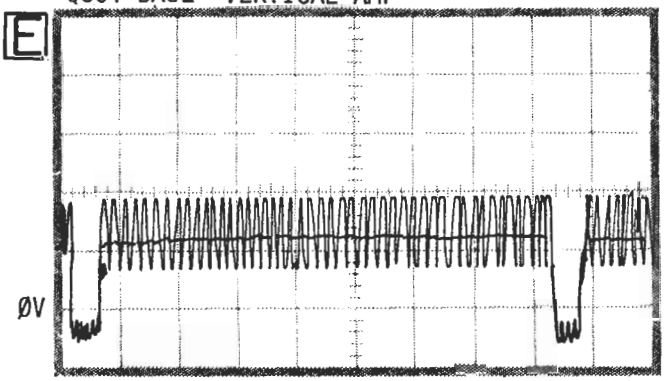
D



V = 2 V/DIV H = 2 mS/DIV

Q304 BASE VERTICAL AMP

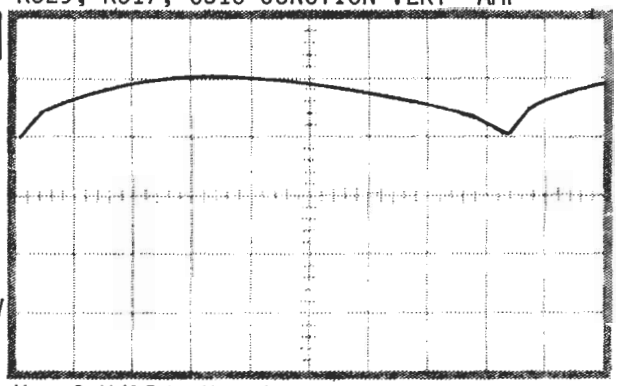
E



V = .5 V/DIV H = 2 mS/DIV

R329, R317, C316 JUNCTION VERT AMP

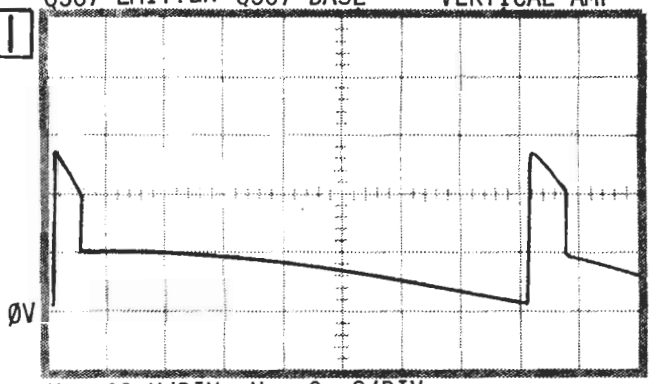
H



V = 2 V/DIV H = 2 mS/DIV

Q307 EMITTER Q307 BASE VERTICAL AMP

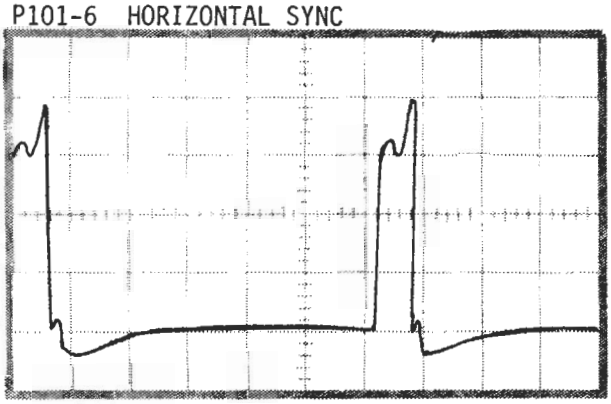
I



V = 10 V/DIV H = 2 mS/DIV

P101-6 HORIZONTAL SYNC

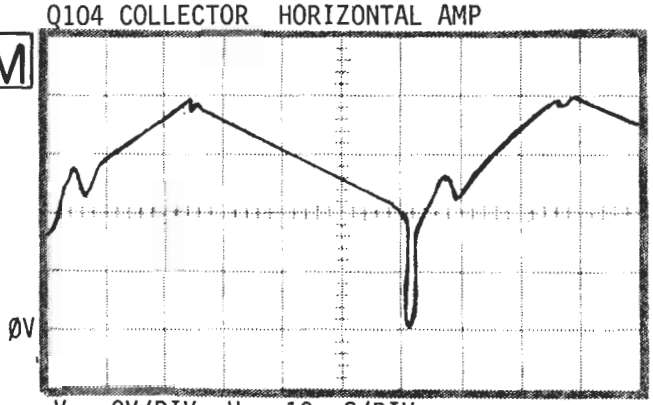
L



V = 1V/DIV H = 10 μS/DIV

Q104 COLLECTOR HORIZONTAL AMP

M

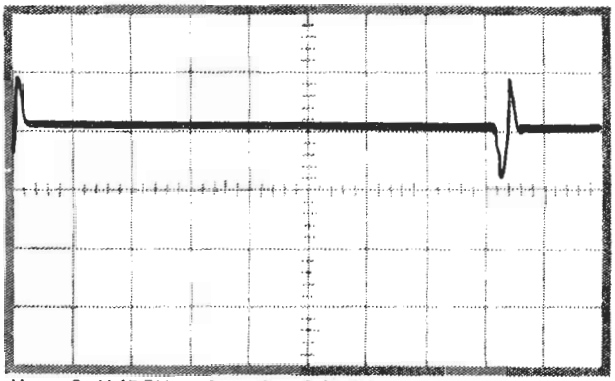


V = 2V/DIV H = 10 μS/DIV

HS-120 VIDEO SWEEP BOARD WAVEFORMS

Q301 COLLECTOR VERTICAL OSC.

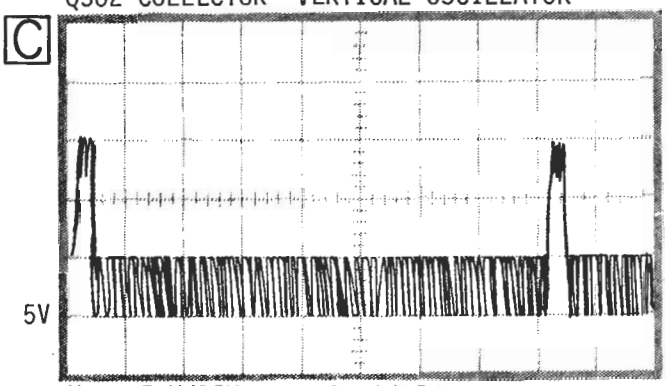
B



V = 2 V/DIV H = 2 mS/DIV

Q302 COLLECTOR VERTICAL OSCILLATOR

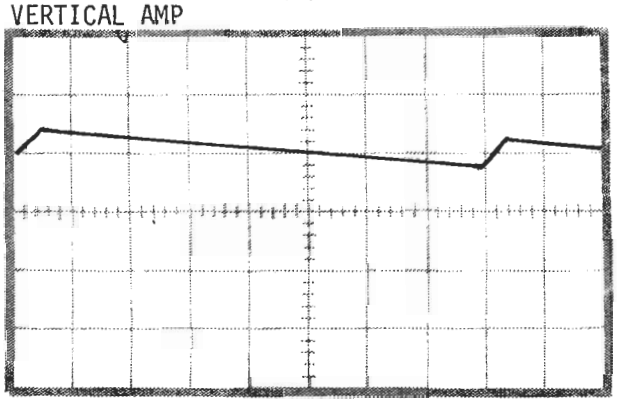
C



V = .5 V/DIV H = 2 mS/DIV

R313, R316 JUNCTION/Q303 EMITTER VERTICAL AMP

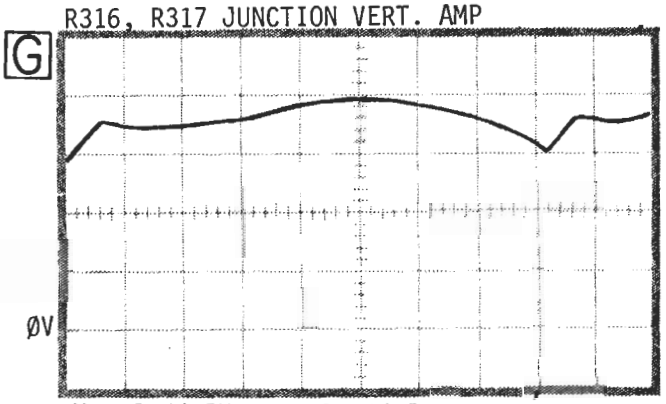
F



V = 2V/DIV H = 2 mS/DIV

R316, R317 JUNCTION VERT. AMP

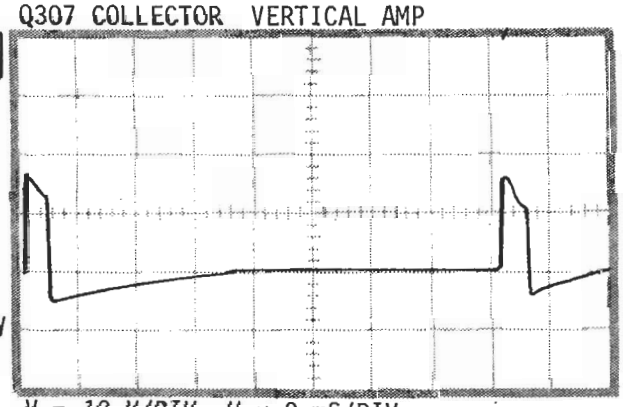
G



V = 2 V/DIV H = 2 mS/DIV

Q307 COLLECTOR VERTICAL AMP

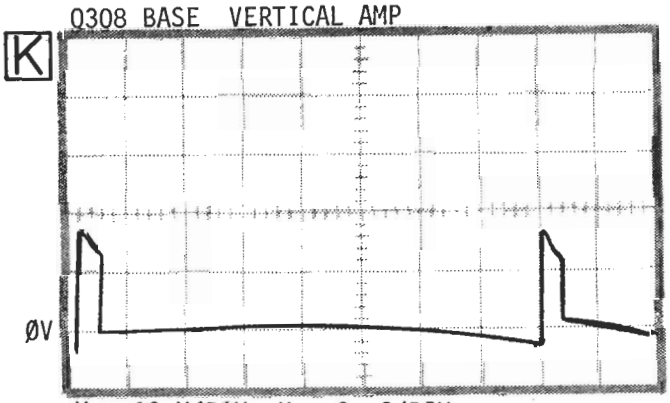
J



V = 10 V/DIV H = 2 mS/DIV

Q308 BASE VERTICAL AMP

K

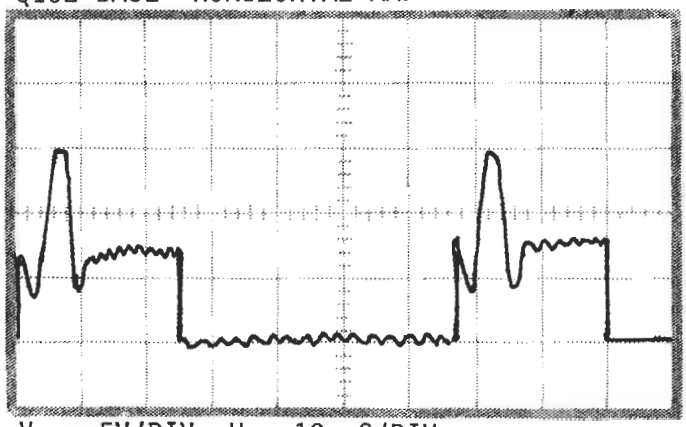


V = 10 V/DIV H = 2 mS/DIV

5/83

N

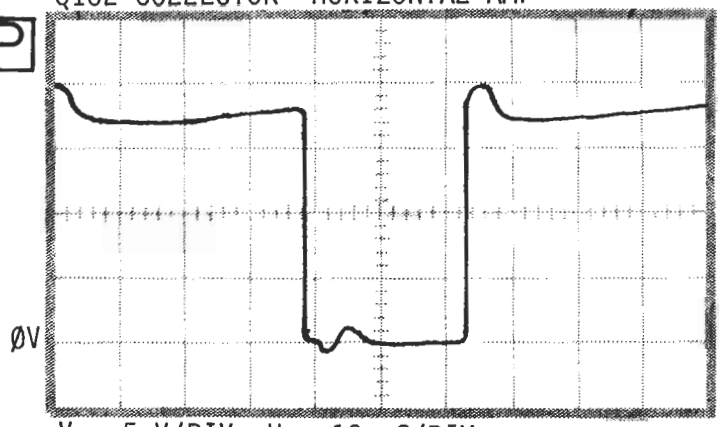
Q102 BASE HORIZONTAL AMP



V = .5V/DIV H = 10 µS/DIV

P

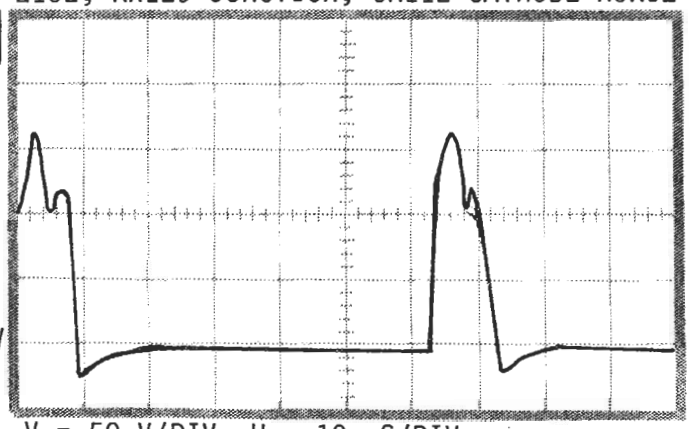
Q102 COLLECTOR HORIZONTAL AMP



V = 5 V/DIV H = 10 µS/DIV

S

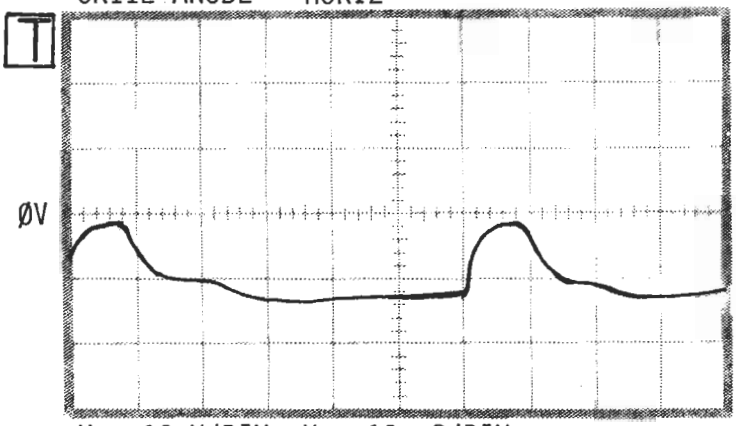
L102, RX129 JUNCTION, CR112 CATHODE HORIZ



V = 50 V/DIV H = 10 µS/DIV

T

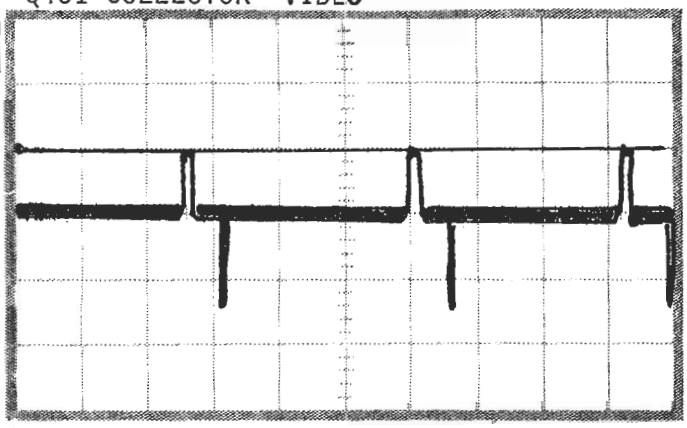
CR112 ANODE HORIZ



V = 10 V/DIV H = 10 µS/DIV

W

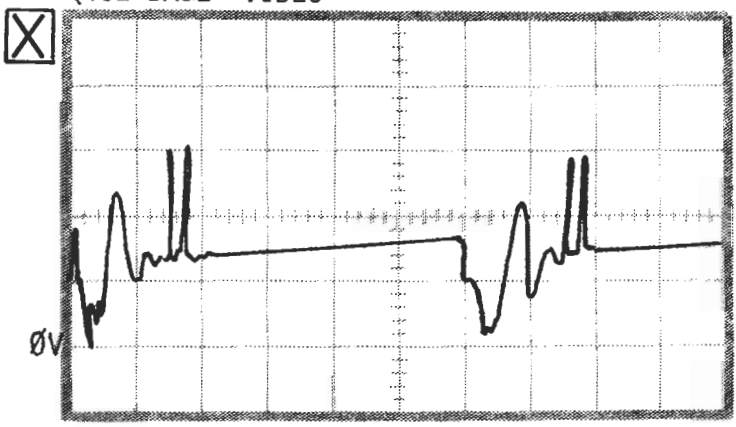
Q401 COLLECTOR VIDEO



V = 10 V/DIV H = .5 mS/DIV

X

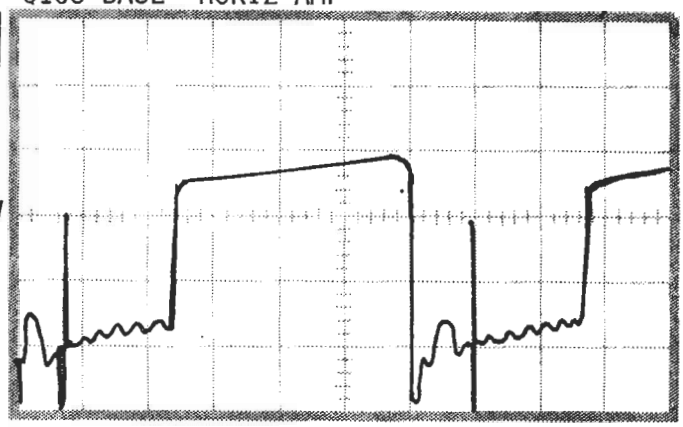
Q402 BASE VIDEO



V = 0.5 V/DIV H = 10 µS/DIV

Q

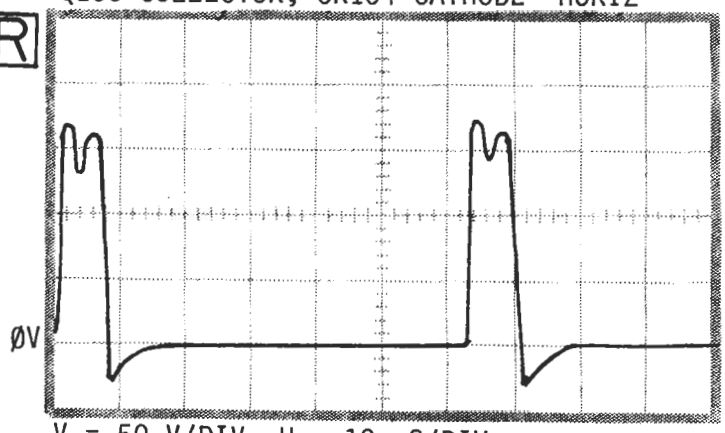
Q103 BASE HORIZ AMP



V = 1 V/DIV H = 10 µS/DIV

R

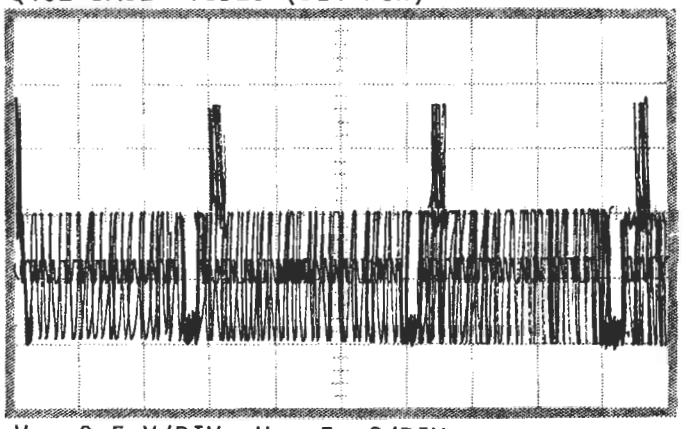
Q103 COLLECTOR, CR104 CATHODE HORIZ



V = 50 V/DIV H = 10 µS/DIV

U

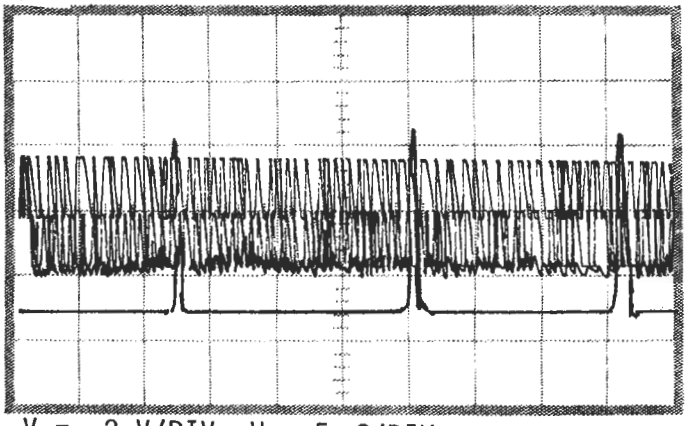
Q402 BASE VIDEO (J14 FCW)



V = 0.5 V/DIV H = 5 mS/DIV

V

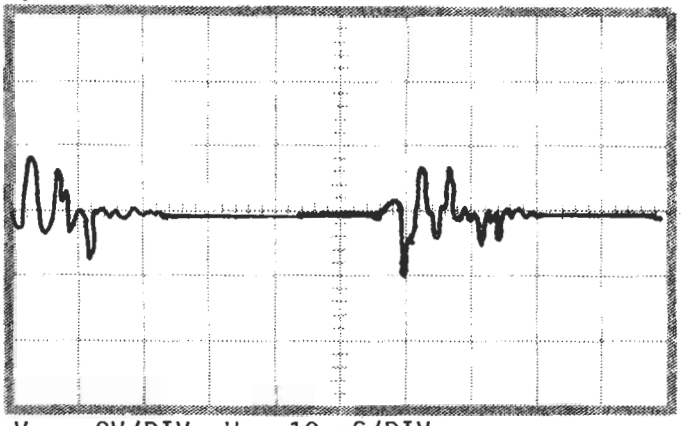
Q402 COLLECTOR VIDEO



V = .2 V/DIV H = 5 mS/DIV

Y

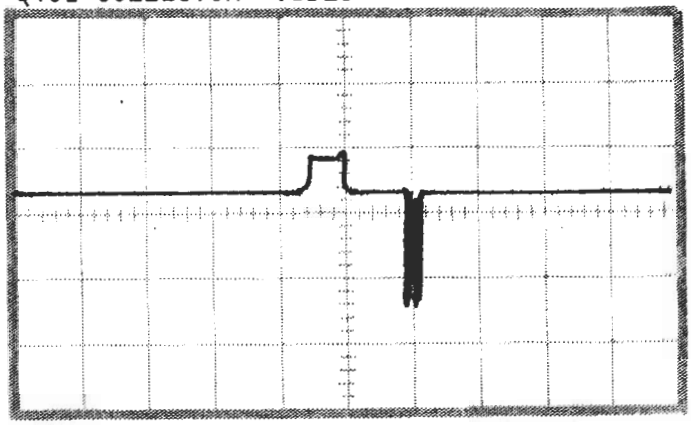
Q402 COLLECTOR VIDEO



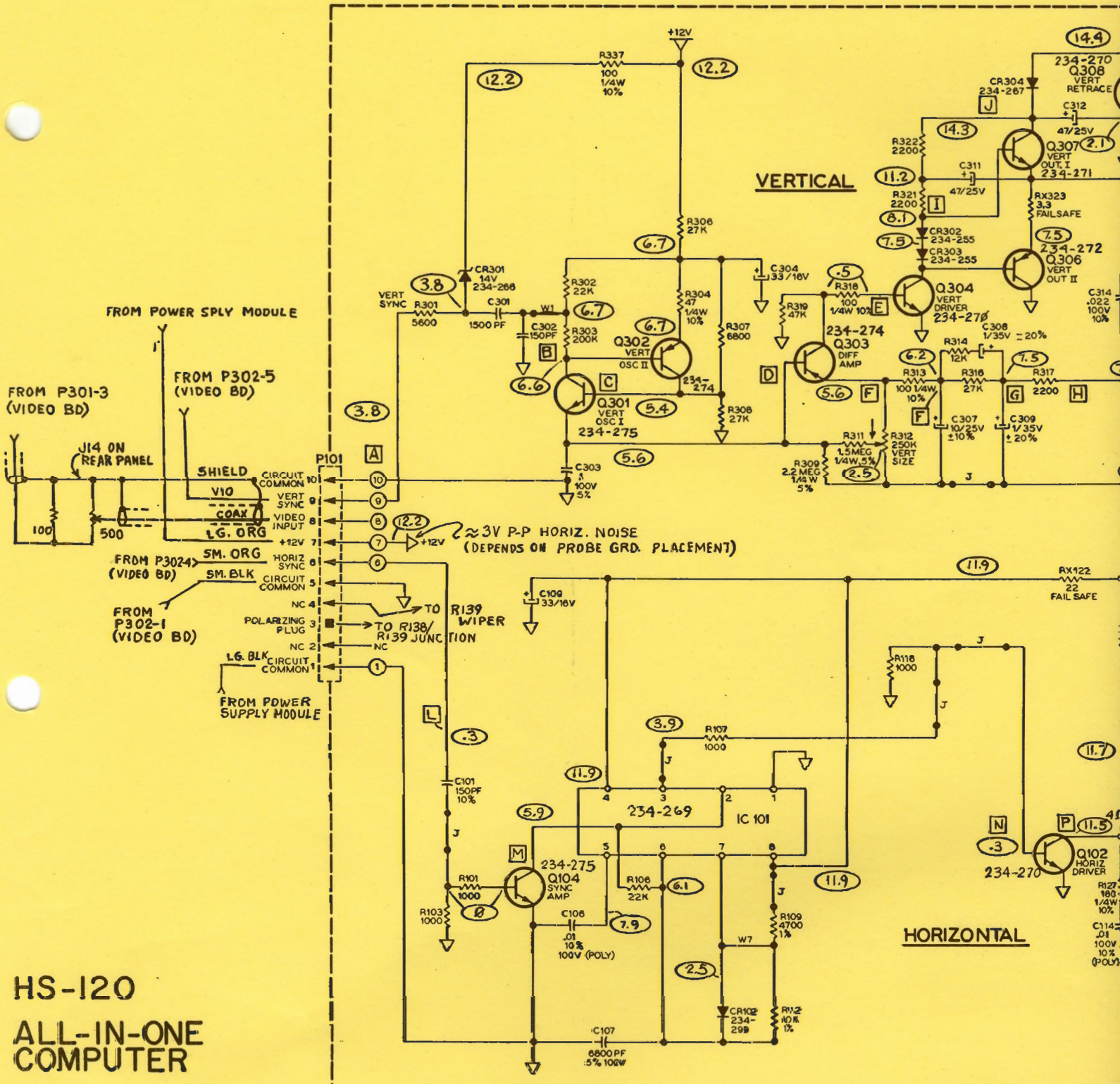
V = .2V/DIV H = 10 µS/DIV

Z

Q401 COLLECTOR VIDEO



V = 10 V/DIV H = 10 µS/DIV



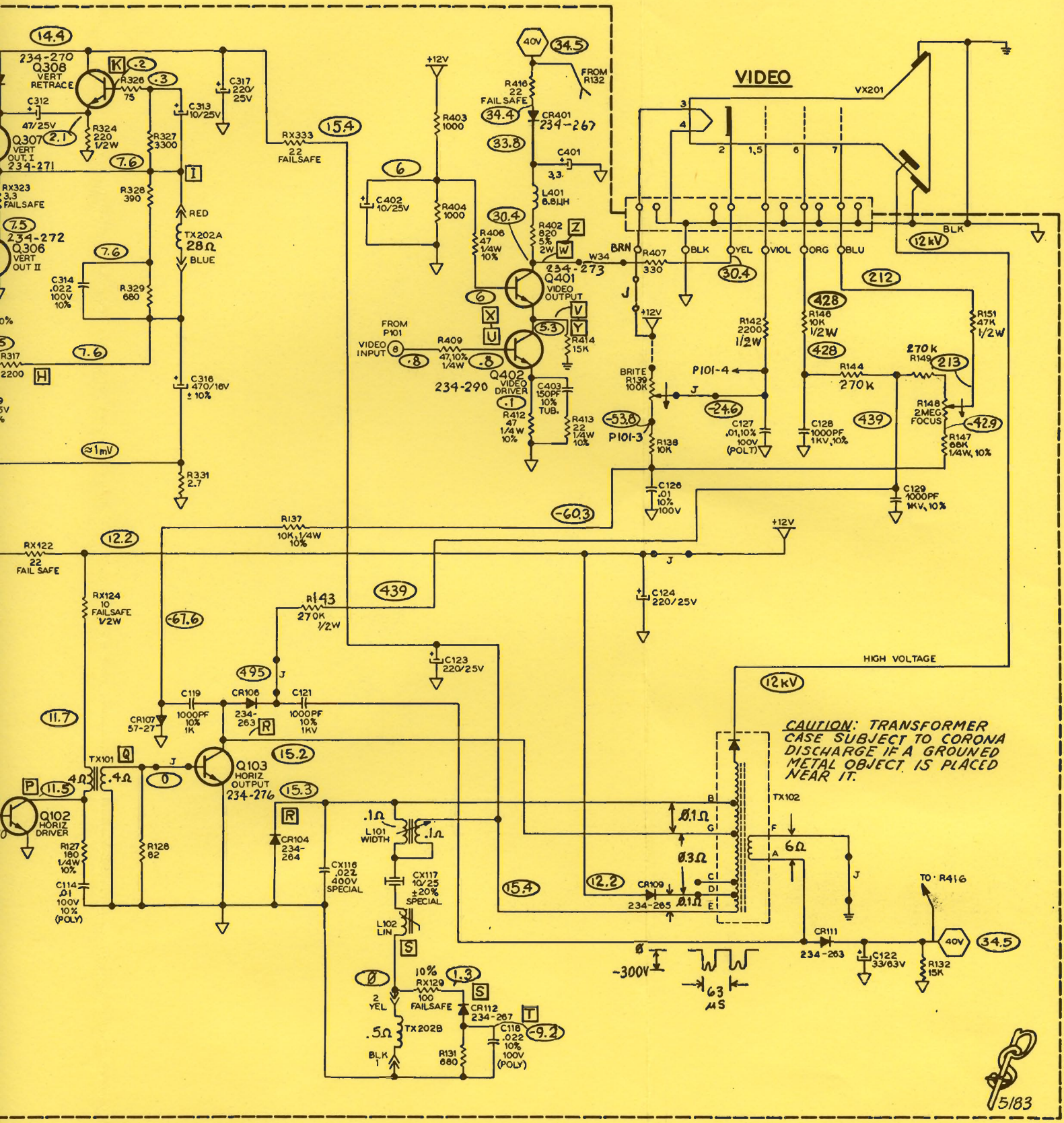
HS-120

ALL-IN-ONE COMPUTER

VIDEO CIRCUIT BOARD

SCHEMATIC NOTES:

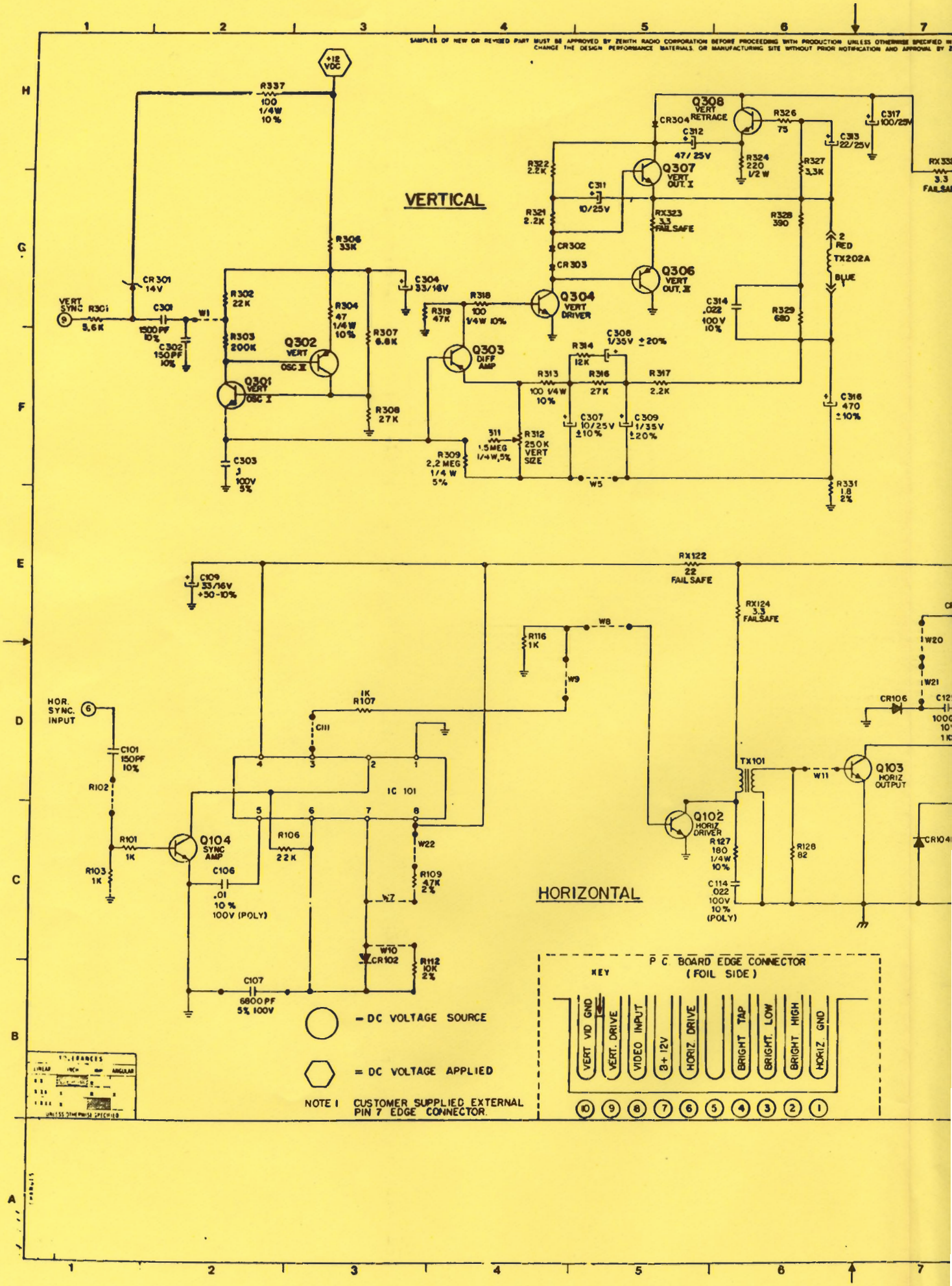
1. ALL RESISTOR VALUES ARE IN OHMS (Ω) OR kΩ (1,000 OHMS); UNLESS NOTED OTHERWISE, ALL RESISTORS ARE 1/4 WATT, 5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS (μF) UNLESS OTHERWISE IDENTIFIED AS pF (PICOFARADS).
3. ▽ REPRESENTS A CIRCUIT BOARD GROUND.
4. ⏚ REPRESENTS A CHASSIS GROUND.
5. +5V ▽ CONNECTION TO A VOLTAGE SOURCE.
6. +5V ▽ SUPPLY VOLTAGE.
7. MALE CONNECTOR PIN.
8. JUMPER WIRE CONNECTION.
9. INDICATES CLOCKWISE ROTATION OF THE CONTROL AS SEEN FROM BOARD SHIELD (FOIL SIDE).
10. TEST EQUIPMENT GROUNDS CONNECTED TO CIRCUIT BOARD SHIELD NEAR REAR MOUNTING SCREW.
11. ◯ IND WIT CON

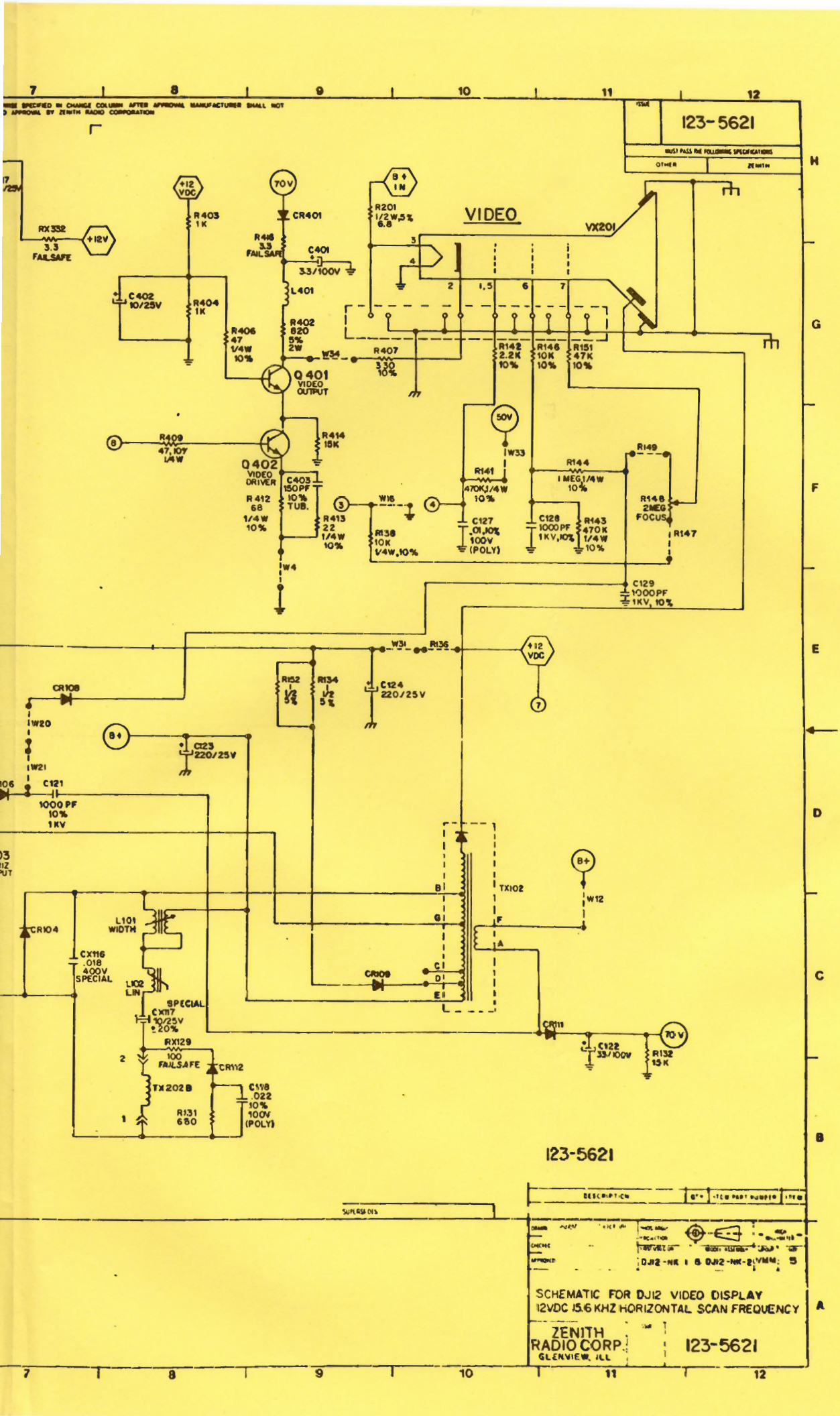


11. ⬭ INDICATES DC VOLTAGE TO GROUND. VOLTAGES MEASURED WITH HIGH-IMPEDANCE DVM (IM-2202) UNDER THE FOLLOWING CONDITIONS:

A) THE SYSTEM HAS BEEN RESET.
B) AUTO-BOOT IS DEFEATED.
C) THE BRIGHTNESS CONTROL ON THE BACK OF THE CHASSIS (J14) IS FCW.
D) THE HAND PROMPT IS VISIBLE ON THE CRT.
E) SYSTEM CONNECTED TO VARIABLE AC SUPPLY (IP-5220) AND ADJUSTED TO 120 VAC.

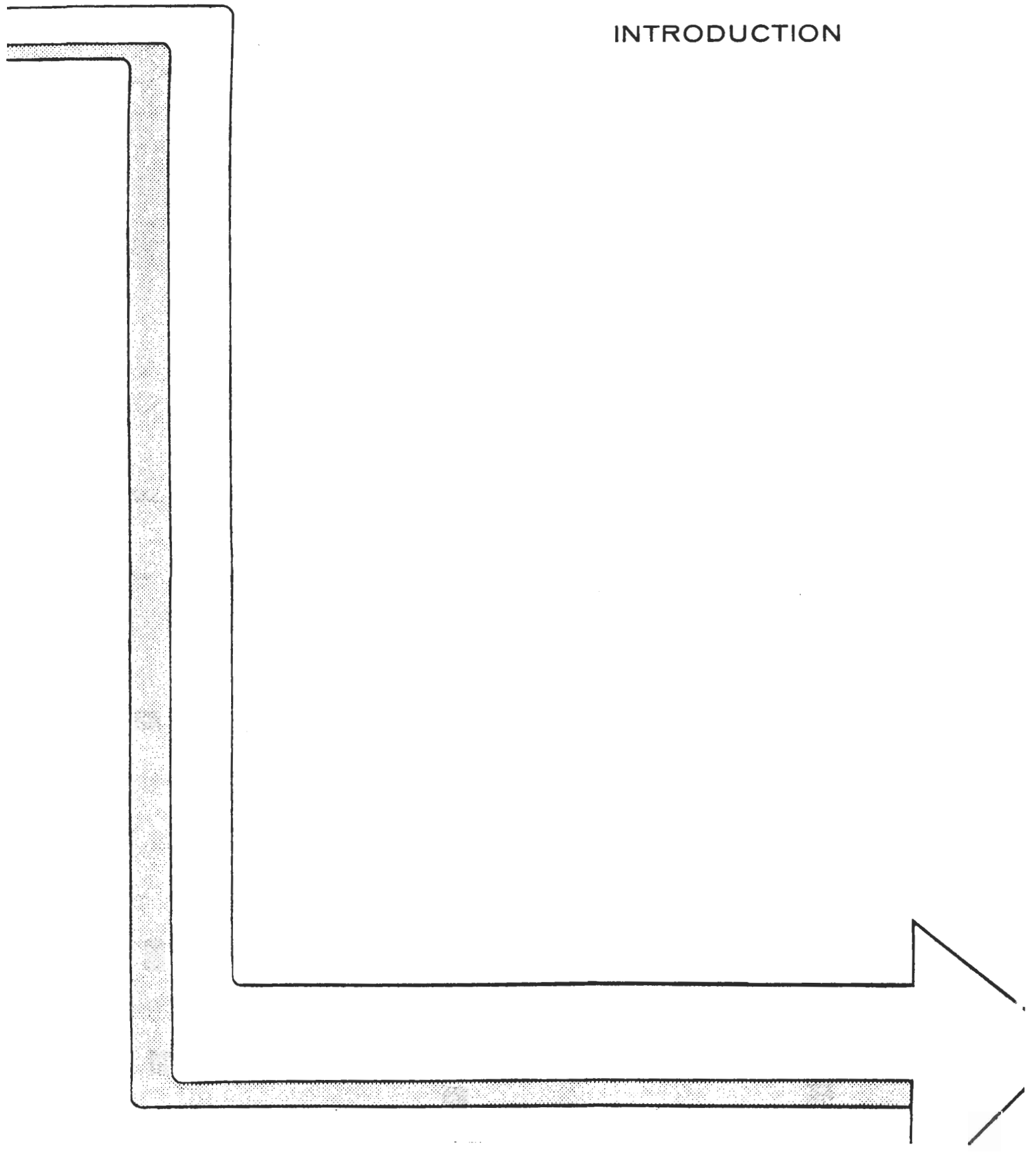
12. [A] LOCATOR KEY FOR WAVEFORMS. WAVEFORMS MEASURED WITH SO-4510 OSCILLOSCOPE, DC TO 15 MHz. SET-UP CONDITIONS SAME AS IN NOTE 11. NOTE THAT THE HORIZONTAL WAVEFORMS MAY VARY SLIGHTLY DUE TO TEST EQUIPMENT GROUND PLACEMENT.


VERTICAL
HORIZONTAL
+12 VDC
R337 100 1/4W 10%
R306 33K
CR301 14V
VERT SYNC
R301 5.6K
C301 1500PF 10%
C302 150PF 10%
W1
R302 22K
R303 200K
Q302 VERT OSC II
Q301 VERT OSC I
R304 47 1/4W 10%
R307 6.8K
R308 27K
C303 J 100V 5%
C304 33/16V
R319 47K
R318 100 1/4W 10%
Q304 VERT DRIVER
Q303 DIFF AMP
R309 2.2 MEG 1/4 W 5%
311 1.5MEG 1/4W,5%
R312 250K VERT SIZE
C308 1/35V ±20%
R314 12K
R313 100 1/4W 10%
R316 27K
R317 2.2K
C307 10/25V ±10%
C309 1/35V ±20%
W5
Q308 VERT RETRACE
CR304
C312 47/25V
R322 2.2K
Q307 VERT OUT. I
C311 10/25V
R321 2.2K
RX323 3.3 FAIL SAFE
CR302
CR303
Q306 VERT OUT. II
R326 75
R324 220 1/2 W
R327 3.3K
R328 390
C313 22/25V
C317 100/25V
RX33
3.3 FAILSA
2 RED
TX202A
BLUE
C314 .022 100V 10%
R329 680
C316 470 ±10%
R331 1.8 2%
C109 33/16V +50-10%
RX122 22 FAIL SAFE
RX124 3.3 FAILSAFE
R116 1K
W8
W9
1K R107
HOR. SYNC. INPUT
C101 150PF 10%
R102
R101 1K
R103 1K
C111
IC 101
Q104 SYNC AMP
R106 22K
C106 .01 10% 100V (POLY)
W22
R109 47K 2%
W7
W10
CR102
R112 10K 2%
C107 6800 PF 5% 100V
TX101
Q102 HORIZ DRIVER
R127 180 1/4W 10%
C114 022 100V 10% (POLY)
R128 82
W11
Q103 HORIZ OUTPUT
W20
W21
CR106
CR104
= DC VOLTAGE SOURCE
= DC VOLTAGE APPLIED
NOTE 1 CUSTOMER SUPPLIED EXTERNAL PIN 7 EDGE CONNECTOR.
P C BOARD EDGE CONNECTOR (FOIL SIDE)
KEY
VERT VID GND
VERT. DRIVE
VIDEO INPUT
B+ 12V
HORIZ DRIVE
BRIGHT TAP
BRIGHT. LOW
BRIGHT HIGH
HORIZ. GND
10 9 8 7 6 5 4 3 2 1


123-5621
VIDEO
VX201
R403 1K
R404 1K
C402 10/25V
R406 47 1/4W 10%
R402 820 5% 2W
R418 3.3 FAILSAFE
C401 33/100V
L401
CR401
70V
+12 VDC
RX332 3.3 FAILSAFE
+12V
R201 1/2W,5% 6.8
B+ 1N
R407 330 10%
W34
Q401 VIDEO OUTPUT
R409 47,10% 1/4W
R414 15K
Q402 VIDEO DRIVER
C403 150PF 10% TUB.
R412 68 1/4W 10%
R413 22 1/4W 10%
W4
W16
R138 10K 1/4W,10%
R141 470KJ/4W 10%
C127 .01,10% 100V (POLY)
50V
W33
R142 2.2K 10%
R146 10K 10%
R151 47K 10%
R144 1 MEG 1/4W 10%
C128 1000PF 1KV,10%
R143 470K 1/4W 10%
R149
R148 2MEG FOCUS
R147
C129 1000PF 1KV, 10%
W31
R136
R152 1/2 5%
R134 1/2 5%
C124 220/25V
CR108
W20
W21
C123 220/25V
C121 1000 PF 10% 1KV
CR104
L101 WIDTH
CX116 .018 400V SPECIAL
L102 LIN
SPECIAL
CX117 10/25V ±20%
RX129 100 FAILSAFE
CR112
TX202B
R131 680
C118 .022 10% 100V (POLY)
TX102
B+
W12
CR109
CR111
C122 33/100V
R132 15K
123-5621
DESCRIPTION
SUPERSEDES
DJ12-NK-1 & DJ12-NK-2(VMM) 5
SCHEMATIC FOR DJ12 VIDEO DISPLAY
12VDC 15.6 KHZ HORIZONTAL SCAN FREQUENCY
ZENITH RADIO CORP. GLENVIEW, ILL
123-5621

KEYBOARD

INTRODUCTION



The keyboard of the H/Z-100 has 95 keys connected in a matrix configuration. Included on the keyboard are 13 function keys and an 18 key keypad. The keyboard uses the universally accepted standard typewriter format. All the keys, except the CAPS LOCK key, are momentary contact. Each keystroke is affirmed by an audible click.

The keyboard of the H/Z-100 features two modes of operation. These modes are called the ASCII mode and the Event mode. When the keyboard is in the ASCII mode, a pressed key will generate a single-byte character. When the keyboard is in the Event mode, two characters are generated. One character is generated when the key is pressed and the other character is generated when the key is released. The Event mode is especially useful in real time games.

Other features of the H/Z-100 keyboard are:

- 17 character FIFO buffer.
- Autorepeat of a key when held down.
- A dedicated microprocessor.
- Power-on indicator in reset key.

The information in this section of the manual will familiarize you with the keyboard. Once familiar with this information, you will be able to efficiently determine if the keyboard or the support circuitry is at fault.

DESCRIPTION

OVERVIEW

The H/Z-100 keyboard is a standard QWERTY-type keyboard; it also contains a numeric keypad and several special-function keys for a total of 95 keys. The keyboard is step-sculptured and has textured keytops. All of the keys are momentary contact except the CAPS LOCK key, which is an alternate position key.

The keyboard processor is the 8041A Universal Peripheral Interface (UPI). This IC is actually a dedicated CPU with built-in RAM and ROM to convert the pressed key into the appropriate code. See the motherboard circuit description and the IC data sheets for more information on this IC.

The primary function of the keyboard processor is to determine which key is pressed. It does this by scanning the keyboard for the pressed key, generating the appropriate code, and sending the code to the central processing unit. The H/Z-100 uses a 2-key lockout scanning algorithm. This is a method which stops scanning the keyboard when 2 keys are found down at the same time. Scanning is resumed when either one or both of the 2 keys are released.

FEATURES

The keyboard processor provides the following features:

Autorepeat A key is repeated when it is held down. This may be disabled via software.

Key click A click sound is heard when a key is pressed. This function may also be disabled via software.

FIFO A 17-key FIFO (first in first out) buffer is maintained by the keyboard processor. This means that 17 keystrokes will be stored until the master processor is free to service the keyboard. Once the FIFO is full, any more keystrokes will be lost. The FIFO may be cleared by software, but the data register of the keyboard processor will still contain one key which may be read and tossed out.

Alternate Encoding Mode When placed in this mode, the keyboard processor sends a unique code each time a key is pressed. This is a non-standard code with bit 7 cleared. When the key is released, the same code is sent with bit 7 set. This will be covered in more detail later.

PROGRAMMING AND CONFIGURATION

I/O PROTOCOL

Keyboard I/O routines are automatically taken care of by the H/Z-100 monitor and whichever disk operating system you're using. However, if you want to write your own keyboard I/O routines, the program should obey the following rules:

OUTPUT TO UPI

Wait until the Input Buffer Full flag (IBF) is zero. This is found by reading the status port.

Output the command to the command port of the keyboard processor.

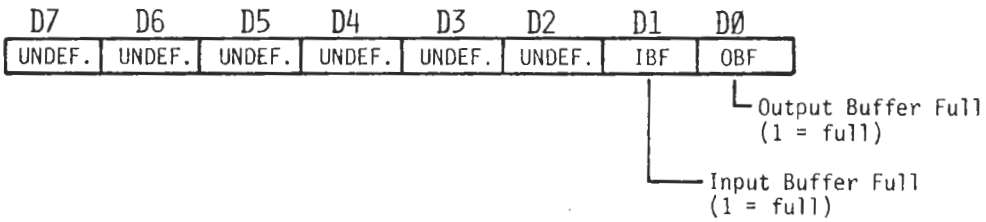
Currently, there is no valid information which may be written to the data port. Anything written to the data port will be ignored by the keyboard processor. Illegal commands will also be ignored by the processor.

INPUT DATA FROM UPI

The only information which may be read from the data port are key codes. There are two ways to determine when there is a key waiting to be read:

Interrupts An interrupt will be generated whenever a key is pressed. This interrupt is an IR6 to the master 8259A. Though this interrupt request is always enabled, it is up to the user to properly set up the 8259A interrupt processors. The interrupt request is cleared by reading the data port.

Polling The Output Buffer Full bit (OBF) of the status register will always be set when a key is placed on the data port. The bit is cleared when the data port is read.



STATUS REGISTER

INPUT STATUS FROM KEYBOARD PROCESSOR

The status port may be read at any time without disturbing the operation of the keyboard. The bits of the status port are defined as follows:

OBF - Output Buffer Full Indicates that there is a key ready to be read at the data port. OBF is cleared by reading the data port.

IBF - Input Buffer Full This bit is set when a byte is output to the keyboard. IBF is cleared when the keyboard is ready for input.

COMMAND DEFINITIONS

Reset

The RESET command restores the keyboard processor to the power up configuration except for the output buffer full flag. The only way to clear the OBF is by reading the data port.

Autorepeat On

This command enables the autorepeat function. Autorepeat causes a key to be repeated when it is held down.

Autorepeat Off

This command disables the autorepeat function.

Key Click On

When the key click is enabled, the UPI generates a click at the speaker whenever a key is pressed. When in the normal scanning mode the SHIFT, REPEAT, CTRL, CAPS LOCK, and RESET keys do not produce clicks.

Key Click Off

Disables the key click function.

Clear FIFO

This command empties the first-in first-out buffer of the keyboard processor. The output buffer of the keyboard processor is not cleared by this command. Only an input from the data port will clear the OBF.

Click

Produces one click from the keyboard speaker.

Beep

Produces a beep from the keyboard speaker.

Enable Keyboard

Used to enable the keyboard if it has been disabled by the Disable Keyboard command.

Disable Keyboard

This command will cause all keystrokes to be ignored except for a CTRL-RESET. To enable the keyboard, the software must issue an Enable Keyboard command; otherwise, you must press CTRL-RESET or turn the computer off and then on again.

Key Up/Down Mode

Sending this command to the keyboard processor will cause a different scanning algorithm to be used. This is covered later in the Alternate Encoding Mode section.

Normal Scan Mode

The keyboard processor returns to the power up scanning algorithm. The data sent to the CPU are standard ASCII code.

To send one of the previously described commands to the keyboard processor, output the appropriate code shown below to port 0F5 hex.

COMMAND SUMMARY

COMMAND	CODE (Hex)
RESET	00
AUTOREPEAT ON	01
AUTOREPEAT OFF	02
KEY CLICK ON	03
KEY CLICK OFF	04
CLEAR FIFO	05
CLICK	06
BEEP	07
ENABLE KEYBOARD	08
DISABLE KEYBOARD	09
KEY UP/DOWN MODE	0A
NORMAL SCAN MODE	0B

POWER-UP CONFIGURATION

After power up or a hard reset, the keyboard processor is initialized as follows:

Autorepeat is enabled.

Key click is enabled.

The FIFO and the output buffer are cleared.

The keyboard processor is in the normal scan mode.

ALTERNATE ENCODING MODE

The alternate encoding mode is a key up/down scheme. This method of encoding a keyboard is sometimes referred to as event-driven.

Basically, the keyboard processor outputs a code for a key when it is pressed and outputs another code for that key when it is released. Each key has a unique code including CTRL, REPEAT, CAPS LOCK, and the SHIFT keys. Because of this, there is no longer a shifted key. Instead, a byte is output for the SHIFT key and a byte is output for the primary key.

The high order bit is used to distinguish between a key down and a key up. When a key is pressed, bit 7 is logic zero; when released, bit 7 is logic 1.

The RESET key is the only key that doesn't generate a code. This is because it isn't scanned by the keyboard processor. See the motherboard circuit description for more details.

See the Key Codes section for a hexadecimal chart of the codes generated by the UPI.

PORT ADDRESSES

The following port addresses are assigned to the keyboard processor. See the UPI IC data sheet for detailed programming information.

COMMAND PORT = 0F5 (hex)

DATA PORT = 0F4

STATUS PORT = 0F5

KEY CODES

The following charts show the hexadecimal byte value the UPI sends to the CPU when a key is pressed. The codes for some of these keys depend on the state of the "modifier" keys. The modifier keys are: SHIFT (right or left), CTRL (control) and CAPS LOCK. Some keys are not affected by any of the modifiers, such as the DELETE key. The code of this key (7F) is always the same regardless of the modifier keys. Other keys are affected by all of the modifiers, such as the "A" key.

When using the key-code table, an "x" under a modifier indicates that the modifier does not affect the code for that key.

Under the Down/Up column, the hex value to the left of the slash is the code generated when the key is pressed. The code to the right of the slash is generated when the key is released.

KEY CODES

KEY	NOT SHIFTED	SHIFTED	CONTROL	CONTROL SHIFT	CAPS LOCK	DOWN/UP CODE
) 0	30	29	X	X	X	5B/DB
! 1	31	21	X	X	X	57/D7
@ 2	32	40	32	00	X	56/D6
# 3	33	23	X	X	X	55/D5
$ 4	34	24	X	X	X	54/D4
% 5	35	25	X	X	X	53/D3
^ 6	36	5E	36	1E	X	52/D2
& 7	37	26	X	X	X	51/D1
* 8	38	2A	X	X	X	50/DØ
(9	38	28	X	X	X	5A/DA
A	61	41	01	01	41	07/87
B	62	42	02	02	42	13/93
C	63	43	03	03	43	15/95
D	64	44	04	04	44	05/85
E	65	45	05	05	45	0D/8D
F	66	46	06	06	46	04/84
G	67	47	07	07	47	03/83
H	68	48	08	08	48	02/82
I	69	49	09	09	49	08/88
J	6A	4A	0A	0A	4A	01/81
K	6B	4B	0B	0B	4B	00/8Ø
L	6C	4C	0C	0C	4C	10/9Ø
M	6D	4D	0D	0D	4D	11/91
N	6E	4E	0E	0E	4E	12/92
O	6F	4F	0F	0F	4F	19/99
P	70	50	10	10	50	1A/9A
Q	71	51	11	11	51	0F/8F
R	72	52	12	12	52	0C/8C
S	73	53	13	13	53	06/86
T	74	54	14	14	54	0B/8B
U	75	55	15	15	55	09/89
V	76	56	16	16	56	14/94
W	77	57	17	17	57	0E/8E
X	78	58	18	18	58	16/96
Y	79	59	19	19	59	0A/8A
Z	7A	5A	1A	1A	5A	17/97
BACK SPACE	08	X	X	X	X	5F/DF
TAB	09	X	X	X	X	4E/CE
LINE FEED	0A	X	X	X	X	44/C4
RETURN	0D	X	X	X	X	4C/CC
ESC	1B	X	X	X	X	4F/CF
SPACE	20	X	X	X	X	45/C5
" '	27	22	X	X	X	48/C8
< ,	2C	3C	X	X	X	4D/CD
--- _	2D	5F	2D	1F	X	5C/DC
> .	2E	3E	X	X	X	4A/CA

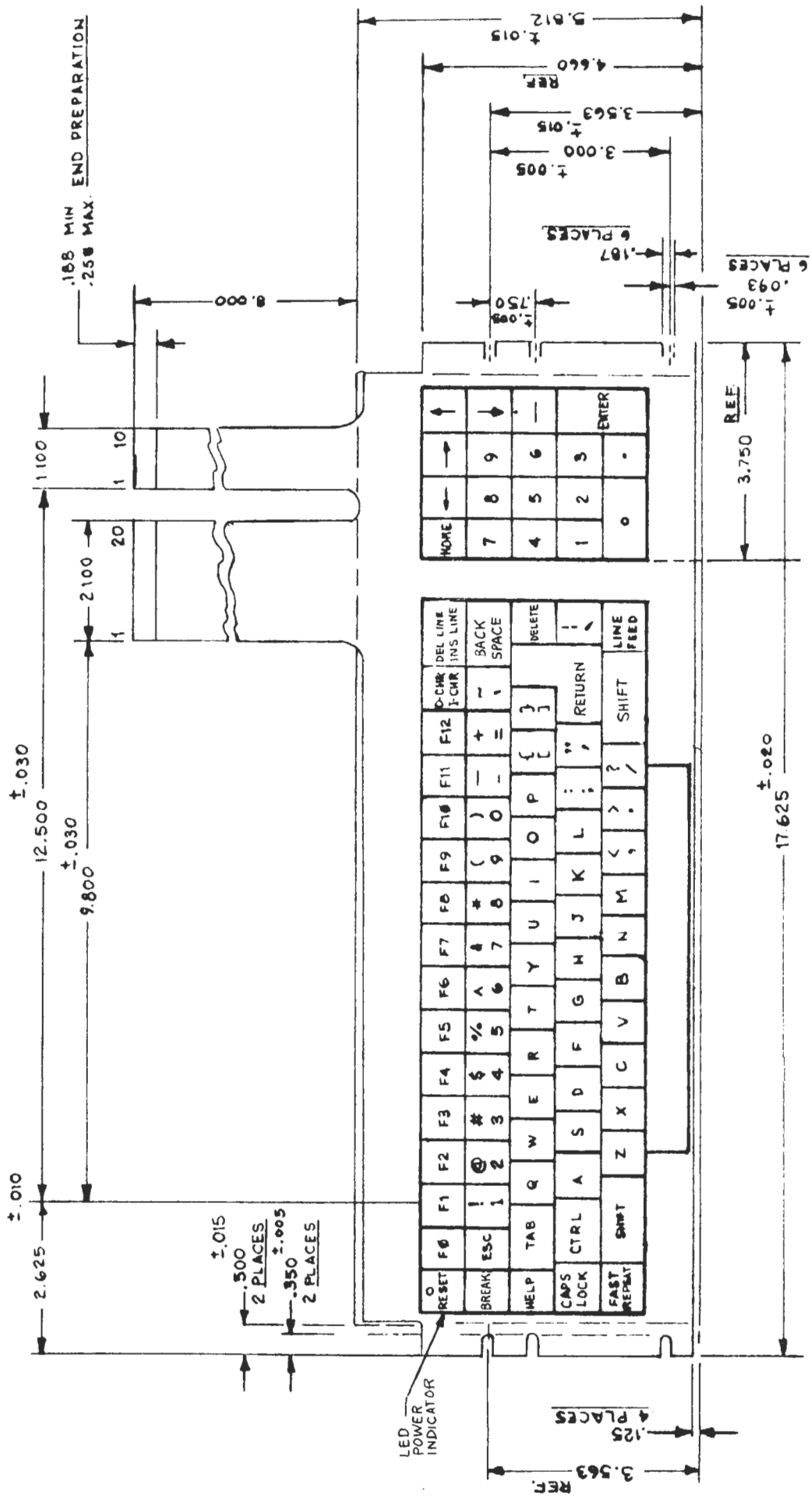
KEY CODES (CONTINUED)

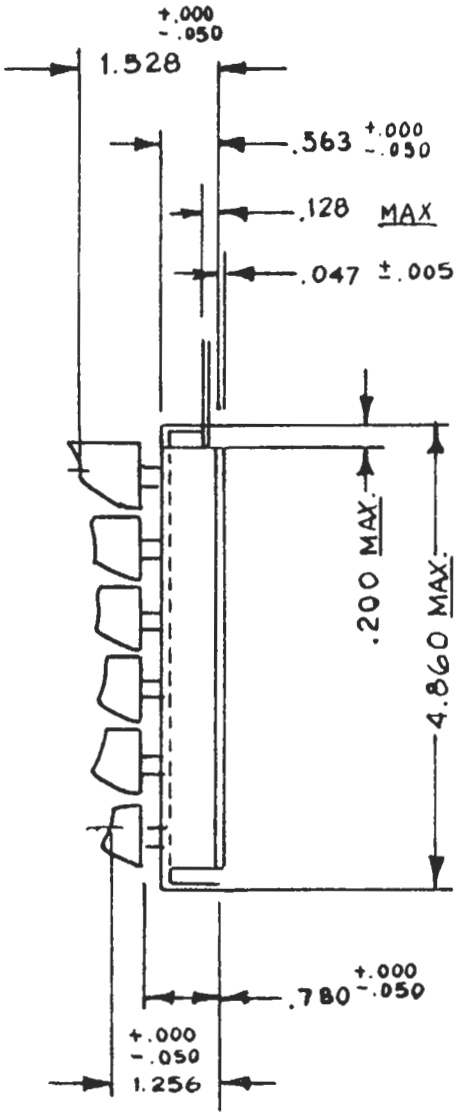
KEY	NOT SHIFTED	SHIFTED	CONTROL	CONTROL SHIFT	CAPS LOCK	DOWN/UP CODE
? /	2F	3F	X	X	X	4B/CB
: ;	3B	3A	X	X	X	49/C9
+ =	3D	2B	X	X	X	5D/DD
{ [	5B	7B	1B	7B	X	59/D9
¦ \	5C	7C	1C	7C	X	43/C3
}]	5D	7D	1D	7D	X	58/D8
~ `	60	7E	X	X	X	5E/DE
DELETE	7F	X	X	X	X	42/C2
ENTER	8D	CD	X	X	X	38/B8
HELP	95	D5	X	X	X	46/C6
FØ	96	D6	X	X	X	27/A7
F1	97	D7	X	X	X	26/A6
F2	98	D8	X	X	X	25/A5
F3	99	D9	X	X	X	24/A4
F4	9A	DA	X	X	X	23/A3
F5	9B	DB	X	X	X	22/A2
F6	9C	DC	X	X	X	21/A1
F7	9D	DD	X	X	X	20/AØ
F8	9E	DE	X	X	X	29/A9
F9	9F	DF	X	X	X	2A/AA
F10	A0	E0	X	X	X	2B/AB
F11	A1	E1	X	X	X	2C/AC
F12	A2	E2	X	X	X	2D/AD

KEY	NOT SHIFTED	SHIFTED	CONTROL	CONTROL SHIFT	CAPS LOCK	DOWN/UP CODE
D CHR I CHR	A3	E3	X	X	X	2E/AE
D LINE I LINE	A4	E4	X	X	X	2F/AF
(UP ARROW)	A5	E5	X	X	X	3B/BB
(DOWN ARROW)	A6	E6	X	X	X	3A/BA
(RIGHT ARROW)	A7	E7	X	X	X	33/B3
(LEFT ARROW)	A8	E8	X	X	X	3F/BF
HOME	A9	E9	X	X	X	37/B7
BREAK	AA	EA	X	X	X	47/C7
- (KEYPAD)	AD	ED	X	X	X	39/B9
. (KEYPAD)	AE	EE	X	X	X	40/CØ
0 (KEYPAD)	B0	F0	X	X	X	41/C1
1 (KEYPAD)	B1	F1	X	X	X	34/B4
2 (KEYPAD)	B2	F2	X	X	X	3C/BC
3 (KEYPAD)	B3	F3	X	X	X	30/BØ
4 (KEYPAD)	B4	F4	X	X	X	35/B5
5 (KEYPAD)	B5	F5	X	X	X	3D/BD
6 (KEYPAD)	B6	F6	X	X	X	31/B1
7 (KEYPAD)	B7	F7	X	X	X	36/B6
8 (KEYPAD)	B8	F8	X	X	X	3E/BE
9 (KEYPAD)	B9	F9	X	X	X	32/B2
REPEAT	X	X	X	X	X	60/EØ
CAPS LOCK	X	X	X	X	X	61/E1
RIGHT SHIFT	X	X	X	X	X	62/E2
CTRL	X	X	X	X	X	63/E3
LEFT SHIFT	X	X	X	X	X	64/E4

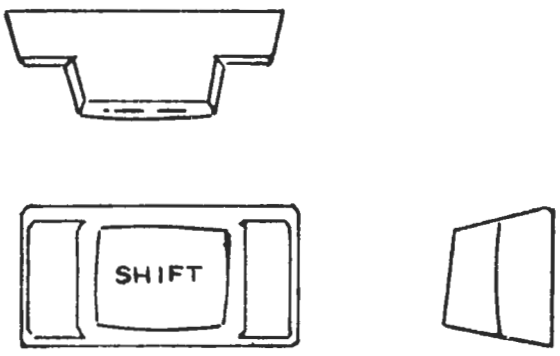
VISUAL CHECKS

KEYBOARD DIMENSIONS



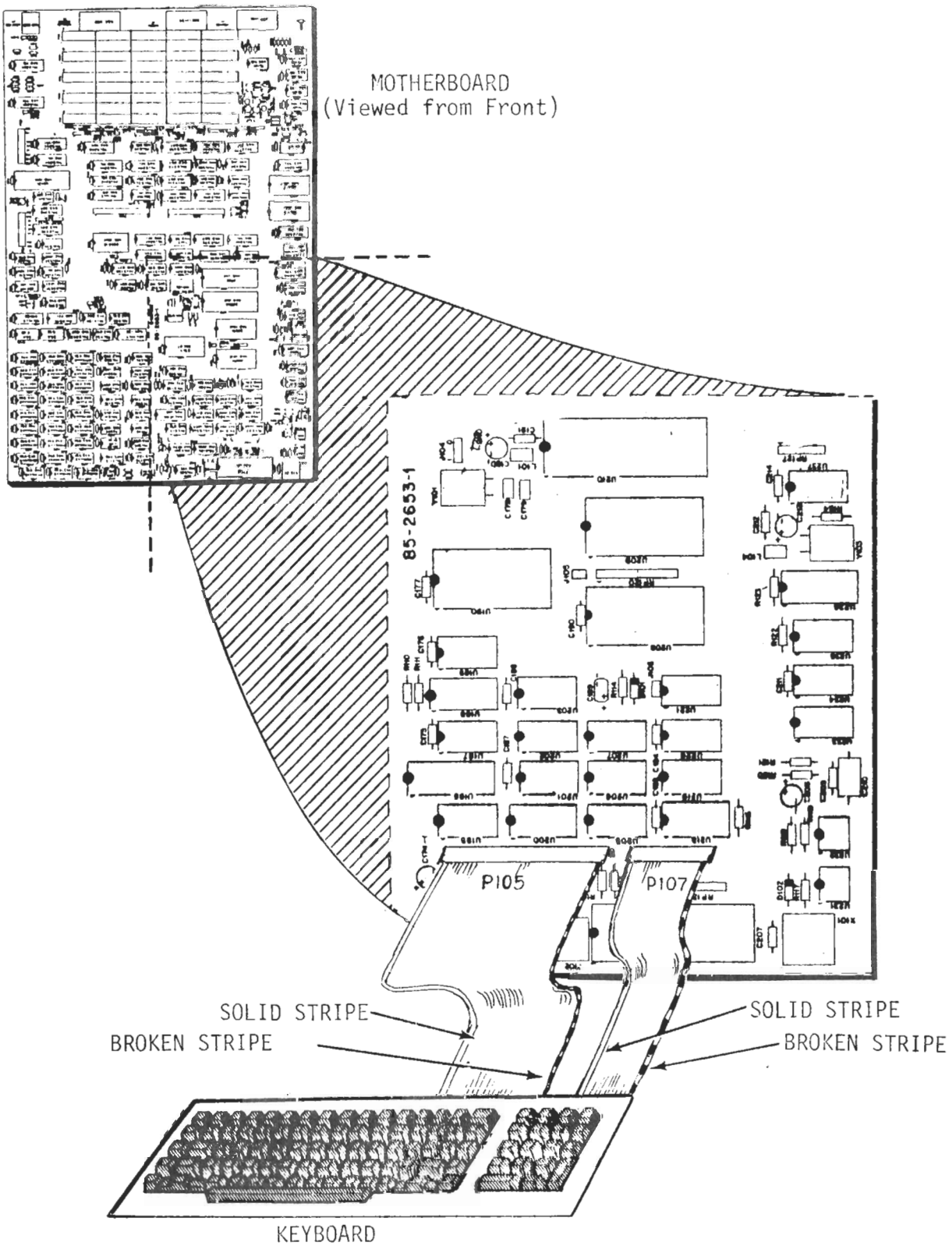


SIDE VIEW

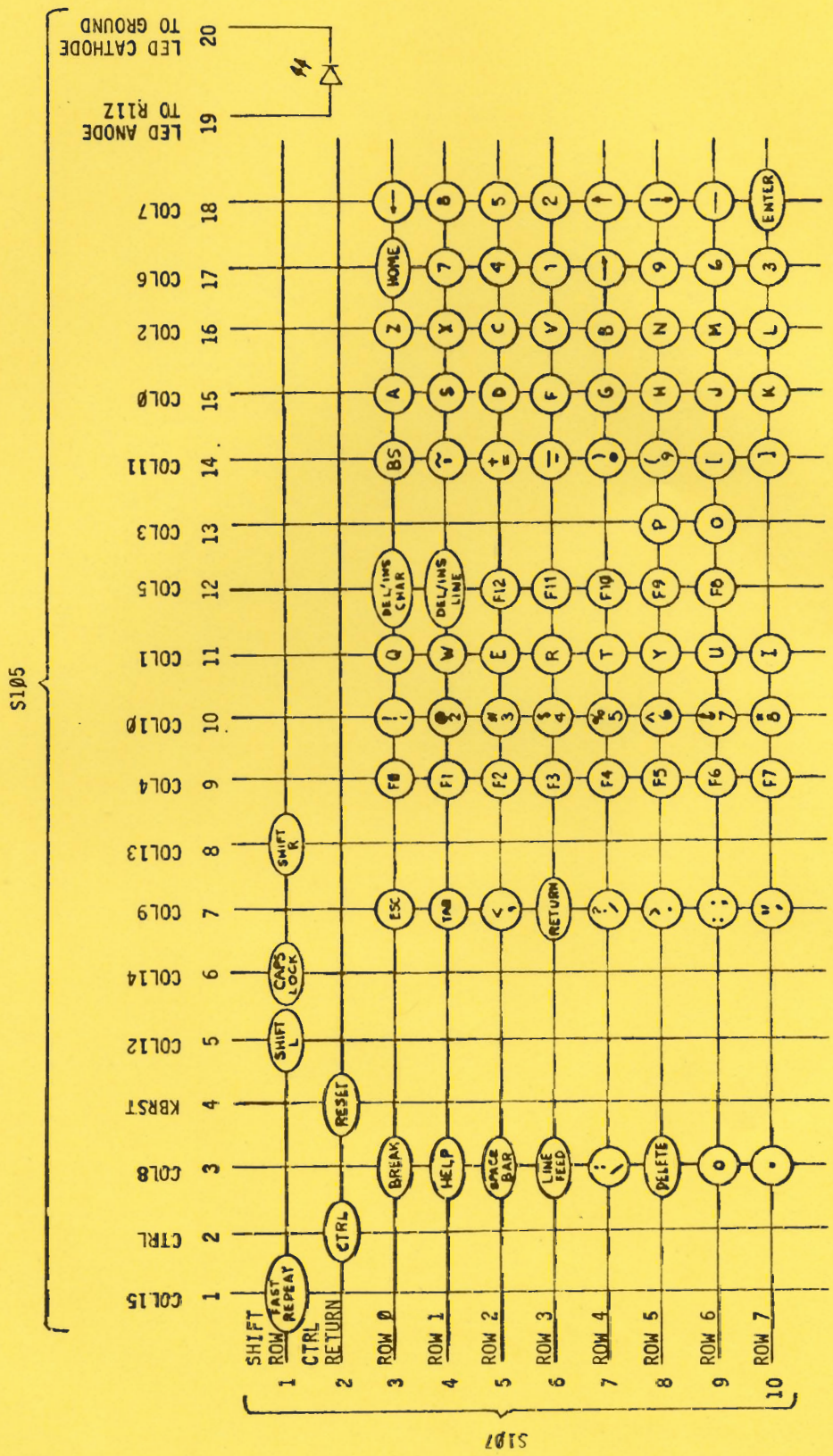


SHIFT KEY DETAIL

KEYBOARD DIMENSIONS (CONTINUED)

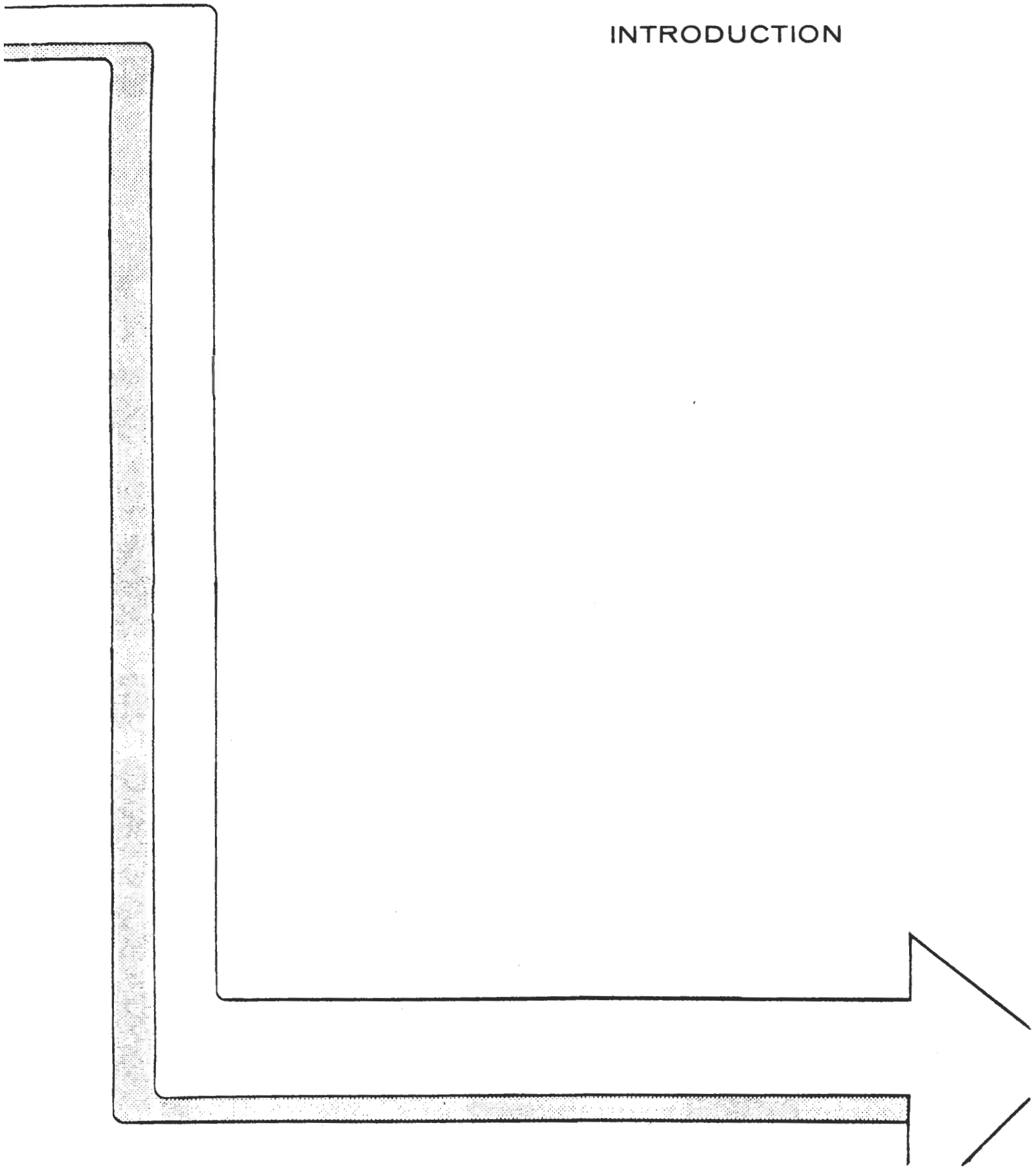


KEYBOARD CONNECTIONS


KEYBOARD SCHEMATIC
S105
S107
LED ANODE TO R112
LED CATHODE TO GROUND
SHIFT
CTRL
RETURN
ROW 0
ROW 1
ROW 2
ROW 3
ROW 4
ROW 5
ROW 6
ROW 7
COL15
CTRL
COL8
KBRST
COL12
COL14
COL9
COL13
COL4
COL10
COL1
COL5
COL3
COL11
COL0
COL2
COL6
COL7
FAST REPEAT
SHIFT R
CAPS LOCK
SHIFT L
RESET
CTRL
BREAK
HELP
SPACE BAR
LINE FEED
DELETE
ENTER
HOME
BS
DEL/INS CHAR
DEL/INS LINE
RETURN
ESC
TAB
F0
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12

POWER SUPPLY

INTRODUCTION



The power supply provides regulated voltages used by the various components within the H/Z-100. It is located on the left side on the chassis floor. The power supply comes in two external designs, one for the All-in-One and one for the Low Profile. The two power supplies may look different on the outside, but internally they are the same.

The power supply of the H/Z-100 series is known as a switching power supply. It has this name because of the circuitry design within it. In this type of power supply, the rectified line voltage is switched on and off at a very high frequency. The resulting square wave is then filtered into a DC voltage. This design results in a power supply that has high efficiency.

The power supply contains many other features. Some of them are:

- 240 watts of available power.
- Internal cooling fan.
- Two position line voltage switch; 115 or 230.
- Detachable line cord.

Primarily, this section will familiarize you with the power supply design and operation. Since the power supply is a sealed unit, it cannot be serviced; however, the information contained in this section will aid you in determining if the power supply is defective.

CIRCUIT DESCRIPTION

BASIC CONVERTER

This supply is an off-line, voltage-fed, half-bridge, switch-mode power supply. This topology first converts the AC power mains to DC. This DC is then chopped to a quasi-square wave. This quasi-square wave is used to drive the primary of an inverter transformer. The secondaries are converted to low voltage DC by using rectifiers and low-pass filters.

EMI FILTER

COMPONENTS

All power entering the power supply passes through an EMI filter. The filter is comprised of C1, C2, C3, C4 and L1.

FUNCTION

The main function of this filter is to reduce conducted emissions emanating from the power supply to a point where it complies with the regulatory agencies.

LINE TRANSIENT SUPPRESSOR

MOV1 is a surge suppressor. Its function is to attenuate high voltage transients from entering the power supply.

POWER MAINS TO DC CONVERSION

COMPONENTS

CR1, RT1, RT2, C5, C6 and R1-R4 form the AC-to-DC conversion circuit.

115 VAC OPERATION

When the 115/230 switch is closed, this circuit is configured in a voltage doubler mode. Each half-power line cycle, C5 and C6 are alternately charged to 1.414 times the rms line voltage. Since the load is across the two capacitors, the voltage is two times the voltage across each capacitor. (Note: The two lower diodes of CR1 are not used in this mode.)

230 VAC OPERATION

When the 115/230 switch is open, the AC-to-DC conversion circuit is configured in a full-wave bridge mode. Now C5 and C6 are charged in series each half cycle. The load "sees" the same DC voltage regardless of the power line voltage selected.

INRUSH LIMITING

Thermistor RT1 and RT2 limit power line inrush when the supply is first turned on.

MAINS DISCHARGE

Resistors R1-R4 discharge C5 and C6 when the supply is turned off (UL requirement).

DC TO QUASI-SQUARE WAVE CONVERSION

OPERATION AND COMPONENTS

Transistors Q1 and Q2 form two active switches that "chop" the DC. They operate 180 degrees out of phase. They are driven through driver/isolation transformer, T1. Diodes CR2, CR3, CR4 and CR5 and C11 and C12 form two turn-off enhancement circuits. When Q1 or Q2 is forward biased, C11 or C12, respectively, charges up to approximately 1.2 volts. When the drive circuit signals either transistor to turn off, it does this by effectively shorting out the primary of transformer T1. Since the secondaries are now effectively shorted, the last charged capacitor is placed across the emitter-base junction of the forward biased transistor. Therefore, at the first instant, the emitter-base junction is reverse biased to approximated 1.2 volts. This supplies not only sufficient IB2, but keeps the transistors reverse biased to prevent false turn on.

CATCH DIODES

Diodes CR6 and CR7 are "catch" diodes that return any inductive energy to the input capacitors, C5 and C6. They also protect Q1 and Q2 from reverse breakdown. R5 and C13 form a "snubber" network. This circuit limits the "ringing" due to leakage inductance in T3 and T4.

BASE DRIVE SCHEME - TRANSFORMER

The base drive scheme is a proportional type. The three-turn winding of T1 has the entire primary current of inverter transformers, T3 and T4, circulating through it. As the output load is increased, so does the amount of base drive to Q1 and Q2. This provides optimum drive under all load conditions.

BASE DRIVE SCHEME - ACTIVE COMPONENTS

Transistors Q5 through Q8 form a "push-pull" inverter drive circuit. Transistors Q5 and Q7 provide the turn-on signal to its respective inverter transistor. Transistors Q6 and Q8 provide the turn-off signal to its respective inverter transistor. Diodes CR36 and CR38 allow the current to commutate during turn off. Transistors Q3 and Q4 act as logic inverters between the switching regulator IC1 and the inverter drive circuit.

INTEGRATED SWITCHING REGULATOR - OPERATION

The switching regulator control is IC1. Resistors R28 and C30 determine the clock frequency. The inputs to the error amplifier portion of the control IC are pins 1 and 2. Pin 16 is an internal reference of approximately 5 volts. Approximately 2.5 volts is applied to pin 2 by dividing down the reference through resistors R21, R22, and R23. C29 is a noise-decoupling capacitor. The +5 volt output is divided down to approximately 2.5 volts to be applied to pin 1 through R17 and R18. Pin 9 is the output of the error amplifier. Frequency compensation, for proper roll-off and phase margin, is provided by C26, C43, and R19.

CROSS CONDUCTION PROTECTION

To prevent cross conduction of inverter transistors Q1 and Q2, at any time, a "dead time" limiting circuit is incorporated. R24, R25 and CR26 form this circuit. R24 and R25 form a 2.5 volt voltage divider off the +5 volt internal reference. If the output of the error amplifier ever attempts to slew above this 2.5 volt level, CR26 is forward biased. This clamps the output. The result is the maximum duty ratio attainable is approximately 90%.

SLOW START CIRCUIT

Diodes CR24 and CR25, R20 and C27 form the slow start circuit. This circuit prevents the output from the supply from overshooting on turn-on. The circuit also limits the amount of current the inverter transistors must sustain during turn-on.

At turn-on, C27 is at zero volts. Diode CR25 clamps the output of the error amplifier to one diode drop. Through IC1 logic, this forces Q3, Q4, Q6, and Q8 to conduct. This prevents Q1 or Q2 from switching. Now C27 is charged through R20. This allows the output of the error amplifier to rise. Eventually, IC1 allows a minimal on-time to occur on one of the inverter transistors. A short time later, the other inverter transistor conducts for the same duration. Now, the outputs begin to rise. This process of "walking" up the outputs continues until the inputs of the error amplifier are equal. At this point, the "loop" is closed. Capacitor C27 continues to charge to the internal reference voltage and CR25 is reverse biased. Diode CR24 resets the slow-start capacitor, C27, when the supply is turned off.

OUTPUT STAGES

+5 VOLT OUTPUT

Diode CR9 comprises a full-wave Schottky rectifier that changes a secondary quasi-square wave to a positive polarity square wave for the +5 volt output. L2 and C14 form a low-pass filter to convert the square wave to DC. R6 is a discharge resistor. C21 is a high frequency by-pass capacitor.

+12 VOLT QUASI-REGULATED OUTPUT

Diode CR10 comprises a full-wave rectifier that changes a secondary quasi-square wave to a positive polarity square wave for the +12 volt output. L3 and C17 comprise a low-pass filter to convert the square wave to DC. R76 is a discharge resistor. C22 is a high frequency by-pass capacitor. R56, R57, C39 and C40 are two snubber networks to dampen the ringing due to the leakage inductance of T3.

+8 VOLT OUTPUT

Diode CR8 comprises a full-wave Schottky rectifier that changes a secondary quasi-square wave to a positive polarity square wave for the +8 volt output. L6 and C16 form a low pass filter to convert the square wave to DC. R7 is a discharge resistor. C20 is a high frequency by-pass capacitor.

+16 VOLT OUTPUT

Diodes CR12 and CR14 comprise a full wave rectifier that changes a secondary quasi-square wave to a positive polarity square wave for the +16 volt output. L4 and C18 form a low-pass filter to convert the square wave to DC. R77 is a discharge resistor. C23 is a high frequency by-pass capacitor. The DC fan for the supply is ran off this line through RT3. (This is so the fan will not run faster if the box gets too hot.) This output is also used for "boot strapping" the bias supply through CR33. The purpose of this is twofold. One reason is to maintain the bias voltage once the power to the supply is turned off for output carryover. The second purpose is to allow the use of a small bias transformer, T5, which is used only on start up.

Another use of the +16 volt output is the power source for the +12 volt regulated output. The operation of this regulator is described in the +8 Volt Output section.

+12 VOLT REGULATOR OPERATION

The +12 volt linear regulator is made up of discrete transistors Q9 thru Q11. The +5 volt output, used as a reference, is applied to the emitter of Q9. Since, at the first instant, the +12 regulated output is zero, Q9 is off. R54 pulls the base of Q11 high. Since Q10 and Q11 are in a Darlington configuration, both Q10 and Q11 are turned on. The +12 regulated output begins to rise until Q9 becomes forward biased through voltage divider R50 and R51. At this point, the circuit is in equilibrium. The dynamic resistance of Q10 drops the +16 volt line to the +12 volt regulated output potential.

-16 VOLT OUTPUT

Diodes CR11 and CR13 form a full-wave rectifier that changes a secondary quasi-square wave to a negative polarity square wave for the -16 volt output. L5 and C19 form a low pass filter to convert the square wave to DC. R10 through R13 are discharge resistors as well as a minimum load to ensure that the filter inductor remains critical at all times. R58, R59, C41, and C42 are two snubber networks used to dampen the "ringing" due to the leakage inductance of T4.

PROTECTION CIRCUITS

CURRENT LIMIT PROTECTION

Transformer T2 is a current-sense transformer that monitors primary current. R14 provides a load for the transformer. This converts current to a voltage. Full-wave bridge, CR15 through CR18, converts this quasi-square wave voltage to a positive polarity square wave. R15 is adjusted to extract the amount of voltage that would constitute an overcurrent condition. R16 and C25 is a low-pass filter and time delay. The time delay prevents false shutdowns for momentary transients. CR19 resets C25 every time primary current falls to zero. During dead time, CR30 is an isolation diode, since the remainder of this circuit is shared with the overvoltage protection circuit. If the voltage of C25 is of sufficient amplitude to exceed the 5-volt reference on the inverting input of comparator IC2C, the output will go high. This forward biases CR30 and CR29; the thyristor, CR29, will latch into conduction pulling its cathode high. This will also pull pin 10 of IC1 high. A high on pin 10 will inhibit all switching action and the outputs will fall to zero. To recover from this condition, the AC power must be removed from the power supply, the overcurrent condition corrected, and the power returned to the power supply.

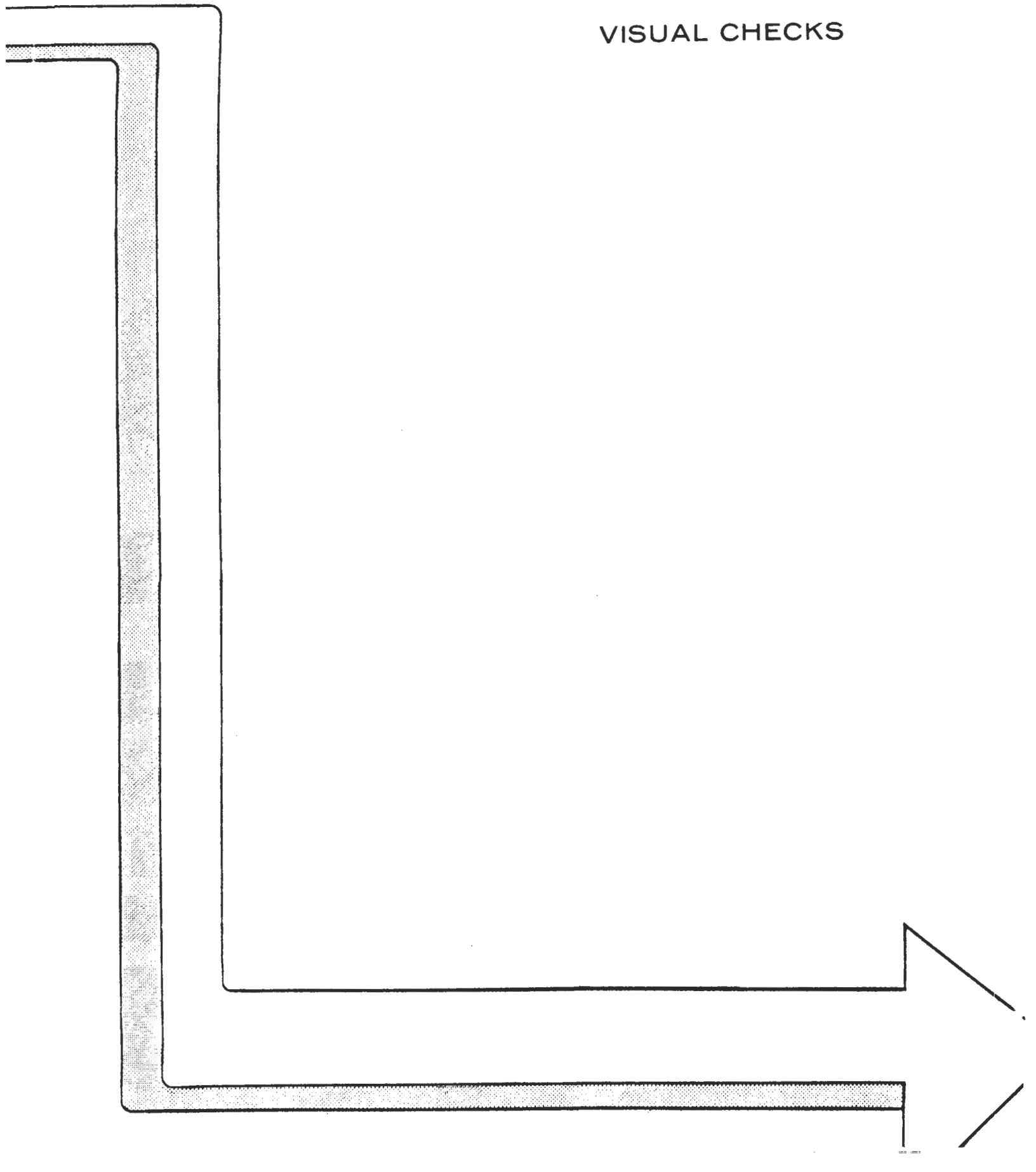
OVERVOLTAGE PROTECTION

IC2A is the overvoltage comparator. A 2.5 volt reference is applied to the inverting input of the comparator. The +5 volt output is applied to the non-inverting input of the comparator. The +5 volt output is applied to the non-inverting input of the comparator through voltage divider R39 and R40. If the +5 volt output exceeds approximately 6.2 volts, the output of the comparator will go high, forward biasing CR32. This will, similar to an overcurrent, forward bias CR29. CR29 will latch and pull pin 10 of IC1 high. Once again, all outputs will fall to zero. The supply will not restart until the overvoltage condition has been corrected and the power line recycled.

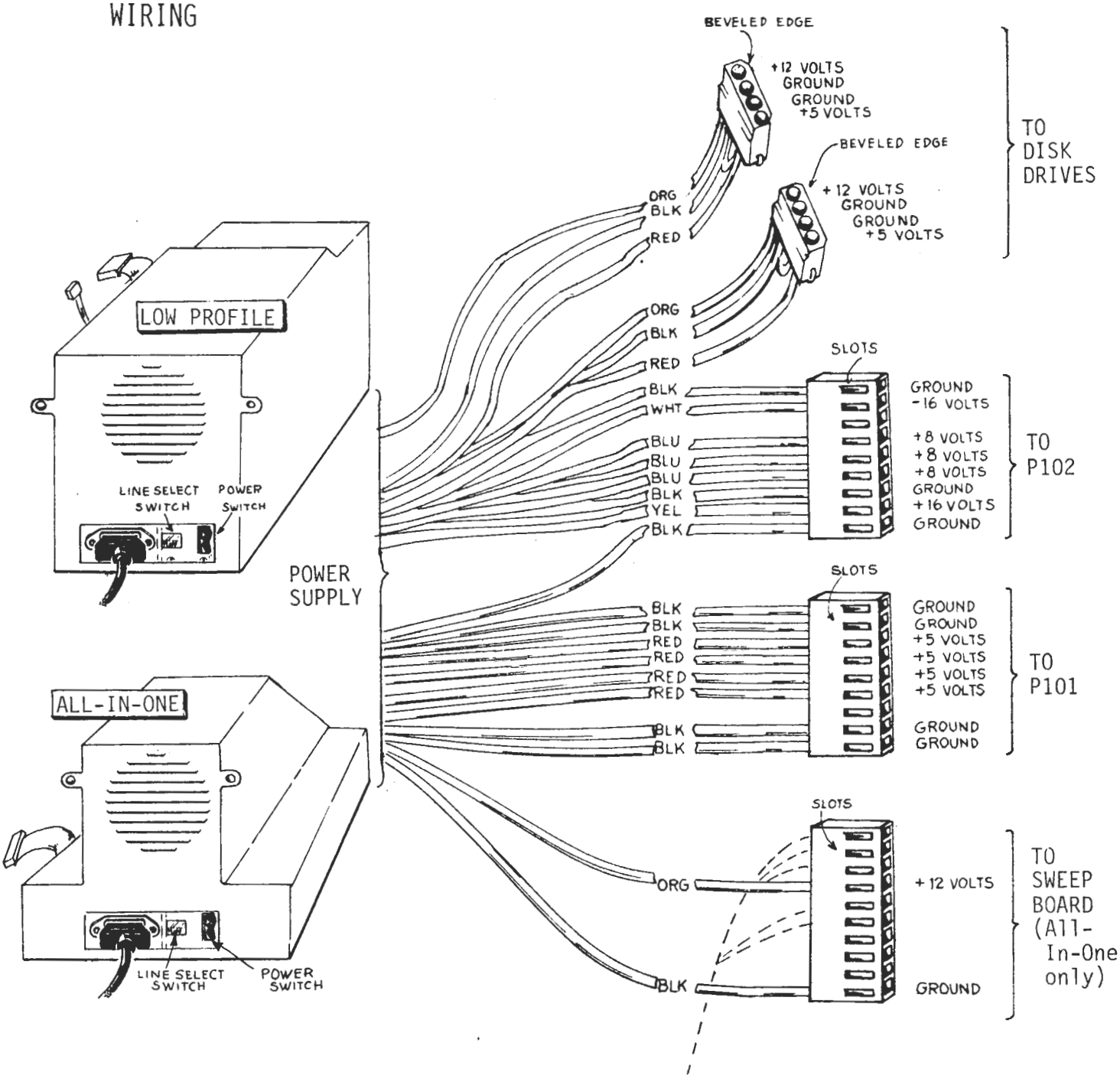
+12 VOLT REGULATOR OVERCURRENT PROTECTION

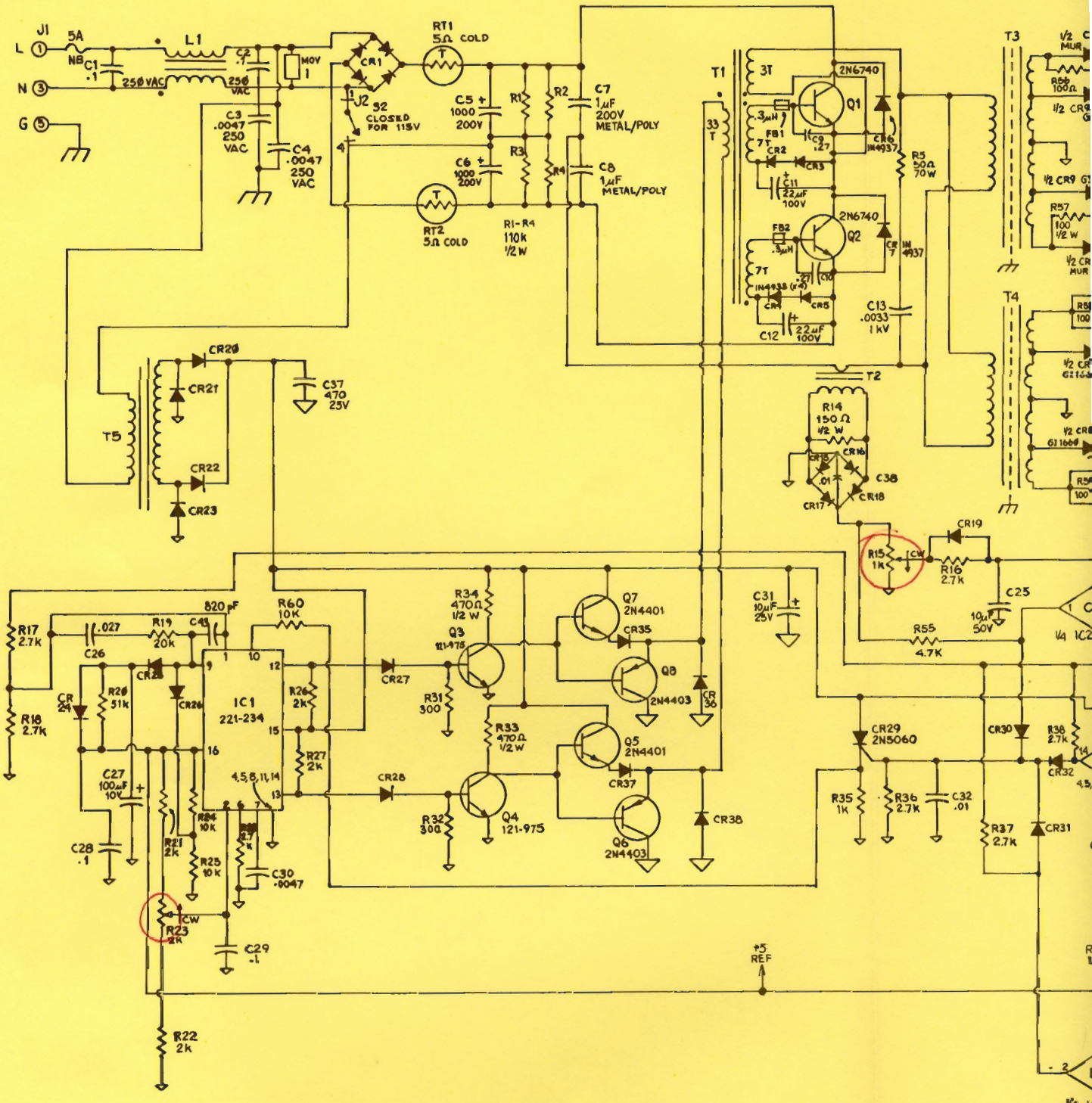
IC2B is used as an overcurrent comparator on the +12 volt regulated output. If the voltage on the output side of R45 drops too low because of an excessive current drain, the output of IC2B will go high, forward biasing CR31. This will, similar to an overcurrent, forward bias CR29. CR29 will then latch and pull pin 10 of IC1 high. Once again all outputs will fall to zero. The supply will not restart until the overcurrent condition has been corrected and the power line recycled. This condition on the +12 volt regulated output could destroy Q10 without activating the primary overcurrent circuit.

VISUAL CHECKS



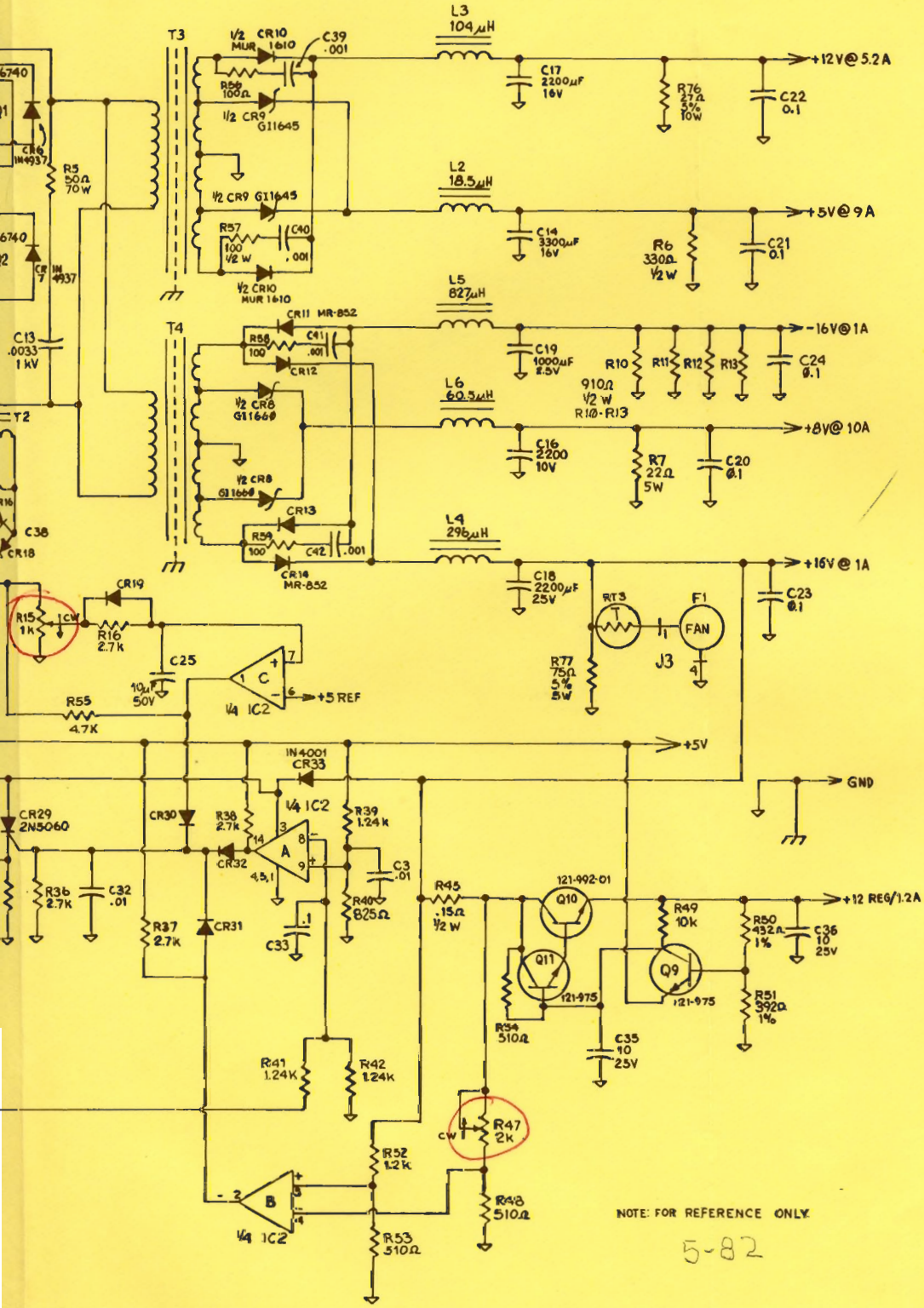
WIRING


BEVELED EDGE
+12 VOLTS
GROUND
GROUND
+5 VOLTS
BEVELED EDGE
+12 VOLTS
GROUND
GROUND
+5 VOLTS
TO DISK DRIVES
ORG
BLK
RED
ORG
BLK
RED
BLK
WHT
BLU
BLU
BLU
BLK
YEL
BLK
SLOTS
GROUND
-16 VOLTS
+8 VOLTS
+8 VOLTS
+8 VOLTS
GROUND
+16 VOLTS
GROUND
TO P102
LOW PROFILE
LINE SELECT SWITCH
POWER SWITCH
POWER SUPPLY
ALL-IN-ONE
LINE SELECT SWITCH
POWER SWITCH
BLK
BLK
RED
RED
RED
RED
BLK
BLK
SLOTS
GROUND
GROUND
+5 VOLTS
+5 VOLTS
+5 VOLTS
+5 VOLTS
GROUND
GROUND
TO P101
ORG
BLK
SLOTS
+12 VOLTS
GROUND
TO SWEEP BOARD (All-In-One only)



H/Z-100 POWER SUPPLY

HE 234-200



R23 - Adj, all but +12v for video

R15 - Current limiting

R47 - +12v for CRT over cur. Adj.

5-82

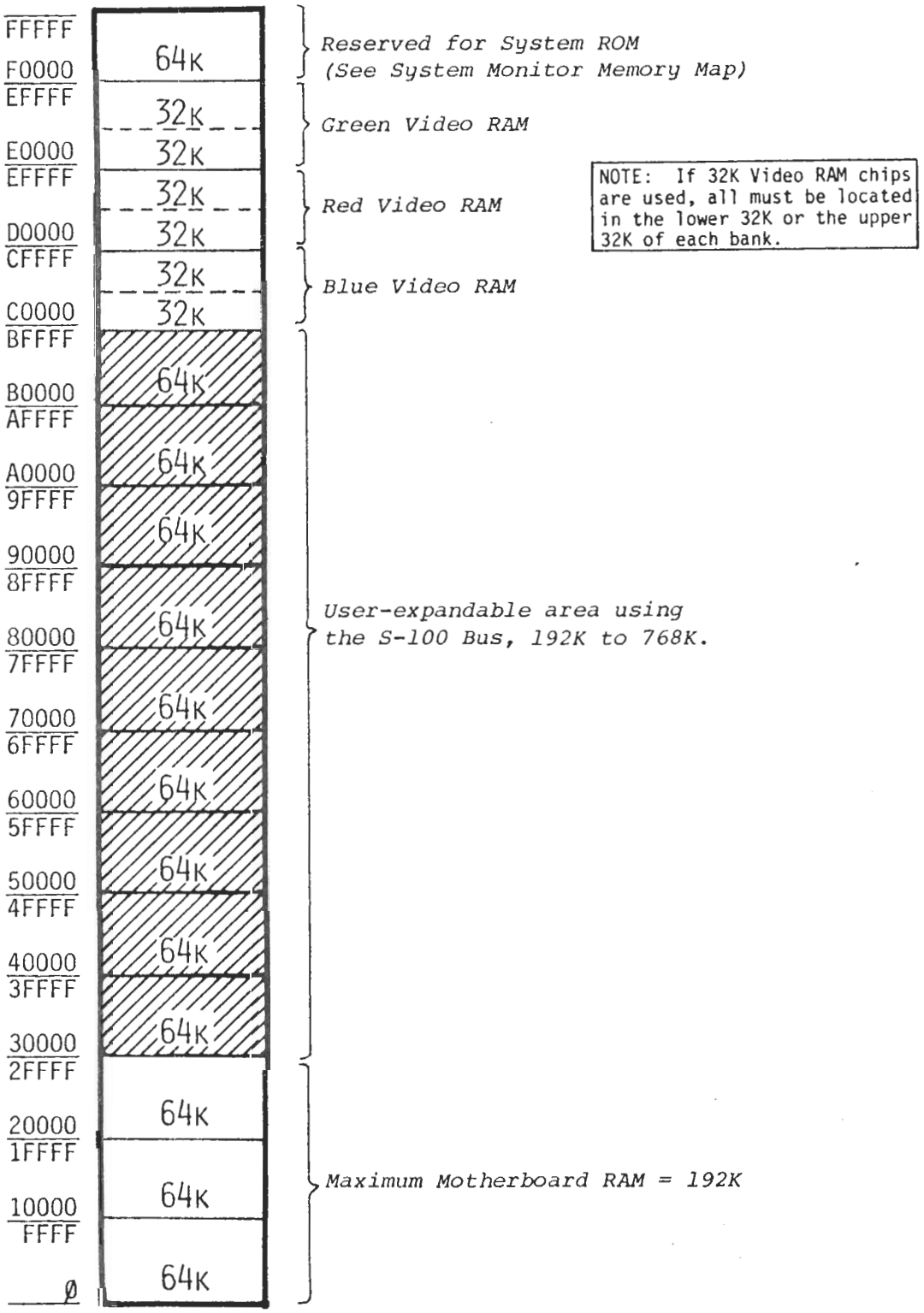
MEMORY MAPS AND I/O PORT INFORMATION

INTRODUCTION

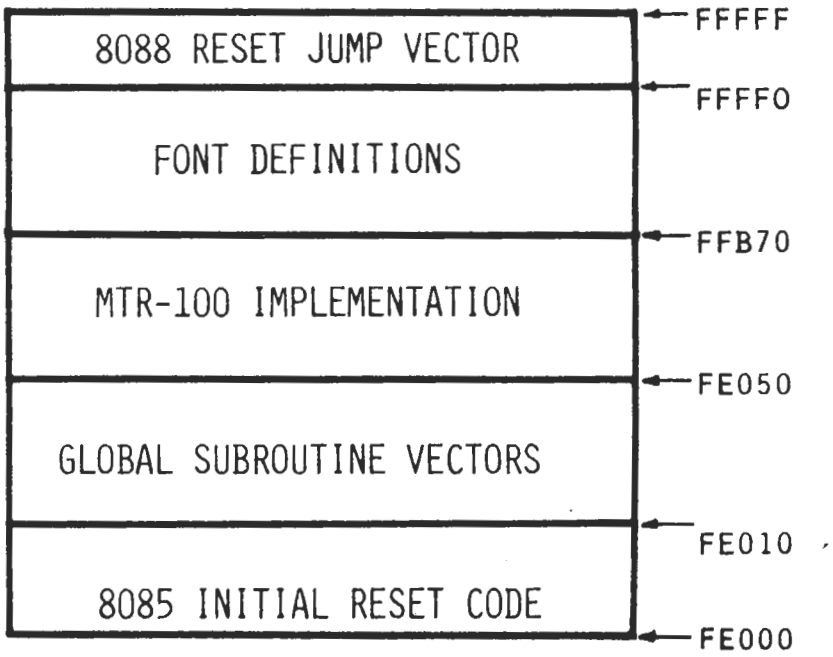
The following pages provide a quick reference to the H/Z-100 memory and port locations. The memory maps include MTR-100 layout information and RAM bank switching information. The I/O port information shows port addresses and read/write status. For a detailed description of these maps, refer to the appropriate circuit description in the H/Z-100 Service Data Manual.

Programming information for the keyboard port and map select port is also included. Programming the other ports can easily be done by using the I/O drivers in Z-DOS or CP/M. Refer to the appropriate software user's manual.

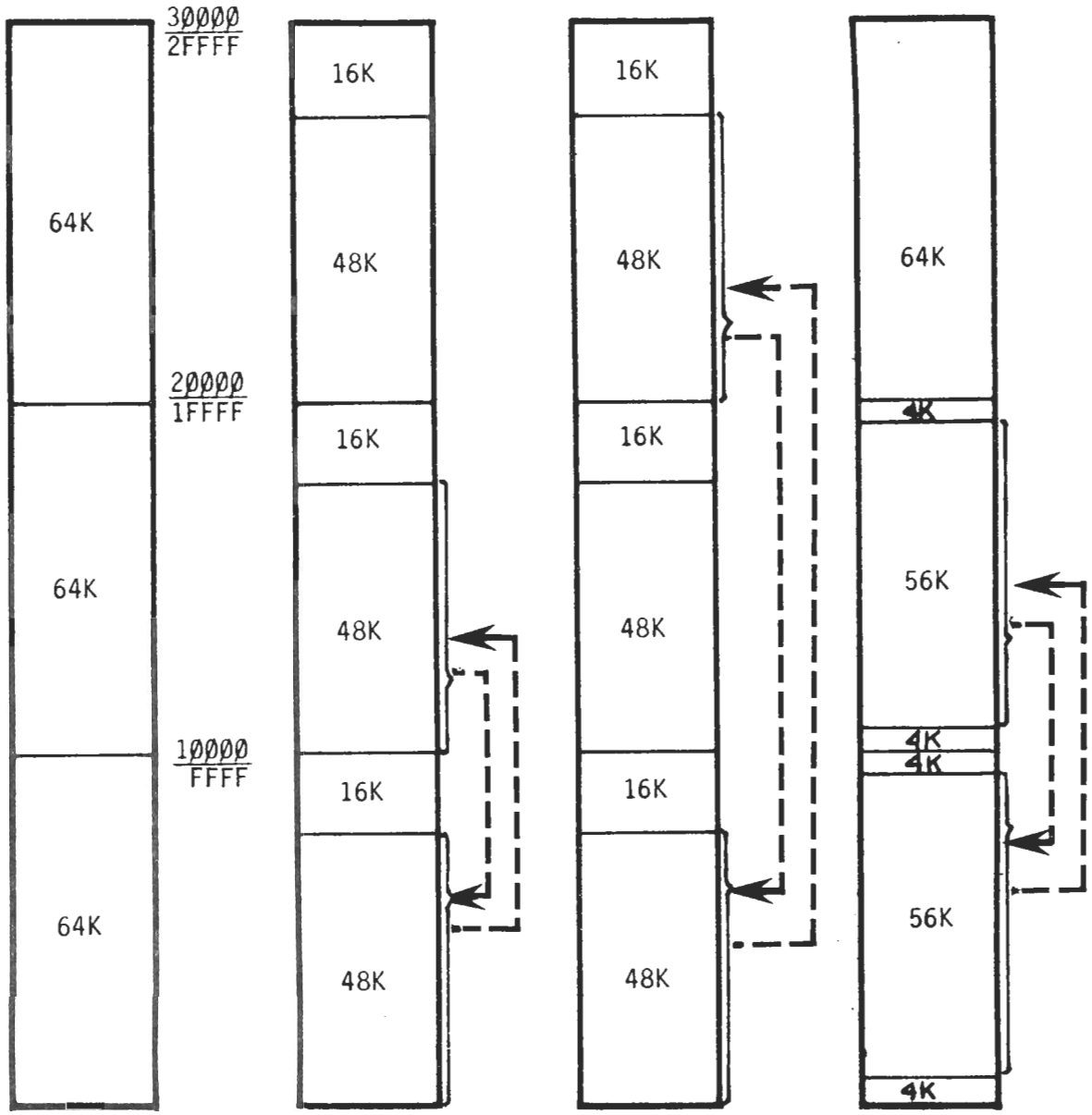
H/Z-100 MEMORY MAP



SYSTEM MONITOR MEMORY MAP (Monitor-100 ROM)



MEMORY BANK SWITCHING CONFIGURATIONS



MAPSELØ = Ø
MAPSEL1 = Ø
CONFIGURATION #1 (Power-Up Configuration)

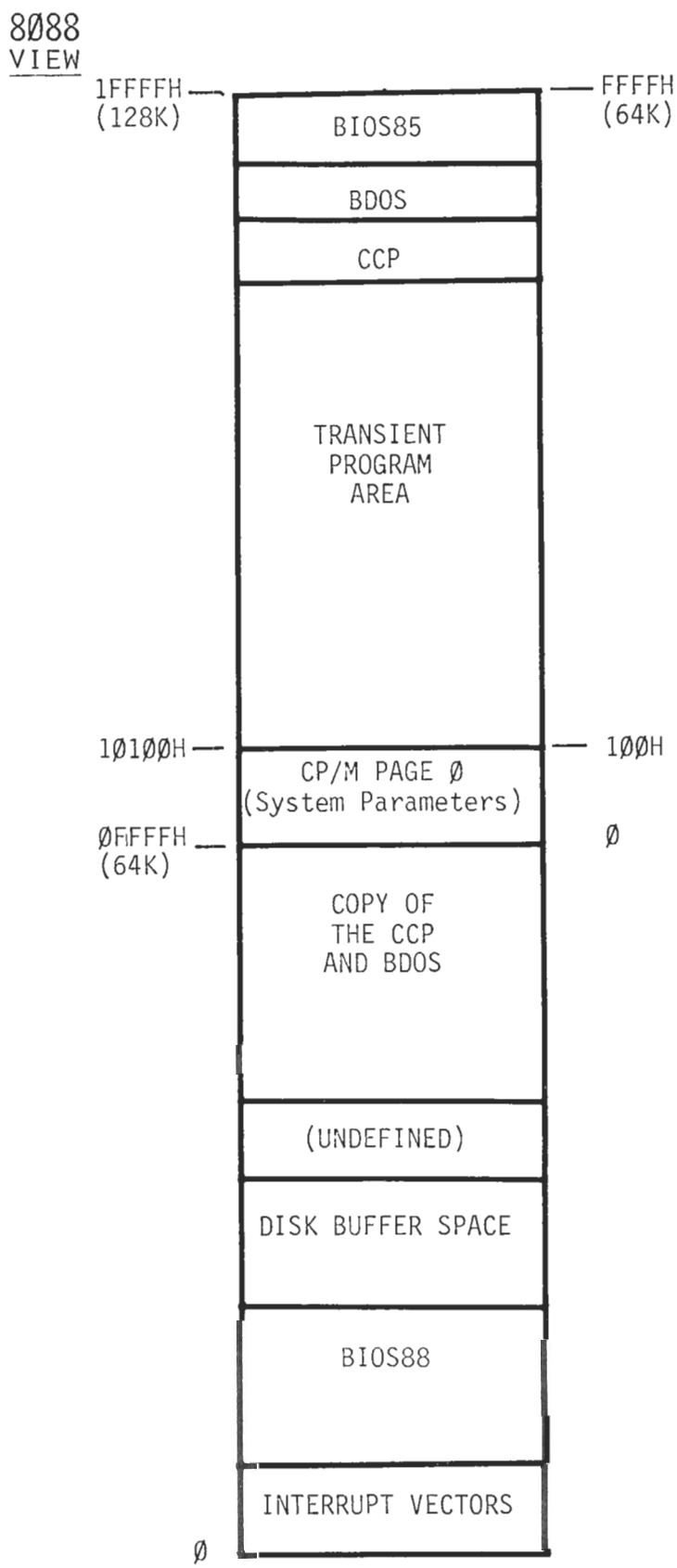
MAPSELØ = 1
MAPSEL1 = Ø
CONFIGURATION #2

MAPSELØ = Ø
MAPSEL1 = 1
CONFIGURATION #3

MAPSELØ = 1
MAPSEL1 = 1
CONFIGURATION #4

*See Memory Control Latch Options.

CP/M-85 MEMORY MAP



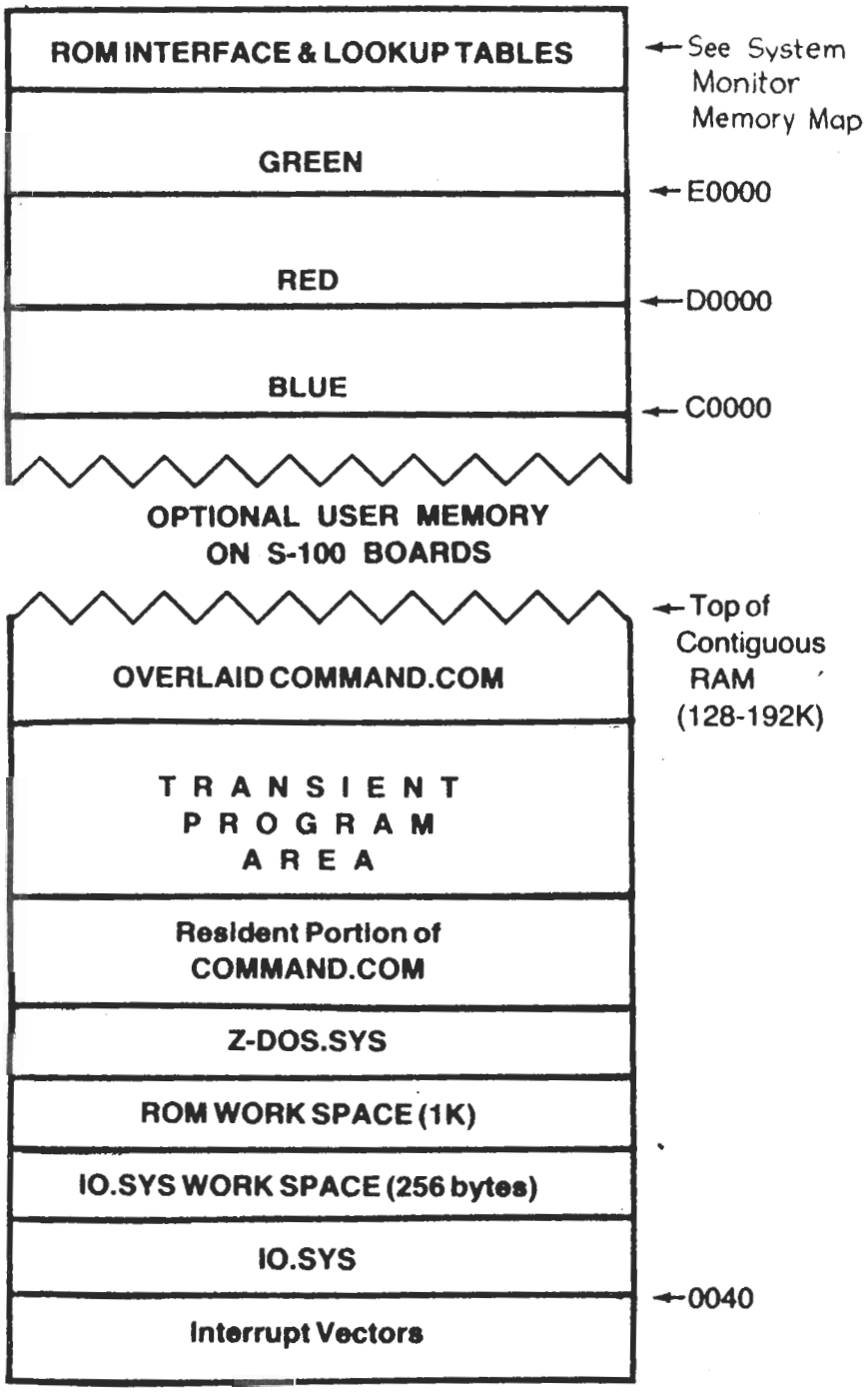
NOTES:

1. As far as the CP/M programmer is concerned, the system is located between ØK and 64K.

2. If an I/O operation takes place, the 8Ø88 activates to process the input of output (I/O operations are passed from BIOS85 to BIOS88).

3. A warm boot activates the 8Ø88, which transfers the BDOS/CCP copy to the BDOS and CCP areas above the TPA.

Z-DOS MEMORY MAP



H/Z-100 I/O PORT ASSIGNMENTS

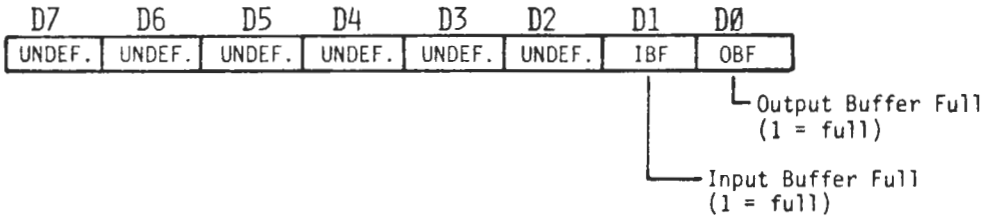
Port Address	Device Name	Type of Operation
FF	S101 DIP Switch	Read
FE	Swap Port (PSP)	Write
FD	High Address Latch (HIGHADDR)	Write
FC	Memory Control Latch 9MEMCTL)	Write
FB	Timer Status (TIMRSTAT)	Read/Write
FA	(Reserved)	
F9	(Reserved)	
F8	(Reserved)	
F7	(Reserved)	
F6	(Reserved)	
F5	Keyboard Command Register	Write
F5	Keyboard Status Register	Read
F4	Keyboard Data Register	Read/Write
F3	Master Interrupt (PIC)	Read/Write
F2	Master Interrupt (PIC)	Read/Write
F1	Slave Interrupt (PIC)	Read/Write
F0	Slave Interrupt (PIC)	Read/Write
EF	Serial Port B Command Register	Read/Write
EE	Serial Port B Mode Register	Read/Write
ED	Serial Port B Status Register	Read
ED	Serial Port B SYN/DLE Control Registers	Write
EC	Serial Port B Receiver Holding Register	Read
EC	Serial Port B Transmitter Holding Register	Write
EB	Serial Port A Command Register	Read/Write
EA	Serial Port A Mode Register	Read/Write
E9	Serial Port A Status Register	Read
E9	Serial Port A SYN/DLE Control Registers	Write
E8	Serial Port A Receiver Holding Register	Read
E8	Serial Port A Transmitter Holding Register	Write
E7	Timer Control Word Register	Write
E6	Timer Counter #2 Data	Read/Write
E5	Timer Counter #1 Data	Read/Write
E4	Timer Counter #0 Data	Read/Write
E3	Parallel Port Control Register B	Read/Write
E2	Parallel Port Peripheral/Data Direction Reg. B	Read/Write
E1	Parallel Port Control Register A	Read/Write
E0	Parallel Port Peripheral/Data Direction Reg. A	Read/Write

Port Address	Device Name	Type of Operation
DF	(Reserved)	
DE	Light Pen Counter (LTPNCS)	Read
DD	CRTC (6845CS) R0-R17 Registers	Read/Write
DC	CRTC (6845CS) Address Register	Write
DB	Video 68A21 (CRTIOCS) Control Register B	Read/Write
DA	Video 68A21 (CRTIOCS) Peripheral/Data Direction Reg. B	Read/Write
D9	Video 68A21 (CRTIOCS) Control Register A	Read/Write
D8	Video 68A21 (CRTIOCS) Peripheral/Data Direction Reg. A	Read/Write
D7 ... C0	(Reserved)	
BF	Secondary Z-207 (undefined)	
BE	Secondary Z-207 (undefined)	
BD	Secondary Z-207 Status Port (U31)	Read
BC	Secondary Z-207 Control Latch (U30)	Write
BB	Secondary Z-207 Data Register (1797)	Read/Write
BA	Secondary Z-207 Sector Register (1797)	Read/Write
B9	Secondary Z-207 Track Register (1797)	Read/Write
B8	Secondary Z-207 Status Register (1797)	Read
B8	Secondary Z-207 Command Register (1797)	Write
B7	Primary Z-207 (undefined)	
B6	Primary Z-207 (undefined)	
B5	Primary Z-207 Status Port (U31)	Read
B4	Primary Z-207 Control Latch (U30)	Write
B3	Primary Z-207 Data Register (1797)	Read/Write
B2	Primary Z-207 Sector Register (1797)	Read/Write
B1	Primary Z-207 Track Register (1797)	Read/Write
B0	Primary Z-207 Status Register (1797)	Read
B0	Primary Z-207 Command Register (1797)	Write
AF ... A8	(Reserved)	

KEYBOARD PROGRAMMING OPTIONS (PORTS F4H, F5H)

PORT	ADDRESS
Command Port	F5
Status Port	F5
Data Port	F4

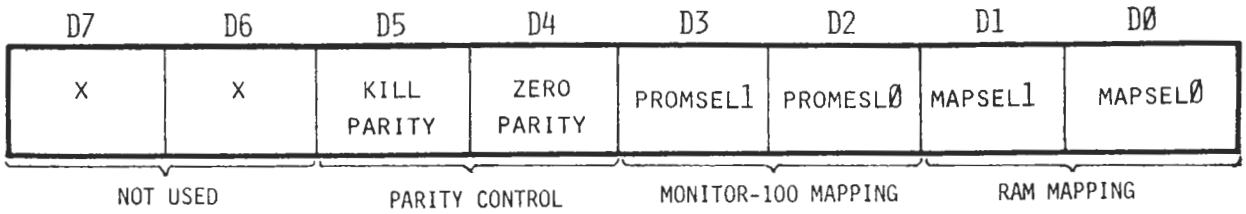
STATUS REGISTER



COMMAND SUMMARY

COMMAND	CODE (Hex)
RESET	00
AUTOREPEAT ON	01
AUTOREPEAT OFF	02
KEY CLICK ON	03
KEY CLICK OFF	04
CLEAR FIFO	05
CLICK	06
BEEP	07
ENABLE KEYBOARD	08
DISABLE KEYBOARD	09
KEY UP/DOWN MODE	0A
NORMAL SCAN MODE	0B

MEMORY CONTROL LATCH OPTIONS (PORT FCH)



DATA BYTE TO MEMCTL

RAM (See Memory Bank Switching Configurations)

D1 = Ø, DØ = Ø: *Configuration #1*

D1 = Ø, DØ = 1: *Configuration #2*

D1 = 1, DØ = Ø: *Configuration #3*

D1 = 1, DØ = 1: *Configuration #4*

MTR-100

D3 = Ø, D2 = Ø (Option Ø): *For a memory read, the monitor appears to be in all of the address space. For a memory write, the conditions are similiar to Option 2.*

D3 = Ø, D2 = 1 (Option 1): *Puts the monitor at the top 8K of each 64K page of memory.*

D3 = 1, D2 = Ø (Option 2): *Places the monitor in the top 8K of the 8088's natural 1 megabyte address space.*

D3 = 1, D2 = 1 (Option 3): *Disables the monitor.*

ZERO PARITY

D4 - Ø: *Writes a binary Ø into each parity RAM location.*

D4 = 1: *Permits the parity RAM to store the parity bit.*

KILL PARITY

D5 = Ø: *Disables the parity checking circuits.*

D5 = 1: *Enables the parity checking circuits.*