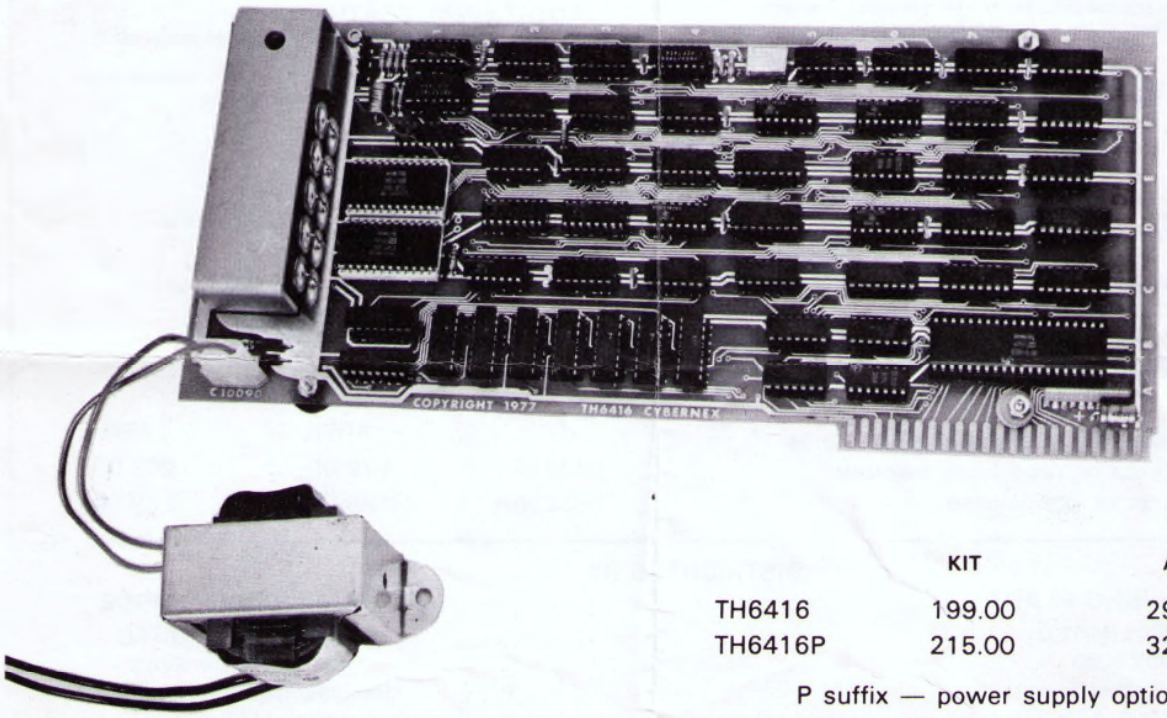
THE CYBERNEX
TH6416
Video Terminal Card Kit

- generates one page of 16 lines, 64 characters per line.
- includes UART for TTL level serial asynchronous communication.
- operates at 110, 150, 300, 600, 1200, 2400, 4800 or 9600 baud.
- generates 128 character USASCII with lower case
- cursor control includes up, down, forward, back, return, home.
- edit functions include clear page and clear to end of line.
- depressing "HERE IS" key displays control codes for debugging.
- block see through cursor surrounds and inverts letter - "▒".
- delete code is inhibited from display.
- video output is 75 ohm and is formatted for normal TV set.
- accepts input from 7 unit ASCII keyboard with low true strobe.
- optional on card power supply will drive 5V .2A keyboard too.



	KIT	ASM
TH6416	199.00	299.00
TH6416P	215.00	320.00

P suffix — power supply option

For more information consult your local computer store

CYBERNEX

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TH6416

SPECIFICATIONS

DISPLAY

format	64 characters per line one page of 16 lines
font	5 X 7 dot matrix
repertoire	128 character USASCII
refresh rate	60 Hz
memory	2102A-4 MOS RAM

COMMUNICATIONS

data I/O	serial asynchronous 10 or 11 unit code TTL compatible
baud rates	110, 150, 300, 600, 1200, 2400, 4800, 9600 selectable at the edge connector

COMPUTER/KEYBOARD CONTROL

cursor control	backspace, forward space, line feed, cursor up, home, return to start of line
cursor edit	clear page, clear to end of line

OPERATOR CONTROLS

full/half duplex
cursor on/off
parity enable
even/odd parity
baud rate select
BREAK
HERE IS (transparency mode)
one or two stop bits

These control inputs and the keyboard data inputs are available on the edge connector.

PARITY

If parity is enabled and a parity error is received, a question mark is written at the cursor position.

POWER REQUIREMENTS

+5 volts, 900 milliamps nominal.

CURSOR DISPLAY

The block see-thru cursor completely surrounds and inverts any character it overlays.

Cursor control is wrap-around in the forward direction. If the line is overflowed the cursor automatically moves to the start of the next line.

The cursor does not backspace beyond the start of the line.

ROLL UP/DOWN

With the cursor on the bottom line, if the line is overflowed or a LINE FEED is executed, the display scrolls up one line. The bottom line is cleared, the top line is lost and the cursor remains on the bottom line.

If the cursor is on the top line and CURSOR UP is executed, the display scrolls down one line. The top line is cleared, the bottom line is lost and the cursor remains on the top line.

TRANSPARENCY MODE

With the lower case option (128 character set) if transparency is enabled all characters are written into memory. Control codes do not execute but are displayed as symbols. Parity errors and DELETE inhibit are ignored.

DELETE INHIBIT

The DELETE or RUB OUT code is inhibited from display since this is often used as a fill character for printers on time - share utilities.

VIDEO OUTPUT

The horz sync, vertical sync, cursor display and character display are combined into a single 75 - ohm output for connection to a TV video amplifier or video monitor.

Horz and vertical drive pulses are also available for direct drive data displays.

ADDITIONAL FEATURES

Power on ititialization clears the page and moves the cursor to the home position.

The 8-bit parallel input port can be used for keyboard input or parallel input from a microprocessor.

complete with sockets for all integrated circuits and edge connector.

KEYBOARD REQUIREMENTS

Keyboard input must be TTL compatible, 7 unit ASCII code with low true strobe. If the keyboard is connected to the optional power supply, keyboard ratings must be +5 volts, 200 milliamps maximum.

OPTIONAL POWER SUPPLY

The optional on card power supply provides 1200 milliamps at +5 volts. This supply option includes the power transformer.

Also available CYBERNEX **TH3216**

- 2 pages of 32 characters by 16 lines
- page dump or read from memory
- 64 character upper case

	KIT	ASM
TH3216	179.00	269.00
TH3216P	195.00	289.00

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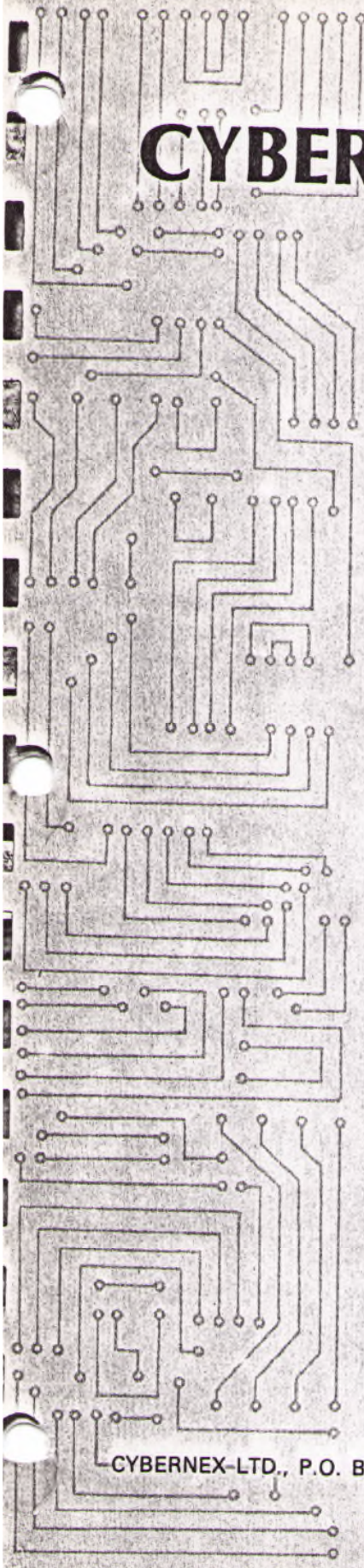

CYBERNEX

TH6416
DOCUMENTATION

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2183 DUNWIN DRIVE, MISSISSAUGA, ONTARIO L5L 1X2 (416) 828-2810

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I. TH-6416 OPERATIONAL SPECIFICATIONS

A. Display Specifications

Display Format	64 characters per line. 16 lines per page. 1 page.
Character Generation	5 x 7 dot matrix in a 7 x 11 field. NRZ-L coding of video display data. 64 USASCII character set. 128 USASCII optional character set.
Memory	MOS RAM; 2102-1 or 2102A-4 or equivalent.
Frame Size	264H (H = horz scan line).
Vertical Blanking	88H.
Vertical Sync	5H.
Vertical Drive	5H.
Vertical Sync Rate (refresh rate)	60 Hz.
Horz Blanking	0.33H.
Horz Sync	0.08H.
Horz Drive	0.38H.
Horz Sync Rate	15.840 KHz.
Video Output	The horz sync, vert sync and display information are combined into a single 75 ohm output capable of directly driving a TV video amplifier or a standard video monitor.
Horz and Vertical Drive	Separate horz and vertical drive outputs are available for data display monitors requiring direct drive.

The horz and vertical sync and drive signals are generated synchronously from a crystal controlled timing chain, thus eliminating any display jitter or swim.

The large percentages of vertical and horz blanking are necessary since a television and most video monitors are overscanned up to 30% (non-viewable area of screen). For further information refer to EIA RS-170 and RS-344 specifications.

B. Communications Specifications

Normally communications with the TH-6416 is serial in and out. A keyboard is connected in parallel to the UART.

Serial data I/O lines are TTL compatible, the output line can sink 4 TTL loads.

The UART is strapped for an 8-bit byte (mark, space or parity bit and 7 bit ASCII code).

C. Cursor Format And Controls

The cursor is a block see-thru type, that is a solid 7 x 11 dot font which completely surrounds and inverts any character it overlays.

8 control functions are decoded;

7 bit Hex.	7 bit OCTAL	TTY Function	Keyboard Operator	Terminal Function
08	010	BS	CNTL H	backspace cursor
09	011	HT	CNTL I	forward space
OA	012	LF	CNTL J	line feed
OB	013	VT	CNTL K	home cursor
OC	014	FF	CNTL L	home and clear page
OD	015	CR	CNTL M	return to start of line
OE	016	SO	CNTL N	reverse line feed
OF	017	SI	CNTL O	clear to end of line

All other control codes are inhibited. In transparency mode all control codes are inhibited.

Cursor control is wrap-around in the forward direction. If the line is overflowed the cursor automatically moves to the start of the next line.

The cursor does not backspace beyond the start of the line, that is, there is no wrap-around in the reverse direction.

D. Edge Connector Controls and Data I/O

The convention for inputs is as follows;

A logic one (1) is high. The inputs are driven to a logic one when unconnected (open) by pullup resistors on the board. It is not necessary to pull up UART inputs since this device has internal pull up resistors.

To effect a logic zero (0) on any control line it is grounded.

For data inputs a logic one must be between + 2.4 and +5.0 volts. A logic zero must be between 0.0 and +0.5 volts.

1. DATI Serial data input, TTL compatible. This line is pulled up by the SIP and thus if left unconnected will remain in the mark (logic one) state.

2. DATO Serial data output. This output is TTL compatible and can sink 4 TTL loads (6.4 ma).

3. KIS Keyboard input strobe. This requires a low going pulse or logic zero pulse of 0.0 to 0.5 volts. Minimum pulse width is 250 ns (nanoseconds). Parallel input data on KIØ to KI7 lines must be true for 40 ns before and after the pulse occurs to properly load the UART transmitter.

4. KIØ - KI6 Keyboard data inputs. These seven parallel input lines must be ASCII encoded.

5. KI7 Eighth data input bit. For keyboard data input this line is normally left open. This inserts a mark data bit in the serial data output character. If grounded it inserts a space. If parity is selected this input is ignored.

6. TBMT Transmitter buffer empty. This output can be used if the TH-6416 is utilized as a parallel input display device loaded from a micro processor. KIS becomes the data input strobe. KIØ - KI7 are used for data inputs. The baud rate control inputs are left open (thus programming the fastest data rate of 9600 baud). The DATI input is left open. The full/half duplex input is grounded thus looping serial data back into the UART receiver.

TBMT is used as a flag to tell the micro processor when another character can be loaded. If this output is high the UART is ready to accept another byte,if low it is not ready.

7. TSB Number of stop bits. If left open (logic one) two stop bits are inserted into the serial data byte for a total of 11 bits (start bit mark or space or parity bit, 7 data bits, and two stop bits).

   If this input line is grounded only one stop bit is inserted for a 10 bit code.

8. NP No parity. If left open the eighth data bit (K17) is inserted into the serial data byte. If grounded either odd or even parity is inserted. The UART is strapped such that the total number of data bits remains at eight.

   With parity enabled, if a parity error is received for any character a question mark is displayed at the cursor position.

9. EPS Even/odd parity select. If left open even parity is select, if grounded, odd parity is selected.

10. Cursor On/Off If open the cursor is displayed. If grounded the cursor is turned off.

11. Full/Half Duplex If left open the unit is in full duplex. UART data is written to the output line only and must be echoed to the DATI line by the computer to be displayed on the screen.

    For half duplex operation this line is grounded. Data is simultaneously transmitted on the DATO line and received by the UART.

    To test the TH-6416 locally, half duplex mode must be used to enable data to be written on the screen. The DATI input line should be disconnected for local testing.

12. BAUD Rate Select Three binary encoded input lines are used to select one of eight baud rates from 110 to 9600. These lines are denoted as Rate 2, Rate 1 and Rate 0.

OCTAL SW	RATE 2	RATE 1	RATE 0	BAUD RATE
7 —	0	0	0	110
6 —	0	0	1	150
5 —	0	1	0	300
4 —	0	1	1	600
3 —	1	0	0	1200
2 —	1	0	1	2400
1 —	1	1	0	4800
0 —	1	1	1	9600

1 = OPEN (PULL-UPS ON-BOARD)
0 = GND'D

A one is open and a zero is grounded. Thus if these lines are left unconnected the baud rate is 9600.

13. Break This is normally connected to the Break key on the keyboard. When this input is grounded the DATO line is forced low (space). This is often used by computer operating systems.

14. Here is This is normally connected to the Here Is key on the keyboard for use with the lower case option. When this input is grounded all data is in transparency mode. That is all data is written on the screen; control functions are displayed as symbols rather than being executed and parity errors are ignored. This is a very useful feature for debugging computer programs containing various control code sequences.

15. Video Out The composite video 75 ohm output is available at the edge connector for driving a video monitor or TV video amplifier. A six pin output is also provided for direct drive data display.

For pin out assignment of these functions refer to APPENDIX.

E. Roll Mode

For rollup operation if the bottom line is overflowed or a LINE FEED is executed when the cursor is on the bottom line, the data is scrolled up one line on the display. The bottom line is cleared, the cursor remains on the bottom line and the top line is lost.

This unit also executes rolldown. If the cursor is on the top line and a REVERSE LINE FEED is executed, the displayed data scrolls down one line. The top line is cleared, the cursor remains on the top line and the bottom line is lost.

F. Additional Functions

The DELETE code (177 octal) is inhibited from writing on the screen. This code is often used as a fill character on time-share utilities for printers. The DELETE code is enabled in transparency mode.

Any combination of data or control characters can be received by this unit at maximum speed without the need for fill characters with one exception. At 9600 baud one fill character is required after the CLEAR PAGE control code to allow sufficient time for the screen to clear. This fill code can be non executing control code or the DELETE code.

A power up initialization circuit clears the page and homes the cursor.

G. Power Supply Requirements

A single +5 volt power supply is required for this board accurate to within ± 5%, ripple not to exceed 50 millivolts. The current requirement is nominally 900 milliamps depending on components of different manufacture.

The optional on-card power supply is capable of supplying about 1.2 amps at +5 volts and thus there is a reserve of approximately 300 ma for driving a keyboard. The heat sink should be relatively well exposed. If placed in an airtight enclosure the temperature may rise sufficiently for the regulator to go into thermal shutdown. The operator will then have to wait for the regulator to cool sufficiently before proceeding.

SECTION II

II. BLOCK DIAGRAM DESCRIPTION

A. General

This terminal is designed for use with a raster scanned television set, the limitations of which were considered in the design.

A TV set operates at VHF frequencies between 52 and 213 MHz. The incoming signal is mixed with a local oscillator, amplified in an IF strip, and rectified in a video detector. This signal is input to a video amplifier which modulates the CRT electron gun. Following the video amplifier is a sync separator which detects the horz sync with a differentiator and the vertical sync with an integrator. The horz sync synchronizes the horz oscillator at 15.750 KHz and the vertical sync synchronizes the vertical oscillator at 60 Hz. This synchronization provides the reference for the picture frame.

Normally a TV picture and most video monitors are overscanned, that is, not all of the picture frame can be seen. The EIA RS-170 specification states that manufacturers provide a viewable portion of 70% of the picture in both the horizontal and vertical directions. This specification also states that the horz sync be 0.075H $\pm$0.005H (where H is a horizontal scan line at 15.750 KHz) and the vertical sync be 3H nominal.

For the terminal the composite video output contains the video information and the sync pulses. It is equivalent to what would be seen at the output of the video detector in a TV set. Thus it is only necessary to put a switch on the input to the video amplifier to switch between the output of the video detector and the output of the terminal. This is normally simple on black and white TV sets because the video amplifier and detector are on separate boards connected with a wire.

The obvious question is why not build a VHF modulator to hook onto the antenna? In the United States the FCC has all but banned this practice. In Canada regulations exist which specify the maximum field strength allowable of radiated VHF in microvolts per meter at a fixed distance from the radiation source. However the onus is on the user not to interfere with anyone's reception even if these standards are met. This company will accept no responsibility for radiated interference.

To connect to the TV video amplifier a piece of 75-ohm coaxial cable (such as RG-59U) or twisted pair of wires, 28 AWG or larger, with at least one twist per centimeter should be used. The overall length should not exceed 3 meters, the shorter the better.

In TV video transmission the effective bandwidth is halved by transmitting two interlaced fields of 262.5 lines each. The required bandwidth of the TV video amplifier is approximately 3.5 MHz.

However on terminals interlacing is rarely done because of the added logic complexity and more importantly, the interlace shimmer caused by a combination of fast flourescent decay of the P4 phosphor and the high contrast ratio of a bright character on a dark background. The dot clock rate in this terminal is 10.644 MHz and since the coding is NRZ-L this is halved to 5.32 MHz. Video monitors and most recent solid state black and white TV sets exceed the minimum bandwidth requirements and therefore can display a 64 character line. However older TV sets with lesser bandwidths may result in considerable smearing of characters.

Though TV sets utilize a horz sync rate of 15.750 KHz this can be varied between 15.5 and 16.0 KHz. Variation outside this range may produce problems since the high voltage supply for the CRT is derived from the horz oscillator. This is a resonant circuit, thus "pulling" the frequency can seriously affect its efficiency.

The vertical sync rate from the terminal is exactly 60 Hz. The reason is that any stray power line field (such as from the line transformer is the TV set) will couple energy into the CRT yoke. If the vertical sync rate of other than 60 Hz were used, a beat frequency of the difference would occur. This results in a side to side movement of the displayed data and is commonly called swim.

The general characteristics of this terminal will now be discussed in more detail. A 5 x 7 dot matrix is used to display a given character, that is, a character can be a maximum of 5 dots in width and 7 scan lines in height. In addition 2 dot widths are used for intercharacter spacing on a scan line and 4 scan lines (dot widths) are used for vertical spacing between characters. Thus the character field is 7 x 11 dots and in this design the 5 x 7 character is centered in this field. The cursor occupies a full field.

The page format is 16 lines of 64 characters each. That is a line of characters must consist of 64 fields in the viewable portion of the TV screen. Note that each character can be as much as 7 scan lines in height and since the video information must be presented serially to modulate the CRT beam as it sweeps across the screen, each character must be accessed 7 times in memory to be displayed. Each horz scan line of this character is called a slice.

The vertical sync rate is 60.000 Hz with a vertical sync pulse of 5H (5 horz scan lines). Each frame consists of 264 H which gives a horz sync rate of; 264 x 60 = 15.840 KHz.

Each character line consists of 11H (field is 11 lines) and thus there are 264/11 = 24 character lines. 16 of these are viewable; the other 8 are blanked. Thus 16/24 = .66F or 66% of the frame is viewable in the vertical direction on the screen.

Each horz scan line consists of 96 fields, 64 of which are viewable 96/64 = .66H or 66% of the horizontal line is used to display characters; the rest is blanked, part of which time is used in horz retrace. In the center of the horz blanked portion of 16H, a horz sync pulse of 8 field widths is produced for each line. Thus the horz sync pulse is 8/96 = 0.083H or approximately 8%.

The frequency at which each character is accessed in memory is 15.840 x 96 = 1520.64 KHz. Thus the memory access time must be within; 1/1520640 = 658 manoseconds. Since various propagation delays can amount to 100 ns the memory must be capable of 550 ns access. Thus 2102-1 or 2102A-4 or faster is required.

Since the character field is 7 dot widths the dot clock rate is 1.520624 x 7 =10.644 MHz which is the crystal oscillator frequency.

Before the terminal logic is described in detail, the functional block diagram will be discussed. Where possible the blocks are located in the corresponding position to the detailed drawing and the predominant integrated circuit locations are marked in each block.

B. Timing Chain

The heart of the display unit consists of the timing chain (all blocks on the top of the drawing). A 10.644 MHz oscillator provides the dot clock. This drives the 7 phase clock which provides the 7 dot times for each character field. The dot clock also drives the display shift register providing the dot pattern on the screen.

One phase of the 7 phase clock drives the horz counter which counts the 96 character field positions on a horz scan line. This counter also gates one phase of the 7 phase clock to load the display shift register from the character generator for 64 of the 96 character positions. A horz sync pulse is produced during the horz blanking period (the other 32 positions) once during every cycle of the horz counter.

The horz sync pulse drives the slice counter which provides the 11 lines for each character field; 7 lines for character display and 4 lines for vertical spacing.

Each cycle of the divide by 11 slice counter counts the divide by 24 line counter. 16 of these character fields are used for data display; the other 8 are blanked (vertical blanking). This line counter cycles at 60Hz. A vertical sync pulse of 5 H is provided at the center of the vertical blanking period. The vertical drive pulse is also 5 H.

C. Cursor Display

The next blocks to consider are the horz address and the line address. These are used for two purposes; to provide the means for displaying the cursor position and to provide the read/write memory address. The divide by 64 horz address provides the cursor position on the line and the divide by 16 line address indicates the line of the page. Note that 64 x 16 = 1024, the total number of memory locations.

The horz match circuit compares the horz address to the horz counter. The match is only valid during 64 of the 96 positions of the horz counter. Also the line match compares the line counter to the line address and again the comparism is only valid during 16 of the 24 counts of the line counter. When both circuits are matched the cursor is displayed. The horz match is valid for 7 dot widths and the line match is valid for 11H (one cycle of the slice counter). Thus the cursor occupies a full 7 x 11 dot field.

The cursor can be turned off (for display only applications) without affecting the terminal operation.

D. Data Display Refresh

During refresh the entire memory contents of the selected page are displayed 60 times per second. To perform this function the RAM memory is addressed by the horz counter and the line counter. Note that the horz counter always provides the horz address for the RAM. However the line counter provides the RAM refresh address thru the line multiplexer for only 8 of each 11 line cycle of the slice counter.

For storage of the 64 character ASCII code set, the memory must be 6 bits wide. The memory must be 7 bits wide for the full 128 character set. This RAM data output becomes the ROM (character generator) address which is in fact a "look-up" of the dot pattern for each stored character. 3 binary coded lines from the slice counter provide the remainder of the ROM address, which in turn provides a unique dot pattern for each slice of the displayed character. For this particular ROM only 7 of the 8 binary addresses from the slice counter provide dot patterns; binary zero produces a blank output. Thus the character is a maximum of 7 dots high.

During the remaining 3 of 11 lines of the slice counter the display shift register is inhibited, producing a blanked output.

E. Data Read/Write

When serial data is received by the UART it is presented in parallel at the receiver buffer. The control function decoder decides whether to execute a control or read/write function. Assuming that a write into memory is to occur, recall that the refresh cycle used 8 of the possible 11 line times of the slice counter cycle. During this time all control function decoding and read/write is inhibited, since the refresh address is not the proper read/write address. Now during the other 3 line times of the slice counter cycle the line multiplexer switches to the line address, and read/write is enabled. With the proper line address the RAM memory address is valid when horz match occurs and thus data is written into memory at this time. the UART receiver is simultaneously reset to allow the next character to be received.

F. Control Function Decode

If the data presented at the UART receiver is a control function (000 to 037 octal) a control function is decoded to perform some cursor movement or editing. The write circuits are inhibited. For reasons of simplicity all control functions are also executed during a valid RAM address.

G. Roll Control

The roll control is activated by underflow or overflow of the line address. For roll up operation the line address overflows which activates the roll logic and increments the line offset counter. The roll logic freezes the line address at the bottom of the page and selects this address thru the line multiplexer. The line address and offset counter are added together in the line adder to give the address of the line to be cleared (which is the top line of the page). When refreshing is resumed the refresh address from the line counter is added to the offset counter thru the line multiplexer and adder. Since the offset address was incremented by one display of data begins one line earlier giving the appearance on the display of a roll up operation.

For roll down, the operation is similar except that the line address is frozen at the top of the page and the offset counter is decremented. Thus the offset counter is a pointer to the addressed line in memory.

H. Clear Logic

When a CLEAR PAGE is executed the horz and line addresses are reset to Zero thus moving the cursor to the HOME position. The offset counter is cleared and the line multiplexer selects the line address. The memory write control is set to provide a continuous stream of write pulses.

The horz counter is used to scan the memory addresses on each line. The horz sync pulse is used to increment the offset counter to provide the next line to be cleared in memory. After all 16 lines have been cleared the offset counter overflows and turns off the clear control.

Power up initialization is similar except that the offset counter may continue for several cycles.

I. Baud Rates

Three binary coded input lines are available at the edge connector to select one of eight baud rates from 110 to 9600. All baud rates are 1.0% in error. To illustrate this consider the baud rate of 9600. The input from the horz counter is 280.16 KHz; the decade counter divides this by 2.5 to give 152.064 KHz. The UART divides this by 16 to give 9504 baud. The percentage error is;

$$\frac{9600 - 9504}{9600} \times 100 = 1.0\%$$

Since the error is cumulative, the jitter on the 10th bit (first stop bit) of the serial input data is 10%.

Since the data transmission mode is NRZ-L and the UART samples near the center of each bit, the maximum allowable error is 50% which also includes the start bit verification jitter of approximately 6%. Thus the baud rate timing can be in error by as much as 4% before data is lost in this form of asynchronous communication.

With one exception, no fill characters are required to receive a stream of data into the terminal. Consider the baud rate of 9600. One serial data byte requires 11 bit times of 11/9600 = 1.1458 milliseconds. Each horz scan line requires 1/15840 = 0.0631 milliseconds. The number of scan lines that can occur in the time required to receive one character is 1.1458/0.0631 = 18.16. Since read/write is inhibited during refresh, the maximum memory access rate for this architecture is once every 9H (8H for refresh +1H for address access time). This is obviously much less than 18.16H and thus the terminal can comfortably accept data at 9600 baud.

The exception is the CLEAR PAGE control. As previously mentioned this function requires up to 17H to execute. Add to this the 8H for refresh lockout and the result is 25H worst case execution time. Since this is greater than 18.16H the character immediately following the clear page code could be missed. To ensure that this does not happen, a non-executing fill character such as an unused control code or DELETE is inserted into the data stream after the CLEAR PAGE control code. Of course at lower baud rates this fill character is not required.

J. Line Control

1) full/half duplex - In half duplex, data entered from the keyboard is loaded into the UART transmitter and routed to the data output line and into the UART receiver simultaneously. In full duplex mode, data is routed to the output line only and must be echoed by an external device (such as a processor) to be written into the terminal.

2) BREAK and HERE IS are explained in I.D.13 and I.D.14 respectively.

K. Parity

Two lines are available at the edge connector for parity control. If parity is enabled, the eighth (most significant) bit is the lateral parity checksum of the seven data bits. The EVEN/ODD parity control determines whether this checksum is even or odd.

If parity is enabled and a parity error is received for any character, a question mark is written into memory. In transparency mode parity errors are inhibited and the received character, whether it is correct or not, is written into memory.

III. DETAILED DESCRIPTION

A. General

It is assumed that the reader is familiar with the functional operation of digital intergrated circuits. If not, the reader must obtain data books or data sheets on these devices and become familiar before proceeding with this section. These data books are available from the manufacturers and distributors of integrated circuits.

The chronological order of the BLOCK DIAGRAM DESCRIPTION will be followed where possible.

The convention for naming logic elements is as follows; each element of an integrated circuit package will be lettered A, B, C etc. starting from the lowest order pin numbers. For instance a 7474 IC consists of two D flops. The flop with pin numbers 1 thru 6 is denoted as A while the flop with pin number 8 thru 13 is B. A 7400 IC consists of four two-input NAND gates and are designated as A,B, C, and D for each of the gates designated by Pin numbers 1, 2, 3 and 4, 5, 6 and 8, 9, 10 and 11, 12, 13 respectively.

B. Timing Chain

The oscillator is a series resonant circuit consisting of a crystal, two resistors, a capacitor and two inverter gates H4A and H4B. These gates are used in a linear mode of operation. Feedback coupling is provided by two 470 OHM resistors and the 100 pf capacitor. These components can be varied by $\pm$ 50% without affecting the circuit performance. (Undercoupling of this circuit will result in an oscillator that will not; overcoupling will result in an oscillator independent of the crystal frequency). The output of the oscillator is squared by the buffer H4F to provide the DOT CLK. This is used to drive the 7-phase clock and the display shift register E1.

The 7-phase clock consists of an 8 bit shift register H5 and the 8 input NAND gate H6. One low going pulse is circulated in the shift register. The output of the NAND gate is low only when the first 6 shift register outputs are high. When this low input is shifted in,the output of the NAND gate is asserted high and remains high for the next 6 cycles of the dot clock. The seven phases are shown in Fig. 1.

This 7-phase clock is used to drive the horz counter, time the read/write cycle, time the cursor position, latch the memory outputs and load the display shift register.

Since the 7-phase clock is a divide-by-7 circuit the frequency of each phase is; 10.644 MHz / 7 = 1.520 MHz.

Phase PØ is used to clock the horz counter C3 and C4. One cycle of the horz counter is 96 counts (character positions) representing one horz scan line (H) on the display. Of the 96 character positions, 64 are used as valid RAM addresses for addressing any character position on one of 16 lines. The other 32 character positions are for horz blanking which is further sub-divided into three segments; the front porch (12 character positions), the horz sync pulse (8 character positions) and the back porch (12 character positions). The horz sync (HS) is produced thru gating of F1F and F2C to enable clocking of H2B.

Horz sync rate is PØ/96 or 1.52 MHz/96 = 15.840 KHz.

As mentioned previously each character field is 11 dots high. 7 dots are used for displaying the character, the other 4 dots are blanked. Each dot in height is actually represented by a horz scan line. Each horz scan line that makes up a character is called a slice.

The horz sync pulse clocks the modulo 11 slice counter E2. This counter is made divide-by-11 by the feedback gate E3C. The least significant bits of the slice counter (SLØ, SL1 and SL3) provide the row address for the character generators C1 and D1. Slice 3 (SL3) is high for 3 of 11 lines the display register E1 is inhibited from displaying data by assertion thru F2D. The vertical interspace between characters is actually 4 lines. The top row of the character generators i blank. Refer to Fig 2 for the SLICE COUNTER TRUTH TABLE.

The line counter consisting of F4B and E4 is clocked when the slice counter reaches 1010 binary to center the cursor on the displayed character in the vertical direction. The line counter is modulo 24 to produce 24 character fields. Of these, 16 are valid refresh RAM addresses and valid cursor addresses for the 16 character lines of displayed data. The other 8 character fields are used for vertical blanking during which the display shift register E1 is inhibited thru F2D by VB H.

The vertical sync (VS H) is produced starting at the centre of the vertical blanking interval by clocking F4A high when the line counter reaches 10100 binary (refer to the truth table of Fig. 3). The slice counter resets F4A after a duration of 5H by the assertion of SL high thru inverter H4E.

The VERTICAL DRIVE pulse is produced by power gate H1B from the vertical sync.

Note that the slice counter and subsequently the line counter are clocked by the horz sync pulse which occurs well into the horz blanking period. This is necessary since the last character of each displayed line is skewed into the horz blanking region.

The vertical sync occurs once per cycle of the line counter. Thus the refresh rate is;

$$\frac{15840}{11 \times 24} = 60 \text{ Hz}$$

C. Cursor Display

The horz address is given by D2, D3. This counter is incremented by FORWARD SPACE and whenever a data write occurs thru gate E3B. When the counter overflows (advances past the 64th character) F3B is clocked to provide a low pulse into E3D which resets D2, D3 by loading all zeroes into these counters. The pulse also increments the line address F6 thru gate E7B. This gives the cursor wrap around in the forward direction. The horz address is cleared and the line address is incremented which moves the cursor to the start of a new line.

The horz address is decremented by BACKSPACE input to D2-4. When the cursor is backspaced to the beginning of the line the underflow from D3-13 is used to load D2, D3 with zeroes. Thus the cursor will remain at the beginning of the same line.

C2 and D4 are quad 2 input EXCLUSIVE-NOR gates which are used as comparators. The open collector out puts are tied to a common pullup resistor of 2.2k. This out put goes high when there is a match between the horz counter and the horz address. Note that this comparison can only occur for 64 addresses. C4-11 is high during the horz blanking period and is compared to a zero on D4-8 and thus no match can occur.

The line comparator F5 is another EXCLUSIVE-NOR package used to compare the line counter to the line address. When a match occurs the cursor is present and the common output of F5 is high. Note that this match is true for one count of the line counter which is one cycle of the slice counter. Thus the cursor is 11 dots (scan lines) high.

The cursor is delayed for nearly two character times by H3 to allow the cursor to be displayed coincident with the display of the character from memory. This character is delayed by the RAM and character generator ROM access before it is loaded into the shift register E1.

Note that H3B is inhibited by VBL and thus the cursor cannot be displayed during vertical blanking. Also H3A is enabled only when a line match occurs. The horz match occurs for one count of the horz counter or one cycle of the 7-phase clock. Thus the output of H3A is seven dot widths since it is clocked on and off by P5.

Therefore the cursor is displayed thru H1D as one character field; 7 x 11 dots.

A line is provided on the edge connector to ground the line comparator output and thus inhibit H3A and the cursor display.

D. Data Refresh

The entire contents of the memory are displayed on the screen 60 times per second, or once for every cycle of the line counter.

To refresh the display, data is sequentially accessed in RAM memory by the addresses given by the horz counter and the line counter. The address of the horz counter is connected directly. The address from the line counter is directed thru multiplexer E5 and added to the offset counter address in D6 to form a line address pointer on the outputs of the adder D5. The multiplexer presents the line counter outputs to the adder for 8 of the 11 lines of the slice counter when SL3 is low via H4C and E6B.

The data output of the RAM is latched in A1, B1. The output of these latches become the look-up address for the character generator ROMs; C1 and D1. Three address lines from the slice counter provide the dot pattern look-up for each slice of the character.

The dot pattern is loaded into the display shift register by LD SR L which is delayed by almost two character times by F3A and F2A. Data loading is inhibited during vertical blanking and horz blanking by asserting VB L and HB H respectively to F3A. The load pulse is one phase of the clock P5 and is coincident with the start of the cursor display (if the cursor is present). The cursor and character are combined in the exclusive-nor gate H1D so that if the cursor overlays a character, this character will appear dark on a white cursor background. Refer to Fig. 4 for timing.

E. Data and Control Code Input

Assuming that the UART has received a character, the DATA AVAILABLE (UART-19) goes high one clock period of the baud clock after the receiver parallel output data lines are set. When a horz match occurs the output of A5B is high. If the terminal was currently doing a display refresh SL3 is low which inhibits B6A. When SL3 becomes high the line multiplexer E5 presents the line address of F6 to the adder to obtain the proper memory address. The next horz match provides a high to the input of B6A-2. B6A is clocked on by P1 (P1 is chosen to allow for propogation delay in the horz counter). This resets the data available on the UART-18. DA (UART-19) goes low and thus the next occurrence of P1 clocks B6A off. Thus B6A produces one pulse which is one character field in width (or one cycle of the 7-phase clock).

The steering of this pulse is determined by the received data character code. If the two most significant data bits (UART-6,7) are low the received data byte is a control character in the range 000 to 037 octal. D7A-4 is low which inhibits the write circuits by asserting A6A-2 low. The low output of D7A-4 enables D7B. If the character was a control code in the range 010 to 017 octal, D7B-10 is low which enables B5A to pass the pulse from B6A to the control code decoder C6. Thus one of the control codes is executed. If the control code was not in this range nothing happens.

If the input code was a DELETE code (177 octal), C5-8 is low which also disables the write circuits. No operation is performed.

If a data write is to occur the input character code must be in the range of 040 to 176 octal. This ensures that A6A is enabled (A6A - 2 is high). The pulse is steered to B6B thru gate A6C to produce a write pulse and load the character into memory. The output of A6A also increments the horz address via E3B.

There are two exceptions to the write data logic. These are given in Section III.L.Parity and III.M.Transparency Mode.

F. Character Generator Select

There is a link on the printed circuit board below the character generator C1 and to the right of the resistor. This link is shown on the schematic on the output of gate C2C.

If both character generators are used, this link must be out. If only the upper case character generator C1 is used, the link must be in. The printed circuit card is manufactured with the link out.

With the link out C2-10 is low for any stored ASCII code between 040 and 137 octal. This enables C1 by asserting C1-11 low. D1 is disabled by asserting D1-11 high thru F1E. When the stored code is between 000 and 037 octal (for stored control characters) or between 140 and 177 octal (for lower case characters), C2-10 is high disabling C1 and enabling character generator D1.

The outputs of these character generators are tri-state and are wire-ored into the display shift register inputs E1. Each dot pattern is loaded into E1 by one phase of the seven phase clock thru LD SR L and shifted out by the DOT CLK.

G. Data Read/Write Timing

The timing for data read/write is shown in Fig. 5. The horz counter is advanced on the falling edge of clock phase PØ. Each clock phase of the 7 phase clock is one period of the DOT CLK or approximately 94 ns (nanoseconds).

THC is the propagation time of the horz counter and is in the range of 20 to 100 ns depending on which bits of the counter are changing. If data is entered or a control function is to be executed the rising edge of P1 clocks B6A on and off for one period of the 7-phase clock or approximately 660 ns. This is shown in the timing diagram as DA STB L.

TAW is the address to write set up time for the 2102-1 or 2102A-4 RAM and is a minimum of 200 ns. TWP is the write pulse width and is asserted from the rising edge of P2 to the falling edge of P6 for a total time of 3 x 94 = 282 ns. TWR is the write recovery time and is a minimum of one clock phase or 94 ns.

The maximum data access for this RAM is 500 ns. The total access on this card is the maximum horz counter propagation time plus the RAM access or 100 + 500 = 600 ns. RAM output is latched on the rising edge of P6 which is 660 ns after the address begins to change.

The maximum access time for character generators is 450 ns. The ROM data outputs are loaded into the display shift register E1 by LD SRL (P5) which allows for 570 ns from the time that the data was latched by P6 into A1, B1.

The ROM dot pattern output begins one clock phase later, the maximum width of the character is 5 dots and is represented by DØ - D4 in Fig 5. The dot output is NRZ-L (non-return-to-zero-level) and the worst case bandwidth requirement would be alternate ones and zeroes. Each cycle would consist of two clock phases and thus the maximum output frequency is 1/2 x 94 ns = 5.32 MHz.

The cursor output occurs one clock phase before and remains for one phase after the dot pattern output for a total of seve dot widths.

H. Roll Logic

To execute a roll-up the display must appear to move up on the screen one line. Effectively this means that the refresh logic must begin accessing the memory one line later or that all line addresses must be incremented by one.

The line refresh address is given by F4B and E4 thru multiplexer E5 and is added to the offset counter D6 thru the adder D5. This line address output LØ - L3 is presented to the RAM memory. To roll the display up the offset counter is incremented; to roll the display down the offset counter is decremented.

The line address F6 displays the position of the cursor on the page. A roll up is executed only when F6 overflows (cursor is at bottom of page). This occurs when the horz address overflows or a LINE FEED is asserted thru E7B. The carry output on F6-12 goes low, resetting the direction flop F7B such that the parallel load inputs F6-15, 1, 10, 9 are all high. The rising edge of this pulse is asserted thru E7D to set flop H7 thus loading F6-11 with all ones. This holds the cursor address at the bottom of the page. Simultaneously this carry out put of F6-12 also increments the offset counter thru E7C. All logic remains in this state until the rising edge of the horz sync pulse (HSL) clocks H7A high. H7-6 becomes low resetting H7B thus removing the load condition from F6-11. Also H7-6 low steers the multiplexer E5 to the line address outputs F6. Thus the line address is added to the offset address thru the adder D5. Since the offset address was incremented by one and the line address has not changed, the line address is now pointed to the line that previously was at the top of the page. This is the line to be cleared and displayed at the bottom of the page.

H7-5 high (CLR LINE H) disables the multiplexers C8-15 and C7-15 so that the multiplexer outputs are driven low. Also B5-6 is driven high such that the memory inputs become the SPACE code (040 octal).

CLR LINE L from H7-6 is asserted on A6B to enable the memory write pulse to be generated from B6-8. Note that the blanks (Space codes) do not start writing into the memory until the horz blanking interval is done. The write pulse is inhibited by HB H on gate B5C.

The line to be cleared is addressed sequentially by the horz counter address lines HØ - H5. 64 memory locations are cleared (one line). At the end of the line HB H is again asserted disabling further memory write pulses. The rising edge of the horz sync pulse clocks H7A off, releasing all of the multiplexers. Thus the display has scrolled up one line, the top line has been cleared off and moved to the bottom line of the display and the cursor has remained on the bottom line.

Roll down is very similar. If the cursor is on the top line and a RLF (cursor up) is executed the line address F6 produces a borrow pulse on F6-13 which sets the direction flop F7 such that F7-8 is low and thus the parallel load inputs to F6-15, 1, 10, 9 are also low. The offset counter D6 is decremented by assertion of the borrow pulse to D6-4. The remainder of the operation is identical to the roll up description. The end result is that the display has scrolled down one line, the previous bottom line is cleared and moved to the top line of the display and the cursor remains on the top line.

CLR EOL (clear to end of line) is executed by immediately starting a clear operation, with the assertion of CLR EOL to set H7A. Note that the line address and offset address are not affected and thus the cursor position and display position remain unaltered. The clear operation terminates when the rising edge of HSL clocks H7A off.

I. Clear Page Logic

The clear page code (CLR) is asserted thru E7A to set F7A and clear the offset counter D6, the line address F6 and the horz address D2, D3. F7-6 low sets H7B. The memory clearing begins when HSL clocks H7A on. HS H is asserted thru E6C and E7C to increment the offset counter D6 and begin clearing on the second line of the display.

The clear operation continues clearing for 15 lines until the offset counter D6 generates a carry on D6-12 which clocks F7A off and releases H7B. Since this is coincident with HSL, H7A remains on for one more line to clear the top line of the display. Thus the clear logic remains on for 16 lines.

As mentioned previously when the CLR character is received by the UART, B6A is held off during refresh by SL3 low. Thus the access time for executing any write or control code operation is 8H + 1H for worst case. The total execution time for a clear page operation is thus 9H +16H = 25H. Since 1H = 1/15840 = 631 microseconds, 25H requires 1.58 milliseconds. At 9600 baud, a 10 bit serial code requires; 10/9600 = 1.04 ms. Thus a fill character (such as DELETE, 177 octal) must follow the CLEAR PAGE control code if packed characters are sent from the computer. This is the only case requiring a fill character. All roll operations at any baud rates and CLR PAGE operations at baud rates of other than 9600 do not require fill characters.

The power up initialization also clears the memory and homes the cursor in similar fashion to the CLR code. The RC time constant is approximately 40 milliseconds and PWR UP L is asserted thru F1A to set the clear flop F7A. There is one important difference for the power up clear. F7A is held on for several cycles of the offset counter D6. This allows the power supply to ramp up to + 5 volts when turned on. Note that if an external power supply is used (particularly switching supplies) the time constant for power supply turn on must not exceed 40 ms, or the power up initialization circuit will not function properly. If the external power supply does exceed 40 ms turn on then the capacitor in the power up circuit should be increased.

Note also that PWR UP H initializes the UART by assertion of a RESET high pulse on UART - 21.

To test the operation of the clear logic, offset counter, and write pulse logic F1-3 can be grounded.

J. Baud Rates

The input to the baud rate counters is derived from C3-8 of the horz counter. This frequency is 10.644 MHz/7 x 4 = 380 KHz. This is further divided by 2.5 in H8 to produce; 380 KHz/2.5 152 KHz on H8-9. The UART requires 16X baud rate, therefore the baud rate is 152 KHz/16 = 9500. The percentage error 9600 baud is;

$$\frac{9600 - 9500}{9600} \times 100 = 1.0\%$$

On the serial input, the UART samples NRZ-L (non-return to zero level) coding near the centre of each bit. Since this 1.0% error is cumulative the jitter on the 10th serial data input bit (first stop bit) is 10%. with center sampling the maximum allowable jitter is $\pm 50\%$ and therefore the baud rate clock can be in error of nearly $\pm 5\%$. Therefore 1% is more than tolerable.

All other baud rates 4800, 2400, 1200, 600, 300 and 150 are derived by H8 and F8 by dividing each successive count by two. The 110 baud rate is derived by dividing the 1200 baud rate by 11 in E8 and E6A.

The outputs of the baud rate counters are selected by the 8 to 1 line multiplexer D8. Three binary coded inputs provide one of eight selection. See Section I.12.

K. Line Control

For half duplex operation, the FULL/HALF input line is grounded which allows the serial output data to be input back into the UART via B5D and A5C. If the FULL/HALF input line is high (open) then B5D is inhibited and data is output on A5D only. This is full duplex mode.

When the BREAK input is grounded, the data output of A5D is held in the SPACE (low) state.

L. Parity

Parity mode is selected by grounding UART-35. To preserve an 8-bit length data code, the number of data bits is shortened to 7 by simultaneously grounding UART-38. If UART-39 is high (open) then EVEN parity is inserted into the eighth bit. If grounded ODD parity is inserted. Most time share systems use EVEN parity.

If parity mode is enabled and a parity error is received by the UART, UART-13 is asserted high which drives A6-11 low to select the alternate multiplexer inputs C7, C8. These inputs are set to 077 octal which is the question mark code. Note also that A6-8 is driven high which disables the control decoder D7 and enables the write circuits. Thus for any received character (except DELETE) a question mark is written into memory.

M. Transparency Mode

When HERE is in high (open) the logic is set for normal data write and control decode mode. However when HERE is grounded parity ERRORS are ignored by asserting A6-13 low which forces all multiplexer data C7, C8 to be taken from the UART. Also the DELETE code is enabled by asserting C5-6 low. The control code decoders are disabled by asserting D7-1 high. Thus all received codes are written into memory. If the optional lower case character generator D1 is present, all control codes written into memory are displayed as symbols. DELETE is displayed as a block.

N. Video Output and Drive Pulses

The dot pattern and cursor are combined in the exclusive nor gate HLD. When the cursor overlays a character, the character is dark on a white background.

The horz and vertical sync pulses are combined in the exclusive nor gate H1C. The output swings between 2.5 and 0.4 volts for sync data and 2.5 and 0.8 volts for video data. The output is pulled up and down by 150 ohm resistors providing a 75-ohm output suitable for driving coaxial cable such as RG-59U or a twisted pair. This output is available on the 22 pin edge connector for driving a TV video amplifier or a video monitor requiring a composite video input.

If a DC data display chassis is used which requires separate horz and vertical drive pulses a six pin connector is available above IC location H1. Each of the three outputs video out, vertical drive and horz drive are alternated with ground pins. Each output should be a twisted pair with one wire to ground.

Fig. 1 7 PHASE CLOCK

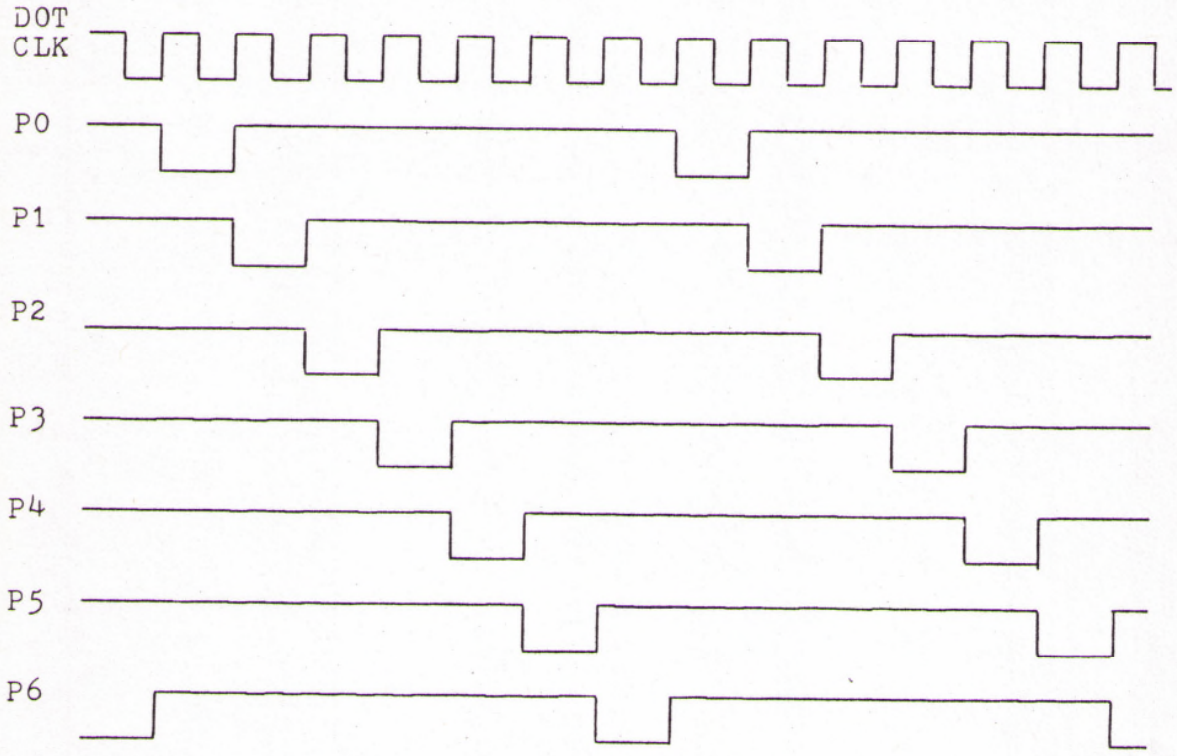


Fig. 2 SLICE COUNTER TRUTH TABLE

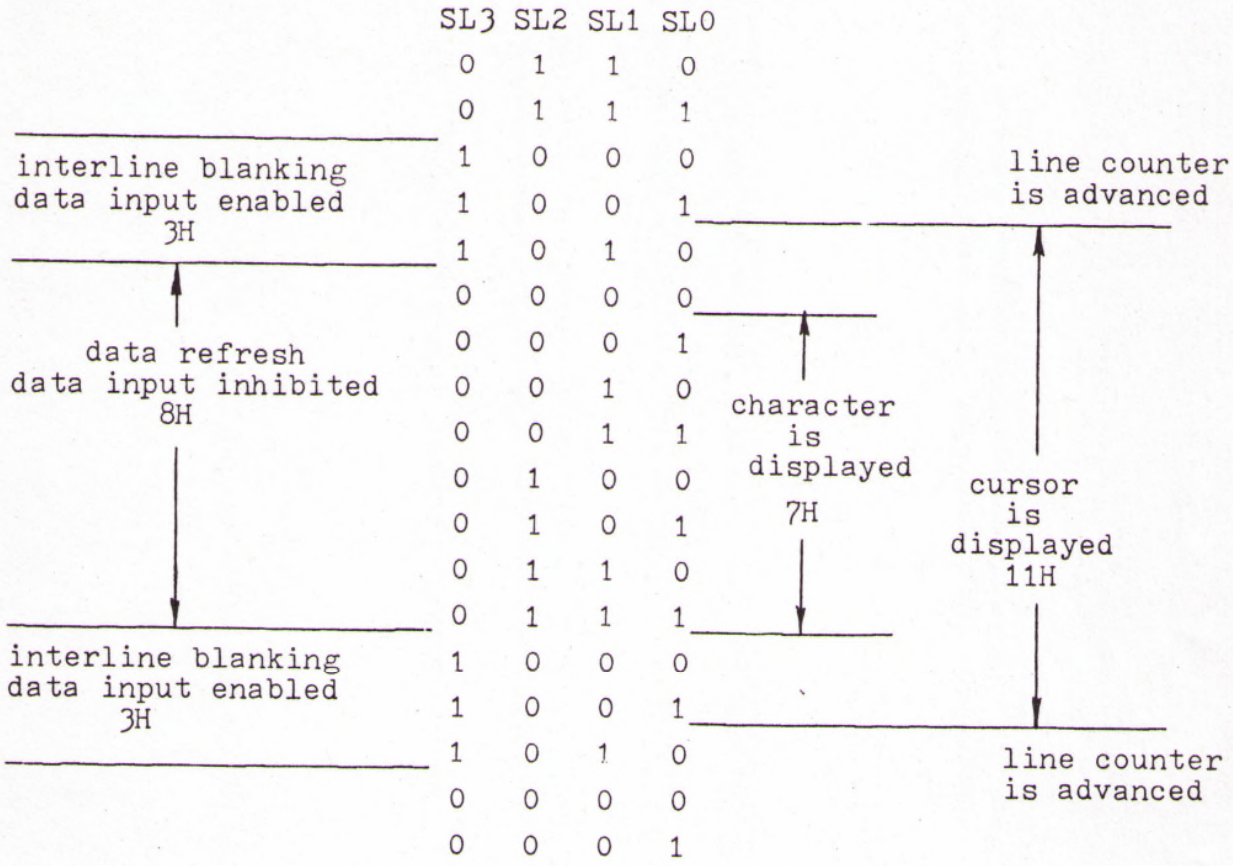
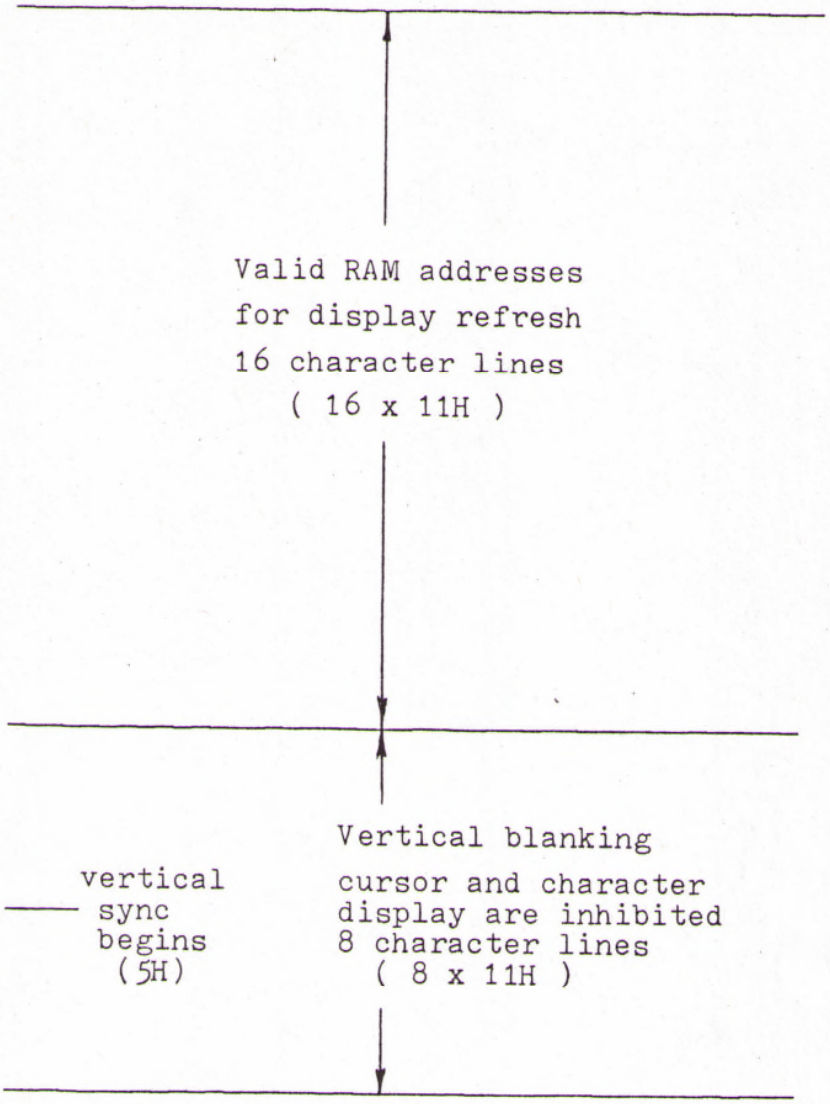


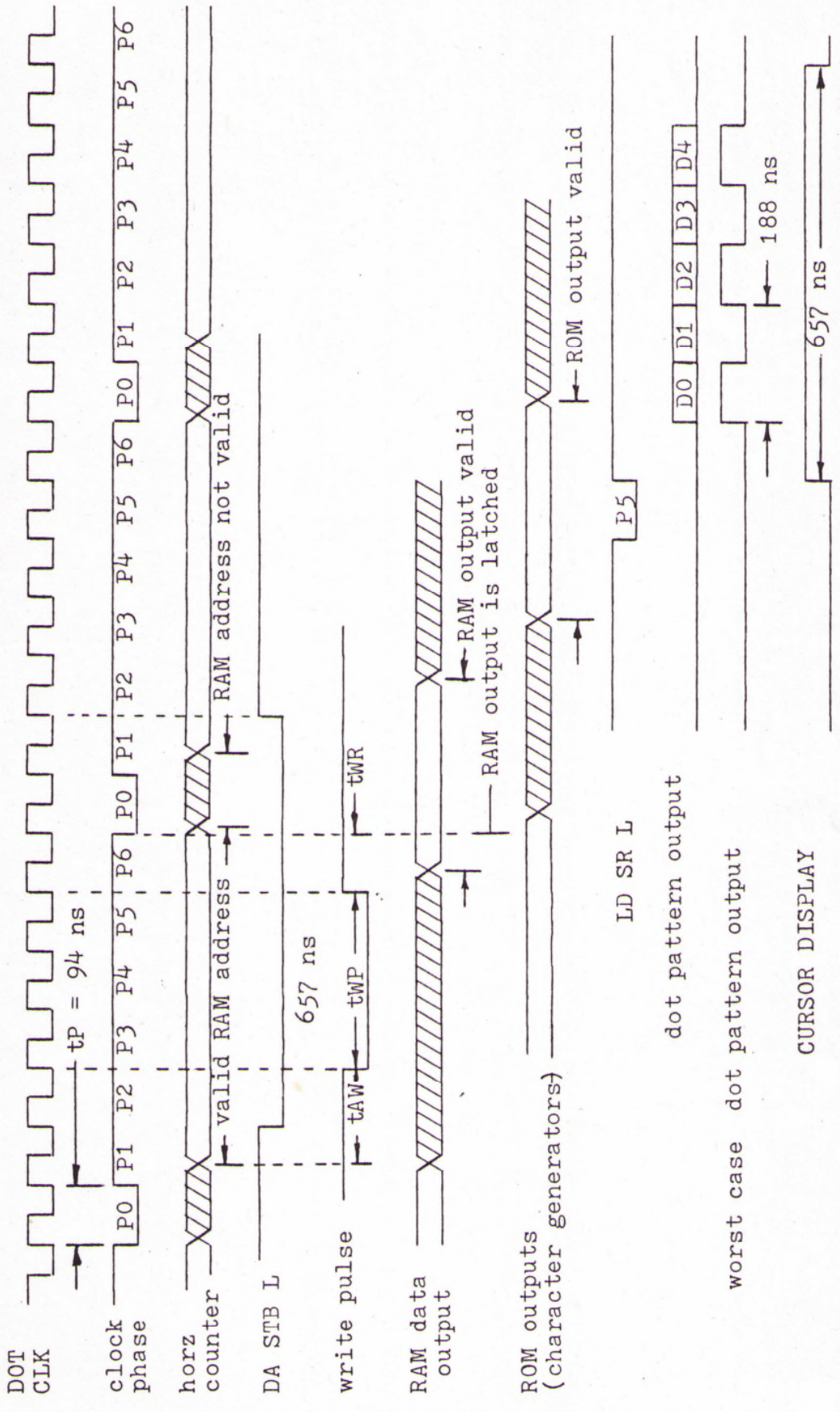
Fig. 3 VERTICAL COUNTER TRUTH TABLE

VB	LC3	LC2	LC1	LC0
0	0	0	0	0
0	0	0	0	1
0	0	0	1	0
0	0	0	1	1
0	0	1	0	0
0	0	1	0	1
0	0	1	1	0
0	0	1	1	1
0	1	0	0	0
0	1	0	0	1
0	1	0	1	0
0	1	0	1	1
0	1	1	0	0
0	1	1	0	1
0	1	1	1	0
0	1	1	1	1
1	0	0	0	0
1	0	0	0	1
1	0	0	1	0
1	0	0	1	1
1	0	1	0	0
1	0	1	0	1
1	0	1	1	0
1	0	1	1	1
0	0	0	0	0
0	0	0	0	1



one character line =
one slice counter cycle = 11H

Fig. 4 READ/WRITE AND DISPLAY TIMING



ASSEMBLY INSTRUCTIONS

APPENDIX A

Before any work is started the following steps should be completed;

1. Read the complete assembly procedure.
2. Unpack, sort and identify all components. Refer to APPENDIX B for the component list. Handle the crystal with care as it can be damaged by mechanical shock.
3. Set up your assembly area and note that the following tools are required;

    . a 25 to 40 watt soldering iron with a fine tip (1/16 1nch or smaller)
    . rosin core solder
    . side cutters
    . needlenose pliers
    . small slot screwdriver

4. Refer to assembly drawing B10090A of APPENDIX B during assembly. All components are on the numbered side of the PCB.

WARNING: Failure to use the proper soldering tool and the rosin core solder may result in permanent damage to the printed circuit card and thus void warranty and repair.

ASSEMBLY check spaces ( ) as each step is completed.

1.( )Install and solder into place all 16 pin sockets. Note that if the lower case option is not provided, IC location AB5 (shown dotted on B10090A) does not have a socket. It may be found helpful to bend diagonally opposite corner pins on the sockets after insertion to help retain them in the PCB until soldered in place. Use care when soldering to avoid forming solder bridges between pins and to adjacent traces on the PCB.

2.( )Install and solder into place all 14 pin sockets.

3.( )If the lower case option is provided install and solder the two 24 pin sockets into locations C1 and D1. If only upper case is used, solder the single 24 pin socket into location C1. The dotted socket location D1 on the drawing B10090A is not used.

4.( )INstall and solder in place the 40 pin socket in location AB7.

5.( )Install the 12 .01 mf (10n) capacitors between the +5 volt and ground tracks in the locations shown on B10090A. After inserting each capacitor, spread the leads apart slightly so that they will be retained when the PCB is turned over. Solder and clip off excess leads.

6.( )Following the procedure for step 5, install the 100pf(n10) capacitor as shown in B10090A. Solder in place.

7.( )Following the procedure for step 5, install the following resistors as indicated in B10090A. Solder into place.

R1	one	27 ohm	(red, purple, black)
R2	two	150 ohm	(brown, green, brown)
R3	two	470 ohm	(yellow, purple, brown)
R4	five	2200 ohm	(red, red, red)
R5	one	4700 ohm	(yellow, purple, red)

8.( )Following the procedure of step 5, install the two 22mf electrolytic capacitors as shown in B10090A. Be sure to observe the polarity of this part. Solder into place.

9.( )Install the SIP resistor network near location AB7 as shown in B10090A. Note the position of pin 1 and compare to the dot on the SIP. Solder into place.

10.( )Bend the leads of the 10.644 MHz crystal at right angles about 1/8" from the case and install as shown in B10090A. A piece of double sided tape or adhesive tape should be placed on the board to hold this element in place. It is important to cut the crystal leads after soldering to minimize the shock to the crystal element.

11.( )If your kit includes the power supply option it should be assembled at this point, after reviewing the power supply assembly drawing of B10090B. Note the polarity of both the 1N4001 diodes and the 680 mf capacitors before soldering these into place. The 7805 regulator and heat sink are screwwed down to the board before the regulator leads are soldered. Clip off excess leads.

12.( )Connect the seconday leads (green) of the 166L8 transformer to the two AC input terminals on the PCB is illustrated in B10090B. The primary of the transformer (black leads) should be connected to a suitably fused and switched 115 volt AC source. If you have not had previous experience with primary wiring, get help.

13.( )The power supply is now tested prior to inserting the integrated circuits. The output of the power supply measured across the power and ground tracks on the PCB should be 5 volts $\pm 5\%$. Do not insert the ICs if the voltage exceeds 5.25 volts. If there is no voltage unplug the unit and check for solder bridge between the +5 volt and ground traces.

14.( )Referring to drawing B10090A insert the integrated circuits into the sockets. Note the position of pin 1 on the IC and the corresponding dot indicating pin 1 on the drawing.

Use care to prevent bending of pins when installing the ICs. Be especially careful to avoid having a pin bend underneath the body of the IC rather than enter the socket as this will cause faults that are very difficult to trace.

15.( )Check the orientation of the ICs and that the ICs are in their proper locations before powering the unit up.

The assembly of your TH6416 is now complete. Refer to APPENDIX C for control and data I/O.

COMPONENT LIST

ITEM	QTY	LOCATION	MNF'R
74LSOO	2	A6 E6	all
7404	1	H4	all
74LSO4	1	F1	all
74LSO8	3	A5 E3 E7	all
74LS30	2	C5 H6	all
74LS32	2	B5 F2	all
74LS42	1	C6	all
74LS74	7	B6 F3 F4 F7 H2 H3 H7	all
74LS83	1	D5	all
7490	1	H8	all
7493	6	C3 C4 E2 E4 E8 F8	all
74LS139	1	D7	all
74LS151	1	D8	all
74LS157	3	C7 C8 E5	all
74164	1	H5	all
74165	1	E1	all
74LS175	2	A1 B1	all
74LS193	4	D2 D3 D6 F6	all
74LS266	3	C2 D4 F5	all
8242	1	H1	Sig, Ray
2102-1 or 2102A-4	7*	ABO - AB6	all
RO-3-2513 CGR-001	1	C1	GI
RO-3-2513 CGR-002	1*	D1	GI
AY-3-1015	1	AB7	GI

* includes lower case option

all - Fairchild, National, Raytheon (Ray), Signetics (Sig), Motorola, Texas Instruments

GI - General Instruments

SOCKETS and CONNECTOR

ITEM	QTY	DESCRIPTION
S1	30	14 pin IC socket
S2	21*	16 pin
S3	2*	24 pin
S4	1	40 pin
CONN 1	1	22/44 (0.156 inch spacing) PCB edge connector

DISCRETE COMPONENTS

ITEM	QTY	DESCRIPTION
C1	12	.01 mf, 40 Volt capacitor
C2	1	100 pf, 40 Volt capacitor
C3	2	22 mf, 25 Volt capacitor
R1	1	27 ohms, 0.25 Watt resistor
R2	2	150 "
R3	4	470 "
R4	3	2.2K
R5	1	4.7K
R6	1	4.7K or 10K SIP resistor array
X1	1	10.644 MHz crystal, type HC-18U

LOWER CASE OPTION

ITEM	QTY	DESCRIPTION
S2	1	16 pin IC socket
S3	1	24 pin IC socket
*2102-1 or 2102A-4	1	1024 x 1 bit RAM
RO-3-2513 CGR-0002	1	Lower Case Generator

These components are provided only with the TH6416L or the TH6416LP, NOT with the TH6416 or TH6416P.

POWER SUPPLY OPTION

ITEM	QTY	DESCRIPTION	MNF'R
MC7805	1	+5 Volt regulator	Motorola
IN4001	4	1 Amp, 50 PIV diode	GI
C10025A	1	Heat Sink	custom
C4	5	680 mf, 16 Volt capacitor	Philips
166L8	1	2.0 Amp transformer	Hammond

These components are provided only with the TH6416P or the TH6416LP, NOT with the TH6416 or the TH6416L.

* Note: 2102-1 and 2102A-4 are not compatible and should not be mixed. Either use all 2102-1 or all 2102A-4.

VIDEO CHASIS RS-232 COND

22/44 PIN SOLDER TAIL PCB EDGE CONNECTOR

	PIN	SIGNAL	DESCRIPTION
	1	VID. GND	video ground
	2	-------	unused
	3	DATO	serial data output
	4	DATI	serial data input
	5	--------	unused
1	6	TBE	transmitter buffer empty
2	7	KIS	keyboard input stobe
3	8	KI0	parallel keyb. input (least sig.)
4	9	KI1	parallel keyb. input
5	10	KI2	parallel keyb. input
6	11	KI3	parallel keyb. input
7	12	KI4	parallel keyb. input
8	13	KI5	parallel keyb. input
9	14	KI6	parallel keyb. input
10	15	KI7	not normally used (see doc.)
	16	PARITY ENB.	switch input (parity enb/ground)
	17	TSB	switch (two stop bits-open one stop bit -ground)
	18	EVEN/ODD	switch (even parity - open odd parity - ground)
	19	-------	unused
	20	--------	unused
	21	+5 VOLTS	input (output with option supply)
12+13	22	GROUND	input (output with option supply)
	A	-------	unused
	B	VID OUT	composite video output
	C	-------	unused
	D	-------	unused
	E	-------	unused
	F	-------	unused
	H	-------	unused
	J	-------	unused
	K	-------	unused
	L	-------	unused
	M	-------	unused
	N	-------	unused
	P	-------	unused
	R	BREAK	normally keyboard input, uncoded switch closure to ground
	S	HERE IS (DISPLAY CNTL CHAR)	normally keyboard input, uncoded switch closure to ground
	T	FULL/HALF DUPLEX	line control for serial output data paths
	U	RATE 2	baud rate select (most sig.)
	V	RATE 1	baud rate select
	W	RATE 0	baud rate select (least sig.)
	X	CURSOR ON/OFF	cursor display(open-on, ground-off)
	Y	+5 VOLTS	input (output with option supply)
	Z	GROUND	input (output with option sipply)

NOTES:

1. All switch inputs are SPST (not supplied) and operate normally open (resistive pullups on board) or closed to ground. One side of the switches (ground) should be connected to pins 22 and/or Z.

2. Keyboard parallel inputs must be ASCII encoded. KIS must be a clean low going strobe with a high level between 3.0 volts and 5.0 volts. The maximum low value (strobe active) must be between 0.0 and 0.5 volts. Keyboard input data must be valid 40 nanoseconds minimum before and after the strobe pulse occurs to ensure data is properly loaded into the UART.

3. Without the optional power supply, +5 volt inputs are on pins 21 and/or Y; ground pins are on pins 22 and/or Z. With the on-card power supply, these pins can be used as outputs to power an external keyboard or interface. Maximum current drain for external devices is 0.3 Amps. The heat sink runs about 45 degrees Celcius (hot). If intended to be placed in a restricted enclosure forced air cooling is required or the regulator should be mounted to the enclosure for heat sinking.

4. For connection to a TV video amplifier or a standard video monitor with internal sync separator, a twisted pair can be used with one lead connected to VID. OUT (pin B) and the other to VID.GND (pin 1). Coaxial cable can also be used with the shiel connected to pin 1. This unit can drive approximately 1000 ft. of coaxial cable. If twisted pair is used the lead length should be as short as possible to minimize radiated interference.

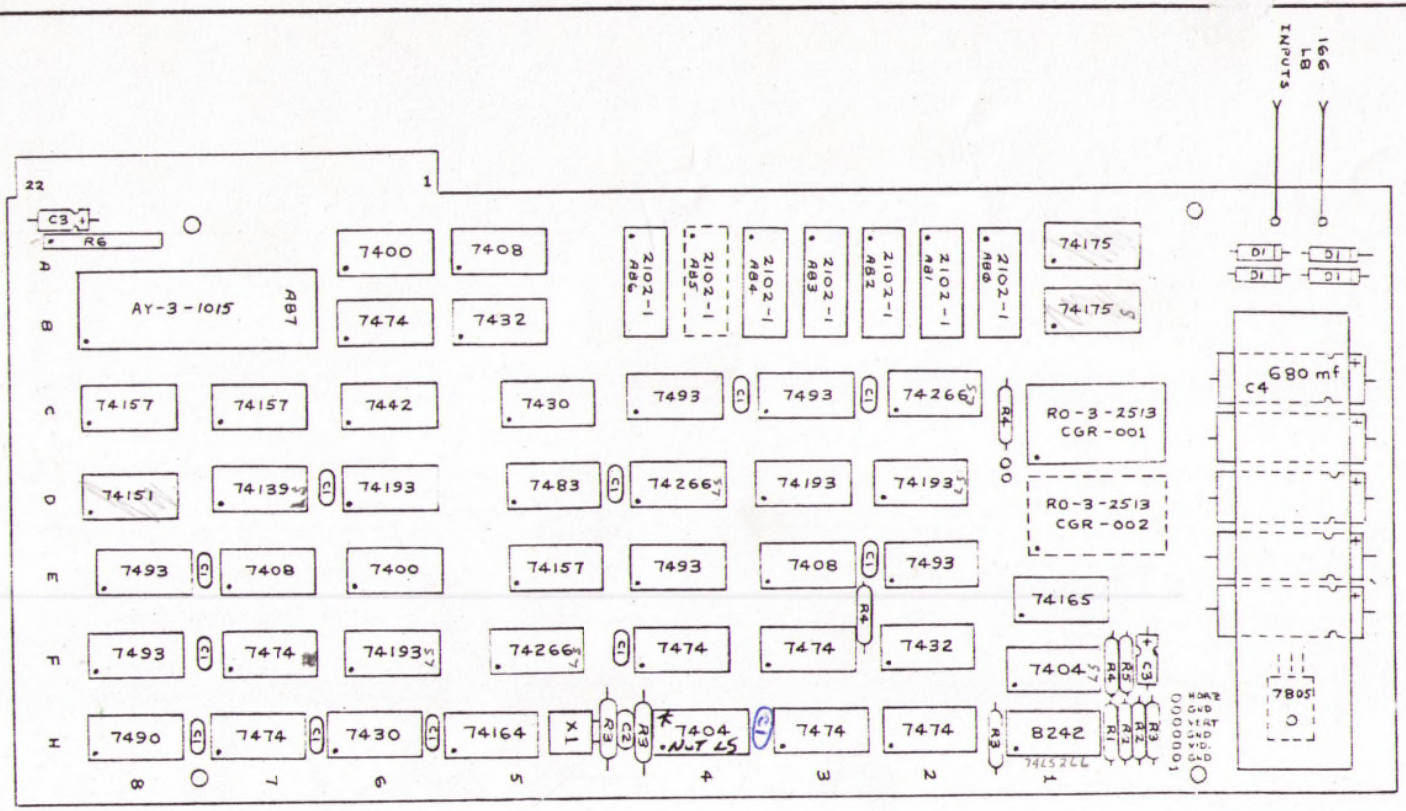
   For direct drive data display monitors, a six pin output is provided above location H1. Numbered from the edge of the card these outputs are;

   1 ground
   2 video out
   3 ground
   4 vertica; drive
   5 ground
   6 horz drive

   Three twisted pairs are required, one lead of each pair is connected to the adjacent ground pin.

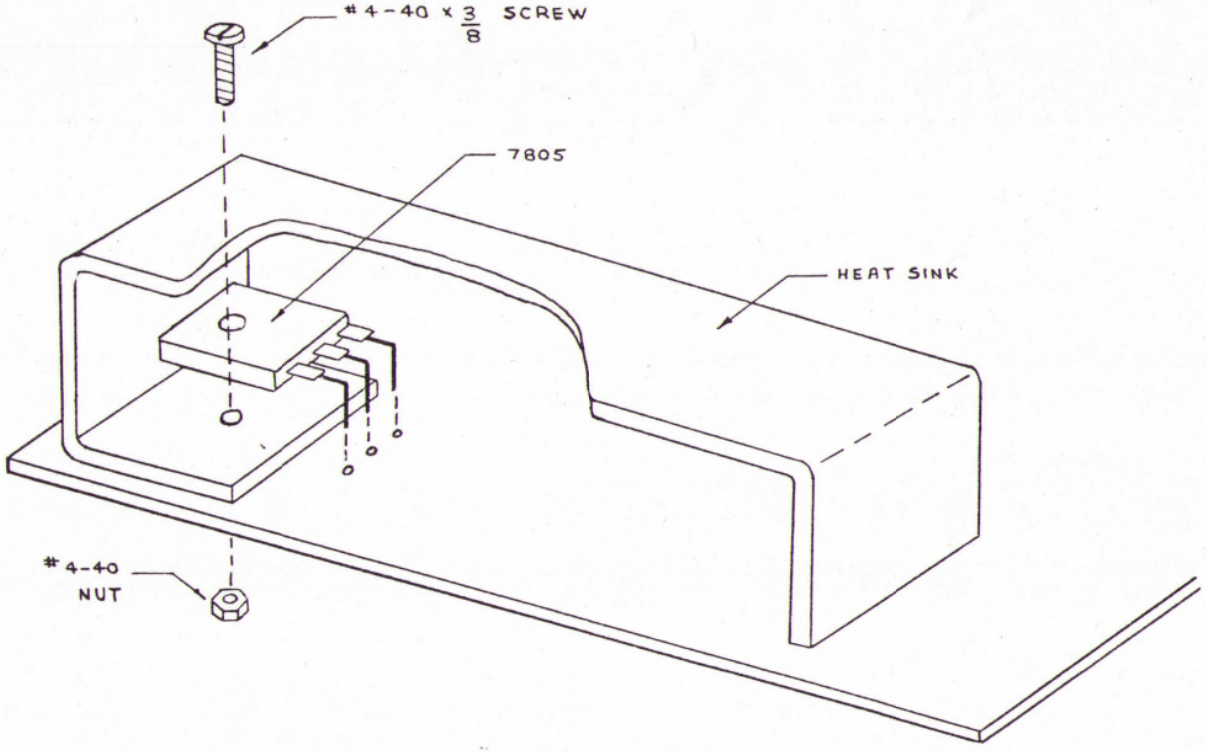
5. For upper case only, a wire link must be soldered into the jumper position below the IC location C1. For both upper and lower case operation (character generator D1 and RAM AB5 are present) this link is left out. The board is shipped with the link out.

6. For the Hammond 166L8 power transformer (available with the power supply option), the BLACK wires are the primary (115 volts) and the secondary is the GREEN wires (8.5 volts). The GREEN wires are connected to the two holes provided near the diode bridge.

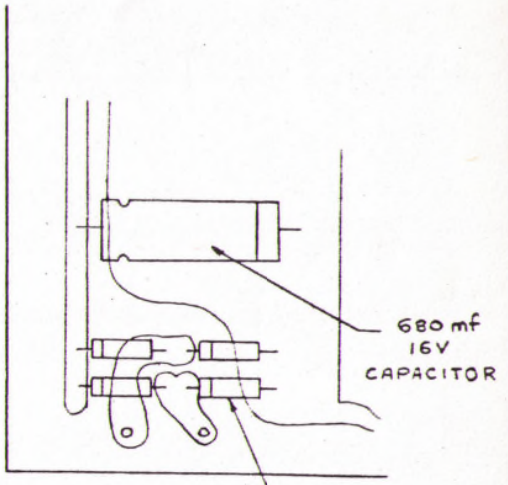


Cybernex ltd. ottawa — canada				
TITLE TH6416				REV A
		DATE	PROJ	
DR	gs.	19/10/77	DWG	B10090A
CK				
ENG			REF	

TRANSTEX 15 100-8-79



MOUNTING DETAIL - 7805 & HEAT SINK

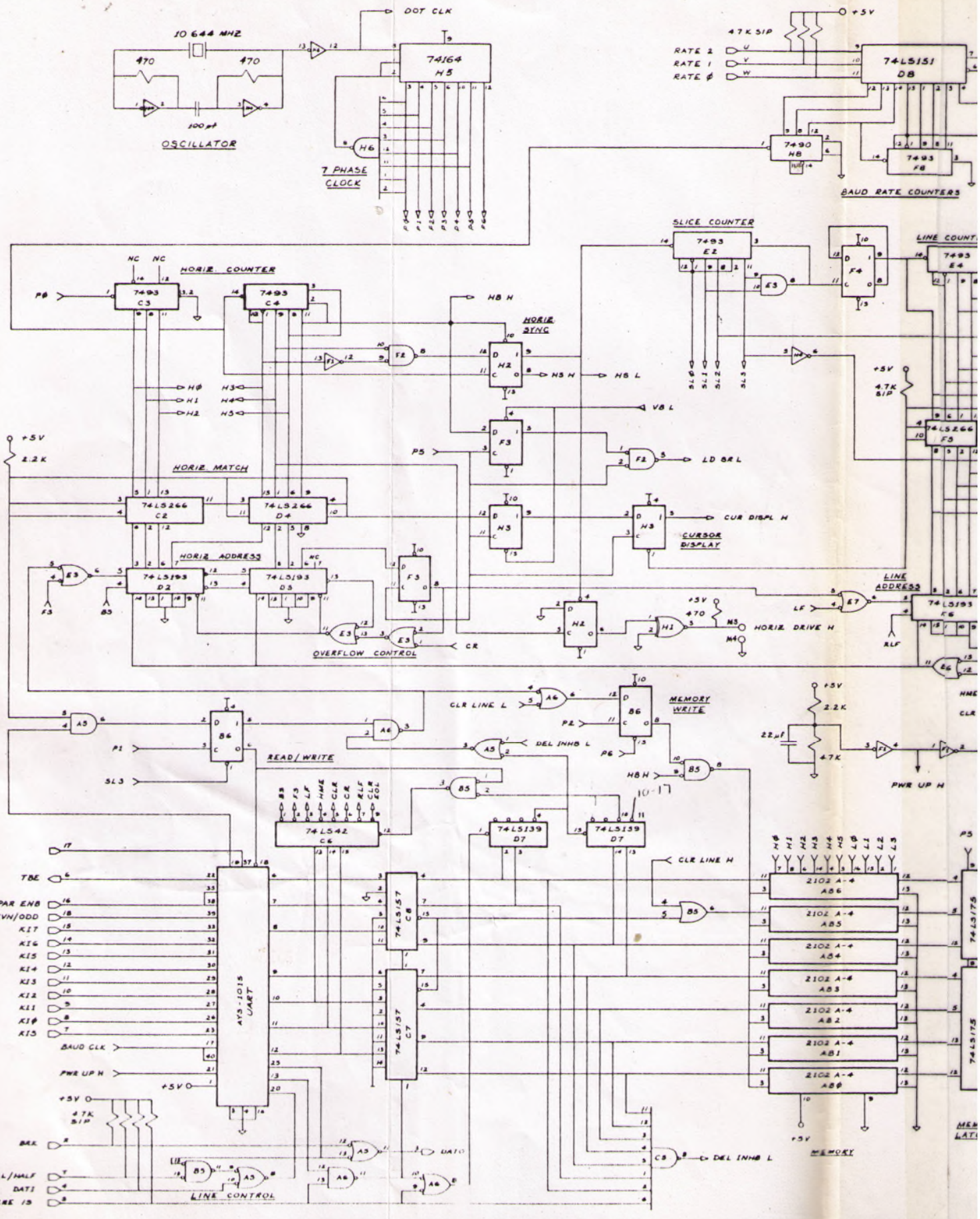


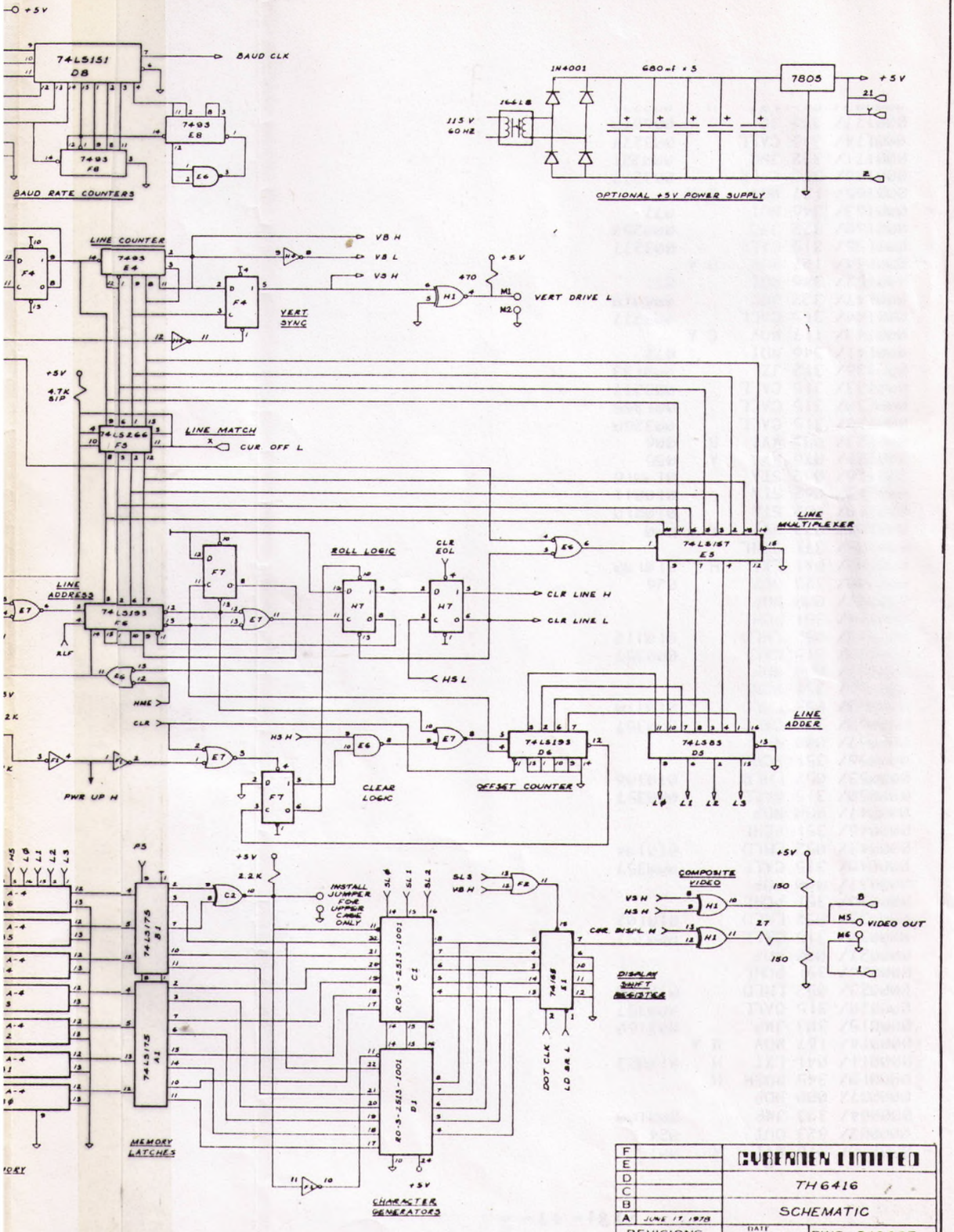
NOTE POSITION OF
CATHODE BAND

Cybernex ltd.
ottawa — canada

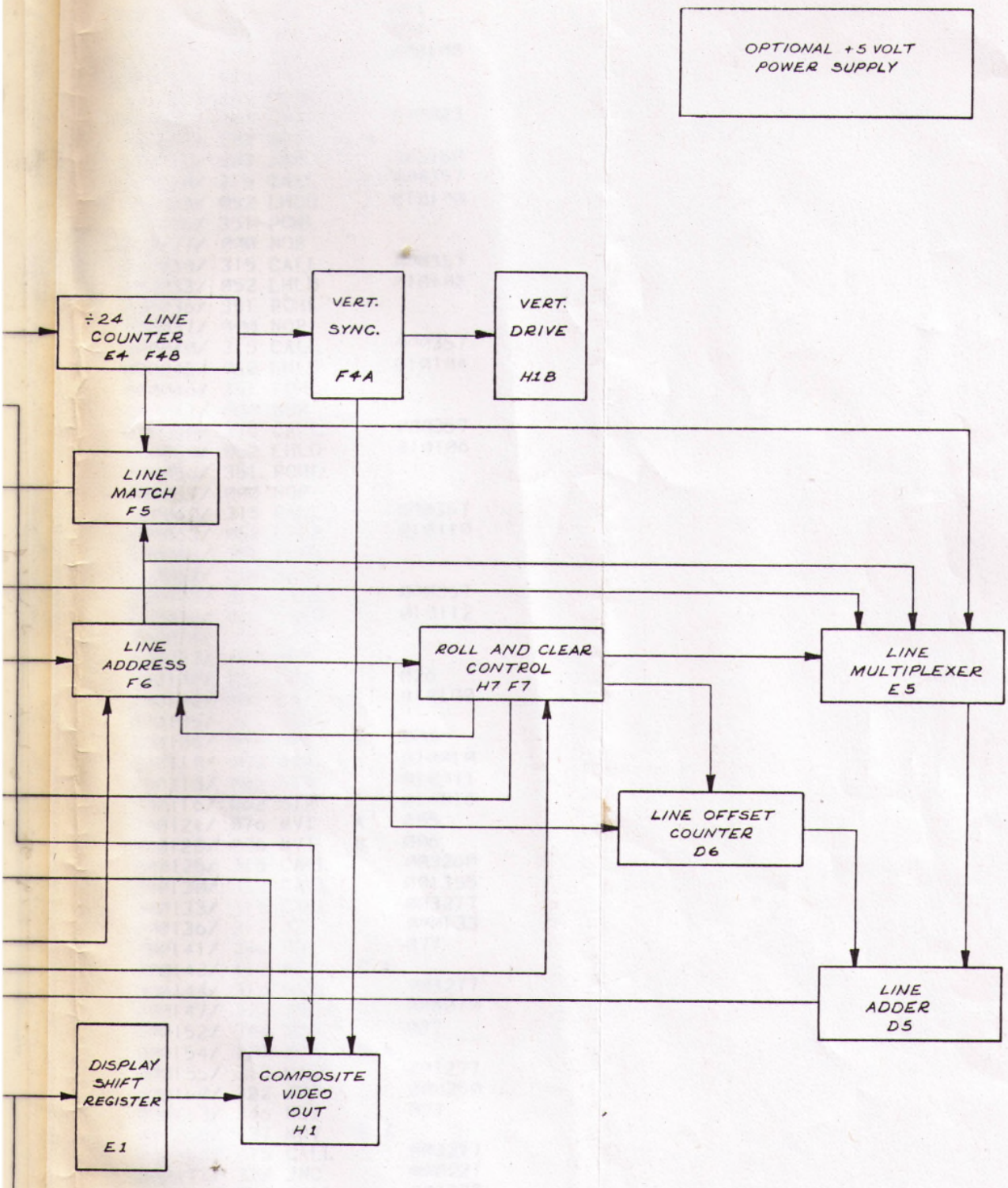
TITLE	TH6416	REV
		A

		DATE	PROJ	
DR	JS.	19/10/77	DWG	B10090B
CK				
ENG			REF	

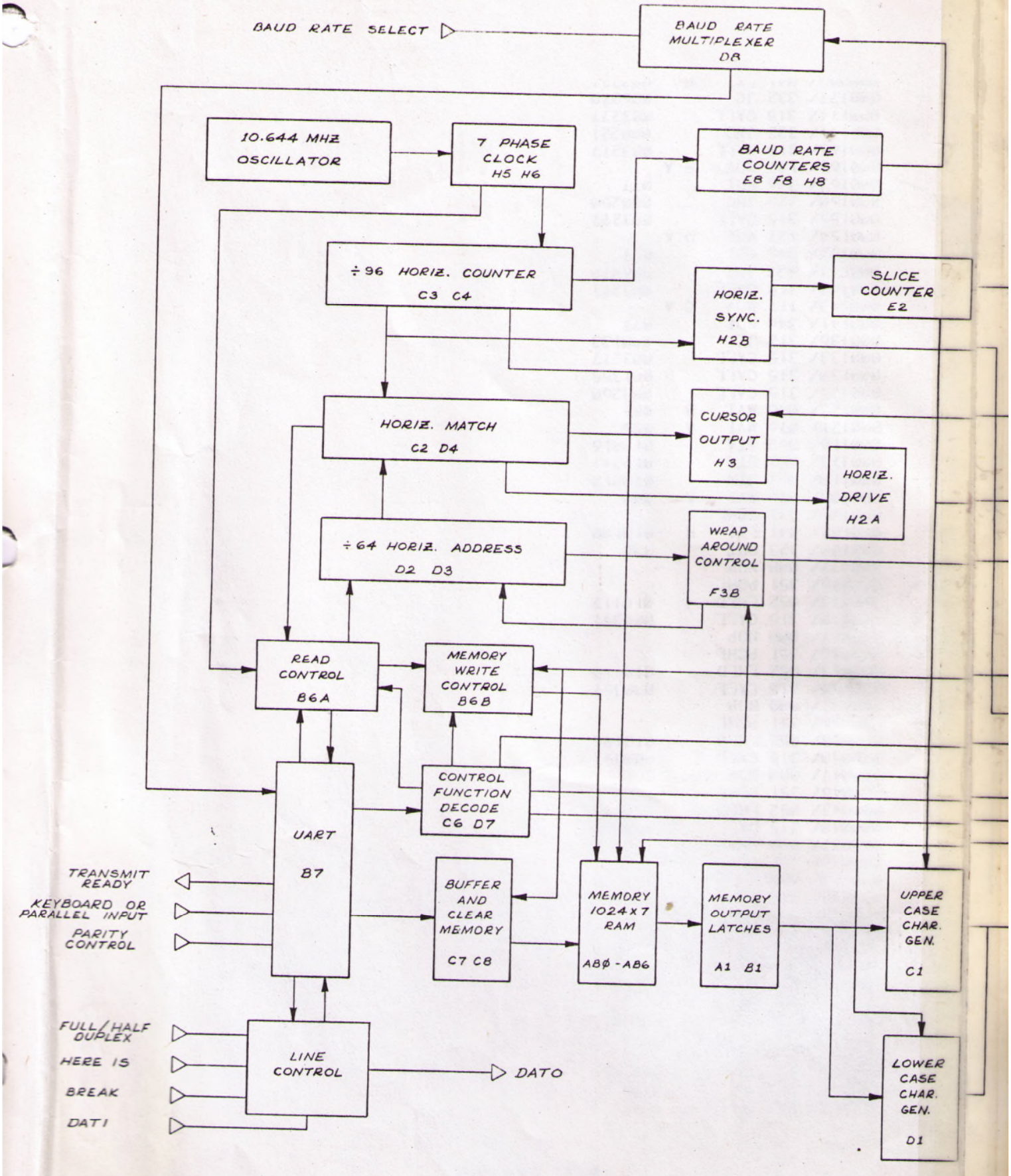

10.644 MHZ
470
470
100 pf
OSCILLATOR
DOT CLK
74164
H5
H6
7 PHASE CLOCK
+5V
4.7K SIP
RATE 2
RATE 1
RATE Ø
74LS151
D8
7490
H8
7493
F8
BAUD RATE COUNTERS
SLICE COUNTER
7493
E2
7493
E4
LINE COUNT
F4
E3
HORIZ. COUNTER
7493
C3
7493
C4
NC NC
PB
HØ
H1
H2
H3
H4
H5
H8 H
HORIZ SYNC
H3 H
H5 L
V8 L
P5
F2
LD SR L
CUR DISPL H
CURSOR DISPLAY
F3
H2
H3
+5V
2.2K
HORIZ. MATCH
74LS266
C2
74LS266
D4
HORIZ ADDRESS
74LS193
D2
74LS193
D3
E3
F3
B3
OVERFLOW CONTROL
CR
H1
470
M3
M4
HORIZ DRIVE H
LINE ADDRESS
74LS193
F6
LF
RLF
E7
E6
+5V
4.7K SIP
74LS266
F3
CLR LINE L
A6
B6
MEMORY WRITE
P2
P6
DEL INHB L
A5
B5
H8 H
+5V
2.2K
22 µf
4.7K
PWR UP H
P1
SL3
READ/WRITE
B3
F3
LF
HME
CLR
CR
RLF
COL
74LS42
C6
74LS139
D7
74LS139
D7
CLR LINE H
74LS157
C8
74LS157
C7
AY3-1015
UART
TBE
PAR ENB
EVN/ODD
KI7
KI6
KI5
KI4
KI3
KI2
KI1
KIØ
KI8
BAUD CLK
PWR UP H
+5V
4.7K SIP
BRK
FULL/HALF
DATI
HERE IS
LINE CONTROL
DATO
DEL INHB L
2102 A-4
A86
2102 A-4
A85
2102 A-4
A84
2102 A-4
A83
2102 A-4
A82
2102 A-4
A81
2102 A-4
A8Ø
+5V
MEMORY
74LS175
74LS175
P5
10-17



F		CYBERNEX LIMITED	
E			
D			
C		TH6416	
B			
A	JUNE 17, 1978	SCHEMATIC	
REVISIONS		DATE OCT. 17, 1977	DWG D10087



TH 6416	
BLOCK DIAGRAM	
OCT. 17, 1977	D 10088


BAUD RATE SELECT
BAUD RATE MULTIPLEXER D8
10.644 MHZ OSCILLATOR
7 PHASE CLOCK H5 H6
BAUD RATE COUNTERS E8 F8 H8
÷96 HORIZ. COUNTER C3 C4
HORIZ. SYNC. H2B
SLICE COUNTER E2
HORIZ. MATCH C2 D4
CURSOR OUTPUT H3
HORIZ. DRIVE H2A
÷64 HORIZ. ADDRESS D2 D3
WRAP AROUND CONTROL F3B
READ CONTROL B6A
MEMORY WRITE CONTROL B6B
CONTROL FUNCTION DECODE C6 D7
UART B7
BUFFER AND CLEAR MEMORY C7 C8
MEMORY 1024 x 7 RAM AB0 - AB6
MEMORY OUTPUT LATCHES A1 B1
UPPER CASE CHAR. GEN. C1
LOWER CASE CHAR. GEN. D1
TRANSMIT READY
KEYBOARD OR PARALLEL INPUT
PARITY CONTROL
FULL/HALF DUPLEX
HERE IS
BREAK
DATI
LINE CONTROL
DATO