THE MOD 8 DATA PACKAGE

The MOD 8 data package includes the following:

1. MOD 8-8 PROM Programmer documentation including parts list and component placement.

2. The audio cassette/MOD 8 interface documentation.

3. Notes on the MOD 8 system including errors in the original MIL manual parts list for the MOD 8.

4. The MOD 8 self test program.

5. Expanding INPUT OUTPUT port capability.

Although I have made every effort to keep the information contained herein free from errors NO responsibility is assumed for inaccuracies. Further, NO responsibility is assumed for the use of any circuitry described herein and NO patent licenses are implied.

Robert Swartz
195 Ivy Lane
Highland Park, Il. 60035

MOD 8-8

BACKPLANE/PROM PROGRAMMER

1.0 INTRODUCTION

The MOD 8-8 printed circuit board was designed to interconnect a full set of MOD 8 boards into a development microcomputer configuration with PROM programming capability. With the inclusion of the seven PROM MONITOR 8 software, power supplies and a teletype, the system becomes an interactive tool for use in all phases of program development for MOD 8 and/or MF8008 oriented applications.

The following features highlight this product application:

1) Lends familiarity with the use and operation of the MOD 8 family of Super Components.
2) Interactively recognizes and interprets MF8008 assembly language mnemonics.
3) Loads and dumps in symbolic, octal or BNPF formats.
4) Executes programs, with or without trapping (breakpoint).
5) Edits in octal representation any portion of R/W (RAM) memory.
6) Allows real-time execution, I/O interconnects, and probing of signal lines.
7) Copies, lists, and programs MF1702/1702A type PROM's.

2.0 PHYSICAL DESCRIPTION

The MOD 8-8 supercomponent is made up of a double sided printed circuit board mounted on a 13.5 x 5.0 x 2.0 inch aluminum chassis. The chassis serves only as a holding medium for the PC card to make up a desk-top prototyping unit. The unit is intended to be powered from external bench supplies through the Molex connector provided. Also provided is an Amphenol communication connector mating with the appropriate receptacle on the card. This serves to connect the teletype to the system.

Power requirements depend on the number of MOD 8 cards included in the system with maximum limits as shown in Fig. 2.

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The six 8 bit input/output channels are brought out to wire wrap pin headers mounted on dual 0.100" centers; this permits cabling of I/O signals using standard ribbon cable connectors.

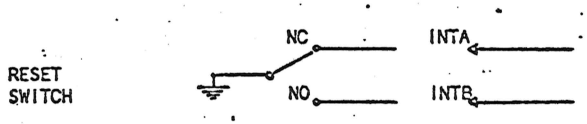
3.0 FUNCTIONAL DESCRIPTION

Over one-half of the 13.5 by 5.0 inch board is taken up by interconnect, nine P.C. edge connectors, a power receptacle, a TTY receptacle, a push button switch, and a set of I/O cable receptacles. The remaining surface is occupied by the PROM programmer hardware, including the 24 pin zero insertion-force socket.

3.1 BACKPLANE SECTION

The nine PC edge connectors and various receptacles are inter-connected as shown in Fig.'s 1 and 2. Four memory slots are allotted for MOD 8-4 and MOD 8-5 boards. Two slots are provided to accept either MOD 8-6, MOD 8-7 or compatible user-designed I/O boards. The remaining three board slots are specifically assigned to MOD 8-1, MOD 8-2, and MOD 8-3 boards. (See Fig. 3)

Some signals are shown in Fig. 1 as on-board interconnections with the PROM programmer and as such will be discussed in the section pertaining to that function. Also shown in a similar fashion are the two signal lines INTA and INTB; these are connected to an SPDT momentary push button switch as shown below.



The following are explanatory notes with reference to Fig. 1:

- The MOD 8-2 TTY-RST edge-connector is pinned-out in a similar fashion to an I/O socket with the six TTY lines and the two RESET SW lines as in-out data. Two extra control lines, TTY INT and $\overline{\text{IBS}}$, link this board with the CPU board and serve as interrupt request and acknowledge.

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- The MOD 8-1 and MOD 8-3 edge connectors are interconnected to form the bus-oriented processing element. The signal lines BSE, IAL, and RAL are also wired commonly and extended into the memory field. The READY signal line is brought out of the CPU socket and connected to all four memory sockets; in a similar fashion, four yet-unassigned tracks also link the CPU socket and the memory field. The above eight lines are not active in the present design of the MOD 8 system and are included in the backplane for future expansion. The user may want to use these in the design of custom memory cards or such.

- The RAL line is jumpered to ground externally in all deliverable MOD 8-8 backplanes; this is necessary for the proper normal functioning of the MOD 8-3 buffer board.

- An extra power track is brought from Pin 5 of the power receptacle to Pin M of the CPU board socket, again for future use of third-generation microprocessors.

- The present design of MOD 8-4 and MOD 8-5 cards only make use of the Bi-Directional data bus, the 14-bit address bus, the two signal lines MRE and $\overline{\text{WRITE}}$, and power. Future MIL super-components or user designed memory boards may use the other interconnects.

- Both I/O card sockets are identical; the lettering on the backplane (Fig. 3) assigns one slot to MOD 8-6 and one to MOD 8-7 only for correspondence in the connector assignment map. All six cable headers have the same bit pin-out assignment as shown by the lettering.

Figure 3 shows a top view of the MOD 8-8 board with card slot assignment and receptable identification.

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3.2 PROM PROGRAMMER SECTION

The PROM Programmer included on the MOD 8-8 board is designed as a peripheral I/O device to the microcomputer and as such includes an address decoder and tri-state data bus buffers. Under software control it is capable of programming both the standard MF1602/1702 and the faster MF1602A/1702A PROM devices. An external 75 volt supply is required. This supply should be capable of .75 amps at 20% duty cycle and need not be regulated. A typical design is shown in Fig. 7; the 1/2 amp 50 volt (AC) transformer is sufficient if a large capacitance is included after the full-wave bridge.

The PROM programming hardware can be functionally broken down into the following:

1) Timing generator
2) Voltage switch/regulator
3) I/O address decoder
4) Data latch/driver/buffer
5) Address latch/driver

The schematic of the first three is given in Fig. 4 and the last two in Fig. 5. The voltage waveforms and timing diagram are given in Fig. 6.

IC 12 in conjunction with IC13b and IC13c forms two independent gated multivibrators with cycle times of 150msec and 15msec respectively. IC 7 acts as a two bit output port, latching DB1 and DB2 during the execution of an OUT 013 instruction. If either bit is set the corresponding multivibrator will be enabled. IC15a, when triggered by either of the oscillators generates a 3.25 usec program voltage enable pulse (PVE). The leading edge of the PVE signal triggers a 60 usec address complemented $\overline{\text{ADCMP}}$ signal via IC14a. IC14b delays the PVE signal by 155 usec before triggering IC15b which gives a 3.0 usec program voltage pulse (PVP).

During a program cycle (PVE=logic 1) T_1 and T_2 are turned off by the $\overline{\text{PVE}}$ signal letting V_{CDS} be pulled to 0.7 volts through D_1. IC16b, T_3 and T_4 buffer the $\overline{\text{PVE}}$ signal which in turn enables the pass transistor T_5 during the program cycle. T_6 acts as a current regulator by shunting T_5 base drive during excessive loading. The MC7805 forms a floating regulator adjusted to give CS_S of +48 volts.

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V_{BBS} is normally held at +5 volts by diode D4 and is clamped at 60 volts during programming by diodes D2 and D3. The program pulse is normally held at +5 by IC16e and diode D6. During the program cycle the pass transistor T_7 is normally conducting, pulling PRG_S to +48 volts. When IC15b generates the PVP signal T_8 is turned on, removing T_7 base drive and PRG_S is pulled to ground through the 10K resistor.

Diodes D7 and D8 allow V_{CCS} to swing from +5 during reading, to +48 during programming. V_{GGS} is pulled from -9.0 during reading to +12 volts during programming by diode D_5. A light-emitting diode is tied to CS_S to serve as programming indicator.

The I/O port strobe signals are generated by IC6 using the MOD 8 $\overline{INP}$ and $\overline{OUT}$ pulses and desired addresses as decoded by IC4.

IC2 is an 8 bit address latch addressed as OUTPUT PORT 010 by the MOD 8 system. During the first 60 usec of the programming cycle $\overline{ADCMP}$ causes IC10 and 11 to complement the address before buffering by T9 through T16. IC1, addressed as OUTPUT PORT 011, forms an 8 bit data latch. During the program cycle the $\overline{PVE}$ line allows transferring this data via IC8 and IC9 to the data drivers T17 through T24. Note that the data to be programmed is complemented by the MONITOR 8 software. During a read cycle the $\overline{PVE}$ line is held at 1, inhibiting all the data buffers. IC3 and IC5 form an input port, address an INPUT PORT 001, sensing the ROM data through diodes D_{11} to D_{18} and feeding the data back to the MOD 8 data bus.

The standard MONITOR 8 software includes a programming routine which will allow programming of standard devices in 2-3 minutes and MF1602A/1702A devices in approximately 1 minute. The routine checks the ROM data byte following each programming pulse. When the data becomes valid, after "n" program pulses, the routine proceeds to cycle the programmer for 4Xn more pulses.

To accomodate 1602A/1702A devices it is necessary to change the programming duty cycle from 2% to 20%. After receiving the initial and final address to be programmed the programming routine will respond with CR/LF "%". The user must then type an "A" or "L" to determine the timing loop. Typing A will give a

program pulse cycle of 20% for 1702A types and an "L" gives approximately 2% duty cycle for normal devices. Under no condition should standard devices be programmed with excessive duty cycles.

It should be noted that attempting to program a standard device using 1602A/1702A timing (20% duty cycle) will destroy the device. Note also that the unprogrammed state for an A series device is all zeros whereas for standard devices it is all ones.

The MONITOR 8 software sees the PROM programming station as an extended memory location, and thus the DUMP OCTAL, DUMP SYMBOLIC, DUMP ENPF and COPY routines will access data from that socket when addresses in the range 200000 through 200377 are specified.

4.0 SET UP PROCEDURES

The MOD 8-8, and in turn all MOD 8 boards are supplied with power through the MOLEX 1612R connector provided. Pin-out assignment is as given in Fig. 2. Care should be taken to assure correct polarity and placement.

The Microcomputer and MONITOR 8 software have been developed to interface with a model ASR-33 teletype set up for full duplex 20 mA current loop serial transmit/receive and incorporating a relay in the tape reader drive circuit. The following procedure can be used to verify that the teletype is in a compatible mode.

1. Disconnect mains line cord.
2. Remove cover.
3. Referring to Fig. 3, locate current source resistor. Verify that BLUE wire is on the 1450 OHM tap; change if necessary.
4. Locate terminal strip at rear; remove protective strip.
5. Verify that the VIOLET wire is on terminal screw #9; if it is on #8, change accordingly.
6. Verify that both the WHT/BLU and BRN/YEL wire are on terminal screw #5. One could be on #4 and the other on #3; if so, change accordingly.
7. Check if a reader relay is incorporated; most teletype supplied through minicomputer manufacturers will include the modification. If a reader relay is not included, one must be built and included; refer to Fig. 9 for recommended design and installation.

Once the teletype has been found to conform to requirements, there remains to make up the interconnection to the MOD 8 microcomputer.

This consists of a six wire cable terminated with the Amphenol connector supplied (#57-40140). Any external signal wire already existing must be removed or isolated through a six pole switch. The cable is connected as shown in Fig. 2.

After both the power and TTY cables have been assembled, the MOD 8-8 backplane can be populated with MOD 8 boards as per assignment (Fig. 3), taking care to insert these with their component side away from programmer.

With proper power applied and correct teletype hook up, the RESET switch should cause the MONITOR 8 software to respond with eight dashes on the teletype. All further interactions are as specified in the MF8008 applications manual.

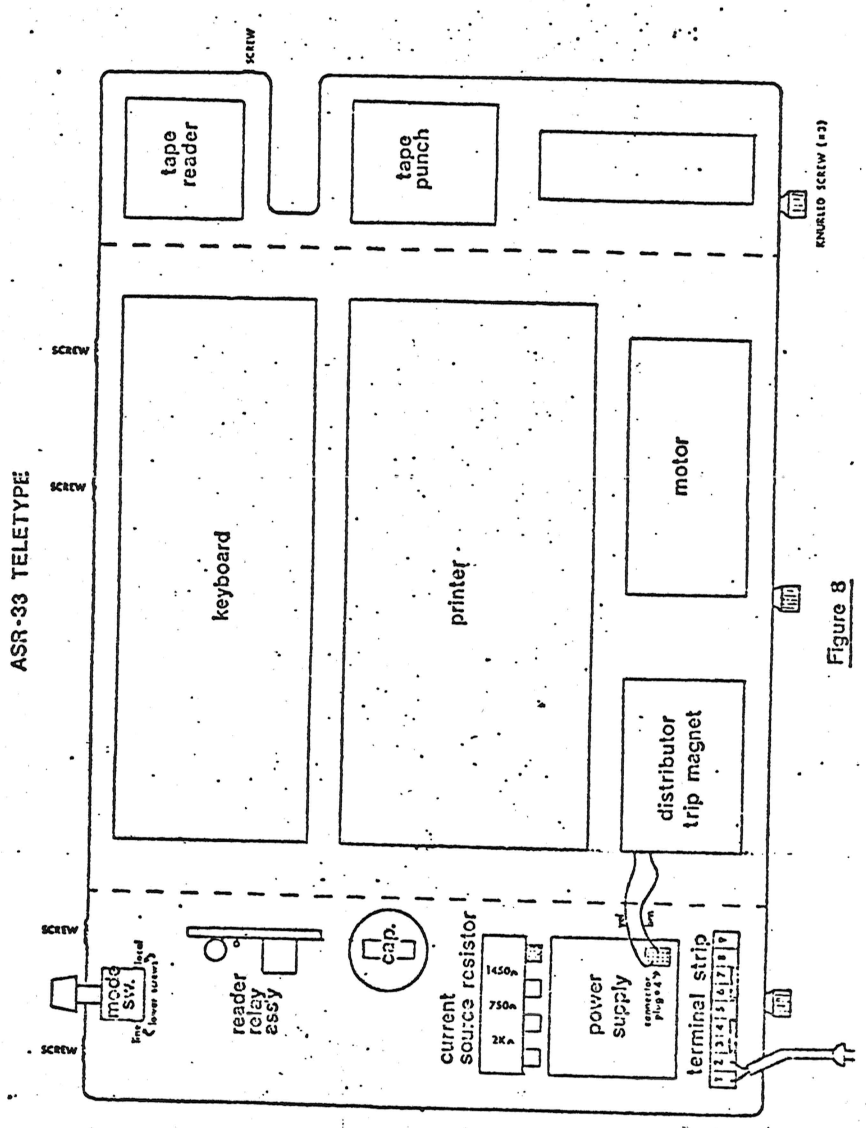
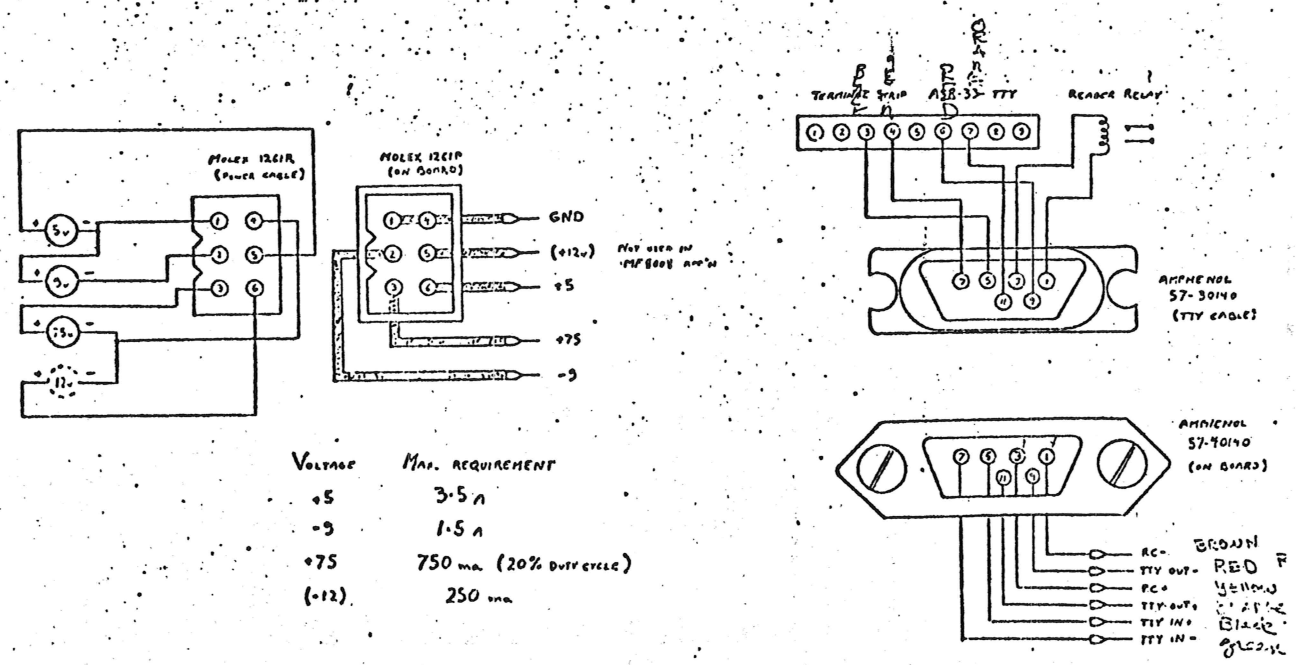


Figure 8



Voltage	Max. requirement
+5	3·5 A
-9	1·5 A
+75	750 ma (20% duty cycle)
(+12)	250 ma

FIGURE 2.

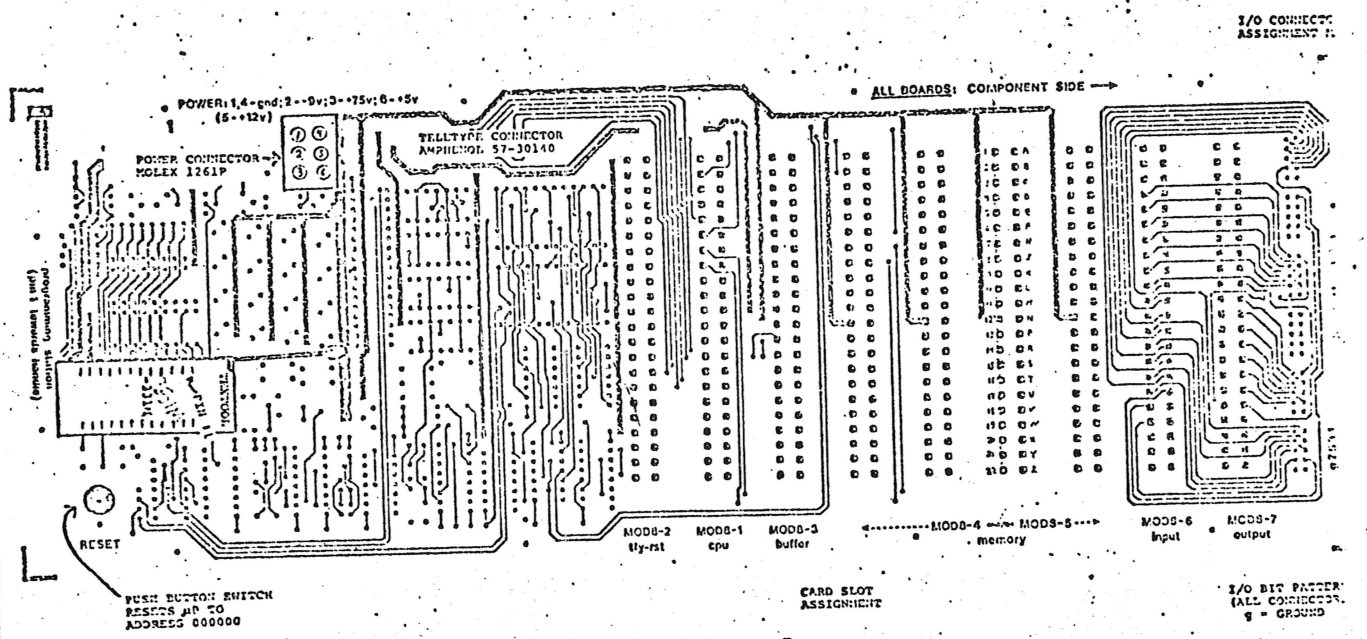
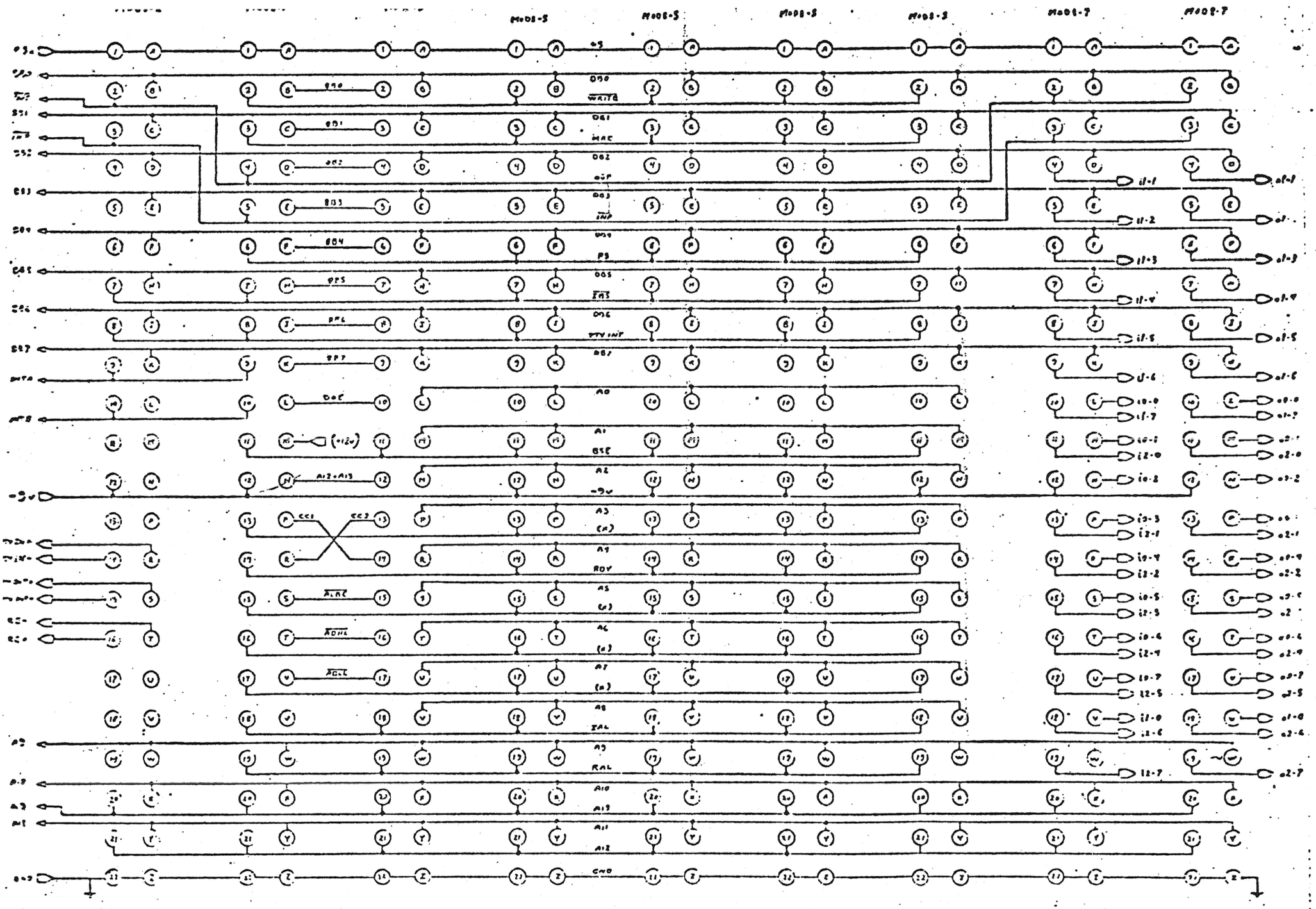
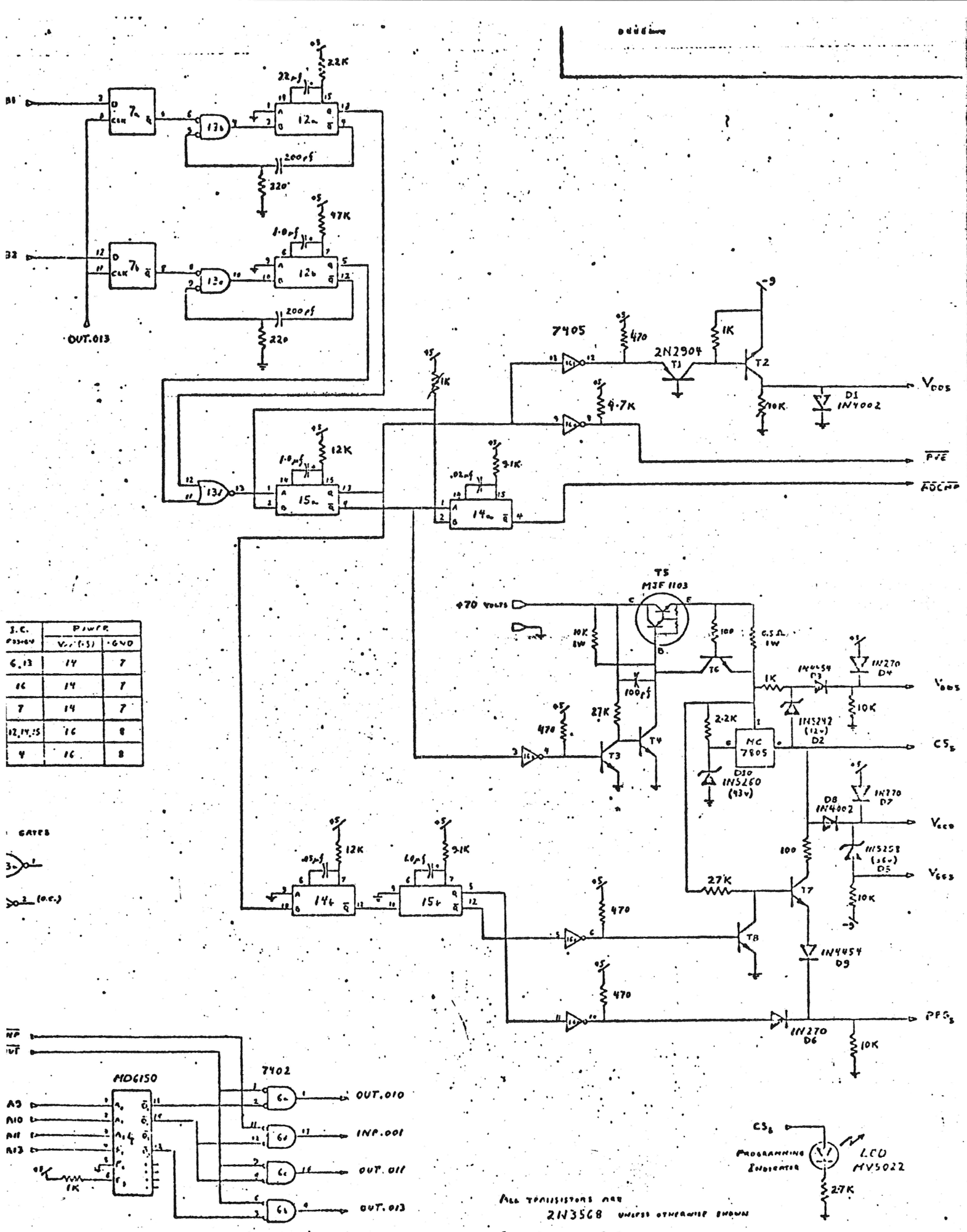


FIGURE 3.



Notes: (X) = UNASSIGNED, FOR FUTURE EXPANSION

Figure 1

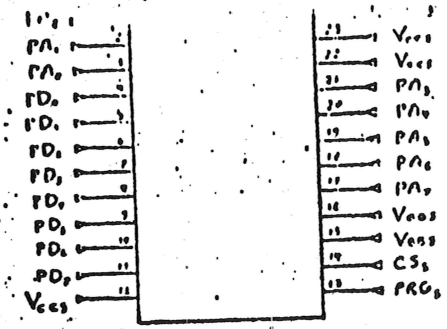


I.C. POSITION	POWER	
	V_{CC} (+5)	GND
6, 13	14	7
11	14	7
7	14	7
12, 14, 15	16	8
4	16	8

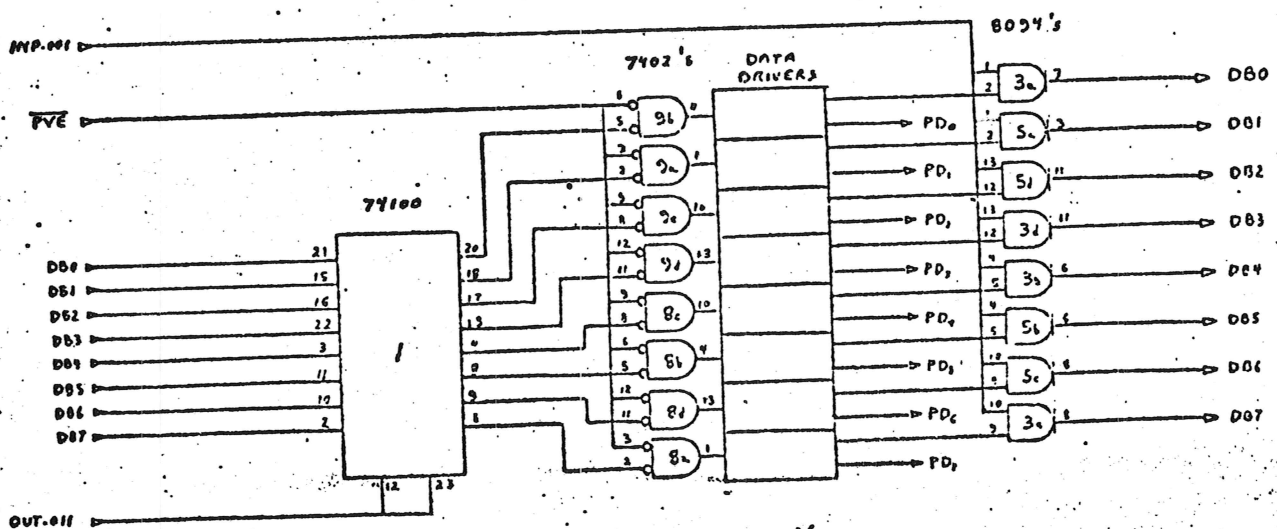
ALL TRANSISTORS ARE 2N3568 UNLESS OTHERWISE SHOWN

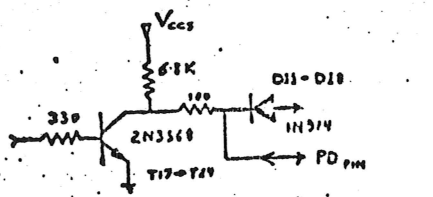
ALL RESISTORS ARE 1/4 W, 10% U.O.I.

FIGURE 4.



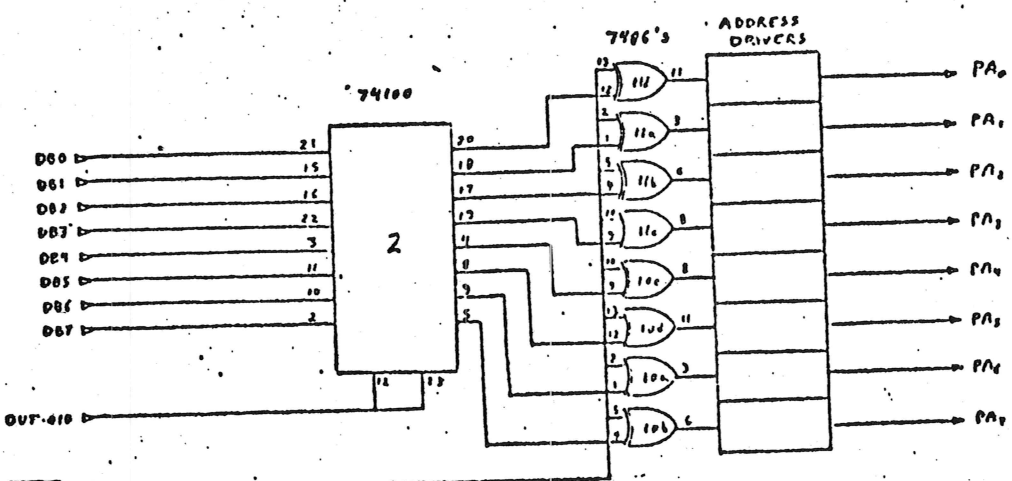
PROGRAMMING SOCKET

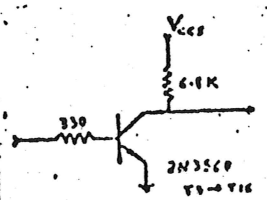




TYPICAL DATA DRIVER

	I.C. ASSIGN	POWER	
		V_{cc} (±5)	GND
2	8, 9	14	7
	10, 11	14	7
	1, 2	24	7
4	3, 5	14	7





TYPICAL ADDRESS DRIVER

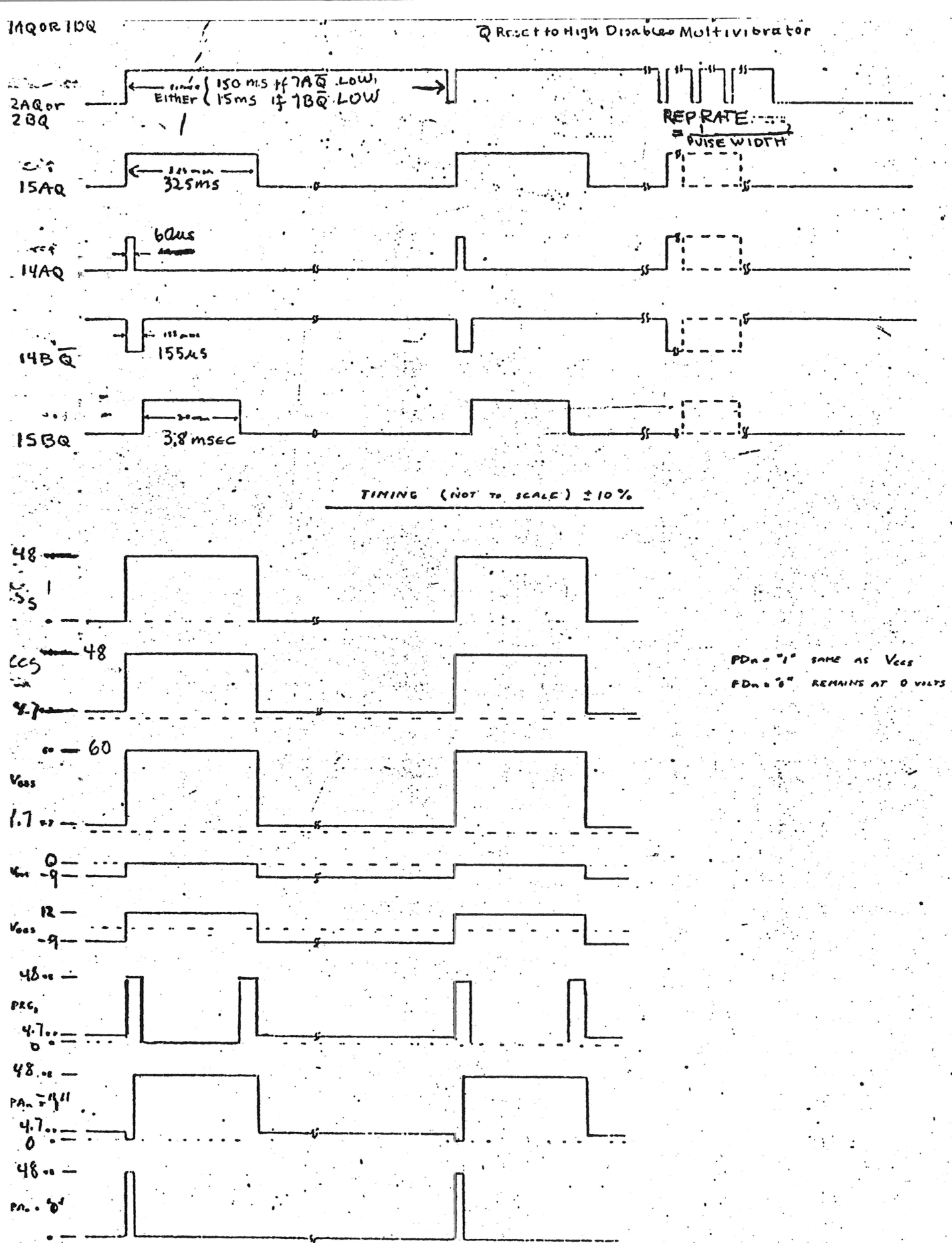
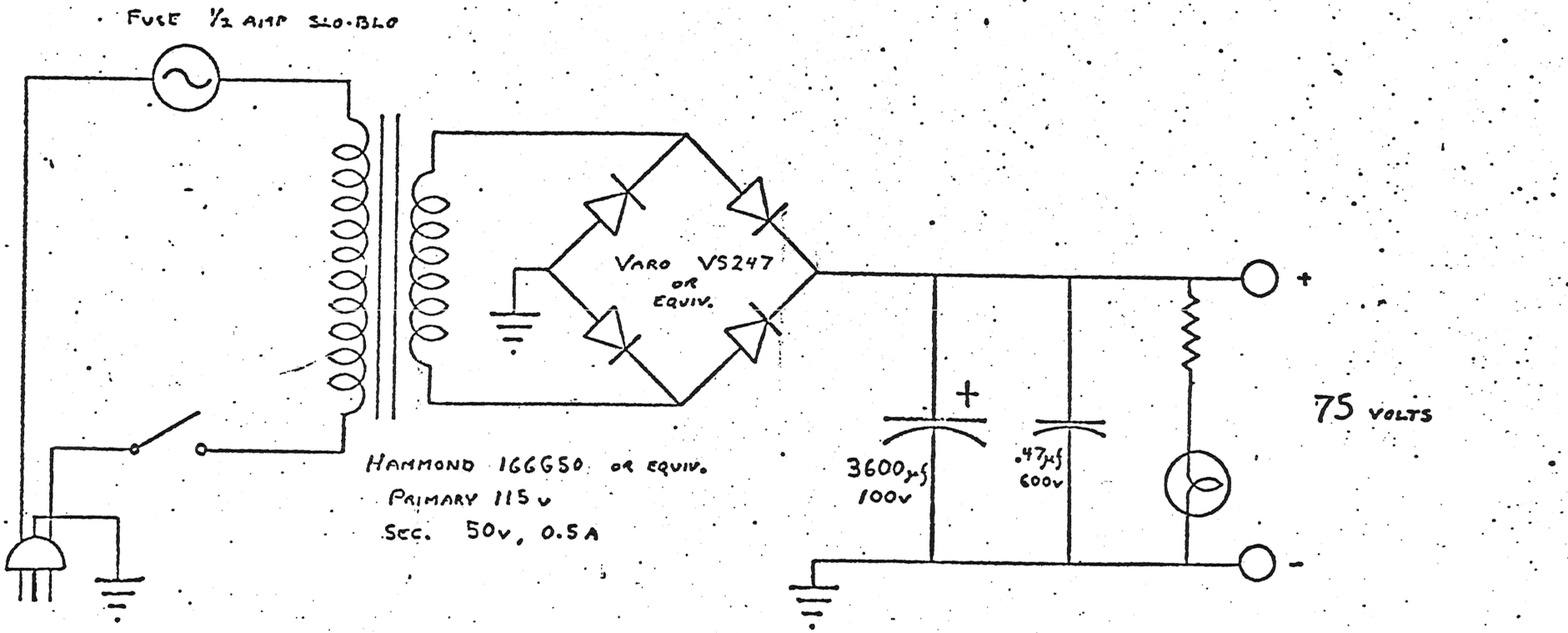

1AQ OR 1BQ
Q Reset to High Disabled Multivibrator
2AQ or 2BQ
Either { 150 ms if 7AQ̄ LOW, 15ms if 7BQ̄ LOW
REP RATE = PULSE WIDTH
15AQ
325ms
14AQ
60us
14BQ̄
155μs
15BQ
3.8 msec
TIMING (NOT TO SCALE) ±10%
48
5.5
CCS
8.7
60
VBBS
1.7
Q
12
PRG
4.7
0
PA
"1"
"0"
PDn = "1" SAME AS VCCS
PDn = "0" REMAINS AT 0 VOLTS
TIME RELATIONSHIPS NOT TO SCALE
(NOT TO SCALE)

FIGURE 6.

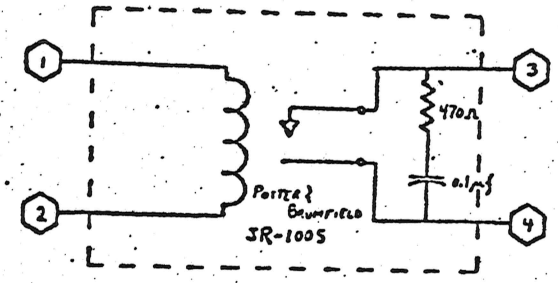


NOTE: INDICATOR SERVES AS BLEEDER. RESISTANCE SELECTED FOR LAMP OPER. VOLT.

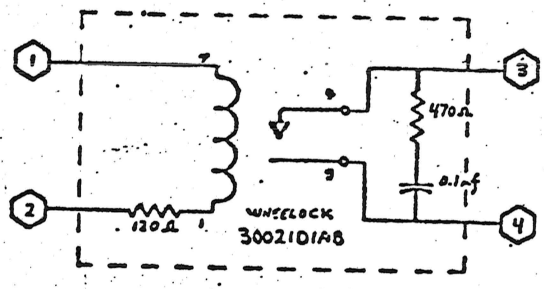
FIGURE 7.

1) RELAY AND PASSIVE COMPONENTS MOUNTED ON SMALL CIRCUIT CARD. (APPROX 2" x 2½")

2) AFFIX INSIDE TELCTYPE WITH 2 SCREWS ON TAB. NEAR CAPACITOR



OR



3) CONNECT AS FOLLOWS

a) READER RELAY COIL THROUGH TTY CABLE TO MODB CONNECTOR

b) RELAY CONTACTS TO LOWER SCREWS ON MODE SWITCH (REF. FIG. 8)

c) WIRE FROM "LOCAL" SCREW TERMINAL SPLICED INTO BROWN WIRE AT CONNECTOR PLUG # 4

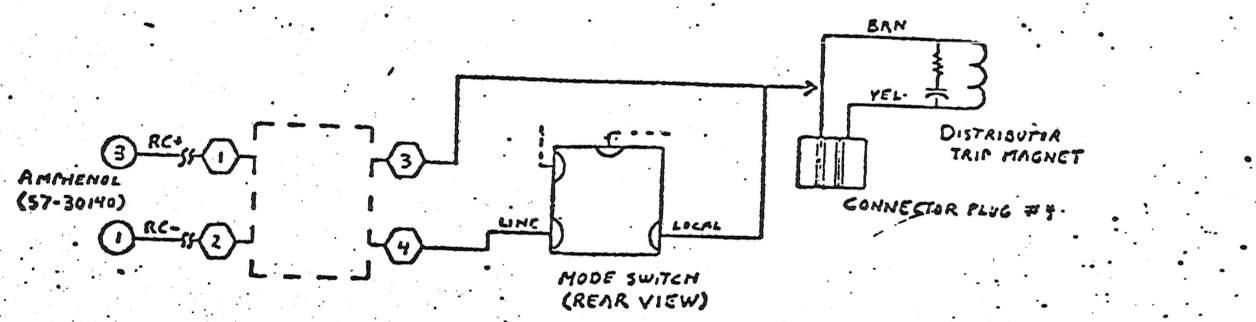


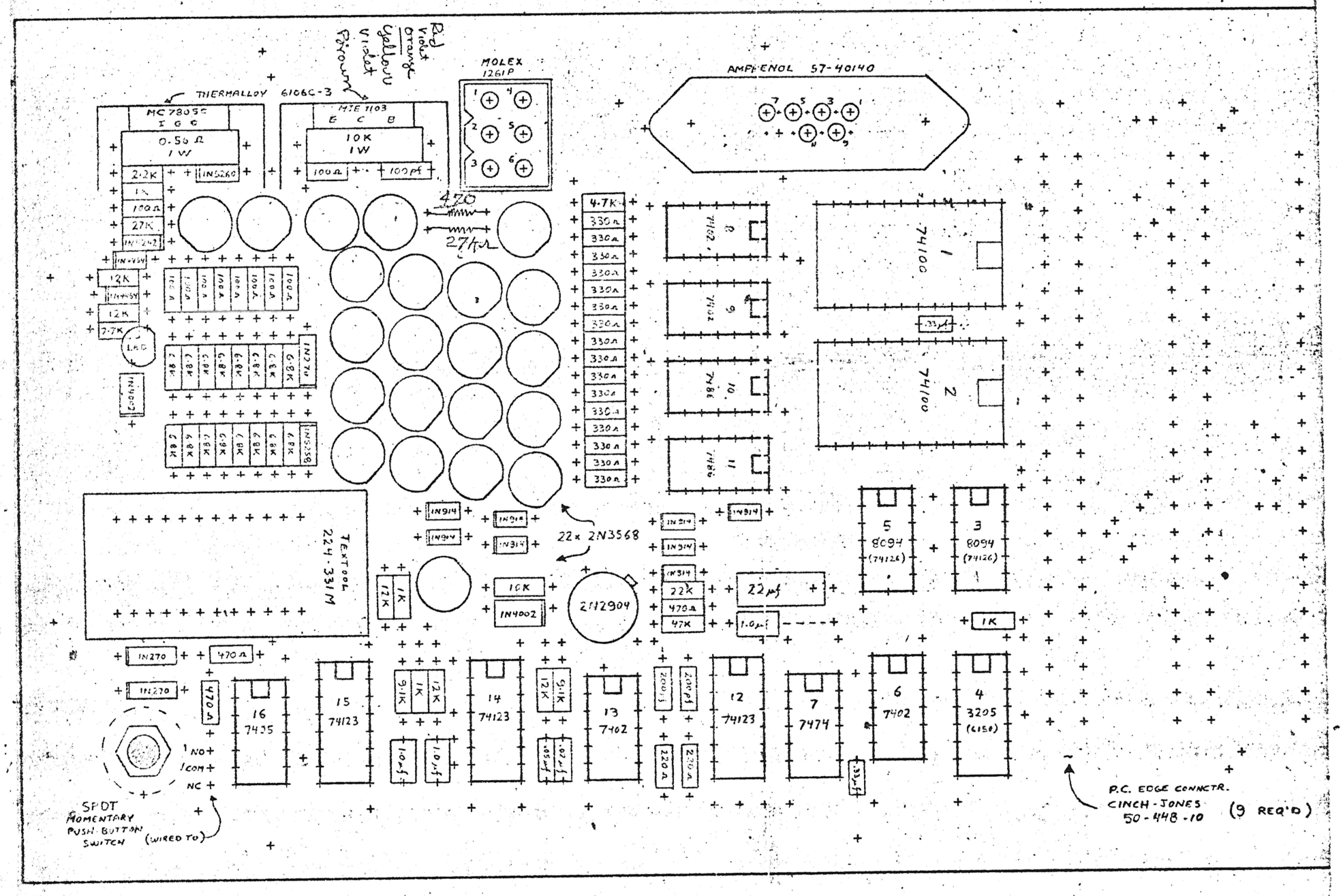
FIGURE 9.

MOD8-8 BACKPLANE/PROM PROGRAMMER PARTS LIST

Quantity	Part No.	Description
9	Cinch Jones 50-44B (10M)	22 pos 44 Contact .156" Edge Connector
1	Amphenol 57-40140	14 Contact Receptacle
1	Amphenol 57-30140	14 Contact Plug
1	Molex 03-09-2062	6 Contact Plug Nylon Housing
1	Molex 03-09-1063	6 Contact Receptacle Nylon Housing
6	Molex 02-09-1103	Crimp Tail Terminal Female
6	Molex 02-09-2133	Solder Tail Terminal Male
1	Alcoswitch MSP-105-F	SPDT Momentary Push Button Switch
2	Berg 65274-1	1 X 36 Straight Header
4	7402	Quad 2 Input NOR
1	7405	Hex Inverter Open-Collector
1	7474	Dual D-Type Flip Flop
2	7486	Quad 2 Input XOR
2	74100	Dual 4 Bit Latch
3	74123	Dual Retriggerable Monostable
1	ML3205 (74LS138)	1 of 8 Decoder
2	8094 (74126)	Quad Gated Tri-State Buffer
1	MJE 1103	Darlington Power Transmitter
1	MC 7805	Monolytic +5 Volt Regulator
2	Thermalloy 6106C-13	Coolers
3	IN 270	Germanium Diode
2	IN4002	Silicon Diode (1 Amp)
2	IN4454	Signal Diode
8	IN914	Signal Diode
1	IN5242B	12V 5% Zener Diode
1	IN5258B	36V 5% Zener Diode
1	IN5260B (IN4755)	43V 5% Zener Diode
1	MV5022	Light Emitting Diode
22	2N3563	60V NPN Transistor
1	2N2904 (2N 2905)	PNP Transistor
10		100 Ohm 1/4W 5% Resistor
2		230 Ohm " " "
16		330 Ohm " " "
4		470 Ohm " " "
4		1K Ohm " " "
1		2.2K Ohm " " "
1		2.7K Ohm " " "
1		4.7K Ohm " " "
16		6.8k Ohm " " "
2		9.1K Ohm " " "
6		12K Ohm " " "
1		22K Ohm " " "
1		27K Ohm " " "
1		47K Ohm " " "
1		10K Ohm 1W " "
1		56 Ohm 1W 10% "
1		100pf Disc Ceramic Capacitor
2		200pf Disc Ceramic Dapacitor
1	8121-050-651-223M	.022 uf Red Caps Ceramic Capacitor
1	8121-050-651-473M	.047 uf Red Caps Ceramic Capacitor
3	8131-050-651-105M	1.0 uf Red Caps Ceramic Capacitor
2	8131-050-651-334M	.33 uf Red Caps Ceramic Capacitor
1	Textool 224-331M	24 Pin Zero Insertion Force Socket

MOD8-8 BACKPLANE/PROM PROGRAMMER PARTS LIST

Quantity	Part No.	Description
1	CS13BF226K	22 uf 35 V Elect. Cap.
1		Mod8-8 Printed Circuit Board
1	Hammond1443-18	13½ X 5 X 2 Printed Al. Chassis
12		#4 X 14 Sheet Metal Screws
A/R		1/8" Shrink Tube
23	Thermalloy 7717-3	Transistor Mounting Pads



MOD 8-8 PARTS LAYOUT

AUDIO CASSETTE/MOD8 INTERFACE

CONTENTS

THIS APPLICATIONS NOTE IS PUBLISHED AS A GUIDE FOR DESIGNERS, CIRCUIT DIAGRAMS AND SOFTWARE LISTINGS SHOWN ILLUSTRATE TYPICAL APPLICATIONS ONLY, AND NO RESPONSIBILITY WILL BE ASSUMED FOR ANY CONSEQUENCE OF THEIR USE. A FULL DESCRIPTION OF THE MICROSYSTEMS INTERNATIONAL LTD. MF8008 BASED MOD8 DEVELOPMENT PACKAGE MAY BE FOUND IN THE MF8008 CENTRAL PROCESSING UNIT APPLICATIONS MANUAL.

1.0 INTRODUCTION

With the increasing use of microprocessors there is a growing need for low cost memory devices. This is especially true during software development when it is desirable to generate back-up copies of RAM subroutines as they are developed. Although paper tape units, usually in the form of a teletype, do offer a permanent back-up medium, they suffer from several draw backs. These are notably the slow data rate of 10 characters/sec and the bulky rolls of paper tape resulting from large dumps. A solution to these problems was found by using a low cost audio cassette unit to store data. Offering ~~330~~ 336 bytes/sec and a very low cost reusable audio cassette as storage medium the complete system is an attractive alternative to the teletype paper tape approach.

2.0 OPERATING PRINCIPLES

There are two popular methods of recording data on cassette units, FSK encoding and tone burst recording. The FSK techniques involve a frequency shift over a relatively narrow frequency range to encode 1 and 0 levels on the magnetic tape. During playback a phase lock loop circuit tracks the tone and the resulting VCO signal is used to determine the logic level (frequency) being received. The tone burst technique relies on the presence of a tone to indicate one logic level and the absence of the tone to represent the other logic sense. (Both approaches were investigated during a "bargin basement" variety of audio cassette unit with varying degrees of success.) With the FSK system, temporary loss of signal due to tape imperfections and the tape "bumping" against the head will force the PLL to lose track of the input frequency. The required relocking of the PLL may require several bit times. Furthermore, wow and tape flutter will cause frequency shifts which could be interpreted as data bit transitions. The simpler tone burst approach will work satisfactorily at low

baud rates but begins to fail above the 200 baud levels. The principal disadvantages are brought about by the automatic level controls (ALC) used in most cassette units which adjust the recording amplifier gain to compensate for signal level differences. If the input goes to a no tone state to record a zero level the ALC will boost the recording amplifier gain to maximum resulting in an unbearable back ground noise being recorded.

A hybrid approach between FSK and tone burst recording was arrived at which took advantage of the low (<8 kHz) high frequency response of cassettes. The system encodes the digital information as two tones, a logic 1 represented by 6 kHz and a logic 0 as 12 kHz. The 12 kHz signal, although well above the response of the cassette, ensures that the ALC circuit does not increase the recording amplifiers gain. During playback a simple bypass capacitor tends to filter any high frequency tones. The lower 6 kHz signal is digitally integrated to provide a logic 1 level. The digital integrator will trap after 1 cycle and hold up to 1 cycle time thus reducing problems due to drop outs and tape noise. The software used to generate and receive the serial data also includes parity checking routines. Furthermore, each bit time is divided into 12 equal sample times and the data read routine averages the samples during each bit time. This further reduces the number of errors due to tape noise and drop-outs. The resulting system will operate very satisfactorily at a 330 baud rate with an error rate better than 1 bit/10^6 bits using a medium quality audio cassette cartridge.

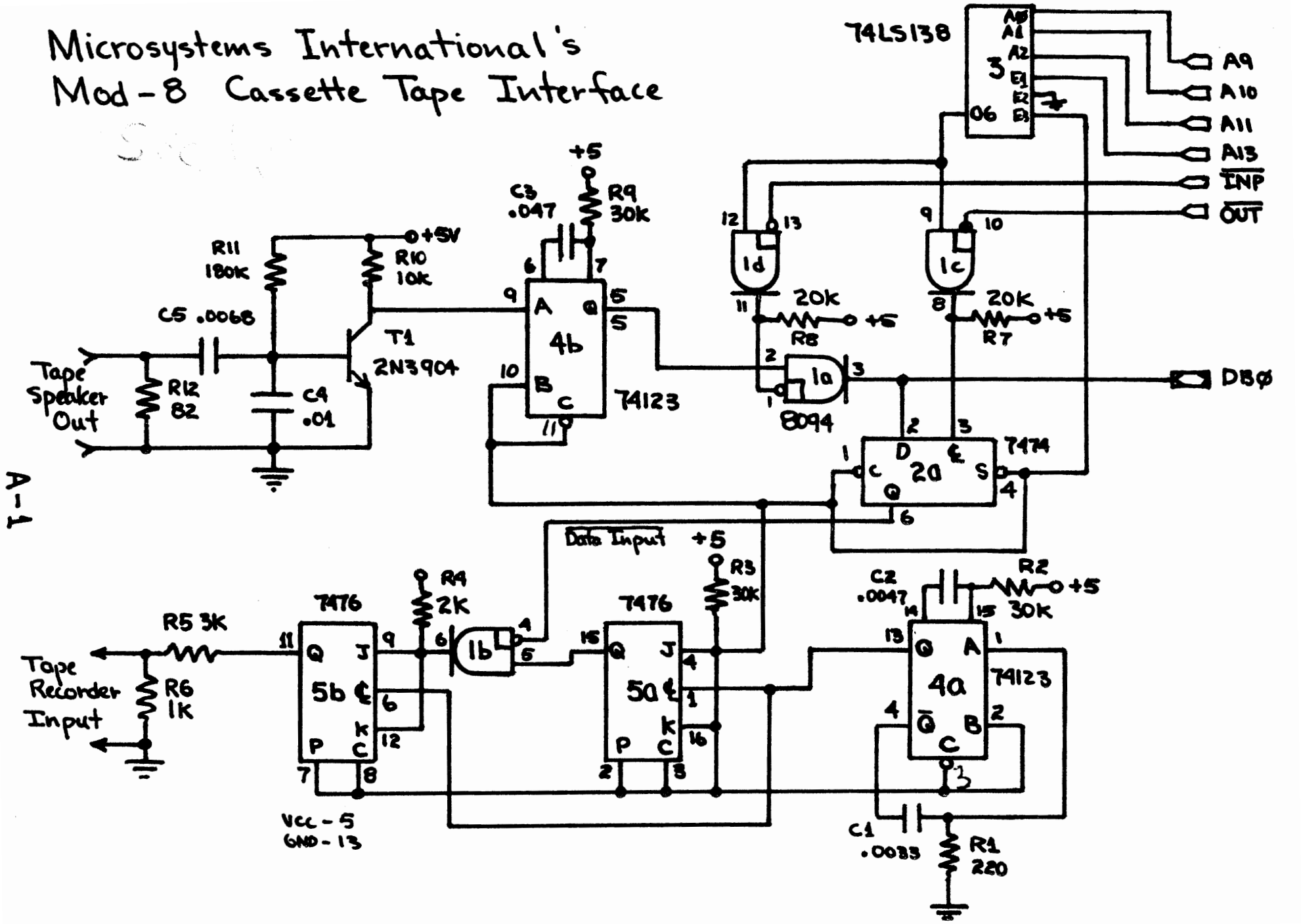
Each 8 bit byte may be recorded as a single word. This further increases the byte/sec rate over the teletype approach which will generally require three or more 8 bit ASC II characters to represent a single byte.

0 HARDWARE

The hardware interface requirements are shown in Figure 1. The monostable 4A with R, C, forms a free running astable with a frequency of 24kHz. The two JK flip flops 5a and 5b and the tristate buffer 1b form a divide by two or divide by four network, depending on the data present at the data input line, pin 4 of 1b. If the data input line is high the tristate buffer output, and the JK inputs of 5b, are held high by the pull-up resistor R4 and the input clock frequency of 4b (24kHz) is divided by two giving 12kHz output to the recorder input. If the data input line is taken low the tristate buffer will pass the output of 5a to the JK inputs of 5b. The two JK's then form a 2 bit synchronous counter, the output of 5b being 6kHz. The serial data stream generated by the MOD8 microcomputor is transferred to the data latch 2a during an OUT 016 command. The inverted data, from $\overline{Q}$ of 2a is then used to drive the DATA INPUT of the write generator.

During playback the 6kHz signal is buffered to TTL levels by T_1. The bypass capacitor C_4 filters the remaining 12kHz signal and C_5 blocks the low frequency noise found in low cost cassette units. The resulting signal is applied to the retriggerable ~~overlot~~ ONESHOT 4_b which has a period of 6.0 msec. The 6kHz tone causes continuous retriggering of the ~~overlot~~ ONESHOT and the Q output of 4b is transferred through the tristate buffer 1a during an INP 006 command. The MOD8 port address lines A_9 - A_{13} are decoded by the 1 of 8 decoder 3 and then combined with the I/O control lines INP and OUT in 1b, 1c to generate the INP ~~006~~ and OUT ~~016~~ control signals which transfer data from the integrator or to the write buffer respectively. The complete unit may be built on a standard 4.5"x6.5" vero card type 11825 which will plug directly into a MOD8 input/output edge connector.

Microsystems International's Mod-8 Cassette Tape Interface



A-1

4.0 SOFTWARE

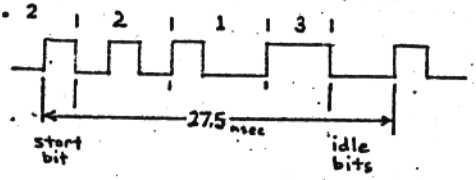
The cassette interface software is found in ROM 007/1 locations 007000 - 007277 inclusive. The software package may be split into three distinct functions: the write routine, the read routine, and the tape monitor routine. The write routine accepts 1 byte of data, contained in the B register and converts this byte to a serial data pattern at the desired bit (baud) rate. It is also responsible for the insertion of start, stop and idle bits, being very similar in function to the teletype output routine found in MONITOR8. The read routine accepts the data from the cassette, converting the serialized data back into a single byte stored in the A and B registers. Its function is the parallel of the TTY input routine of the MONITOR8 package. The tape monitor routine acts as the interface between the read/write routines and the user, allowing dumping, loading and verifying specific memory addresses.

4.1 WRITE ROUTINE

The write routine is found at locations 007200 - 007230 inclusive. The routine first outputs a "1" level for a period of one bit time (2.0 msec) which acts as the start bit to which all other bits of the particular word are referenced. Following the start bit are the 8 data bits of the byte contained in the B register, the least significant bit (LSB) immediately following the start bit, the last data bit is followed by a "0" level stop bit and a 0 level idle time. The required idle time is determined by the complexity of the monitor system which must retrieve the next byte from memory or, if performing a read operation, store the previously read word in memory

during the stop and idle bit times.
Figure 2 shows the byte pattern generated by the write routine transmitting a 312 pattern using the standard 2 usec MOD8 clock speed.

Fig. 2



4.2 READ ROUTINE

The read routine, located at 007231 to 007273 inclusive must convert the serial data pattern generated by the write routine back into an eight bit byte. The routine examines the integrated data from the cassette unit waiting for a logic 1 level, interpreted as the beginning of the start pulse. The routine then waits for the remainder of the start bit time before passing into the data bit read sequence. Each data bit time is subdivided into 12 equal time slots and the input signal from the cassette integrator is summed over these 12 sample times. The resulting sum, ranging between 0 and 13, is then examined and if equal to or greater than 7 the received bit is interpreted as a logic 1, otherwise the bit is taken as logic 0. After 8 such bits have been input and assembled control is returned to the calling routine, the received data being contained in the A and B registers.

4.3 MONITOR ROUTINE

The monitor routine controls the data flow to and from the cassette unit, offering the user three options, dumping to cassette, loading from the cassette and verifying that the cassette data is the same as the memory.

Contained in locations 007000 to 007177 the routine is entered from MONITOR8 by typing XQT 007000. Employing MONITOR8 subroutines the tape monitor first requests the address range to be acted upon in the standard MONITOR8 format as given in the MF8008 Applications Manual. After the address range is entered the tape monitor will type the three options available, dump, load or verify as shown below.

```
    XQT 007000          user request to enter tape monitor
  * XXXXXX YYYYYY       address range entered
    D/L/V:              option request
```

Following the printing of the option list the user should start the cassette unit, either in the record or playback mode depending on the desired function. The desired option is then typed in. An invalid letter (option) will be rejected and the monitor will retype the option list. A CTRL/A will cause a complete abort and return control to MONITOR8. If the W (write) option is chosen the monitor will wait 5 seconds to ensure the tape leader is past the head, write a preamble of 8 377_8 words and a sync word 000. Immediately following the 000 sync word the memory data is recorded as continuous data words. Upon completion the monitor routine returns control to MONITOR8. The read and verify routines, being very similar, use a program transfer to RAM memory in order to minimize program duplication. If the L (load) option is chosen location 013350 is loaded with a LMA (370) command. If the V (verify) option is used location 013350 is loaded with LAA (300). Both the LOAD and VERIFY routines then merge into a common subroutine which first loads location 013351 with a RET (007). The playback routine

reads characters from the cassette until it receives a 377 word and then waits until it receives the sync word 000. The routine then retrieves the CLP, fetches a byte from the cassette, executes the subroutine at 013350 which will rewrite the data byte into memory only if the load option was chosen and then returns to compare the memory locations with the cassette data. The routine updates the CLP and continues until all the specified memory range is loaded or verified at which time control is returned to MONITOR8.

If an error should occur during the verify routine the tape monitor will exit to the MONITOR8 breakpoint execute routine. This routine will print the carry flag, the A, B, C, L and H registers and the contents of memory pointed to by the H and L registers. In this case the A and B registers contain the cassette data and the H and L registers point to the CLP memory address. The verify routine will abort after the first failure, control being returned to MONITOR8 after the breakpoint listing.

```
007000/ 250  XRA
007001/ 135  OUT 016        SET WRITE BUFFER TO ZERO
007002/ 006  LAI 207
007004/ 016  LBI 011
007006/ 104  JMP 003036     FETCH ADDRESS RANGE, RETURN TO 007011
007011/ 066  LLI 170        START OF OPTION LIST ADDRESS
007013/ 056  LHI 007
007015/ 317  LBM            PRINT OPTION LIST
007016/ 025  RST 020
007017/ 060  INL
007020/ 120  JFS 007015     LIST ENDS AT 007177
007023/ 035  RST 030        GET OPTION REQUEST
007024/ 074  CPI 104        TEST IF "D"
007026/ 150  JTZ 007125
007031/ 074  CPI 114        TEST IF "L"
007033/ 026  LCI 371        (LMB)
007035/ 150  JTZ 007047     WAS LOAD OPTION
007040/ 074  CPI 126        TEST IF "V"
007042/ 110  JFZ 007011     NO, GET NEW OPTION
007045/ 026  LCI 300        (LAA)
007047/ 056  LHI 013
007051/ 066  LLI 350
007053/ 372  LMC            013350= C REGISTER (LMB OR LAA)
007054/ 060  INL
007055/ 076  LMI 007        013351= RET
007057/ 106  CAL 007231     GET DATA
007062/ 010  INB            TEST IF 377
007063/ 110  JFZ 007057     NO, TRY AGAIN
007066/ 106  CAL 007231     GET DATA
007071/ 010  INB
007072/ 011  DCB            TEST IF 000
007073/ 110  JFZ 007066     LOOP FOR SYNC (000) WORD
007076/ 106  CAL 001023     GET CLP
007101/ 106  CAL 007231     GET CASSETTE DATA
007104/ 106  CAL 013350     STORE IT AT CLP OR DO NOTHING
007107/ 277  CPM            COMPARE DATA WITH CONTENTS OF CLP
007110/ 110  JFZ 000060     BREAKPOINT EXIT IF NOT EQUAL
007113/ 106  CAL 000362     ADDRESS COMPARE AND INCREMENT
007116/ 104  JMP 007076     KEEP GOING
007121/ 377  HLT
007122/ 377  HLT
007123/ 377  HLT
007124/ 377  HLT
007125/ 026  LCI 300        WAIT 5.0 SEC.
007127/ 075  RST 070
007130/ 021  DCC
007131/ 110  JFZ 007127     LOOP FOR TIME-OUT
007134/ 016  LBI 377        OUTPUT 8  377'S
007136/ 046  LEI 010
007140/ 106  CAL 007200     OUTPUT
007143/ 041  DCE            DO IT 'E' TIMES
007144/ 110  JFZ 007140
007147/ 010  INB            OUTPUT 000
007150/ 106  CAL 007200
007153/ 106  CAL 001023     GET CLP
007156/ 317  LBM            PUT DATA INTO 'B'
007157/ 106  CAL 007200     WRITE IT TO CASSETTE
007162/ 106  CAL 000362     INCREMENT ADDRESS POINTER
007165/ 104  JMP 007153     KEEP GOING TILL DONE

007170/ 315 012 104 057 114 057 126 072
```

```
007200/ 006  LAI 001        SET A=START BIT
007202/ 026  LCI 010        WILL DO 8 TIMES
007204/ 135  OUT 016        OUTPUT START BIT
007205/ 036  LDI 336        TIME OUT 2.5 MSEC
007207/ 075  RST 070

007210/ 321  LAB            GET DATA
007211/ 135  OUT 016        OUTPUT LSB
007212/ 036  LDI 336        TIME OUT
007214/ 075  RST 070

007215/ 012  RRC            ROTATE DATA
007216/ 310  LBA            SAVE AWAY FOR NEXT TIME
007217/ 021  DCC            C COUNTS BITS
007220/ 110  JFZ 007210     DO IT 8 TIMES
007223/ 250  XRA            STOP BIT = 0

007224/ 135  OUT 016
007225/ 036  LDI 310        TIME OUT   5.0 MSEC
007227/ 075  RST 070
007230/ 007  RET             FINISHED
```

ROM 007/1 READ ROUTINE

```
007231/ 026  LCI 011        INPUT 9 BITS
007233/ 115  INP 006
007234/ 032  RAR
007235/ 100  JFC 007233     WAIT FOR START PULSE
007240/ 036  LDI 334        TIME OUT 1 BIT TIME
007242/ 075  RST 070
007243/ 343  LED            CLEAR E
007244/ 021  DCC            COUNT # OF BITS
007245/ 053  RTZ            RETURN IF FINNISHED
007246/ 036  LDI 364        D COUNTS SAMPLES
007250/ 115  INP 006        GET SAMPLE
007251/ 044  NDI 001        MASK IT
007253/ 204  ADE            SUM IT WITH E
007254/ 340  LEA            SAVE SUM IN E
007255/ 030  IND            DO IT 12 TIMES
007256/ 110  JFZ 007250
007261/ 006  LAI 007        TEST IF <7
007263/ 274  CPE            SETS CARRY FLAG
007264/ 321  LAB            B HAS BYTE ASSEMBLED
007265/ 032  RAR            BY ROTATING IN CARRY
007266/ 310  LBA            SET BY COMPARE
007267/ 036  LDI 377        TIME OUT DURING
007271/ 104  JMP 007242     BIT TRANSITION TIME
007274/ 377  HLT
007275/ 377  HLT
007276/ 377  HLT
007277/ 377  HLT
--------
```

PATTERN GENERATOR ROUTINE

```
010000/ 016  LBI 000        ;B HAS DESIRED PATTERN
010002/ 106  CAL 007200     ;GO WRITE DATA
010005/ 104  JMP 010002     ;REPEAT UNTILL RESET BUTTON PUSHED
--------
```

5.0 START-UP PROCEDURE

Once the hardware is connected to the audio cassette it is necessary to adjust the recorder playback level to provide the correct signal levels to the integrator. The recommended procedure is as follows:-

(1) load the pattern generator program given in figure 4 into the MOD8 microcomputer.

(2) connect interface unit to cassette unit and start cassette player in the record mode.

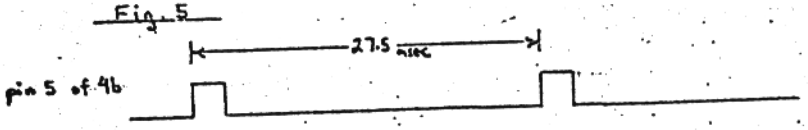
(3) execute the pattern generator routine by typing

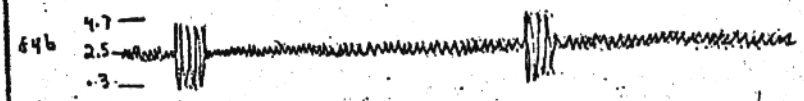
XQT 010000

the routine will write a 000 pattern on the cassette tape until the MOD8 reset button is pushed. Several minutes of this pattern should be sufficient for setting the playback level.

(4) After the reset button is pushed the cassette should be rewound and the cassette unit set to play. Connect a scope to the Q output of the data integrator (pin 5 of 4b) and adjust the cassette volume control to give a stable start bit on the scope (see Fig. 5).

Fig. 5





MOD 8 PARTS LIST 1/5/75

Quantity	Description
8	7400
3	7402
2	7404
6	74L04
1	74H106
4	7407
1	7408
2	7410
2	7474
1	7475
3	74100
2	74123
15	74125
1	74126
5	74LS138 or P3205*
4	74193
1	8008
2	2N3906
1	2N3904
1	1N914
17	1N270
8 or 16	2102**
7 or 8	1702A***
2	.22 uf capacitor
56	.33 uf or .01 uf capacitors
18	6.8 uf tantalum cap.
10	25 uf (shown as 80 uf)
4	350 pf
4	50K trimmers
8	22K ohm 1/4 watt 10% resistors
10	1K ohm 1/4 watt 10% resistors
20	10K ohm 1/4 watt 10% resistors
6	2.7K 1/4 watt 10% resistors
2	330 ohm 1/4 watt 10% resistors
1	910 ohm 1/4 watt 10% resistors
2	16 pin dip headers
2	16 pin dip sockets
1	18 pin dip socket

*note 3205 is shown also as MD 6150 in MOD 8 manual - 74LS138 is alternate part

**8-2102 for 1K
16 for 2K of RAM

***only 7 1702A ROMS are needed for Monitor 8 program

Also for back plane
Viking 2VH22/1AND is a wirewrap replacement shown for the cinch edge connector shown in back plane parts list.

Also - 1 each of MOD 8-1 through MOD 8-7 boards are needed. The MOD 8-8 is back plane and PROM programmer board.

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R. Swartz
195 Ivy
60035

ADDITIONAL NOTES ON MOD 8

1. Jumping shown in corrected manual
   selects output ports 14, 23, and 32
   input ports 5, 6, and 7.

   RAM Board for addresses 010000 to 017377
   ROM Board for addresses 000000 to 007377

   addresses given in MIL split octal notation.

2. 74125 is the same as 8094.

3. 74126 is the same as 8093.

4. All boards are available from Space Circuits at this date at $13.00 each except for MOD 8-8 backplane which is about $26.00. These prices are in U.S. dollars and add $2.50 for postage and handling for the complete set. There is an 8½% duty once landed in the U.S.

5. The following should be noted when building a power supply for the PROM programmer board. The 7805 is used as a floating supply for 48 volts. This is done by referencing it to ground with a 43 volt Zener. The absolute maximum rating on a 7805 is 35 volts. This means that the power supply voltage must be less than 48 volts plus 35 volts or 83 volts. I have found that a 50 volt transformer full wave rectified may give greater than 83 volts and thus destroy the 7805. This is dependent on the line voltage in your area. The recommended value for this supply is 70 volts and a preregulator may be necessary to achieve this. In any event these facts should be considered when building a supply and the voltage out of the supply should be tested to be sure it does NOT exceed the 7805 maximum rating.

6. On some of the Boards from Space Circuits, the following problems have been found to occur on the MOD8-1 Pin 9 of IC 15 or IC 16 has been found to short with one of the bus lines

   On the input board, about an inch above the connector fingers on the component side, there may be a break on one of the traces.

7. There are at least 2 sources of drilled boards for prototyping on the MOD 8 system, Vector Electronic Company, Inc., 12460 Gladstone Avenue, Sylmar, California 91342; and Douglas Electronics, 718 Marina Blvd., San Leandro, California 94577.

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195 Ivy
60035

ERRORS IN MIL APPLICATION MANUAL

BULLETIN 80007 - 1974 EDITION

on the MF 8008

	PAGE	
1.	A-3	Figure of one cycle or processor timing has T_3 and stopped states are reversed.
2.	B-7	In component placement an 1k resistor is missing from the 3205/6150. It is connected to pin 6 of IC6.
3.	B-9	IC4 is a 3205/6150 NOT a 7402 as shown in component placement.
4.	B-14	in schematic IC8 3205/6150 pin 4 is E1, pin 5 is E2.
5.	B-12	in schematic IC11 6150/3205 pin 6 is E3.
6.	B-6	Pins 15 and 18 in schemacic are reversed on MF 8008.
7.	B-7	IC-4 in component placement is a 7408 NOT a 7400.

HELPFUL HINTS IN GETTING A RUNNING SYSTEM

The following hints are for those assembling a MOD 8 system from the boards as I have done:

1. The RAL line must be jumpered to ground for operation of the system.
2. A 74LS138 may be used instead of MD 6150/3205 and works on all boards. They are available at distribution whereas the MIL 3205 is not and are less than Intel's 3205.
3. I found one board from Space Circuits which had bad plate-throughs. I, therefore, suggest that all plate-throughs and all lines be tested for continuity before insertion of components. This process will save considerable time during de-bugging.
4. After components are inserted or sockets inserted, I suggest that all lines be D.C. tested for solder bridges. Here again, a few hours spent will save many hours of de-bugging.
5. The programs attached may be programmed into a 1702A at the locations shown. Each program begins at an address which can be accessed by a restart instruction. To run these programs a diode array with the particular restart instruction on it should be placed into IC location number 6 on the teletype restart board (MOD 8-2). Then to start the program the pushbutton should be pressed. Each program tests another part of the processor as shown below. A 1702A with all of the programs burned into it is available from Wilcox Enterprises, 25W 178 39th Street, Naperville, Illinois, for $35.00.
6. In using this method with above programs a scope or logic probe is, of course, indispensable to look at the data bus lines, the address lines and the other signals. For this method to work the TTY in + TTY - lines must be shorted, otherwise the switch will not interrupt the processor and allow the restart instruction to be jammed into the processor. A logic probe can be used almost everywhere instead of a scope except for setting up a clock. In addition, using a one shot or 555 and a switch, one can design a circuit which will single step the processor. With this and a test ROM it may be an aid in de-bugging (I never found this necessary).

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CYCLE PROCESSOR

```
000000/ 300   LAA       NOP
000001/ 300   LAA       NOP
000002/ 005   RST 000   LOOP AROUND
000003/ 000   HLT
```

READ MEMORY

```
000020/ 300   LAA       NOP
000021/ 300   LAA       NOP
000022/ 066   LLI 001   SET UP L
000024/ 056   LHI 010   SET UP H
000026/ 307   LAM       READ MEMORY
000027/ 025   RST 020   LOOP AROUND
```

WRITE MEMORY

```
000040/ 300   LAA       NOP
000041/ 300   LAA       NOP
000042/ 066   LLI 001   SET UP L
000044/ 056   LHI 010   SET UP H
000046/ 076   LMI 252   WRITE MEMORY
000050/ 045   RST 040   LOOP AROUND
```

READ WRITE AND COMPARE MEMORY

```
000060/ 300   LAA       NOP
000061/ 300   LAA       NOP
000062/ 066   LLI 001   SET UP L
000064/ 056   LHI 010   SET UP H
000066/ 006   LAI 252   LOAD A WITH 252
000070/ 370   LMA       PUT 252 INTO MEMORY
000071/ 277   CPM       COMPARE MEMORY WITH A
000072/ 150   JTZ 000060 IF THE SAME LOOP
000075/ 000   HLT       OTHERWISE HALT
```