1.0 Introduction

This document outlines the addressing and data bit parameters required for programming the MK3 motherboard.

2.0 Address Map

ACIA	CONTROL	$F080
	DATA	$F081
PIA	A SIDE DATA	$F100
	A SIDE CONTROL	$F101
	B SIDE DATA	$F102
	B SIDE CONTROL	$F103
CRTC	ADDRESS REGISTER	$F180
	DATA REGISTER	$F181
EPROM		$F800 to $FFFF
ROM0		$C000 to $DFFF
ROM1		$A000 to $BFFF

2.1 Parallel Interface

	Bit		Function
PIA	A0-A7	Input	Keypad input (asserted high)
	CA1	Input	VS - Vertical Sync (asserted high)
	CA2	Input	Keypad strobe (asserted low)
	B0-B1	Input	Parity select - 00 space 01 mask 10 even 11 odd
	B2	Input	RGB/RF (character size) Select 0 - RF (Format 1) 1 - RGB (Format 0)
	B3	Output	Serial multiplexor select 0 - 25 pin male (external) 1 - 16 pin dip (internal)
	B4	Output	Alpha/graphic select

0 - graphic
1 - alpha

B5	Output	Audio beeper - pulsed output
B6	Output	Off hook/dial pulse signal
B7	Output	DTR and TV (asserted low)
CB1	Input	SDCD (asserted low)
CB2	Output	SRTS (asserted low)

2.2 Serial Device

- parity select from PIA
- baud rates selected by individual switches
- baud clock rate setting
  64X when PIA B5 low
  16X when PIA B5 high
  (baud is 4 times on dip connection)

2.3 EPROM

2.4 ROM 0/1

- masked ROM set selected by SW7 and SW8

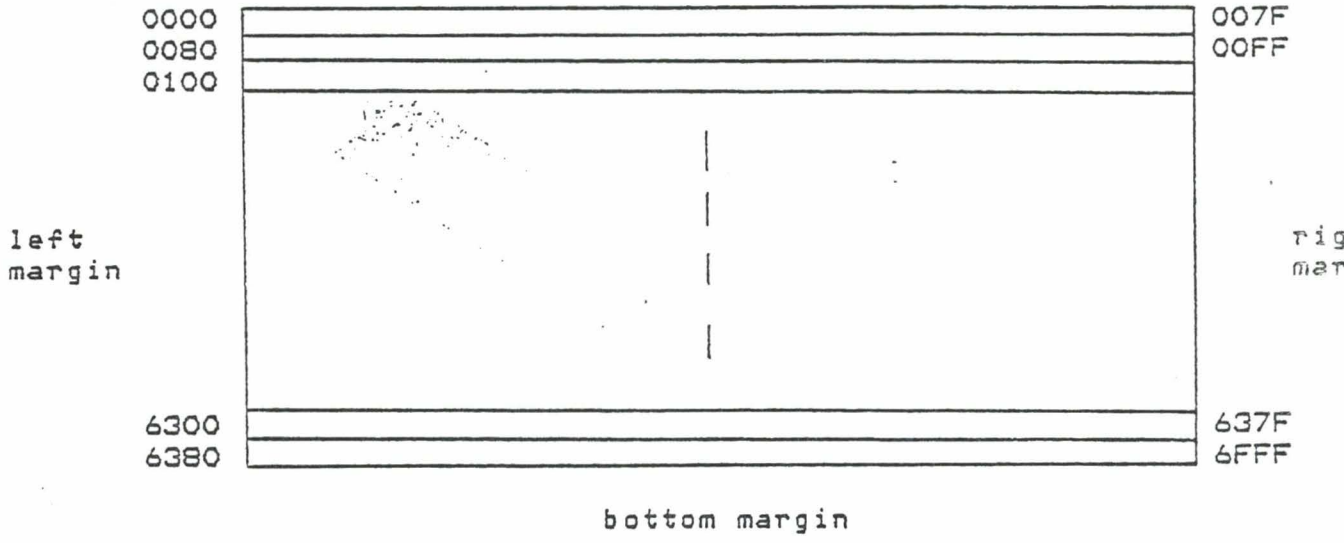
SW7	SW8	ROM0/1 Address Space
0	0	not used
0	1	$A000 - $BFFF
1	0	$A000 - $D7FF
1	1	$A000 - $DFFF

2.5 Video RAM

- Address space is $0000 - $63FF
- Upper left of screen is $0000
- Upper right of screen is $007F
- Lower left of screen is $6380
- Lower right of screen is $63FF
- Data values (pixel value)

Byte sectioning	
7654	3210
left pixel	right pixel

Video screen



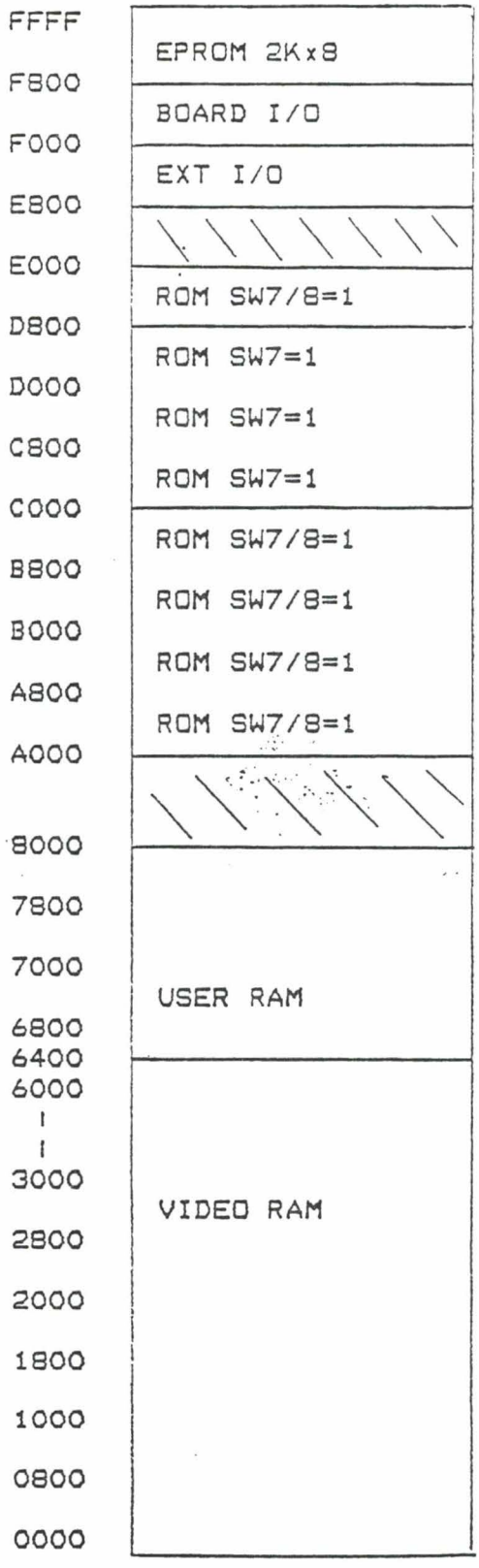


Figure 2 Memory Map

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1.0 Introduction

The alpha generator module is an alphanumeric hardware character generator. It is used in conjunction with an MK3 motherboard to produce an 80 by 24 character display and is switchable under control of the MK3.

For other applications, the format of the display can be altered by programming the board with different attributes.

2.0 General

The alpha board is composed of several basic blocks:

a) CRT controller
b) character display storage (RAM)
c) character set storage (ROM)
d) video output

This module has the majority of its sections based around a 50 conductor microprocessor bus (address, data and control). All data transfers are done under control of a microprocessor external to this board. It is not a stand alone unit.

3.0 CRT controller

One of the main components of this module is a programmable CRT controller I.C. (E17-MC68A45). It interfaces to both the microprocessor bus and to a RAM buffer section.

With a correct set of parameters, the 6845 will generate a display of 80 characters in 24 rows on a video display device. Programming of the CRT controller (CRTC) is via the micro bus. Once programmed, the CRTC will generate refresh addresses (E17-MA0 to MA10) to access data from the RAM memory as bytes, and then using its row counter outputs with external circuitry, generate a serial bit stream of video.

As the display is 80 by 24, a total of 1920 characters may be displayed on the screen. This dictates the use of 2K (2048) bytes of memory for memory.

The 6845 also generates the necessary horizontal, vertical and blanking signals necessary for a video display. Internal features of the CRTC also provide a cursor output that is programmable in size and that may be blinked if desired.

3.1 RAM Memory

The RAM memory, character storage is composed of 2K (2048) bytes of memory. It is implemented in 1K (1024) by 4 static rams (logic diagram sheet 2, E18 to E21 - 2114's).

Two access ports are required of these RAMs in order for them to be display by the CRTC (read access), and to be written by a microprocessor. The latter port is both for reading and writing characters, as single bytes, by the micro in generating the characters to be displayed.

Addresses to the RAMs are multiplexed by three 74LS157's (E11 to E13) to select either the microprocessor address or the CRTC refresh address. The multiplexing is controlled by the pin 1 select signal, MICRO, which is high for micro addresses.

Chip selects on the 2114's are controlled by the highest order address bit A10/MA10, for selecting either the first or second 1K byte block (E13 pins 4,7).

Accessing of the RAM memory space by the microprocessor ($E000 - $E7FF) will cause the multiplexors to switch (E35 pin 12).

It should be noted that the CRTC is being run on a clock that is asynchronous with respect to the microprocessor clock or E. This means that if access into RAM memory occurs during a horizontal display time, glitching will occur on the screen. To overcome this problem, the display enable (E17 pin 18) is tied to an input pin on a PIA (E16 pin 40 - CA1) where it can be monitored so that memory access occurs during horizontal retrace only.

3.2 ROM Memory

The ROM memory contains the character shapes as bit mapped storage. Two ROMs are utilized to provide two complete character sets (E30 and E31). The signal, ALT CHAR SET, selects which of the 2K eproms is used for display.

Data from the RAM storage is latched in E29 (74LS374) before becoming an address into the eproms. Seven address bits are taken from RAM (A4 to A10) to select the character, while four o the bits come direct from the CRTC, row address 0 through 3 (RA 0-3) to become A0 through A3 of the ROMs. These latter four bits select the byte row within character.

Storage wise, each character looks like:

		7	6	5	4	3	2	1	0
Byte	0	0	0	0	1	0	0	0	0
	1	0	0	1	0	1	0	0	0
	2	0	1	0	0	0	1	0	0
	3	1	0	0	0	0	0	1	0
	4	1	0	0	0	0	0	1	0
	5	1	1	1	1	1	1	1	0
	6	1	0	0	0	0	0	1	0
	7	1	0	0	0	0	0	1	0
	8	1	0	0	0	0	0	1	0
	9	0	0	0	0	0	0	0	0
	10	0	0	0	0	0	0	0	0
	11	0	0	0	0	0	0	0	0
	12	0	0	0	0	0	0	0	0
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	14	0	0	0	0	0	0	0	0
	15	0	0	0	0	0	0	0	0

There are 16 bytes of data for each character, which is selected by RA0-3.

Outputs from the roms are passed to E22 (74LS166), an 8 bit shift register, which serializes the data for the video stage.

Jumpers S3, S4, S7 and S5, S6, S8 are used for configuring E30 and E31 respectively, as triple voltage eproms, single voltage eproms or as masked roms.

3.3 Bus Buffers

As mentioned previously, the alpha board connects to a 50 conductor microprocessor bus. Address, data and control lines are all buffered to provide maximum isolation and minimum loading of this module on the bus.

The control lines which consist of E, R/W, RESET L and I/O are all buffered through a 74LS367 (E32).

Address lines A8 through A15 and A0 through A7 are buffered by 74LS244's, octal receiver/drivers, in E25 and E24 respectively.

The data lines, D0 through D7 are buffered through two transceivers, E27 and E26 (74LS245 - octal transceivers). E26 buffers data to and from the data bus connecting the CRTC (6845) and the PIA to the micro bus. The second transceiver, E27, buffers data to and from the static rams. This is necessary as the static rams are being continually read by the CRTC for refresh and bus contention problems would occur.

3.4 Address Decoding

Addressing of the two devices, the CRTC (6845) and the PIA (6821) as well as the ram storage are all handled by several I.C.'s.

The upper four address bits A12 to A15 are decoded by E36 pin 6 (74LS21) as $EXXX. This signal, with A11L is anded in E34 pin 6/E35 pin 12 to form $E000 to $E7FF, or otherwise known as MICRO to decode ram accesses. During a write cycle to static ram, E33 (74LS10) nands E and R/W with MICRO to generate WL (E33 pin 8) which is the write pulse used. Also during ram accesses, the transceiver E27 is enabled by E33 pin 12 as a result of $E000 - E7FF and E being true. Direction of E27 is controlled by R/W only.

The CRTC and PIA are decoded in the I/O segment of the microprocessor's address space, which is $E800 to $EFFF. The PIA is mapped as $EE80 and the CRTC as $EEC0. I.C. E36 pin 8 decodes address space $EEXX which is used as an enable for transceiver E26 via E34 (74LS00), and also as an input to E33 pin 3 (74S10) with A7 and A6 to generate $EEC0 for E17 pin 25. This signal at E36 pin 8 is also directly used to control CS0 on the PIA. The PIA (E16) also decodes CS1, CS2, RS1 and RS0 inputs to select addresses $EE80-3 with A7, A6, A1 and A0.

3.5 Master Clock

Clock generation on the alpha board comes from one source which is a TTL crystal oscillator (E4 -7400, XTL1 - 14.318Mhz). The clock is buffered through E4 pin 8 to be used as DOT CLK and divided by eight by E5 (74LS393) to generate the CHAR CLK (1.789 Mhz).

3.6 Parallel Interface

The PIA or parallel interface (E16) is used primarily as an output control device on the video display. Several options are available on the video display that allow the user under program control to set:

a) ALT CHAR SET - alternate character set
bit 7 0 - standard
1 - alternate

b) CURSOR MIX/INV - cursor mixing with video or inverting the video
bit 6 0 - mix
1 - invert

c) EXTRA BLINK - blinking video on ASCII characters above $F7
bit 5 0 - no blink
1 - blank

d) EXTRA INV - inverting video or ASCII characters above $7F
bit 4 0 - no invert
1 - invert

Bits 0 to 3 on the A side of the PIA are unused and are pulled high so that they may be used as inputs. Inputs CA1 and CA2 are tied to D15P EN and VS respectively, allowing interrupts to be generated on horizontal or vertical sync pulses from the video generator. (For hidden writing as mentioned before).

The PIA B side is used exclusively as inputs set by switches 1 to 8. Ideally the switches are read by the microprocessor and conditionally set video control bits in the A side. Switch 1 is read as well as hard wired to the screen invert control line. Signals CB1 and DB2 are pulled up as before.

3.7 Blink Clock

When the EXTRA BLINK control is used for video display, it enables the BLINK CLK L signal which is generated by E6 (74LS390). The duty cycle of E6 pin 9 is 1 second on, 0.5 seconds off.

3.8 Video

Data from the character ROM's is loaded into E22 (74LS166) 8 bit shift register, by a load pulse from E14 (74LS74). The character clock, CHAR CLK, sets E14 pin 8 low on its rising edge and is reset when E14 pin 5 ripples through and clears E14 pin 8. Shift register load pulse E22 pin 15, remains for one DOT CLK time.

Video is shifted out of the shift register at a rate of 14Mhz to the decoder rom E8 to the A0 input. Data bit D7 from the ram output latch passes through E7 (74LS174), to delay by one character time, to become the A1 input of E8.

The cursor and blanking (DISP EN) signals each must be delayed by two character times to achieve synchronism with the video before becoming A2 and A8 respectively of decoder E8. All control lines, screen invert, cursor mix/invert, extra blink, and extra invert are tied to the video decoder as address bits A4 through A7.

Address A3 is the extra blink clock input.

3.9 Alpha/Graphics Switching

The alpha board is used in conjunction with a MK3 motherboard to display the character video. In normal operation of a MK3 motherboard and an alpha board, the sync signals from the motherboard must be routed from output to input when display graphics (E23 - DIP1).

Pin number 6 of the dip header, provides the ALPHA/GRAPHIC control to switch multiplex E15 (74LS157) from motherboard sync to alpha board sync and video during alpha operation.

TABLE OF CONTENTS

1.0 INTRODUCTION

This document is a summary of board addressing and register function. Further detail is available from reference 1.

The Memory Extension board provides its host system with increased memory and I/O capability. The host system has control over all board operations; the status/control register pair allows the host to direct certain operations and have access to board status.

I/O ability is provided by two serial ports. Port 2 can operate a RS232C serial line or a tape interface. The RS232C line operated by port 1, is intended for console terminal hookup.

On board memory can be configured in different ways. Some boards (EPS) have 64K in the form of eight 8K byte pages, accessed from 8000 to 9FFF. Other boards (GPI) have two 8K pages, one (page 7) accessed from $8000 to 9FFF and the other (page 6) accessed from $A000 to BFFF.

Provision is made for use of up to 16K of EPROM on the board. The 16K region is divided into two 8K banks, each of which can contain four 2K chips.

2.0 MEMORY MAP

Board functions are memory mapped into four basic addressing regions including three 8K byte areas called RAM, ROM 0, ROM 1, and a 256 byte region for I/O. (See figure 1). The I/O region is typically from $EF00 to EFFF (hex). The RAM region is from $8000 to 9FFF, ROM 1 from $A000 to BFFF, and ROM 0 from $C000 to DFFF. Also, each ROM memory space can have an 8K page of RAM mapped over it; page 7 maps over ROM 0 and page 6 over ROM 1. Hardware switches determine whether the board will respond at all to memory requests in the regions ROM 0 and ROM 1, and if so, whether ROM or the appropriate page of RAM will be used. The programmer must know how the memory is configured.

1) NOTE: The control signal I/O is generated externally to the board, and forms part of the effective serial I/O port, and register addresses. Typically, it is generated when address lines specify an address in the region $E800 to EFFF. Board hardware then selects the input/output region, $$EF00 to EFFF. (See ref. 1).

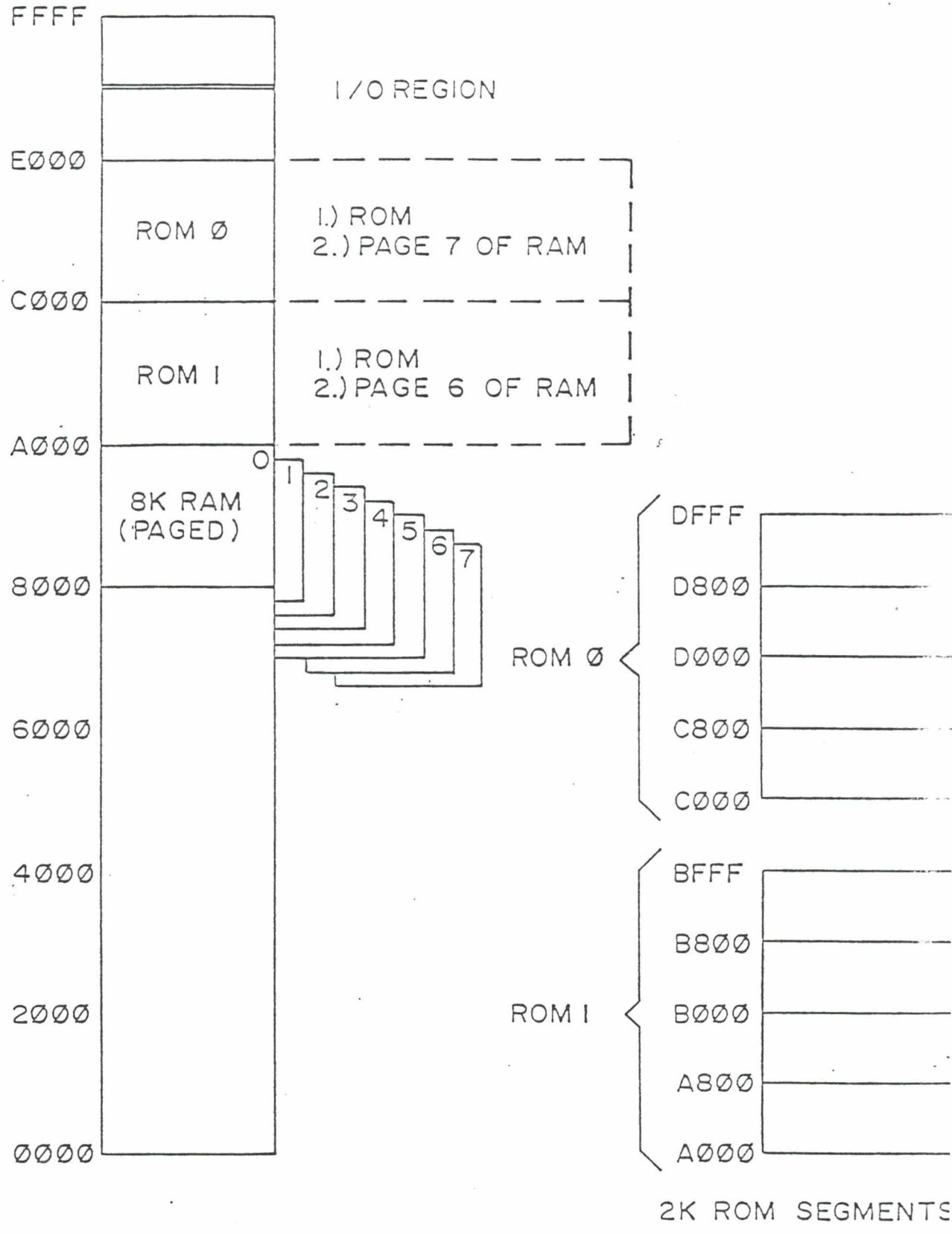

FIGURE 1 = MEMORY MAP

DATA LINE	READ REGISTER STATUS OUTPUTS	WRITE REGISTER CONTROL INPUTS
D7	SW1	NOT USED
D6	SW2	NOT USED
D5	SW3	DTR2 - Data terminal ready for serial port 2.
D4	SW4	DTR1 - Data terminal ready for port 1.
D3	0	TAPE - Logic 1 enables tape inputs to serial port 2.
D2	DTR2	PG2 - RAM page address
D1	DTR1	PG1-- RAM page address
D0	TAPE	PG0 - RAM page address

TABLE 1: Bit representations of status and control registers.

REGION 0
$C000 to DFFF

Switch 1	Switch 2	Memory Configuration
0	X	No Memory response
1	0	ROM (Usually EPROM)
1	1	RAM Page 7

REGION 1
$A000 to BFFF

Switch 1	Switch 2	Memory Configuration
0	X	No Memory resp
1	0	ROM (Usually E
1	1	RAM Page 6

Logic 0 - Switch closed

Logic 1 - Switch open

X - Does not matter

TABLE 2: Switch setting for configuring memory

3.0 STATUS/CONTROL REGISTERS

Both the status and control registers are accessed at $EFC0. A read operation to this address accesses board status, while a write operation loads the control register. See table 1 for the bit representation of these registers.

In the read status register, D4 to D7 represent the status of the on board memory configuration switches. See table 2 for a summary of their function. Lines D2 and D1 represent serial interface modem control signals DTR2 and DTR1, both active low. The TAPE line at D0 indicates whether tape inputs or serial line inputs are supplied to serial port 2; if D0 is at a logic 1 level (high) tape inputs are being used.

Six board control signals can be written into and stored by the write register, including DTR1, DTR2, TAPE, and a three bit RAM page address, PG0, PG1 and PG2.

The page address lines select a RAM page between 0 and 7, with PG 0 the low order bit and PG2 the high order bit. Changing these lines immediately changes the page accessed at addresses 8000 to 9FFF.

Note that DTR1, DTR2 and TAPE are written into and read from respective registers, on different data lines.

4.0 RAM

Data can be read from or written into the RAM area from $8000 to 9FFF with the write register providing the page address. Additionally, RAM pages can be mapped over ROM 0 and/or ROM 1 regions as described. In this case, the control register RAM page address is irrelevant. However, RAM pages 6 and 7 are still accessible from $8000 to 9FFF when the control register addresses them.

5.0 ROM

ROM memory can be accessed in either address block ROM 0 or ROM 1, both blocks, or not at all, depending on SW1 to SW4. Each 8K block is divided into 4, 2K segments. (See figure 1). When an 8K bank is enabled for use, single EPROM chips can occupy any or all segments.

6.0 I/O

The four registers of serial port 1 are control, status, data to transmit and data received.

The control register is accessed by a write operation to $EF40 and the status register by a read operation to that address. With address $EF41, a write operation will load the transmit data register, and a read operation will access the receive data register.

The same holds for serial port 2, using addresses $EF80 and $EF81. See table 3 for the serial port address summary. For details on the serial port registers (MC68A50 A.C.I.A. chip), consult reference 2.

ACIA REGISTER ADDRESSES	TYPICAL ADDRESS		OPERATION
	PORT 1	PORT 2	
RECEIVE DATA	$EF41	$EF81	READ
TRANSMIT DATA	$EF41	$EF81	WRITE
STATUS	$EF40	$EF80	READ
CONTROL	$EF40	$EF80	WRITE

TABLE 3: SERIAL PORT ADDRESS SUMMARY

7.0 · ADDRESS MAP SUMMARY

EFFF

I/O REGION

ADDRESS	FUNCTION
EFC0	BOARD CONTROL/STATUS
EF81	SERIAL PORT 2: TRANSMIT/RECEIVE DATA
EF80	PORT 2: CONTROL/STATUS
EF41	PORT 1: TRANSMIT/RECEIVE DATA
EF40	PORT 1: CONTROL/STATUS

EF00

UNUSED

E000

ROM 0

ROM, page 7 of RAM, or no board response according to switches 1,2.

C000

ROM 1

ROM, page 6 of RAM, or no board response according to switches 3,4.

A000

RAM

Eight 8k pages of RAM. Write register contents provide page address.

8000

NOTE: Above register pairs are write accessed/read accessed.

8.0 REFERENCES

1. D3832. MEX 3 Theory of Operation Manual

2. The complete Motorola Microcomputer Data Library page 1-211.

3. D3831. MEX Logic Sheets

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The ROM memory contains the character shapes as bit mapped storage. Two ROMs are utilized to provide two complete character sets (E30 and E31). The signal, ALT CHAR SET, selects which of the 2K eproms is used for display.

Data from the RAM storage is latched in E29 (74LS374) before becoming an address into the eproms. Seven address bits are taken from RAM (A4 to A10) to select the character, while four o the bits come direct from the CRTC, row address 0 through 3 (RA 0-3) to become A0 through A3 of the ROMs. These latter four bits select the byte row within character.

Storage wise, each character looks like:

		7	6	5	4	3	2	1	0
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There are 16 bytes of data for each character, which is selected by RA0-3.

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	6	1	0	0	0	0	0	1	0
	7	1	0	0	0	0	0	1	0
	8	1	0	0	0	0	0	1	0
	9	0	0	0	0	0	0	0	0
	10	0	0	0	0	0	0	0	0
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3.3 Bus Buffers

As mentioned previously, the alpha board connects to a 50 conductor microprocessor bus. Address, data and control lines are all buffered to provide maximum isolation and minimum loading of this module on the bus.

The control lines which consist of E, R/W, RESET L and I/O are all buffered through a 74LS367 (E32).

Address lines A8 through A15 and A0 through A7 are buffered by 74LS244's, octal receiver/drivers, in E25 and E24 respectively.

The data lines, D0 through D7 are buffered through two transceivers, E27 and E26 (74LS245 - octal transceivers). E26 buffers data to and from the data bus connecting the CRTC (6845) and the PIA to the micro bus. The second transceiver, E27, buffers data to and from the static rams. This is necessary as the static rams are being continually read by the CRTC for refresh and bus contention problems would occur.

3.4 Address Decoding

Addressing of the two devices, the CRTC (6845) and the PIA (6821) as well as the ram storage are all handled by several I.C.'s.

The upper four address bits A12 to A15 are decoded by E36 pin 6 (74LS21) as $EXXX. This signal, with A11L is anded in E34 pin 6/E35 pin 12 to form $E000 to $E7FF, or otherwise known as MICRO to decode ram accesses. During a write cycle to static ram, E33 (74LS10) nands E and R/W with MICRO to generate WL (E33 pin 8) which is the write pulse used. Also during ram accesses, the transceiver E27 is enabled by E33 pin 12 as a result of $E000 - E7FF and E being true. Direction of E27 is controlled by R/W only.

The CRTC and PIA are decoded in the I/O segment of the microprocessor's address space, which is $E800 to $EFFF. The PIA is mapped as $EE80 and the CRTC as $EEC0. I.C. E36 pin 8 decodes address space $EEXX which is used as an enable for transceiver E26 via E34 (74LS00), and also as an input to E33 pin 3 (74S10) with A7 and A6 to generate $EEC0 for E17 pin 25. This signal at E36 pin 8 is also directly used to control CS0 on the PIA. The PIA (E16) also decodes CS1, CS2, RS1 and RS0 inputs to select addresses $EE80-3 with A7, A6, A1 and A0.

3.5 Master Clock

Clock generation on the alpha board comes from one source which is a TTL crystal oscillator (E4 -7400, XTL1 - 14.318Mhz). The clock is buffered through E4 pin 8 to be used as DOT CLK and divided by eight by E5 (74LS393) to generate the CHAR CLK (1.789 Mhz).

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The PIA or parallel interface (E16) is used primarily as an output control device on the video display. Several options are available on the video display that allow the user under program control to set:

a) ALT CHAR SET - alternate character set
bit 7 0 - standard
1 - alternate

b) CURSOR MIX/INV - cursor mixing with video or inverting the video
bit 6 0 - mix
1 - invert

c) EXTRA BLINK - blinking video on ASCII characters above $F7
bit 5 0 - no blink
1 - blank

d) EXTRA INV - inverting video or ASCII characters above $7F
bit 4 0 - no invert
1 - invert

Bits 0 to 3 on the A side of the PIA are unused and are pulled high so that they may be used as inputs. Inputs CA1 and CA2 are tied to D15P EN and VS respectively, allowing interrupts to be generated on horizontal or vertical sync pulses from the video generator. (For hidden writing as mentioned before).

The PIA B side is used exclusively as inputs set by switches 1 to 8. Ideally the switches are read by the microprocessor and conditionally set video control bits in the A side. Switch 1 is read as well as hard wired to the screen invert control line. Signals CB1 and DB2 are pulled up as before.

3.7 Blink Clock

When the EXTRA BLINK control is used for video display, it enables the BLINK CLK L signal which is generated by E6 (74LS390). The duty cycle of E6 pin 9 is 1 second on, 0.5 seconds off.

3.8 Video

Data from the character ROM's is loaded into E22 (74LS166) 8 bit shift register, by a load pulse from E14 (74LS74). The character clock, CHAR CLK, sets E14 pin 8 low on its rising edge and is reset when E14 pin 5 ripples through and clears E14 pin 8. Shift register load pulse E22 pin 15, remains for one DOT CLK time.

Video is shifted out of the shift register at a rate of 14Mhz to the decoder rom E8 to the A0 input. Data bit D7 from the ram output latch passes through E7 (74LS174), to delay by one character time, to become the A1 input of E8.

The cursor and blanking (DISP EN) signals each must be delayed by two character times to achieve synchronism with the video before becoming A2 and A8 respectively of decoder E8. All control lines, screen invert, cursor mix/invert, extra blink, and extra invert are tied to the video decoder as address bits A4 through A7.

Address A3 is the extra blink clock input.

3.9 Alpha/Graphics Switching

The alpha board is used in conjunction with a MK3 motherboard to display the character video. In normal operation of a MK3 motherboard and an alpha board, the sync signals from the motherboard must be routed from output to input when display graphics (E23 - DIP1).

Pin number 6 of the dip header, provides the ALPHA/GRAPHIC control to switch multiplex E15 (74LS157) from motherboard sync to alpha board sync and video during alpha operation.

Table of Contents

1.0 Introduction

The Telidon MK3 Motherboard Module is designed as a fixed format, full function Telidon (PDI) terminal.

The major feature of the board is its memory mapped video display which is interfaced to a programmable CRT controller. This makes for a simpler, more cost-effective design.

2.0 General

The motherboard module contains several basic blocks which include:

a) microprocessor
b) CRT controller
c) video memory
d) program memory
e) serial interface
f) parallel interface

Refer to figure 1 for a block view of the system.

All components are based around a simple microprocessor bus which includes data, address and control lines. Data transfers occur on this bus under control of the microprocessor.

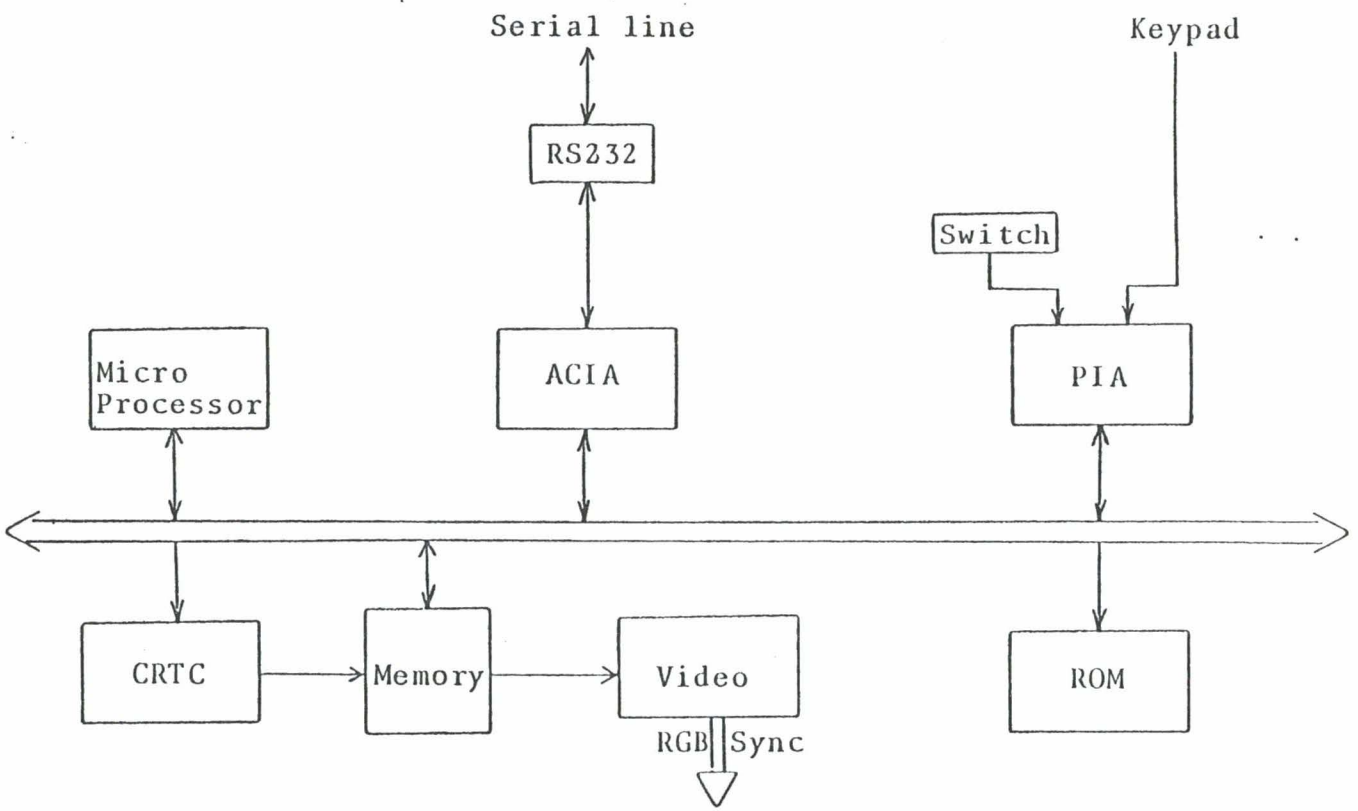


Figure 1 MK3 Motherboard Block Diagram

3.0 Microprocessor Operation

3.1 General MC6809

The microprocessor used on this module is the Motorola MC68A09 (U6G). All output and bidirectional lines of the 6809 are buffered for connections external to this motherboard. Internally there is very little buffering used as the micro has its own buffers and the bus itself is fairly limited.

The control lines BA, BS, E, Q, and R/W are all buffered via U6P (74LS367). Tri-state control of R/W is taken from the bus available signal (BA). These outputs are used both on board and off board.

Address lines A0 through A15 are buffered off board via U5R and U6R (74LS244). These devices will go tri-state releasing the external bus during DMA or SYNC operations, again via the BA signal.

Data lines D0 through D7, being bi-directional, are interfaced to the external bus via a transceiver, U4S (74LS245). Its direction is controlled via the R/W signal and enabled by a decoding ROM (U5N).

Inputs to the 6809 are open collector. NMI, FIRQ, IRQ, HALT and DMAREQ are all pull high via 4.7K ohm resistors (U8G). The RESET input is controlled by the reset circuitry, which will be explained later. The MRDY signal, which is required for slow memories, is not used and is also pulled high.

Clocking of the uprocessor is a TTL clock at four times the bus frequency going into the EXTAL input. TTL operation is selected by XTAL (pin 39) being grounded.

3.2 Reset

There are two provisions for resetting the 6809 microcomputer. Both a power up reset and a manual reset are available.

The power up reset is initiated by a power fail or start up operation. At time zero, when power is applied, capacitor C2 is at zero volts and therefore Q3 (PNP) is

turned on. This keeps Q1 (NPN) from turning on and consequently R17 holds the RESET line at a low condition. Over time, leakage current in the base-emitter junction of Q3 charges up C2, an eventually Q3 turns off. Transistor Q1 turns on and holds the RESET line high. Diode D1 discharges C2 when the power is removed from the circuit.

Manual reset is provided via an external D.I.P. header (DIP 2) which, if pins 2 or 15 are grounded, causes a uprocessor bus reset.

3.3 Interrupt Sources

Various types of interrupts are supported by the 6809; IRQ, FIRQ, and NMI. Externally, all three interrupt types are supported, whereas internally only IRQ is utilized.

On the motherboard, all I/O devices are wired to IRQ line.

3.4 Memory Map

The MK3 motherboard has RAM, ROM and I/O components as part of its memory configuration. Figure 2 shows the memory map of the MK3.

On board, the address map breaks down to several signals

a) ROM0
b) ROM1
c) EPROM
d) BDIO
e) VRAM

With the exception of VRAM, all decoded signals are generated by U5N and U4N which are decoder ROMs. Inputs to the ROMs include A11 to A15, E, R/W and two jumpers, SW7 and SW8.

Decoder ROM number one, Norpak D3488-1, generates the ROM chip select signals ROM0 L, ROM1 L, and EPROM L. See figure 3 for the boolean equations used. The second address decoder, Norpak D3488-2, generates the enable control for U4S, the data bus transceiver, and the two I/O signals BDIO and I/O. Again see figure 3 for the boolean equations.

Jumpers SW7 and SW8 are used for controlling whether ROM0 and ROM1 are on board or off board:

SW7	SW8	ROM 1	ROM 0
0	0	off board	off board
0	1	on board	off board
1	0	on board	6K on board 2K off board
1	1	on board	on board

The normal positions for SW7 and SW8 are out (1) and in (0) respectively.

Device enable for the CRT controller is taken from BDIO signal and addresses A7 and A8 to generate CRTC L (U2S-12).

Decoding of RAM is not taken from the decoding ROMs but directly from the microbus. The signal VRAM (U3S-3) is the RAM memory enable.

Figure 2

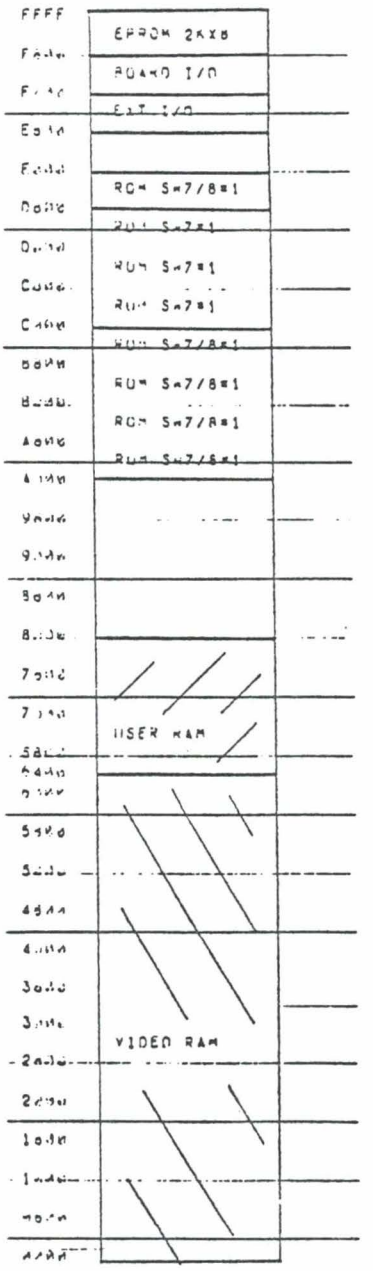


FIGURE-2 MEMORY MAP

$$\text{ROM 0 L} = \overline{\text{E.R/W.A15.A14.}\overline{\text{A13}}.(((\overline{\text{A12}} + \text{A12}.\overline{\text{A11}}).\text{S7}) + (\text{A12.A11.S7.S8}))}$$

$$\text{ROM 1 L} = \overline{\text{E.R/W.A15.}\overline{\text{A14}}.\text{A13}.(.\text{S7} + \overline{\text{S7}}.\text{S8})}$$

$$\text{EPROM L} = \overline{\text{E.R/W.A15.A14.A13.A12.A11}}$$

$$\text{BDI 0,} = \text{A15.A14.A13.A12.}\overline{\text{A11}}$$

$$\text{I/O} = \text{A15.A14.A13.}\overline{\text{A12}}\text{.A11}$$

$$\text{EN L} = \text{E.A15.}\left[\begin{array}{l}(\overline{\text{A14}}.\overline{\text{A13}}) \\ (\overline{\text{A14}}.\overline{\text{A13}}.\overline{\text{S7}}.\overline{\text{S8}}) \\ (\text{A14}.\overline{\text{A13}}\ (\overline{\text{A12}} + \text{A12}.\overline{\text{A11}}).\overline{\text{S7}}) \\ (\text{A14}.\overline{\text{A13}}.\text{A12.A11(S7} + \text{S7.S8})) \\ (\text{A14.A13.A12})\end{array}\right]$$

$$\text{CRTC L} = \overline{\text{A15.A14.A14.A12.}\overline{\text{A11}}\text{.A8.A7}}$$

Figure 3 Boolean Equations

3.5 Serial Interface

The bulk of the serial interface is formed with a baud rate generator, an ACIA (asynchronous communications interface adaptor) and EIA RS-232-C buffers.

Buad rates are generated by U6B which has crystal XTL2 and resistor R20 to form its tank circuit. The primary frequency, 1.8432 Mhz, is prescaled internally, as selected by the A and B inputs, to generate 16 times the baud clock rate. Baud rates available are 75 through 9600 baud. Two jumpers are provided for selecting receive and transmit baud rates. The jumpers (SW9 and SW10) connect directly to pins 3 and 4 of U7B, the ACIA.

Primary serial channel signals are produced and received as TTL levels by U7B. Received are RX DATA L, CTS L and DCD L. Transmitted are TX DATA L and RTS L. Secondary channel signals supported are SRTS (EIA-SCA) and SDCD (EIA-SCF), both of which are interfaced to a separate device (PIA).

Output signals TX DATA L, RTS L, DTR, and SRTS are buffered by U9A and U8A (1488) to produce RS-232-C levels, and are connected to P2 and DIP3. This allows for two seperate physical connections of the serial interface. Connector P2 is the standard 25 pin D subminiature plug, whereas DIP3 is a 16 pin socket for interfacing to a teletext or modem module.

Input signals from the two connectors, P2 and DIP3, are buffered by U10C and U9C respectively (1489). These signals are multiplexed by U8C (74LS157) before connecting to the ACIA. Pin 1 of U8C is a program controlled select pin from the PIA (U7G).

The two signals, RX DATA 1 and TX DATA L also connect to DIP2, pins 3/14 and 4/13 respectively, where they may be displayed using external lamp drivers.

ACIA interrupts are done on the IRQ line.

3.6 Parallel Interface

The keypad/keyboard interface is through connector P1 or DIP4 to this parallel interface.

External connections are done via P1 which provides current limited power sources of three voltages +5, +12 and -12 volts. There are 8 data lines A0 through A7 and a strobe line which connect to the PIA (U7G).

The 16 pin socket, DIP4, provides an internal connection for a wireless keypad receiver. Both it and the external keypad/keyboard are wired in parallel. Therefore dual use of internal and external keypads requires that those devices tri-state this mini-bus (A0 to A7 plus STROBE) as all bits are inputs.

The CA2 input on the PIA is used as the strobe input when a key is depressed (asserted low). On the A side of the PIA, the CA1 input (U7G pin 40) is connected to the VS or vertical strobe of the video generator to provide an interrupt source at a rate of 60 Hz. This is used for timing for such instructions as WAIT PDI's.

The B side of the PIA has both inputs and outputs that are used. Bits B0 through B2 are inputs and are used for parity selecting of the ACIA and for default character size selection (ie. RGB or RF operation).

Bit 3 is used as the control select for U8C (74LS157), which can be forced to ground by SW4.

The next bit, B4, is used as a control bit for the video circuitry. It selects an optional RGB decode set and signals, via DIP 5, that an external device may switch its video in to the MK3 module. (This will be explained in further detail).

Bit 5 is the audio transducer control and it must be toggled in order for TD1 (transducer) to emit sound. Transistor Q4 provides the drive current needed for proper operation.

A modem control signal called OH, or dial pulse according to its function, is controlled via bit 6. Its purpose is to provide the dialing pulsing sequencing required for auto dial a telephone line.

Data terminal ready (DTR) and TV control are both provided by bit 7 of the PIA. DTR is buffered through U9A to the RS232 connections whereas TV is passed through a TTL driver U10N to a BNC connector.

Signals CB1 and CB2 are SDCD and SRTS respectively and are used exclusively in half duplex terminal operation. Secondary data carrier detect (SDCD) is selected via U8C and buffered by U10C. The secondary request to send (SRTS) is buffered out via U9A.

Both interrupt lines IRQA and IRQB, A and B side interrupts respectively, are tied to IRQ.

4.0 CRT Controller

The heart of the video refresh display memory is a Motorola MC68A45 (U5G). There are two sets of signals generated that provide most of the logic control of the display. One set is the video timing signals: horizontal sync, vertical sync and display enable or blanking as its is usually called. The second set of signals are the RAM addresses for video refresh.

The key to the memory mapped operation of the display is the clocking of the 6845 with respect to the uprocessor. All bus timing is based on E; whereas the 6845 clock is inverted E (U4A pin 10). In this way the uprocessor and CRT operations are interleaved and memory is addressable from both devices.

It is also possible to external sync the video, which will be discussed later.

The video controller is interfaced to the microprocessor bus via 8 data lines, control lines R/W, E and chip select which CRTC L (U2S pin 12). Device reset is accomplished via the bus reset line.

Pin 3 is an unused input and is grounded.

4.1 RAM Memory

The microprocessor memory is composed of 16 chips of 16,384 bits each (U1A to U1S). Memory is divided into 2 sections; program memory and display memory. Video requires a display of 256 x 200 x 4 bits, which is a total of 25.6 kilobytes. The remaining 6.4 Kilobytes is used as program memory making for a total of 32 kilobytes.

The total memory requirement is implemented in 16K dynamic RAMs (TMS4116). Timing signals for the RAMs is generated as three separate sections:

a) address
b) clocks
c) data

4.1.1 Address -

Addressing of memory requires a total of 15 bits of both microprocessor address and refresh address. The microprocessor address comes directly from the internal address bus of the board. Refresh addresses, as mentioned are produced by the CRT controller, U5G. The upper 14 bits of address are multiplexed by U3E, U4E, U3G, and U4G (74LS257) to form a 7 bit multiplexed address bus to the RAMs. Signals are connected to the memory through series line terminations resistors (U2G).

4.1.2 Control -

Control timing for the memory is derived on sheet 2 of the logic diagram. Refer to figure 4 for the timing diagram.

From the microprocessor, address lines are true at the rising edge of Q, while data lines for a write cycle are true at the trailing edge of Q. All timing is done with respect to the E and Q edges.

Processor memory cycles occur with E while video cycles occur with E L. The signal E exor Q (exclusive or) going false generates the start of all memory cycles. Just prior to this happening, U3A pin 8 is high (1). With the rising edge of E, U3A pin 8 goes low. This presets U3C pin 6 low (0), which is a 74LS74. This generates RAS L directly as well as starting a delay chain composed of U2C (7404).

After 3 dealy times through U2C, the CASMUX signal is generated and after 1 more delay, CASMUX L is generated. These two signals switch U3G and U4G off slightly before U3E and U4E are switched on, thus forming the multiplexing action of row address to column address. Two gate delays later, U2C pin 6 generates CAST L which is either passed through U3E or U3G to form CAS L. This extra delay ensures the address lines are stable for the CAS clock.

Mid-way through the E cycle, the E exor Q signal goes true removing the preset from U3C pin 4. Additionally this signal clocks U3C pin high and U3C pin 8 low. After the six gate delays of U4C (approximately 50 - 60 ns). U3C pin 13 is reset, causing pin 8 to go high. During this period U3C pin 9, (LATCH) which was high, is either a read latch signal or a write pulse.

As U3C pin 8 goes it clocks U3C pin 6 high, terminating RAS L and eventually CASMUX, CASMUX L, and CAST L after the delays through U2C.

The RAMs are divided into 2 banks where bank 1, U1A through U1H, is all the even addresses (A0 = 0) and bank 2, U1J through U1S, is all th odd addresses (A0 = 1). Write enables to the memory are derived from LATCH and R/W L (write operation) and A0 or A0 L with VRAM. This generates a write pulse to either the first or second bank.

4.1.3 Data -

During a read cycle by the microprocessor the LATCH signal and E (U4A pin 11) latch the data into U2J and U2L (74LS373). Selection of VRAM and A0 to A0 L enable either of the data latches (U2J or U2L) via U2A pin 6 or 3, through to the data buffers U4J and U4L (8T28).

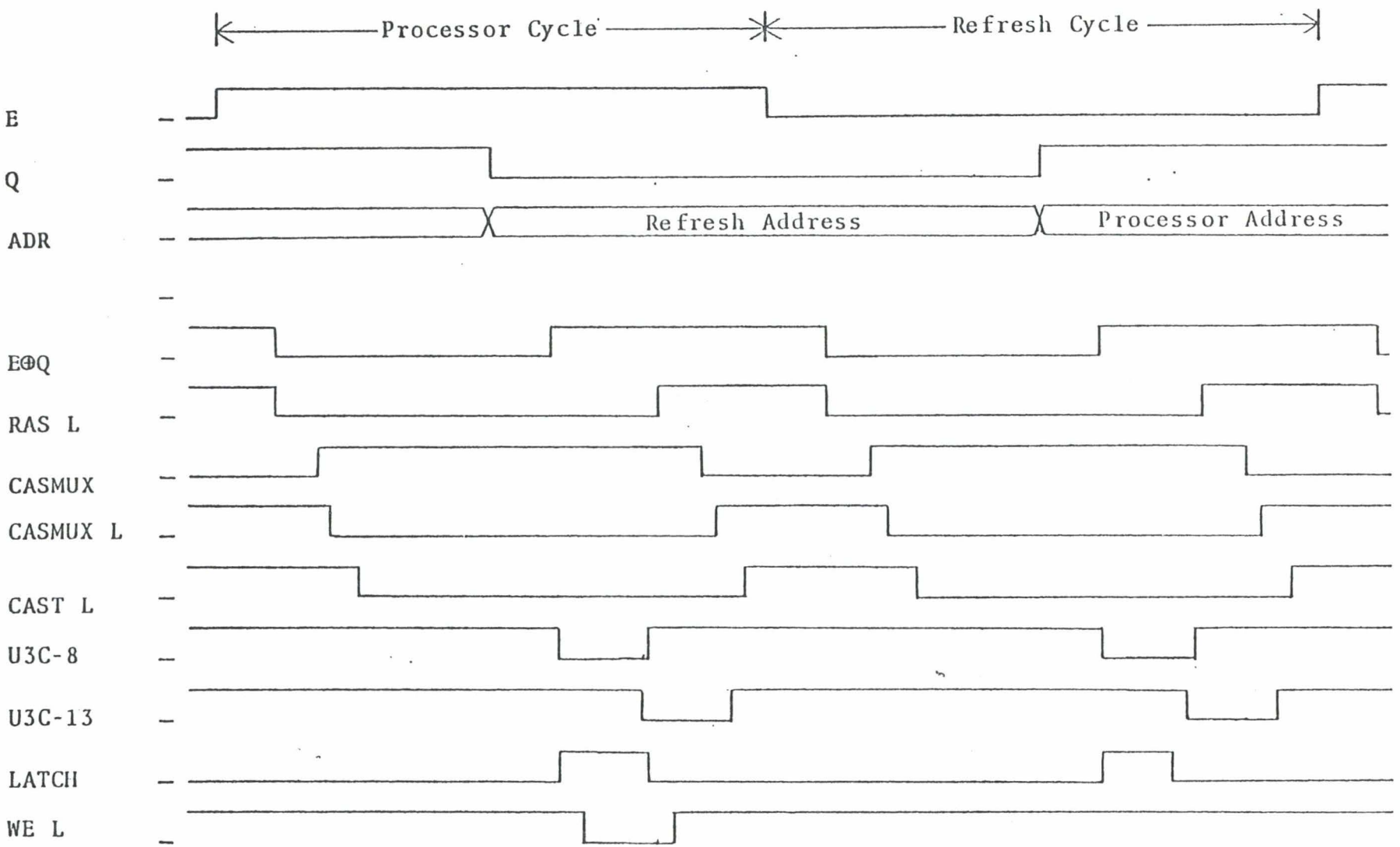


Figure 4 Memory Timing Diagram

5.0 Video

When video refresh is occuring, a CRTC read (E L), the latch signal clocks data into the pair of video latches. U3J and U3L (74LS373). Each cycle clocks 16 bits out, which is actually 4 pixels on the video display.

Data bits from memory are broken down into video pixels in the following manner

Word 0		Word 1	
Pixel	Pixel	Pixel	Pixel
V15	V11	V07	V03
V14	V10	V06	V02
V13	V09	V05	V01
V12	V08	V04	V00

-------- time --------->

Every four data bits a pixel is displayed. This is done in the shift registers U2A, U2N, U3D and U3N. Prior to the start of a new video cycle the data from the '373's is loaded into the 74LS166 shift registers (on the falling edge of E). Data continues to be clocked out the registers at the pixel clock rate (4b x E).

The local signal is generated from E L clocking U7N pin 6 low, resetting U7P pin 5 which in turn resets U7N and clocks U7N pin 11.

The display enable signal (video blanking) is delayed by a total of 8 pixel times by clocking U7J with E L. The final blanking control is clocked by the shift register load pulse, so that both video and blanking signals are clocking on the same edge before being decoded.

5.1 RGB Decode

RGB decoding takes place in two decoding ROMs U8L and U9L. Inputs to these decoders is from the 4 video bit streams, blanking, blink clock (BLINK L) and the ALPHA/GRAPH control. The ROMs decode the video into 4 bits of DAC level and 4 bits of gun control.

The video decoding is composed of:

C/G	G	R	B	
0	0	0	0	grey 0 (black)
0	0	0	1	grey 1
0	0	1	0	grey 2
0	0	1	1	grey 3
0	1	0	0	grey 4
0	1	0	1	grey 5
0	1	1	0	grey 6
0	1	1	1	grey 7 (white)
1	0	0	0	transparent
1	0	0	1	blue
1	0	1	0	red
1	0	1	1	violet
1	1	0	0	green
1	1	0	1	cyan
1	1	1	0	yellow
1	1	1	1	blinking white

In colour mode, a single digital to analog converter (DAC) is used to full level (U8N), its output amplified by Q5 and Q6. This preset video level at R57, is fed via R58, R59 and R60 to gun controls for red, green and blue respectively (U10N – 74L03).

These gun controls are either off or on driving transistors Q7 to Q9 to the proper levels; to black level when off and to full level when on.

When used in grey scale mode, all three colour gun controls are turned on, and the level of the DAC determines the video level. In this way, the colours either are on full or off or follow the DAC level. It is worth noting that the blanking level during video sync is done in the DAC.

Each of the transistor drives is capable of driving a 75 ohm load.

The transparent output control is direct from U9L pin 12 to its drive transistor Q10 which drives a TTL level output to a BNC connector.

6.0 Master Clock

The master clock of the MK3 motherboard is a simple TTL oscillator compsed of a pair of 7400 gates and a crystal (U7S and XTLL). Oscillator output (U7S pin 6) is nanded with the internal clock enable switch, SW6, for use in an external clock mode of operation. Additionally the clock passes through U7S pin 12 where the external clock may be input.

If no external clock is used, SW6 is open and the internal clock operates properly. When external clocking is used off and on, the EXT signal as well as EXT CLK must both be high when switching back to the internal clock.

The clock which is at test point TP1 clocks U7P pin 11, dividing the clock by two to produce the pixel clock (approximately 5.366 Mhz).

7.0 External Sync

The MK3 motherboard may be operated in an external sync mode of operation. This is done by means of an external phase locked loop (PLL) to drive the clock circuit on the board. As mentioned previously, the board master clock may reside off board by means of connector DIP 1 (logic sheet 1-D7). Refer to figure 5a.

For driving the PLL, the horizontal sync output from the 6845 (U5G) is provided at DIP 1. The external video signal must have its horizontal and vertical sync information separated. The external horizontal sync along with the MK3's horizontal sync are used to drive a PLL and generate the master clock EXT CLK L. This will lock the horizontal sync together but not vertical.

Vertical sync from U5G pin 40 clocks U2E pin 8 low at the end of sync, resetting U2E pin 5 which in turn resets U2E pin 8 to a one. Pin 5 of U2E is the clock enable to the 6845, and it will therefore stop the clock until VSYNC L arrives from the external device. In this manner external sync operation is utilized. Refer to figure 5b for timing diagram.

Resistor R76 is important for internal sync operation as it keeps U2E pin 5 high as power rises during a power up sequence. This prevents U2E from getting into a locked state where no VSYNC L will ever come, and the clock to the 6845 is blocked.

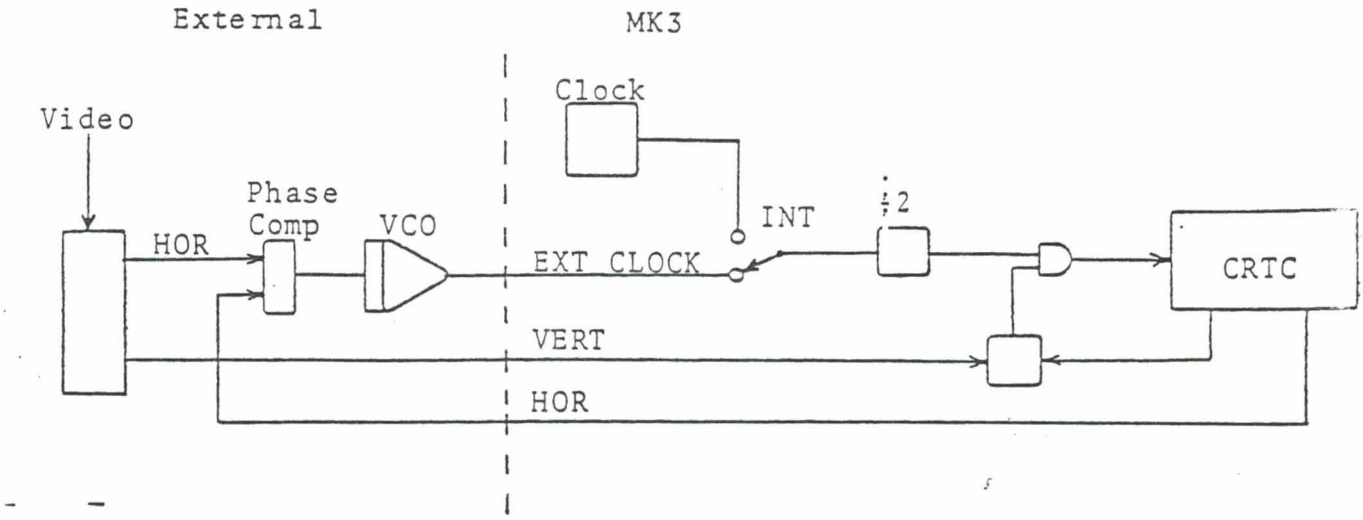


Figure 5a External Sync Operation - Block Diagram

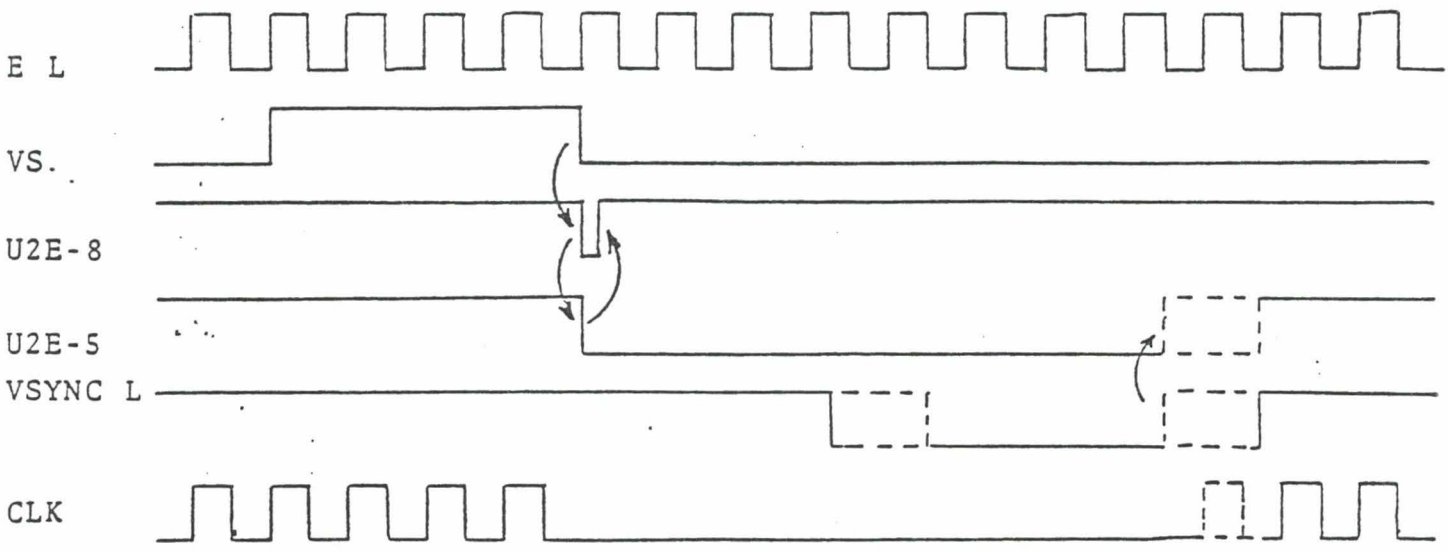


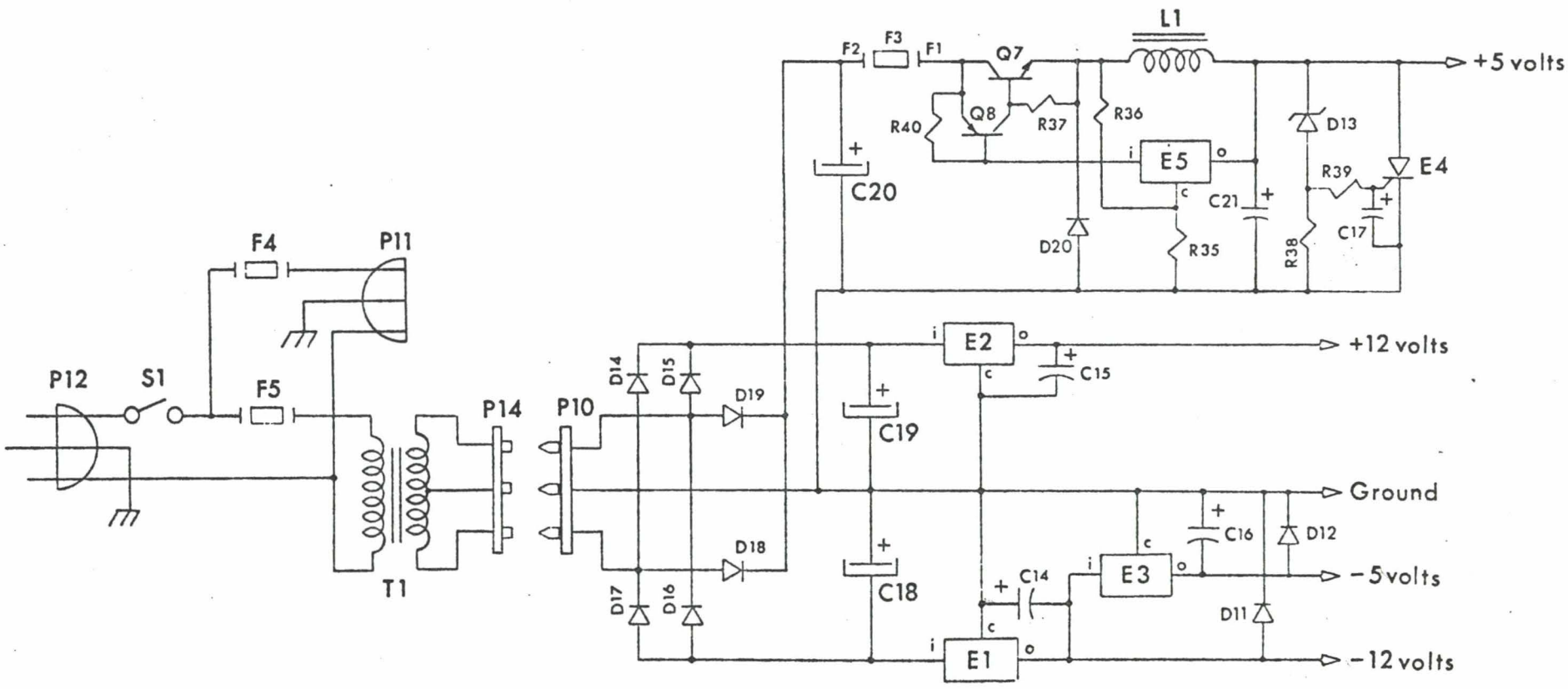
Figure 5b External Sync Operation - Timing Diagram

8.0 Alpha Generator (Optional)

Optional an alphanumeric generator board can be connected to the MK3 motherboard to provide a monochrome 80x24 character display. This is done via DIP5 (logic diagram sheet 5).

The alpha board, when used, must provide its own horizontal and vertical sync as well as video. In order to switch sync sources from on board to off board, the VS in and out jumper S12 and HS in and out jumper, S13, must be cut (at U9J). Externally, the alpha board monitors the ALPHA/GRAPHIC signal. Normally, being low it indicates graphics operation, which is on board along with horizontal/vertical sync. The alpha board routes the motherboard sync signals VS and HS back into the DIP 5 header.

When switched to alpha operation, ALPHA/GRAPHICS high, the alpha module should switch syncs and provide video to DIP 5 pin 8. The ALPHA/GRAPHIC bit will also select a new RGB decoding set in U8L and U9L, which sets the DAC on full and all three gun controls on (U10N).



norpak	NKB4 Power Supply	DR'N BY JG	SCALE
		CH'D BY CRT	DWG. No. D-105 8-1