TABLE OF CONTENTS

1.0 INTRODUCTION

The board is an independent Memory Expansion module with input/output capability.

Main features include:

(1) good flexibility in user selection of memory type and configuration including 64K RAM and provision for additional ROM.

(2) two programmable RS232 serial I/O interfaces.

(3) tape I/O via one of the two serial parts, including FSK coding/decoding, and drive control circuitry.

2.0 GENERAL

2.1 Block Diagram

The board is made up of six main blocks:

a) ROM
b) RAM
c) ACIA 1 (Serial Interface 1)
d) ACIA 2 (Serial Interface 2)
e) TAPE
f) REGISTERS

Refer to figure 1 for block diagram.

The externally controlled bus includes 16 address, 8 data and 8 control lines. All main blocks are bus controlled except "TAPE" which is dependent on ACIA 2 and write register contents.

Standard RS232 lines are available from each serial port. One of the ports also provides tape interface and tape drive control, but will not operate simultaneously in RS232 and tape modes.

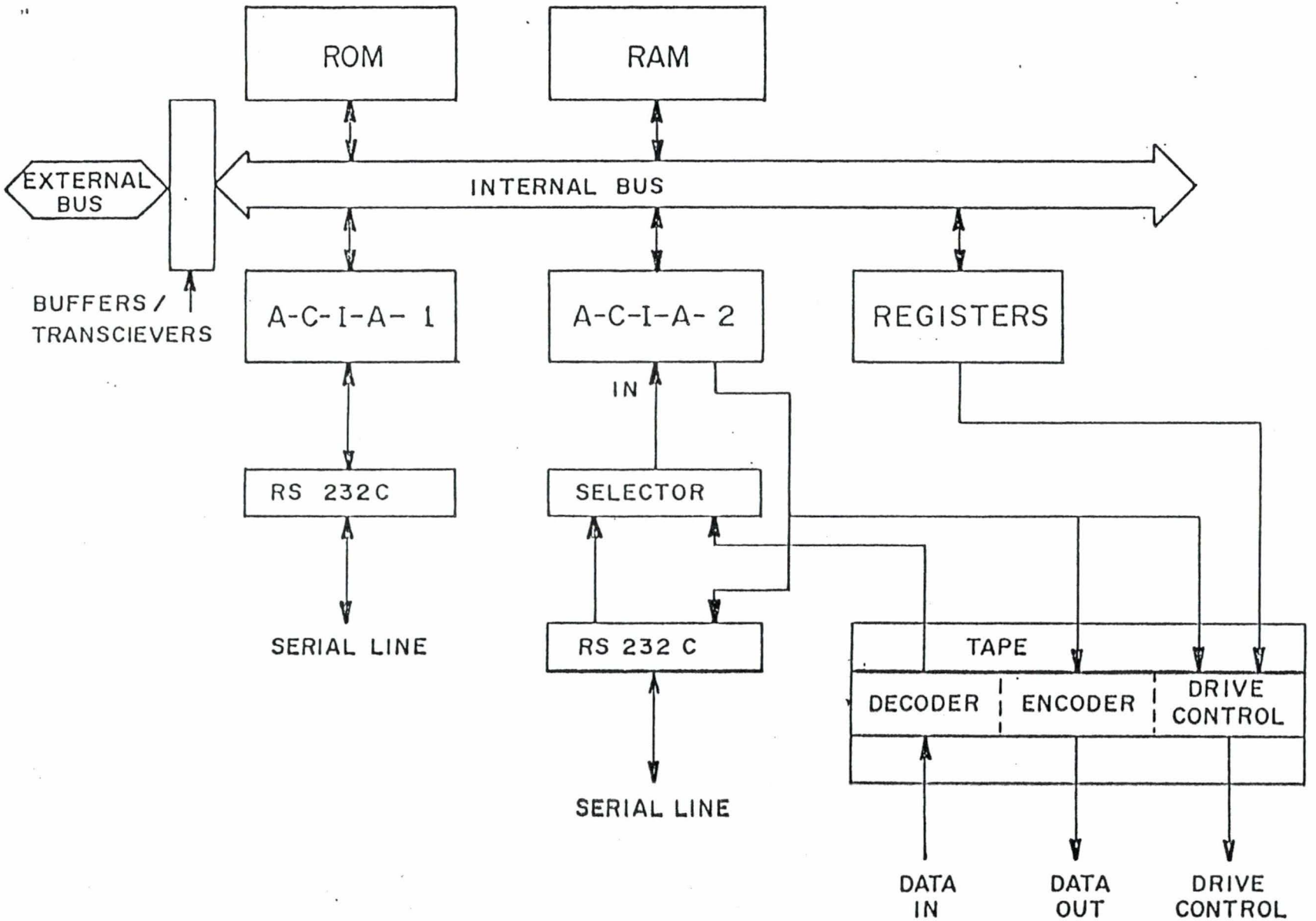

FIGURE I : BLOCK DIAGRAM OF BOARD.

2.2 Memory Configuration

Access to RAM, ROM and board I/O is memory mapped so that address bus decoding enables memory, register or I/O function.

The address map has four basic areas; three 8K byte regions and a 256 byte input/output space. Eight 8K byte pages of RAM occupy the address area $8000 to $9FFF (hex), with write register contents forming the page address, 0 to 7. See figure 2.

The second 8K region (called 1), $A000 to $BFFF, can be occupied by ROM or by page 6 of RAM. The region 0, C000 to DFFF, is used the same way, except that page 7 of RAM can be overlaid. RAM pages 6 or 7 are addressable in the paged region when also enabled over respective regions 1 and 0.

Ports and registers are accessed in the 256 byte block from $EF00 to $EFFF. This address block is subdivided, giving access to serial port one from $EF40 to EF7F, serial port 2 from EF80 to EFBF, and the registers from EFC0 to EFFF.

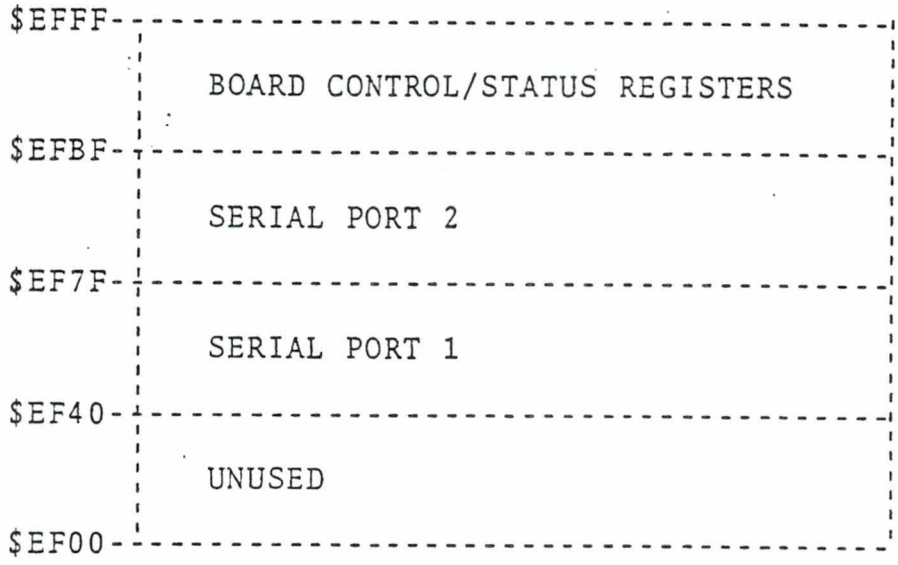

FIGURE 3: Serial Port and register address blocks, within t the I/O region (fig.2).

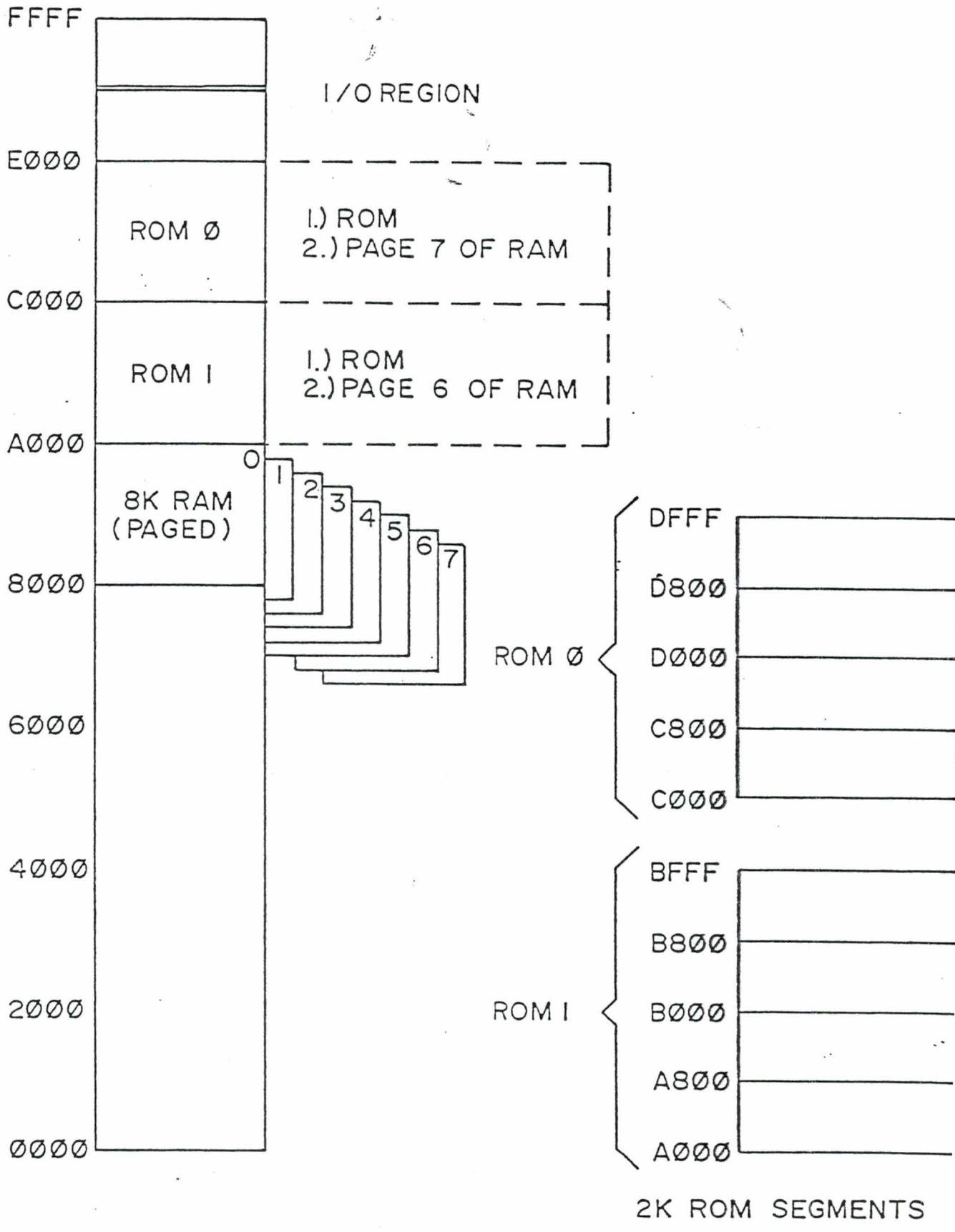

FIGURE 2 = MEMORY MAP

3.0 MEMORY OPERATION

3.1 General

Board RAM is implemented in two basic ways:

1) 64K bytes in eight 8K pages, with optional mapping pages 6 and 7 over regions 1 and 0 respectively.

2) 16K bytes of RAM. One 16K bank of RAM chips is used, giving pages 6 and 7. Page 7 is normally accessed in the paged region $8000 to 9FFF, and page 6 in region 1, $A000 to BFFF.

The following discussion of memory operation applies to either case.

Four on board switches determine:

(a) whether the board responds or not, to addresses in regions 0 and 1.

(b) whether ROM or RAM is used in areas 0 and 1.

When SW1 is left open, board response is allowed to addresses in region 0. If SW2 is closed, ROM must respond, and if open, RAM page 7 is mapped over the region. If SW3 is open, board response is enabled for region 1, with SW4 selecting use of ROM, or RAM page 6. See the switch truth tables in figure 4.

Address Region 0
C000 to DFFF

SW1	SW2	Board Response
1	0	ROM
1	1	RAM Page 7
0	X	NONE

Address Region 1
A000 to BFFF

SW3	SW4	Board Response
0	X	NONE
1	0	ROM
1	1	RAM Page 6

0 - Closed
1 - Open

FIGURE 4: Switch Truth Tables

3.2 Bus Interface

All board functions including memory access, are performed under external control. Address, data and control lines are connected to the host by a standard 50 pin edge connector. Address lines are buffered by 74LS244's at E69 and E70. The bi-directional data bus is interfaced through a tri-state transceiver, 74LS245 at E71, which enables or disables the bus connection under control of an enable signal, at pin 19.

The transciever enable signal is generated during all board operations, because the data bus is always used. Board operation is specified when either E66 pin 6 or 8 is low, E67 pin 12 is low, or E68 pin 6 is low; the significance of these signals is discussed later. The transciever enable signal is generated by logic at E68 and E86 when any one of these lines is low.

The transciever uses a control input, R/W, to specify the direction in which data flow has been enabled. R/W digh is a read from board operation and drives internal bus data onto the external bus. R/W low specifies a write onto board operation and drives data from the external bus onto the internal bus.

Control lines R/W, RESET L, I/O, E and Q are buffered by the 74LS367 at E65.

3.3 ROM

Each of two 8K byte ROM regions, 0 and 1, is implemented using 4, 2K byte chips; use of EPROM (erasable, programmable ROM) is intended but provision is made to use ROM. The signals ROM 0 L or ROM 1 L, enable one of two, 2 to 4 line decoders in the 74LS139 chip at E62. Address lines A11 and A12, inputs common to both decoders, select one of 4 chips in the enabled 8K byte region. Addressing within the selected 2K space is provided by eleven lines, A0 to A10, common to all chips. The data bus is common to all chips.

In order for ROM 0 L to be active, several signals are necessary. First, pin 6 of E66 must be driven low. This happens when SW1 is high (switch 1 open), A14 and A15 are high, and A13 is low. The status of these lines gives the effective enabling address block for the ROM 0 L signal, $C000 to DFFF.

The second set of signals necessary to generate ROM 0 L, are applied at E63. SW2 L must be high (switch 2 closed, enabling ROM), R/W must be high specifying a read operation, and E must be high to give correct signal timing. With these conditions met, ROM 0 L is generated at E63 pin 6.

In a ROM read operation addressed to region 0, ROM 0 L will be generated and a ROM chip will put data on the internal data bus. The data bus transciever will be enabled and since R/W is high, the transciever will gate internal bus data onto the external data bus.

Generation of ROM 1 L is similar, but switch three must be open, switch four must be closed and the effective address region is $A000 to BFFF. ROM 0 L and ROM 1 L will never be active simultaneously because of address bus decoding.

The printed circuit board is configured for use of TMS2716 Tri-supply EPROM chips, requiring +12V, +5V, -5V and ground at pins 19, 24, 21 and 12 respectively. MCM2716 EPROM or MCM68A316E ROM chips can be used, if proper cuts and jumpers are made on the board.

3.4 RAM

3.4.1 General -

RAM memory is arranged in 16K blocks, each of which uses eight TMS4116-15, 16K x 1 bit chips. The 16K address space requires 14 address lines. These lines are supplied as inputs to the address multiplexer at E58, whose seven output lines are common to all RAM chips on the board. Under control of external timing signals, the multiplexer sequentially puts A0 to A6, A7 to A13 and an internally counted refresh address on its output lines.

Data output lines from the 4116's are common to the 16K blocks, and are in the high impedance state except during data output. The 74LS373 D type transparent latch at E61 loads data line levels while enabled, and stores the levels when disabled. The eight latch outputs are split into 2,4 bit groups, one group going to each 8T28 (E60 and E59) tri-state transciever. The transcievers allow control of data bus input to RAM and output from RAM. The 8T28 drives the signal levels of pins 13, 10, 6 and 3 onto pins 14, 11 5 and 2. When READ RAM is high, the 8T28s enable pins 12, 9, 7 and 4 onto pins 13, 10, 6 and 3.

3.4.2 Control -

RAM can be read from the paged region or from region 0 or 1 if so enabled. In the page reading operation, the address is between $8000 and 9FFF. A13 and A14 will be low, while A15 will be high making E67 pin 12 low. For the following discussion, this will be called RAM SELECT L.

Eight pages of RAM occupy this memory address space. Write register output pins 15, 16 and 19 form the page address. Pins 15 and 16 are decoded by a 74LS139 at E75; this 2 to 4 line decoder is enabled by RAM Select L. The effect of OR gate logic at E77 and E76, and NAND gates at E78, is to generate one of the four RAS L signals necessary for memory operation, thereby selecting one of four 16K banks. Address line MA13 effectively selects which 8K region within a bank is addressed. It is generated from pin 19 of the write register.

In reading pages 6 and 7 from address region 0 and 1, MAI3 and RAS L are generated independently of register contents. RAM Select L is high. Pin 12 or 10 of E64 will be high, and if switches, 2 and 4 are opened enabling RAM and disabling ROM, either pin 6 or 8 of E82 will go low. E88 pin 11 will go low, causing RAS4 L to go active, selecting the fourth 16K bank. Also, READ RAM will be generated at E81, if R/W is high. MA13 is produced from the RAM SELECT signal and A13 L at E86; when A13 is low (in region 0) MA13 is high selecting page 7, and when A13 is high page 6 will be laid over region 1.

3.4.3 Timing -

Timing signals are generated by logic based around the two positive edge triggered D-Type flip-flops with preset and clear, at E85. E85-1 refers to the flip-flop at pins 1-6 and E85-2 to pins 8-13.

The board uses two externally generated clock signals of the same frequency, E and Q. Q leads E by one quarter of a cycle. External address lines are valid for memory accessing between the times when Q goes high and E goes low. While E is high the board can operate in the access mode using external control signals and addresses. When E is low, internal memory refresh occurs. See figure 5.

E, Q and E exclusive or Q form the basis for memory timing signals. (See figure 5). E Xor Q going low initiates the timing cycle by presetting E85-1. Since E85-1 is now high one of the RAS L signals at E78 is active, and the row address from multiplexer MC3242A is strobed into one

bank of RAM. Row addresses are selected at this point because CAST L is high at the ROW ENABLE multiplexer input.

After a delay through E80, CAST L becomes active driving the multiplexer input ROW ENABLE, low. This puts the column address on RAM address lines. A further delay through E80 insures that address lines are set up correctly before CAS L is generated, strobing the column address into memory chips.

Next, E Xor Q goes high clocking flip-flop E85-2. Since the D input is high , Q goes high, DATA LATCH at E88 pin 3 is generated, and data from RAM chips is loaded into the latch at E61. Write enable, WE L, is generated at the same time as DATA LATCH, if R/W is low.

At the same time that E85-2 Q goes high, E85-2 NOT-Q goes low. After delay through E84, the clear input of E85-2 goes low, resetting Q and disabling DATA LATCH and WE L; NOT Q is set and after delay, E85-1 is clocked causing the Q output to go low. This disables RAS L, CAST L and CAS L, completing the cycle.

WE L loads addressed RAM with data from the bus through the 8T28 transciever; READ RAM is low during a write operation so latch contents are disabled from the data bus.

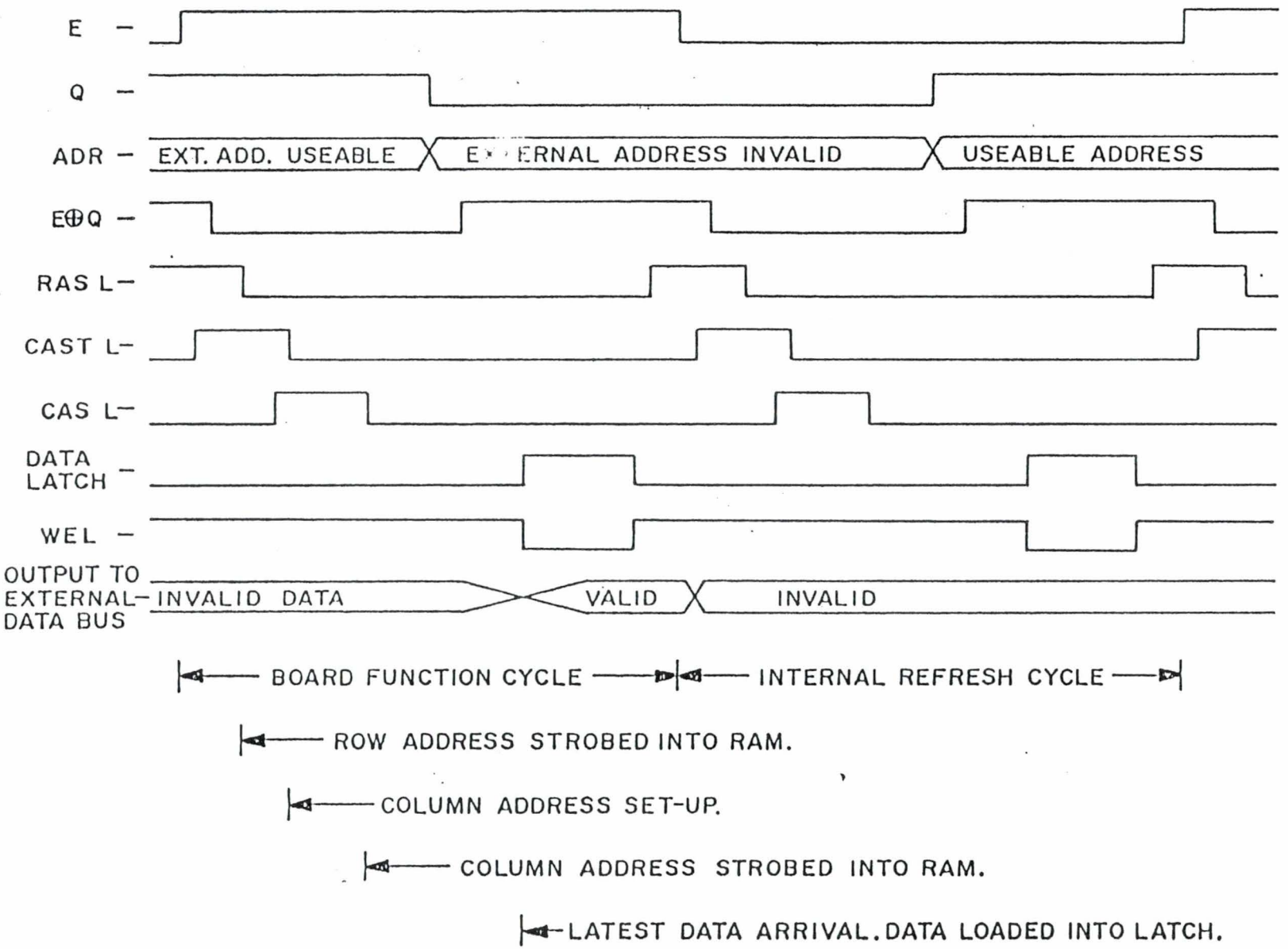

FIGURE 5 : MEMORY TIMING DIAGRAM.

3.4.4 Refresh -

When Q is high, the address multiplexer's seven bit memory refresh counter is incremented once, and external address lines are valid for normal memory operation. When Q goes low, RFRSH ADDR goes high causing the refresh counter contents to be put on RAM address lines. One quarter cycle later E goes low. Then E Xor Q goes low, causing the memory refresh timing cycle to begin. (See figure 5). Since E85-1 Q is high and E is low, logic at E76, E77 and E78 will generate all four RAS L signals thereby refreshing the RAM banks at the counter's address. Q then goes high, the counter increments, and external address lines are available for memory access; E then goes high and the access timing cycle begins. The entire RAM memory is refreshed after 128 clock cycles.

The timing signals generated for normal RAM access, and refresh operations, are the same. Only the RAS L signals and the refresh counter address are necessary for memory refresh; other signals are generated but have no effect.

4.0 INPUT/OUTPUT

4.1 General

Board input/output circuitry includes two independent RS232 serial ports, one read register, one write register and tape interface circuitry.

Two MC68A50 ACIA (asynchronous communications interface adapter) chips provide the serial ports; E51 is port 1 and E52 is port 2. Port 2 has tape interface circuitry providing (up to) 2400 baud serial data communication with separate read and write tape drives. On board encoding and decoding circuitry converts ACIA digital levels into signals suitable for recording and playback on low cost cassette tape machines.

RS232-C and tape inputs to port 2 are multiplexed by the 74LS157 at E50. Pins 2, 5 and 11 are serial line inputs, and pins 3, 6 and 10 are TAPE inputs. When tape is high, tape inputs are selected; when TAPE is low serial line inputs are chosen. TAPE comes from the write register.

4.2 I/O Addressing

Address decoding and the I/O control line can generate the BDIO signal, which enables ACIA and register function. BDIO is generated as the AND of A8, A9, A10 and the I/O signal, at E68 pins 1, 2, 4 and 5. The I/O signal is generated by external logic, typically when address lines specify the region $E800 to EFFF. This gives the effective address block for board input/output operation, $EF00 to EFFF. This block is divided into separate areas for register, serial port 1 and serial port 2 addressing, by A6 and A7. Sections 4.3.2 and 4.4.2 discuss this further.

4.3 Registers

4.3.1 General -

Board status can be read onto the data lines from the read register, or a board control byte may be loaded into the separate write register from the data bus, and stored there.

The read register is really a 74LS244 driver at E73, which gates eight board status lines onto the data bus when enabled by the READ REG L signal active at pins 1 and 19. The write register is a 74LS373 D-type latch at E72, which loads the data bus line levels when enabled by the WRITE REG signal at pin 11 and maintains the inputted levels on its eight output lines.

4.3.2 Addressing -

In order to generate READ REG L or WRITE REG, pin 1 of E79 and pin 3 of E81 must be high. This happens when BDIO, A6 and A7 are high, via pins 1, 2 and 13 of AND gate E81. Since BDIO is high when address lines specify $EF00 to EFFF, the effective register address region is $EFC0 to EFFF. Usually, address EFC0 is used to access both registers.

When address lines specify the register address region and E is high, R/W determines which register will be enabled. If R/W is high E79 will generate READ REG L. If R/W is low E81 pin 12 generates WRITE REG.

DATA LINE	READ REGISTER STATUS OUTPUTS	WRITE REGISTER CONTROL INPUTS
D7	SW1	NOT USED
D6	SW2	NOT USED
D5	SW3	DTR2 - Data terminal ready for serial port 2.
D4	SW4	DTR1 - Data terminal ready for port 1.
D3	low	TAPE - Logic 1 enables tape inputs to serial port 2.
D2	DTR2	PG2 - RAM page address
D1	DTR1	PG1 - RAM page address
D0	TAPE	PG0 - RAM page address

FIGURE 6: Read and write register bit representations.

ACIA REGISTER ADDRESSES	TYPICAL ADDRESS		OPERATION
	PORT 1	PORT 2	
RECEIVE DATA	$EF41	$EF81	READ
TRANSMIT DATA	$EF41	$EF81	WRITE
STATUS	$EF40	$EF80	READ
CONTROL	$EF40	$EF80	WRITE

FIGURE 7: Typical A.C.I.A. register addresses.

4.3.3 Function -

Six of eight write register output pins are used. Two outputs provide the signals DTR1 L and DTR2 L used in serial interfacing to external devices. (See 4.4.3) Output pin 12 gives the TAPE control line which selects tape function of serial port 2 when high. (See 4.1). Pins 15, 16 and 19 provide the page select address to RAM memory. (See 3.4.2).

Read register pins 17 and 15 represent the status of memory control switches for region 0; pins 13 and 11 show the status of the switches for memory region 1. Pins 6, 4 and 2 represent the status of the three write register output lines, DTR2 L, DRT1 L and TAPE. The status of these lines is read on data lines D0, D1 and D2, different from the lines D3, D4 and D5 used to load them into the write register. See figure 6.

4.4 Serial Interface

4.4.1 General -

Each ACIA has data bus connections, and an E clock input to synchronize ACIA operation. Pin 7 of each ACIA is connected to the IRQ L line allowing either ACIA to generate an interrupt request to external logic. Signals BDIO, A7 and A6 are used to address the ACIAs; A0 and R/W address the four registers within each.

4.4.2 Addressing -

The MC68A50 serial interface chip is enabled when CS0 at pin 8 and CS1 at pin 10 are high, while CS2 L at pin 9 is low. The BDIO line, typically high when address lines specify the region EF00 to EFFF, is connected to the CS0 inputs of both chips. Port 1 is enabled when BDIO is high, A6 is high and A7 is low at the CS1 and CS2 input respectively, giving port 1 the address region $EF40 to EF7F. Port 2 is enabled when BDIO is high, A6 is low at CS2 L, and A7 is high at CS1, giving the address region EF80 to EFBF.

ACIA register addressing is done by the R/W and A0 lines. When A0 is low, the control and status register pair is selected. A0 high selects the data registers. R/W simultaneously specifies whether the read or write register

in the chosen pair is accessed. See figure 7 for a table of typical ACIA register addresses.

4.4.3 Function -

A.C.I.A. baud rate clocks control the rate of serial line transmission and are supplied by a MC1411 bit rate generator. The MC1411's internal oscillator is controlled by an external 1.842 MHZ crystal for stability. This high frequency oscillation is divided to produce ten outputs of differing frequency, which can cause the serial port to operate at one of 9600, 4800, 3600, 2400, 1200, 600, 300, 150, 109.9 or 75 baud. Pin 10 of the chip enables the clock outputs when low, and is controlled by the externally generated, RESET L. Two ten position switches provide one output to each ACIA, which acts as both the receive and transmit clock. The actual frequencies on these lines are 16 times the baud rate to provide for A.C.I.A. data sampling in the x16 mode.

Five lines from the ACIA and one line from the write register are connected to external logic for serial communication. Four of these signals, CTS L, DCD L, RTS L and DRT1 L are for modem control. The DCD L, or data carrier detect signal inhibits and initializes the ACIA's receiver section when high. DTR1 L indicates to some external device that the ACIA is ready for communication.

RS232 input and output levels for the two ports are converted to TTL levels by 1488 chips at E47 and E49, and 1489 chips at E46 and E48. External connection to each serial port is done through 25 pin D-type connectors.

4.5 Tape Interface

4.5.1 General -

The tape interface includes data coding/decoding and drive control circuitry. Connections to external tape units are provided by a single D.I.P socket, DIP 1.

For the read from tape operation, the board's write register contents would be loaded to make DTR2 L active. E54 pin 2 goes high and E55 pin 3 pulls one side of the relay low, closing the normally open contacts and turning on the tape drive motor. A serial data stream from the

decoder, arrives at the receive data input (RX) of the ACIA through the input multiplexer. The carrier detect signal is generated by the decoder when valid data is being received, and enables the ACIA's receiver.

The write to tape operation is initiated when a byte of data is written into the ACIA control data register, causing RTS L to go active. E55 pin 6 goes low energizing the coil of relay 1 and turning on the write motor. Simultaneously E54 pin 6 goes low, starting a time delay function in the 555 timer at E56. The delay allows the write drive motor time to come up to speed before CTS L is generated and data is transmitted to the encoding circuitry from the ACIA.

4.5.2 Encoding -

Data encoding is done using F.S.K. for frequency shift keying, a technique whereby digital input levels cause the output signal to be switched between two constant frequency sources. The XR2207 at E4 performs this function.

Data from the T.X. ACIA output is active low. The XR2207 outputs a 2400 Hz signal given a low input and a an 4400 Hz signal given a high input. These are called the mark and space frequencies respectively and will be called just "mark" and "space".

Both mark and space are established by C9 and the setting of R20. R21 provides further adjustment to the space frequency.

The XR2207 provides a triangle wave output at pin 14, which is buffered at E2, then fed to R35 which selects the output level, about 0.5V P-P.

4.5.3 Decoding -

F.S.K. decoding reverses the encoding process by taking an input signal switched between the mark and space frequencies, and outputting digital levels 1 or 0. The XR2211 chip at E5 does this by tracking the input signal with a phase locked loop (P.L.L.).

The P.L.L. can track and lock onto input signals within certain frequency limits. The center frequency of this range is set by external components. The tracking range is specified as a difference +/- dF from the center frequency, and gives the frequency range over which the P.L.L. can retain its lock on the input signal; dF is

approximately equal to the difference between mark and space frequencies. The capture range is slightly narrower than the tracking range and specifies at what input frequencies the P.L.L. can acquire lock to the input. The P.L.L. can lock onto and track signals from below the mark to above the space frequency.

The P.L.L. will identify a locked signal within the tracking range as a mark if the signal is below the center frequency and as a space if the signal is above the center. A logic one or zero will be output respectively.

The XR2211 generates three open collector outputs. Q, NOT Q, and OUT. The Q output pulls CARRIER DETECT low using its pullup resistor R34, when lock is achieved with an incoming signal. When Q is high the NOT Q output is open and data from OUT and its associated pullup resistor, R14, travels through inverter E48 to the serial port. When the P.L.L. is not locked, Q goes high disabling CARRIER DETECT. The NOT Q pin and R14 then force OUT low, disabling data output.