Document No. 154411-34

CURRENT REVISION
including all changes

FEB 20 1976

ENGRG. DATA CONTROL

CIRCUIT CARD DESCRIPTION

CENTRAL PROCESSING UNIT (CCU) CARD

TOP ASSY. NO. 154411

DSD RELEASE DATE 3-29-74
CATEGORY I RELEASE

PREPARED BY: [illegible] DATE 3/2

APPROVED BY: [illegible] DATE 3/2

TOTAL P

Specification No. 154411-340

REV	DATE	BY	REVISION DESCRIPTION	APPROVED BY

CIRCUIT DESCRIPTION
CPU CARD
154411

1.0 Circuit Function

The CPU card is the heart of the CCU central logic. It contains a microprocessor 8008-1 chip which is also known as the CPU chip.

The card receives data and a two phase clock. It then provides timing and sequential data on an 8 bit bus. The sequential data contains the information to control the CCU.

1.1 Important Documents

Top Assembly	154411-100
Printed Wiring Master	154820
Schematic	154411-300
Test Specification	154411-300
Test Procedure	(TBD)
Intel MCS-8 User's Manual	

2.0 Electrical Operation

A block diagram of the card is shown in Figure 1.

A basic 8008-1 basic instruction cycle is shown in figure 2. A CPU state transistion diagram is shown in figure 3. The 8008-1 Instruction Set is shown in figures 4 and 5.

2.1 Microprocessor Chip

The 8008-1 chip, U9, requires a two phase clock which is generated on the oscillator card and is shown in figure 2. The ready line to the CPU is always enabled except for factory testing. The flip flops in U28 and half of U29 along with the 9316 counter control the interrupt line to the 8008-1 just during power turn on. The 8008-1 generates sync and states as indicated in figures 3 and 4. The 8008-1 has an internal program counter which along with the instructions from the external ROM and RAM cards control the sequence and operation of the central logic of the CCU. The instructions and data are entered thru on 8 bit bidirectional bus D0-D7.

2.2 Multiplexers (MUX)

The SN54LS253 chips (U22, U23, U25 and U26) are dual 4 input to 1 tristate output multiplexers. The four inputs are from:

1) Interrupt word bus
2) Input data bus
3) Random Access Memory (RAM) output bus
4) Read Only Memory (ROM) output bus

Each of the input busses are 8 bit busses. Keyboard switch, ring in, and other status conditions within the CCU are entered on the Input Data Bus. The Interrupt Word Bus is externally connected for a RST (restart) at zero command in the CCU.

The U21 chip is an encoder which receives individual controls and converts them to a binary number for selecting the multiplexers. The G input to the multiplexers are the enable controls to output the multiplexer data into the 8008-1 data bus.

2.3 Output Buffers

The inverters in chips U4, U12 and U13 are the output buffers indicated in figure 1. The output CDATAO - CDATA7 represent data from the 8008-1 to the I/O and RAM cards.

2.4 Address and Control Register

The register chips U3 and U11 catch and hold the higher order address information, and two bits which determine the 8008-1 control cycle coding. The U10 decoder chip decodes the higher four bits for selecting the 1K RAM on the RAM card. The U2 decoder chip decodes two bits to select the two ROM cards when they are addressed.

2.5 ROM Power Control

One of the flip flops in U29 determines the time to turn on ROM power. It drives the gate in U20 which in turn drives the U5 ROM power driver. Pulsing the ROM conserves power consumption in the ROM's. Pin 5 and R43 (2.7K ohm provide a means to statically turn on the ROM's during factory testing.

2.6 Timing Logic

The U6 decoder chip decodes the 8008-1 states for timing informatio for the card. One of the notable timing outputs is the LADDSTR which is on pin 72

This is the strobe to the I/O card for catching the lower address and data. Pin 57 is another output. It provides a write control to the RAM card. PWR LOSS, pin comes from the power supply to signal power loss to prevent writing into the RAMs. This signal is sent thru inverter in U16, thru the U20 gate and the write enable flip flop in U27. The T3 anticipation information which appears on pin 65 is used to control input information to the 8008-1 by enabling the input on the I/O card, which in turn enables the address specified to enter data on the MUX Input Data Bus. The output on pin 75 is T3.SYNC.Ø2 time which strobes the I/O card for catching output data with the previously specified address. The other gates and inverters that have not been previously mentioned are part of the timing logic.

3.0 Input Characteristics

All input lines are T^2L logic levels, i.e., $+2.75 \leq$ High $\leq +5.$ volts and $0 \leq$ Low $\leq +0.4$ volt with the excpetion of pin 5 which are 0 ± 0.5 vo and open.

Power requirements are $+5.3 \pm 0.2V$ and $-9.7V \pm 0.2V$.

4.0 Output Characteristics

All outputs are T^2L as defined in paragraph 3.0 except for pin 25 which is $+4.0 \pm 1$ volt and $-9.4 \pm 0.5V$. Rise and fall times are less than 100 nanoseconds for T^2L. Rise and fall times to less than 1 microsecond for pin 25.

5.0 Reliability

The reliability as calculated for the 154411 is as follows:

@ 50^oC is 3.69 FPM.

6.0 Attachments

Figure 1 - Block Diagram of the CPU card

Figure 2 - 8008-1 Basic Instruction Cycle

Figure 3 - CPU State Transistion Diagram

Figure 4 & 5 - 8001 Instruction Set

PARTS LIST	DATA SYSTEMS VAN NUYS, CALIF.	CONTRACT NUMBER DAAB07-72-C-0257	CODE IDENT 13973	PL 154411	REVISION A

TITLE CENTRAL PROCESSING UNIT - CIRCUIT CARD ASSEMBLY

SHEET 2

ITEM NO.	QTY REQD/DASH NO.			-100	UNIT OF MEASURE	CODE IDENT	PART OR IDENTIFYING NUMBER	DRAWING OR DOCUMENT NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REF DES	UNIT WEIGHT	REF SYM	ZONE	LINE REV
1				1			154820		PRINTED WIRING BOARD					
2				1			154952		RETAINER					
3				1			154953		DISSIPATOR, HEAT					
4														
5				4			M39003/01-2289	MIL-C-39003/1	CAPACITOR, 15UF, ±10%, 20V	C1, C4, C8, C10				
6				5			M39014/02-1407	MIL-C-39014/2	CAPACITOR, 1.0UF ±10%, 50V	C2, C3, C5, C7, C9				
7				1			M39014/02-1220	MIL-C-39014/2	CAPACITOR, .015UF ±10%, 100V	C6				
8														
9				1			JANIN3600	MIL-S-19500/231	DIODE	CR1				
10														
11				3			RLR07C102GM	MIL-R-39017/1	RESISTOR, 1KΩ ±2%, 1/4W	R17, R30, R39				
12				14			RLR07C202GM	MIL-R-39017/1	RESISTOR, 2KΩ ±2%, 1/4W	R1, R2, R5, R6, R9, R10, R13, R14, R18, R19, R20, R21, R40, R41				
13				8			RLR07C512GM	MIL-R-39017/1	RESISTOR, 5.1KΩ ±2%, 1/4W	R31 THRU R38				
14				9			RLR07C103GM	MIL-R-39017/1	RESISTOR, 10KΩ ±2%, 1/4W	R3, R4, R7, R8, R11, R12, R15, R16, R42				
15				8			RLR07C223GM	MIL-R-39017/1	RESISTOR, 22KΩ ±2%, 1/4W	R22 THRU R29				
16				1			RLR07C272GM	MIL-R-39017/1	RESISTOR, 2.7KΩ ±2%, 1/4W	R43				

PARTS LIST	DATA SYSTEMS VAN NUYS, CALIF.	CONTRACT NUMBER DAAB07-72-C-0257	CODE IDENT 13973	PL 154411	REVISION A

TITLE CENTRAL PROCESSING UNIT - CIRCUIT CARD ASSEMBLY

SHEET 4

ITEM NO.	QTY REQD/DASH NO.			-100	UNIT OF MEASURE	CODE IDENT	PART OR IDENTIFYING NUMBER	DRAWING OR DOCUMENT NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REF DES	UNIT WEIGHT	REF SYM	ZONE	LINE REV
29				1			888997-0039		MICROCIRCUIT, 8 INPUT PRIORITY ENCODER	U21				
30				1			888995-0021		MICROCIRCUIT, SINGLE 8-BIT PARALLEL CENTRAL PROCESSOR UNIT	U9				
31				1			862526-0016		MICROCIRCUIT, LOW POWER FOUR-BIT BINARY COUNTER	U17				
32														
33														
34				1			154316		INSULATOR - HEAT DISSIPATOR					
35														
36														
37				~~2~~			~~860134-0210~~		~~SCREW, MACHINE, PAN HD, 2-56 X .625 LG~~					
38				~~2~~			~~860127-21~~		~~NUT, HEX, SELF LOCKING NO. 2-56~~			A		
39				~~2~~			~~NAS620C2~~		~~WASHER, NO. 2 FLAT~~					
40				~~AR~~				~~QQ-S-571~~	~~SOLDER~~	~~COMP Sn63 WRMAPE~~				
41				AR			890215-2		COATING, THERMALLY CONDUCTIVE					

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INCORPORATED ECO A1 THRU A5 AND DIRECT DRAWING CHANGE ECO A6	6 FEB 75	

NOTES: UNLESS OTHERWISE SPECIFIED

A. ~~VENDOR ITEM - SEE SOURCE OR SPECIFICATION CONTROL DRAWING.~~

B. APPLICABLE DOCUMENTS:

ELECTRICAL AND ELECTRONIC SOLDERING	893817
CONFORMAL COAT SPEC	893306
IDENT MARKING SPEC	894201
ADHESIVE BONDING SPEC	893111

C. REFERENCE DOCUMENTS:

SCHEMATIC DIAGRAM	154411-300
TEST SPECIFICATION	154411-720

DO NOT SCALE DWG

~~INITIAL APPLICATION SHOWN. FOR COMPLETE USAGE DATA, SEE APPLICATION DATA INDEX SHEET.~~

154184	TOS2
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED

INTERPRET PER MIL-STD-100. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI-Y14.5. DIM VALUES ARE IN INCHES. SURFACE TEXTURE SHALL BE ✓. DIMENSIONS APPLY AFTER PLATING. REMOVE BURRS AND SHARP EDGES. PARENTHETICAL DATA FOR INTERNAL LITTON REFERENCE ONLY.

TOLERANCES

ON DECIMAL DIMENSIONS	ON ANGULAR DIMENSIONS
.X ± .1	CHAMFERS ± 5°
.XX ± .03	FORMED ± 5°
.XXX ± .010	LOCATING ± 0°15'
	MACHINED ± 0°15'

FINISH

MATERIAL

CONTRACT NO. DAAB07-72-C-0257

DWN	Pearsbough	22 JAN 72
CHK	[illegible]	7 JUL 72
ENGR	[illegible]	3-4-72
ELECT SYS	[illegible]	11-1-72
DSD		
OTHER		

LITTON DATA SYSTEMS VAN NUYS, CALIF.

CENTRAL PROCESSING UNIT - CIRCUIT CARD ASSEMBLY

SIZE	CODE IDENT NO.	DRAWING NO.
B	13973	PL 154411

SCALE NONE | WEIGHT | SHEET 1 OF 4

DWG NO. PL 154411 REV A

3-3000 (R-3 12/72)

PARTS LIST	DATA SYSTEMS VAN NUYS, CALIF.	CONTRACT NUMBER DAAB07-72-C-0257	CODE IDENT 13973	PL 154411	REVISION A

TITLE CENTRAL PROCESSING UNIT - CIRCUIT CARD ASSEMBLY

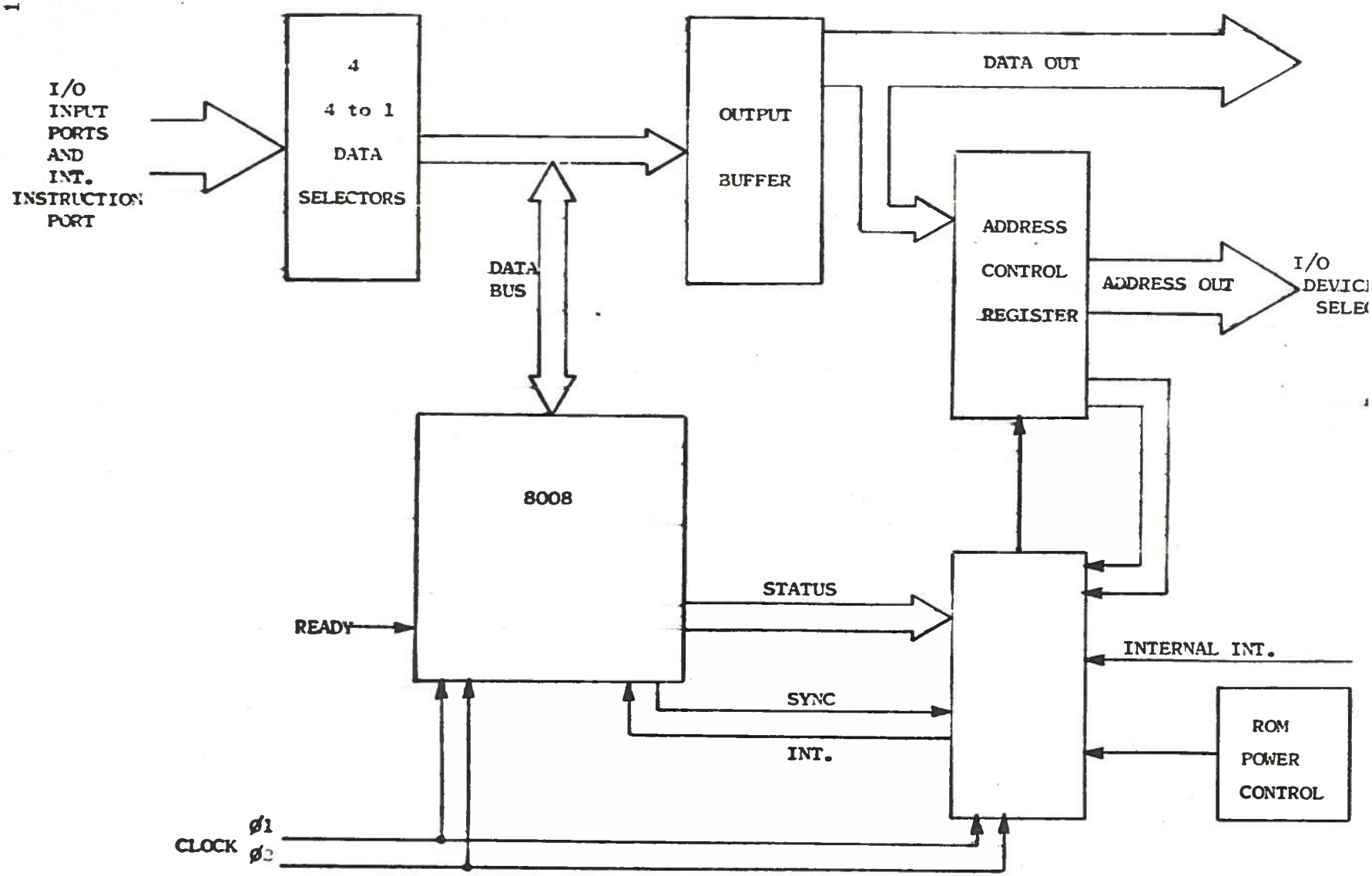
SHEET 3

ITEM NO.	QTY REQD/DASH NO.			-100	UNIT OF MEASURE	CODE IDENT	PART OR IDENTIFYING NUMBER	DRAWING OR DOCUMENT NUMBER	NOMENCLATURE OR DESCRIPTION	MATERIAL OR REF DES	UNIT WEIGHT	REF SYM	ZONE	LINE REV
17														
18														
19														
20				2			862525-0016		MICROCIRCUIT, LOW POWER FOUR-BIT SHIFT REGISTER	U3, U11				
21				4			888995-0001		MICROCIRCUIT, QUAD - 2 INPUT POSITIVE NAND GATE, LOW POWER SHOTTKY TTL	U8, U15, U18, U19				
22				6			888995-0002		MICROCIRCUIT, HEX INVERTER, LOW POWER SHOTTKY TTL	U4, U7, U12, U13, U14, U16				
23				3			888995-0003		MICROCIRCUIT, DUAL-D-TYPE POSITIVE EDGE TRIGGERED FLIP FLOPS, LOW POWER SHOTTKY TTL	U27, U28, U29				
24				2			888995-0004		MICROCIRCUIT, 3 TO 8 LINE DECODER, LOW POWER SCHOTTY, TTL	U6, U10				
25				1			888995-0011		MICROCIRCUIT, DUAL 2 LINE TO 4 LINE DECODER	U2				
26				1			888995-0013		MICROCIRCUIT, CLOCK DRIVER	U5				
27				4			888995-0015		MICROCIRCUIT, DUAL 4 TO 1 LINE SELECTOR WITH TRI STATE OUTPUTS	U22, U23, U25, U26				
28				1			888997-0032		MICROCIRCUIT, DUAL 4 INPUT BUFFER	U20				

3-227SC (R-1 12/72)

154411-340

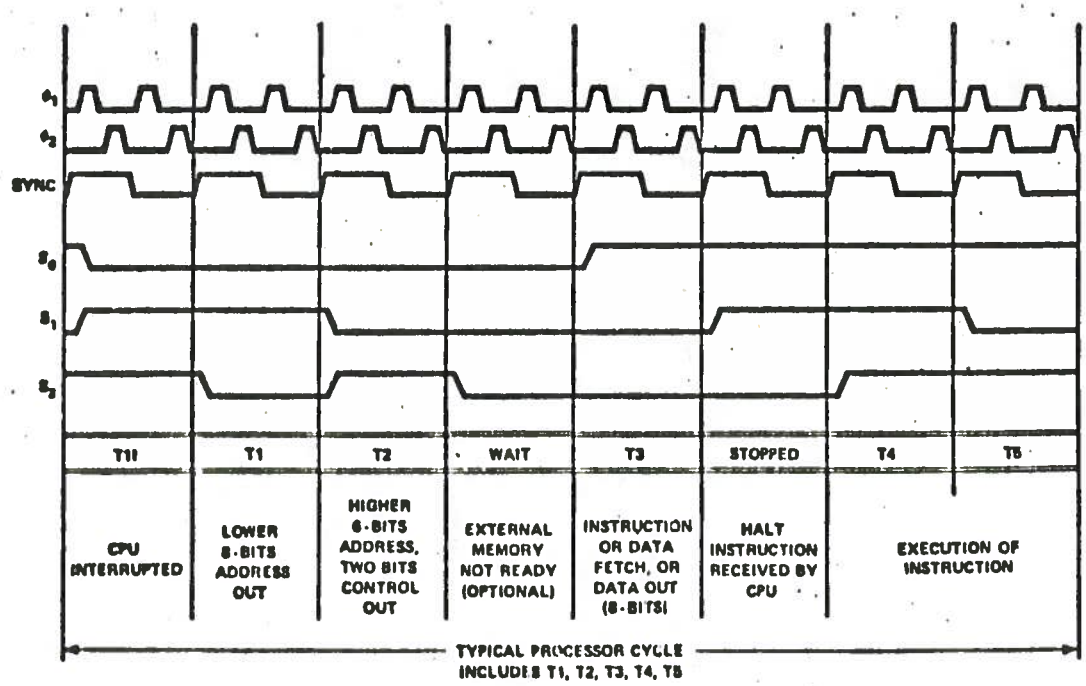
Figure 1



Block Diagram of CPU Card

S_0	S_1	S_2	STATE
0	1	0	T1
0	1	1	T1I
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOPPED
1	1	1	T4
1	0	1	T5

STATE CONTROL CODING

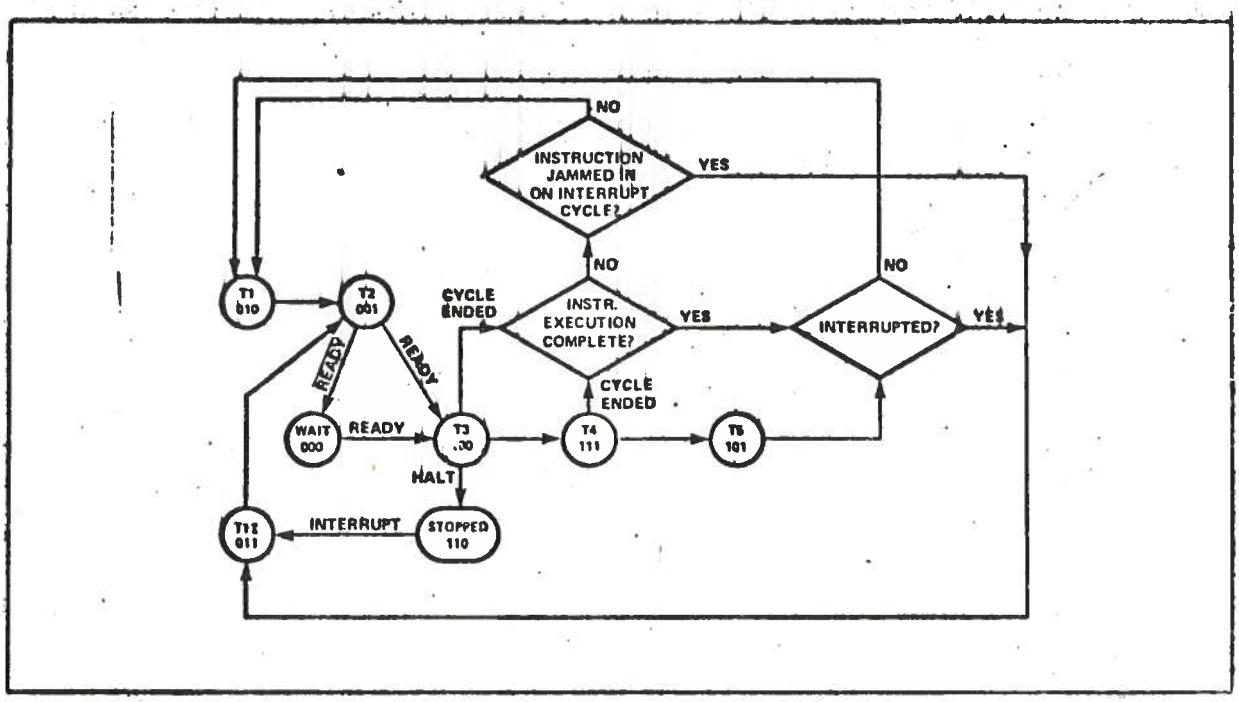


BASIC 8008 INSTRUCTION CYCLE

FIGURE 2

D_6	D_7	CYCLE	FUNCTION
0	0	PCI	Designates the address is for a memory read (first byte of instruction).
0	1	PCR	Designates the address is for a memory read data (additional bytes of instruction or data).
1	0	PCC	Designates the data as a command I/O operation.
1	1	PCW	Designates the address is for a memory write data.

CYCLE CONTROL CODING



CPU STATE TRANSITION DIAGRAM - FIGURE 3

IV. BASIC INSTRUCTION SET

The following section presents the basic instruction set of the 8008.

A. Data and Instruction Formats

Data in the 8008 is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference, I/O arithmetic or logical, rotate or return instructions
Two Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	Immediate mode instructions
Three Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS	JUMP or CALL instructions
X X D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS*	*For the third byte of the instruction, D_6 and D_7 are "don't care" bits.

For the MCS-8 a logic "1" is defined as a high level and a logic "0" is defined as a low level.

B. Summary of Processor Instructions

Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE D_7 D_6	D_5 D_4 D_3	D_2 D_1 D_0	DESCRIPTION OF OPERATION
(1) Lr_1r_2	(5)	1 1	D D D	S S S	Load index register r_1 with the content of index register r_2.
(2) LrM	(8)	1 1	D D D	1 1 1	Load index register r with the content of memory register M.
LMr	(7)	1 1	1 1 1	S S S	Load memory register M with the content of index register r.
(3) Lri	(8)	0 0 B B	D D D B B B	1 1 0 B B B	Load index register r with data B . . . B.
LMI	(9)	0 0 B B	1 1 1 B B B	1 1 0 B B B	Load memory register M with data B . . . B.
INr	(5)	0 0	D D D	0 0 0	Increment the content of index register r (r ≠ A).
DCr	(5)	0 0	D D D	0 0 1	Decrement the content of index register r (r ≠ A).

Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

ADr	(5)	1 0	0 0 0	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADM	(8)	1 0	0 0 0	1 1 1	
ADI	(8)	0 0 B B	0 0 0 B B B	1 0 0 B B B	
ACr	(5)	1 0	0 0 1	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ACM	(8)	1 0	0 0 1	1 1 1	
ACI	(8)	0 0 B B	0 0 1 B B B	1 0 0 B B B	
SUr	(5)	1 0	0 1 0	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUM	(8)	1 0	0 1 0	1 1 1	
SUI	(8)	0 0 B B	0 1 0 B B B	1 0 0 B B B	
SBr	(5)	1 0	0 1 1	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBM	(8)	1 0	0 1 1	1 1 1	
SBI	(8)	0 0 B B	0 1 1 B B B	1 0 0 B B B	

Figure 4

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE $D_7 D_6$	$D_5 D_4 D_3$	$D_2 D_1 D_0$	DESCRIPTION OF OPERATION
NDr	(5)	1 0	1 0 0	S S S	Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
NDM	(8)	1 0	1 0 0	1 1 1	
NDI	(8)	0 0 B B	1 0 0 B B B	1 0 0 B B B	
XRr	(5)	1 0	1 0 1	S S S	Compute the EXCLUSIVE OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
XRM	(8)	1 0	1 0 1	1 1 1	
XRI	(8)	0 0 B B	1 0 1 B B B	1 0 0 B B B	
ORr	(5)	1 0	1 1 0	S S S	Compute the INCLUSIVE OR of the content of index register r, memory register m, or data B . . . B with the accumulator.
ORM	(8)	1 0	1 1 0	1 1 1	
ORI	(8)	0 0 B B	1 1 0 B B B	1 0 0 B B B	
CPr	(5)	1 0	1 1 1	S S S	Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CPM	(8)	1 0	1 1 1	1 1 1	
CPI	(8)	0 0 B B	1 1 1 B B B	1 0 0 B B B	
RLC	(5)	0 0	0 0 0	0 1 0	Rotate the content of the accumulator left.
RRC	(5)	0 0	0 0 1	0 1 0	Rotate the content of the accumulator right.
RAL	(5)	0 0	0 1 0	0 1 0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0	0 1 1	0 1 0	Rotate the content of the accumulator right through the carry.

Program Counter and Stack Control Instructions

(4) JMP	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$.
(5) JFc	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
JTc	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
CAL	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$. Save the current address (up one level in the stack).
CFc	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is false, and save the current address (up one level in the stack.) Otherwise, execute the next instruction in sequence.
CTc	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
RET	(5)	0 0	X X X	1 1 1	Unconditionally return (down one level in the stack).
RFc	(3 or 5)	0 0	0 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
RTc	(3 or 5)	0 0	1 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0	A A A	1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).

Input/Output Instructions

INP	(8)	0 1	0 0 M	M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1	R R M	M M 1	Write the content of the accumulator into the selected output port (RRMMM, RR ≠ 00).

Machine Instruction

HLT	(4)	0 0	0 0 0	0 0 X	Enter the STOPPED state and remain there until interrupted.
HLT	(4)	1 1	1 1 1	1 1 1	Enter the STOPPED state and remain there until interrupted.

NOTES:

(1) SSS = Source Index Register
DDD = Destination Index Register
These registers, r, are designated A(accumulator–000), B(001), C(010), D(011), E(100), H(101), L(110).

(2) Memory registers are addressed by the contents of registers H & L.

(3) Additional bytes of instruction are designated by BBBBBBBB.

(4) X = "Don't Care".

(5) Flag flip-flops are defined by C_4C_3: carry (00-overflow or underflow), zero (01-result is zero), sign (10-MSB of result is "1"), parity (11-parity is even).

Figure 5

DATA SYSTEMS	Test Specification	No. 154411-720
Contract No. DAAB07-72-C-0257	UNIT TITLE CENTRAL PROCESSING UNIT CIRCUIT CARD	
CODE IDENT NO. 13973	ASSY DWG. 154411 SCHEMATIC 154411-300	

ORIGINATOR	[illegible]	8-7-74			
DESIGN ENG.	PINKHAM				
ENG. APPROVAL	O. Morgan	8-7-74			

REV.	DATE	ECO No.	DESCRIPTION	ORIG.	ENG.
A	4 Feb 75	A1	Incorporated Direct Dwg Change - ECO A1	4 Feb 75 [illegible]	[illegible] O. Morgan

CURRENT REVISION
including all changes as of
FEB 20 1976
ENGRG. DATA CONTROL

Category II Kit.

USD Release Date 8-12-75

3-484 REV. 2 (10/73)

1.0 DESCRIPTION

The Central Processing Unit (CPU) card is one of eight cards that make up the central logic portion of the Communications Control Unit. The CPU card, as the name implies, is the heart of the system. It is the CPU card that carries out the instructions contained in memory and processes the data, it also passes on the commands and performs arithmetic operations.

2.0 GENERAL

2.1 All tolerances are ±5% unless otherwise specified.

2.2 All tests shall be performed at prevailing factory or laboratory atmospheric conditions.

2.3 Output Logic Levels

Logic 1 = High = +3.25 VDC ± 1.25 VDC

Logic 0 = Low = +0.45 VDC ± 0.45 VDC

2.4 Input Logic Levels

Logic 1 = High = +3.50 VDC ± 1.50 VDC

Logic 0 = Low =+0.35 VDC ± 0.35 VDC

PARA. NO.	INPUT	CONN/PIN	CONDITIONS	CONN/PIN	OUTPUT
3.0	REQUIREMENTS				
3.1	Initial Conditions				
	+5 VDC	11, 12			
	+5 VDC Return	1, 2			
	-9 VDC Return	1, 2			
	-9 VDC	43			
	Two Phase Clock				
	Ø1	60	See Figure 1		
	Ø2	71			
	Power Loss	74	GND for all tests.		
3.2	GPU Sync Signal				
3.2.1			See Figure 1	77	Sync
3.3	State Codes				
3.3.1			See Figure 2	64	STATEC 2
				66	STATEC 1
				67	STATEC 0
3.4	Control and Timing Signals				

PARA. NO.	INPUT	CONN/PIN	CONDITIONS	CONN/PIN	OUTPUT
3.4.1			See Figure 3	72	LADDSTR
				25	ROMPWR
				65	T3ANTIC*
				75	T3SYCØ3*
				76	T3SYNC*
				68	STOP*
3.5	Write Control				
3.5.1	INTRD 7	21	High	57	Write*
	INTRD 6	17	High	72	LADDSTR
	INTRD 5	30	Low		
	INTRD 4	26	Low		
	INTRD 3	47	Low		See Figure 4
	INTRD 2	44	Low		
	INTRD 1	54	Low		
	INTRD 0	51	Low		
	ROMD 7	24	Low		
	ROMD 6	20	Low		
	ROMD 5	34	High		
	ROMD 4	29	High		
	ROMD 3	50	High		
	ROMD 2	48	High		
	ROMD 1	63	High		
	ROMD 0	58	Low		

PARA. NO.	INPUT	CONN/PIN	CONDITIONS	CONN/PIN	OUTPUT
3.6	Output Address				
3.6.1	ROMD 7	24	High	8	RAMCS 4
	ROMD 6	20	High	9	RAMCS 5
	ROMD 5	34	High	10	RAMCS 6
	ROMD 4	29	High	6	ROMCS 1
	ROMD 3	50	High	7	ROMCS 2
	ROMD 2	48	High		See Figure 5
	ROMD 1	63	High		
	ROMD 0	58	High		
3.7	Input Data Selector And Controls				
3.7.1	INTRD 7	21		40	CDATA 7
	INTRD 6	17		41	CDATA 6
	INTRD 5	30		42	CDATA 5
	INTRD 4	26		78	CDATA 4
	INTRD 3	47		79	CDATA 3
	INTRD 2	44		39	CDATA 2
	INTRD 1	54		60	CDATA 1
	INTRD 0	51		38	CDATA 0
	ROMD 7	24		15	CHADD 7
	ROMD 6	20		16	CHADD 6
	ROMD 5	34		4	CHADD 5
	ROMD 4	29		3	CHADD 4

PARA. NO.	INPUT	CONN/PIN	CONDITIONS	CONN/PIN	OUTPUT
3.7.1	ROMD 3	50		37	CHADD 3
	ROMD 2	48		36	CHADD 2
	ROMD 1	63		35	CHADD 1
	ROMD 0	58		33	CHADD 0
	RAMD 7	23			
	RAMD 6	19			
	RAMD 5	31			
	RAMD 4	28			
	RAMD 3	52			
	RAMD 2	46			
	RAMD 1	59			
	RAMD 0	55			
	INPB 7	22			
	INPB 6	18			
	INPB 5	32			
	INPB 4	27			
	INPB 3	49			
	INPB 2	45			
	INPB 1	56			
	INPB 0	53			
	READY	73	See Figure 1.		Output as shown in Table 2.
	Inputs as shown in Table 1.				

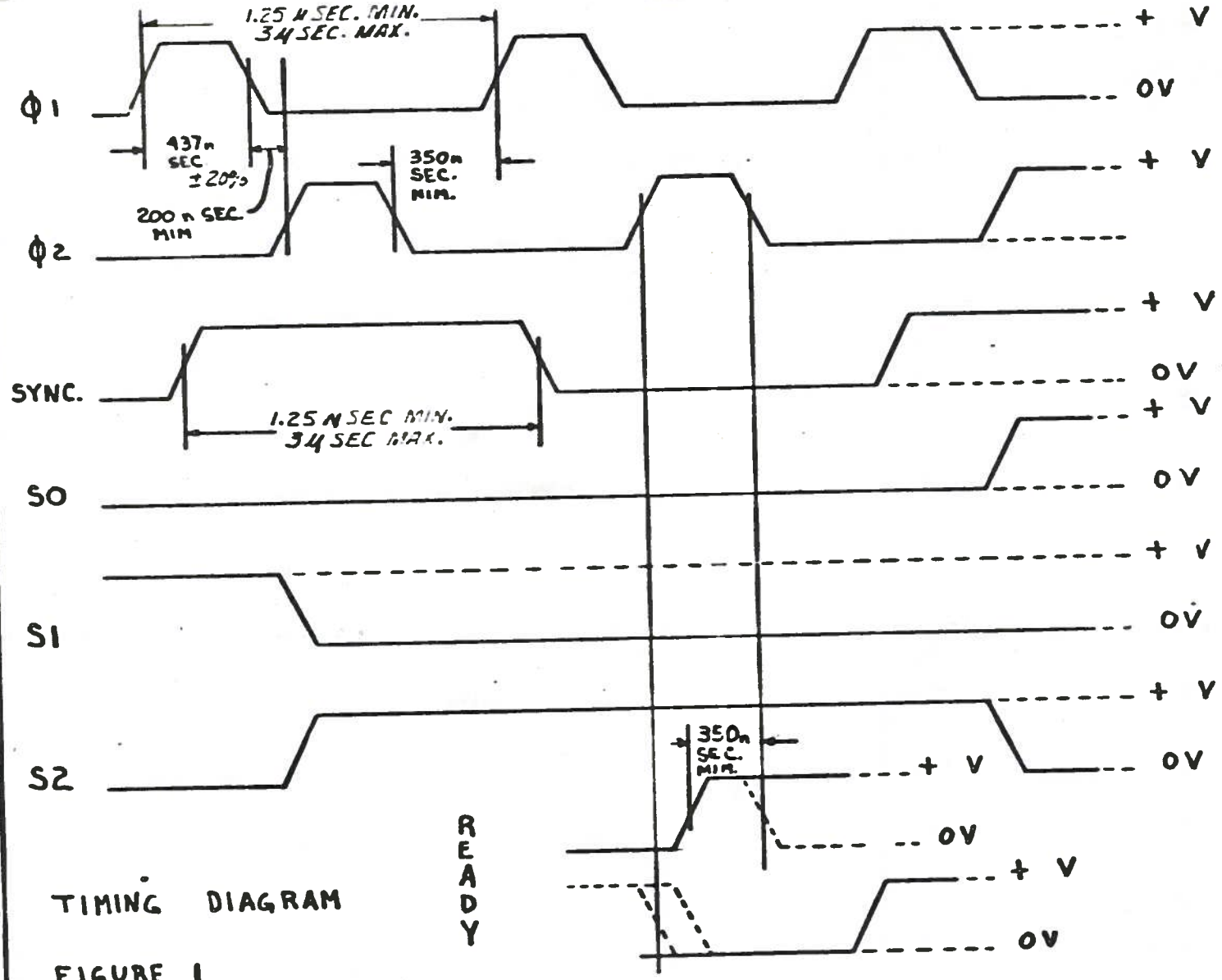
INTRD7-0	ROMD7-0	RAMD7-0	INPB7-0	READY
21 17 30 26 47 44 54 51	24 20 34 29 50 48 63 58	23 19 31 28 52 46 59 55	22 18 32 27 49 45 56 53	73
0 0 0 0 0 1 0 1	0 0 0 0 0 1 0 1	0 1 0 1 0 1 0 1	1 0 1 0 1 0 1 0	(Pulse 4 Times)
1 1 0 0 0 0 0 0	1 1 0 0 0 1 1 1	0 1 0 1 0 1 0 1	1 0 1 0 1 0 1 0	(Pulse 2 Times)
1 1 0 0 0 0 0 0	0 1 1 1 0 1 1 1	0 1 0 1 0 1 0 1	1 0 1 0 1 0 1 0	(Pulse until output reads as shown in Tbl. 2, Line 1, but not to exceed 3 pulses).
Read Output as shown in Table 2, Line 1:				
1 1 0 0 0 0 0 0	0 1 0 0 0 1 0 1	0 1 0 1 0 1 0 1	1 0 1 0 1 0 1 0	(Pulse until output reads as shown in Table 2, Line 2, but not to exceed 6 times)
Read Output as shown in Table 2, Line 2.				

Input Data
Table 1

CDATA 7-0	CHADD 7-0	
40 41 42 78 79 39 60 38	15 16 4 3 37 36 35 33	
0 1 0 1 0 1 0 1	0 1 1 1 0 1 1 1	LINE - 1
1 0 1 0 1 0 1 0	0 1 0 0 0 1 0 1	LINE - 2

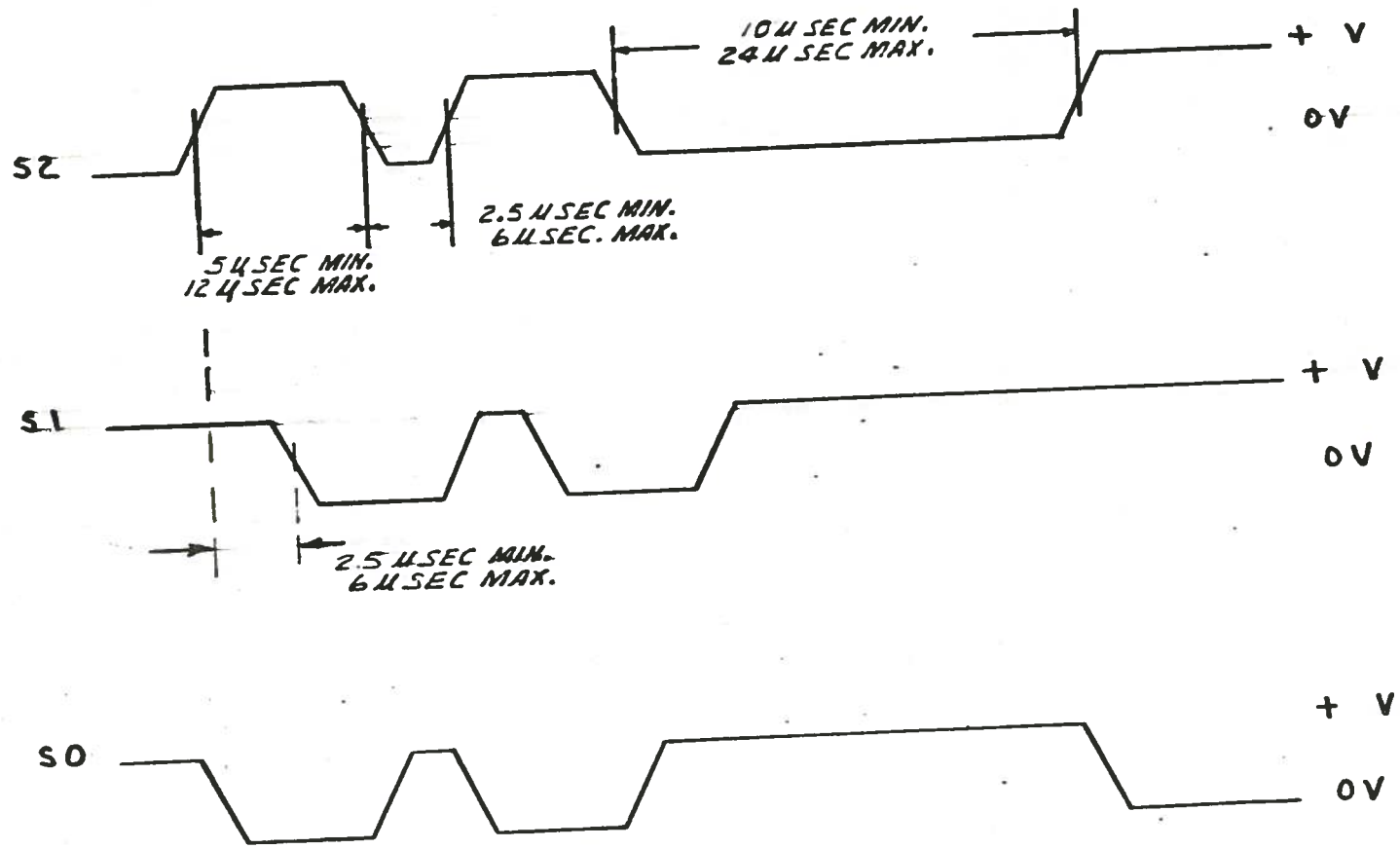
OUTPUT DATA

TABLE 2



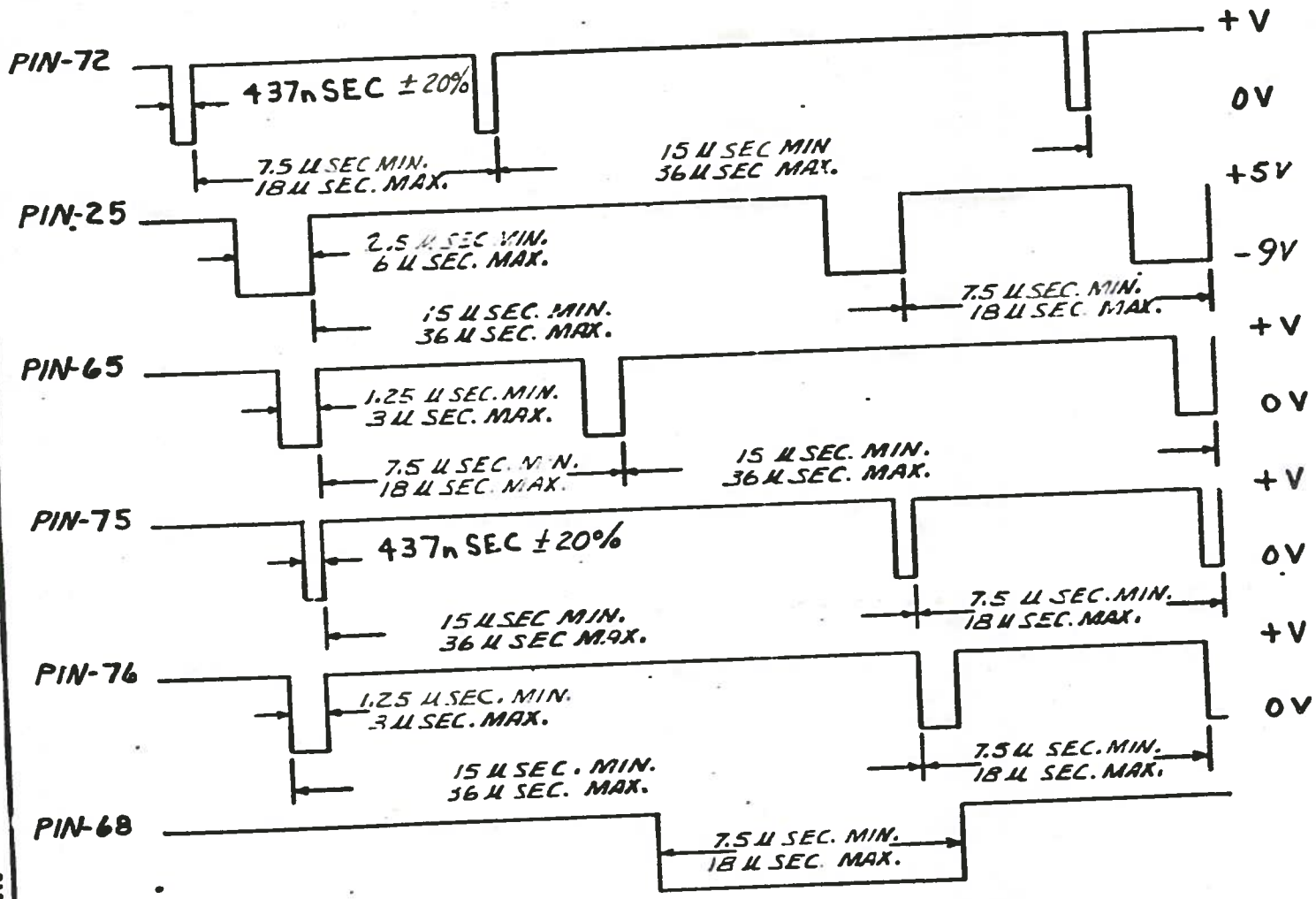
TIMING DIAGRAM

FIGURE 1



STATE COUNTER

FIGURE 2



CONTROL TIMING

FIGURE 3

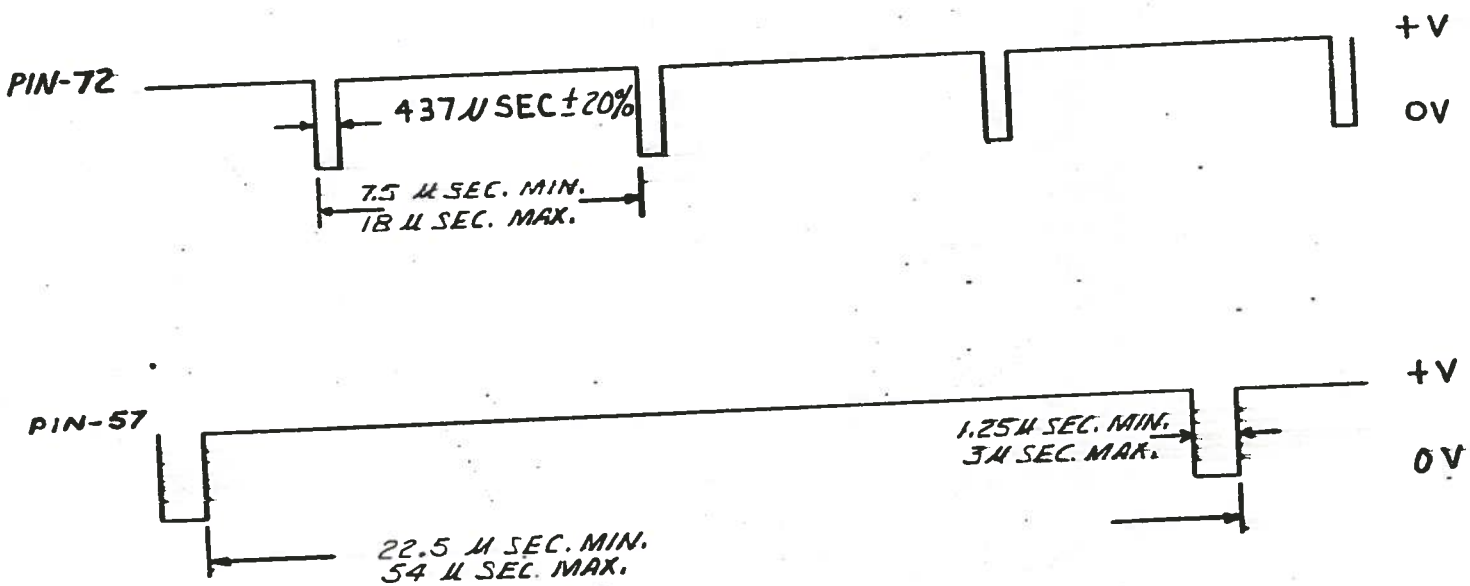

PIN-72
437 μ SEC ± 20%
7.5 μ SEC. MIN.
18 μ SEC. MAX.
+V
0V
PIN-57
22.5 μ SEC. MIN.
54 μ SEC. MAX.
1.25 μ SEC. MIN.
3 μ SEC. MAX.
+V
0V

FIGURE 4

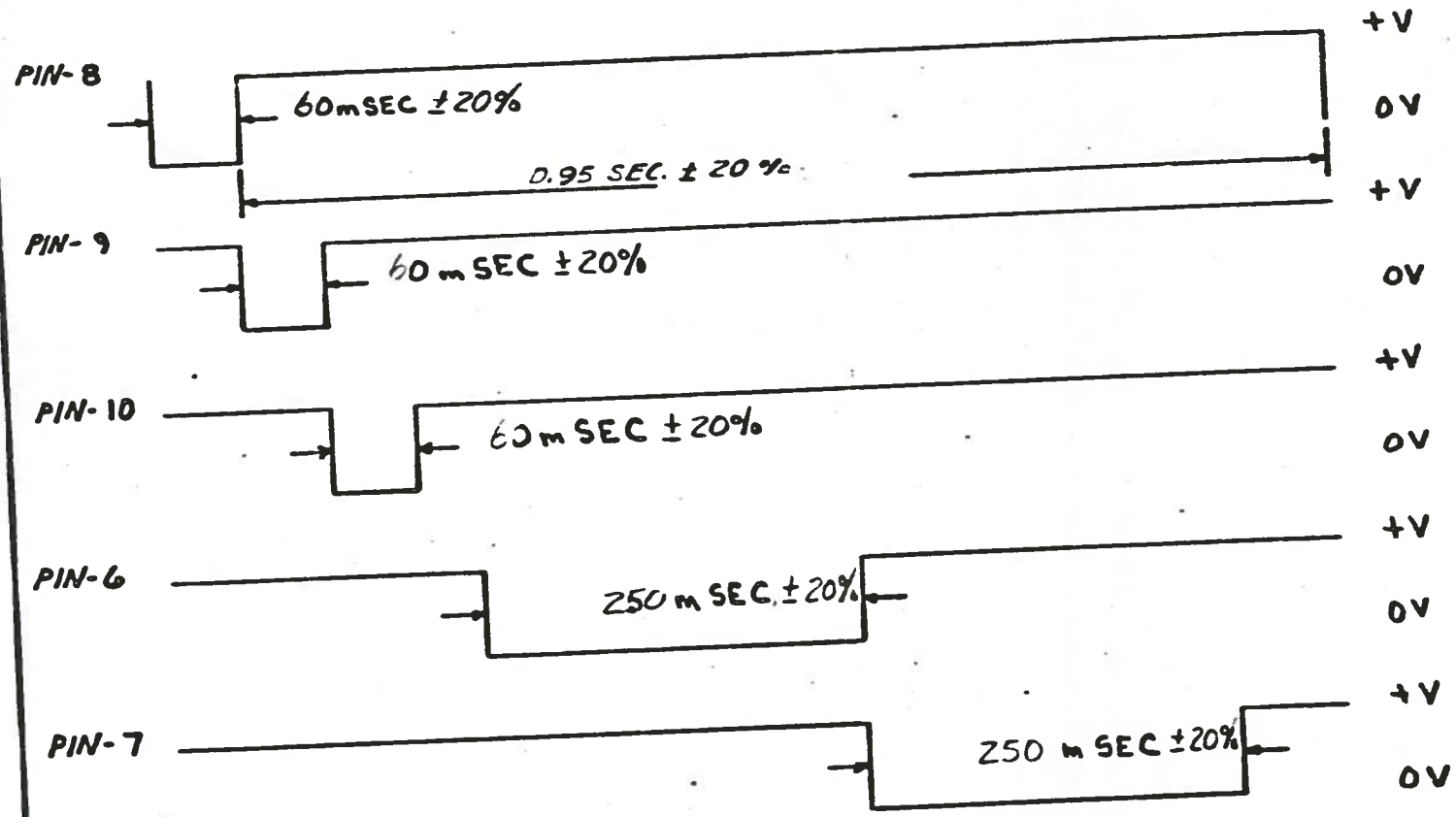

PIN-8
60mSEC ±20%
0.95 SEC. ± 20 %
+V
0V
PIN-9
60 m SEC ±20%
+V
0V
PIN-10
60 m SEC ±20%
+V
0V
PIN-6
250 m SEC. ±20%
+V
0V
PIN-7
250 m SEC ±20%
+V
0V

FIGURE 5